

DAC1617D1G0

Dual 16-bit DAC, LVDS interface, up to 1 Gsps, x2, x4 and x8 interpolating

Rev. 03 — 2 July 2012

Preliminary data sheet

1. General description

The DAC1617D1G0 is a high-speed 16-bit dual channel Digital-to-Analog Converter (DAC) with selectable $\times 2$, $\times 4$ and $\times 8$ interpolation filters. The device is optimized for multi-carrier and broadband wireless transmitters at sample rates of up to 1 Gsps. Supplied from a 3.3 V and a 1.8 V source, the DAC1617D1G0 integrates a differential scalable output current up to 34 mA.

The Serial Peripheral Interface (SPI) provides full control of the DAC1617D1G0.

The DAC1617D1G0 integrates a Low Voltage Differential Signaling (LVDS) Double Data Rate (DDR) receiver interface, with an on-chip $100\ \Omega$ termination. The LVDS DDR interface accepts a multiplex input data stream such as interleaved or folded. An internal LVDS input auto-calibration ensures the robustness and stability of the interface.

Digital on-chip modulation converts the complex I and Q inputs from baseband to IF. A 40-bit Numerically Controlled Oscillator (NCO) sets the mixer frequency. High resolution internal gain, phase and offset control provide outstanding image and Local Oscillator (LO) signal rejection at the system analog modulator output.

An inverse $(\sin x) / x$ function ensures a controlled flatness 0.5 dB for high bandwidths at the DAC output.

Multiple device synchronization allows synchronization of the outputs of multiple DAC devices. MDS guarantees a maximum skew of one output clock period between several devices.

The DAC1617D1G0 includes a very low noise capacitor-free integrated Phase-Locked Loop (PLL) multiplier which generates a DAC clock rate from the LVDS clock rate.

The DAC1617D1G0 is available in an HVQFN72 package (10 mm \times 10 mm).

2. Features and benefits

- Dual-channel 16-bit resolution
- 1 Gsps maximum update rate
- Selectable $\times 2$, $\times 4$ and $\times 8$ interpolation filters
- Very low noise capacitor-free integrated Phase-Locked Loop (PLL)
- Synchronization of multiple DAC devices
- 3-wire or 4-wire mode SPI interface
- Differential scalable output current from 8.1 mA to 34 mA
- External analog offset control (10-bit auxiliary DACs)



- Embedded Numerically Controlled Oscillator (NCO) with 40-bit programmable frequency
- Embedded complex(I/Q) digital IF modulator
- 1.8 V and 3.3 V power supplies
- LVDS DDR compatible input interface with on-chip 100 Ω terminations
- LVDS DDR input clock up to 370 MHz
- LVDS or LVPECL compatible DAC clock
- Interleaved or folded I and Q data input mode
- High resolution internal digital gain and offset control to support high performance IQ-modulator image rejection
- Internal phase correction
- Inverse (sin x) / x function
- Power-down mode and Sleep mode; 5-bit NCO low-power mode
- On-chip 1.25 V reference
- Industrial temperature range -40 °C to +85 °C
- 72 pins small form factor HVQFN package

3. Applications

- Wireless infrastructure: LTE, WiMAX, GSM, CDMA, WCDMA, TD-SCDMA
- Communications: LMDS/MMDS, point-to-point
- Direct Digital Synthesis (DDS)
- Broadband wireless systems
- Digital radio links
- Instrumentation
- Automated Test Equipment (ATE)

4. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|---------------|---------|--|----------|
| | Name | Description | Version |
| DAC1617D1G0HN | HVQFN72 | plastic thermal enhanced very thin quad flat package; no leads; 72 terminals; body 10 × 10 × 0.85 mm | SOT813-3 |

5. Block diagram

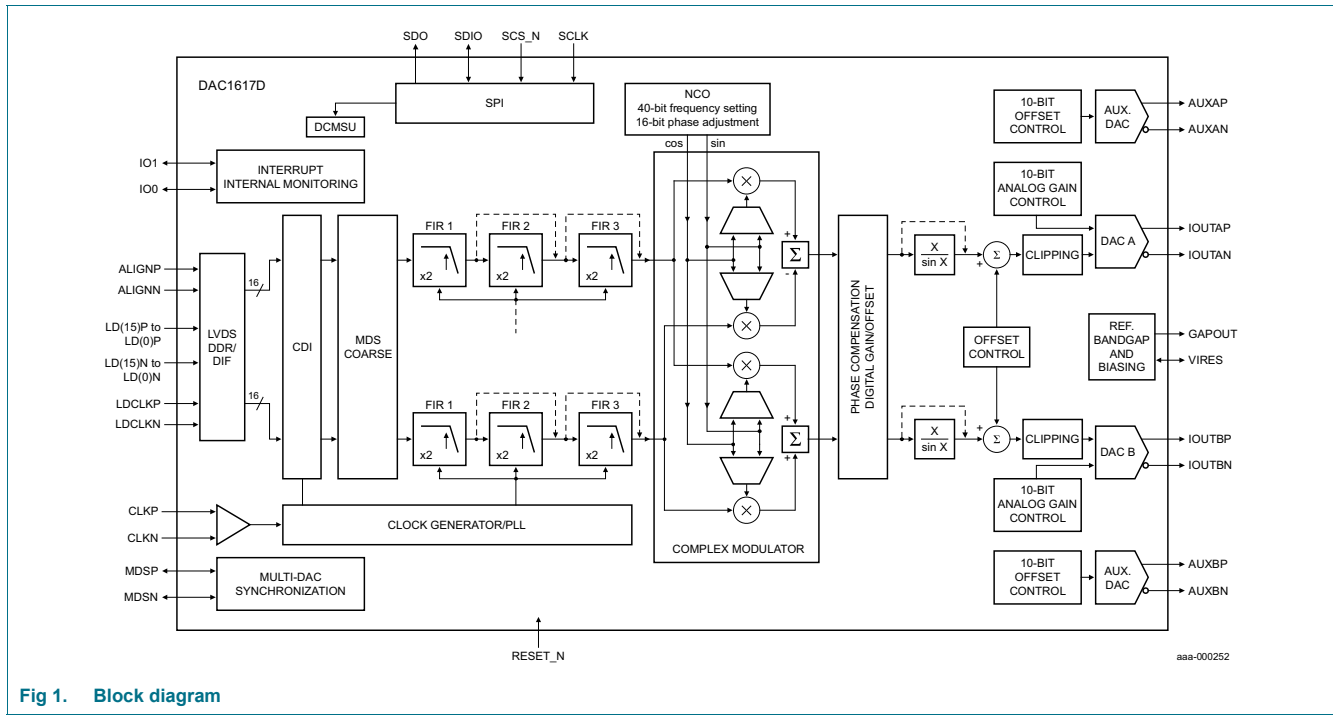


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

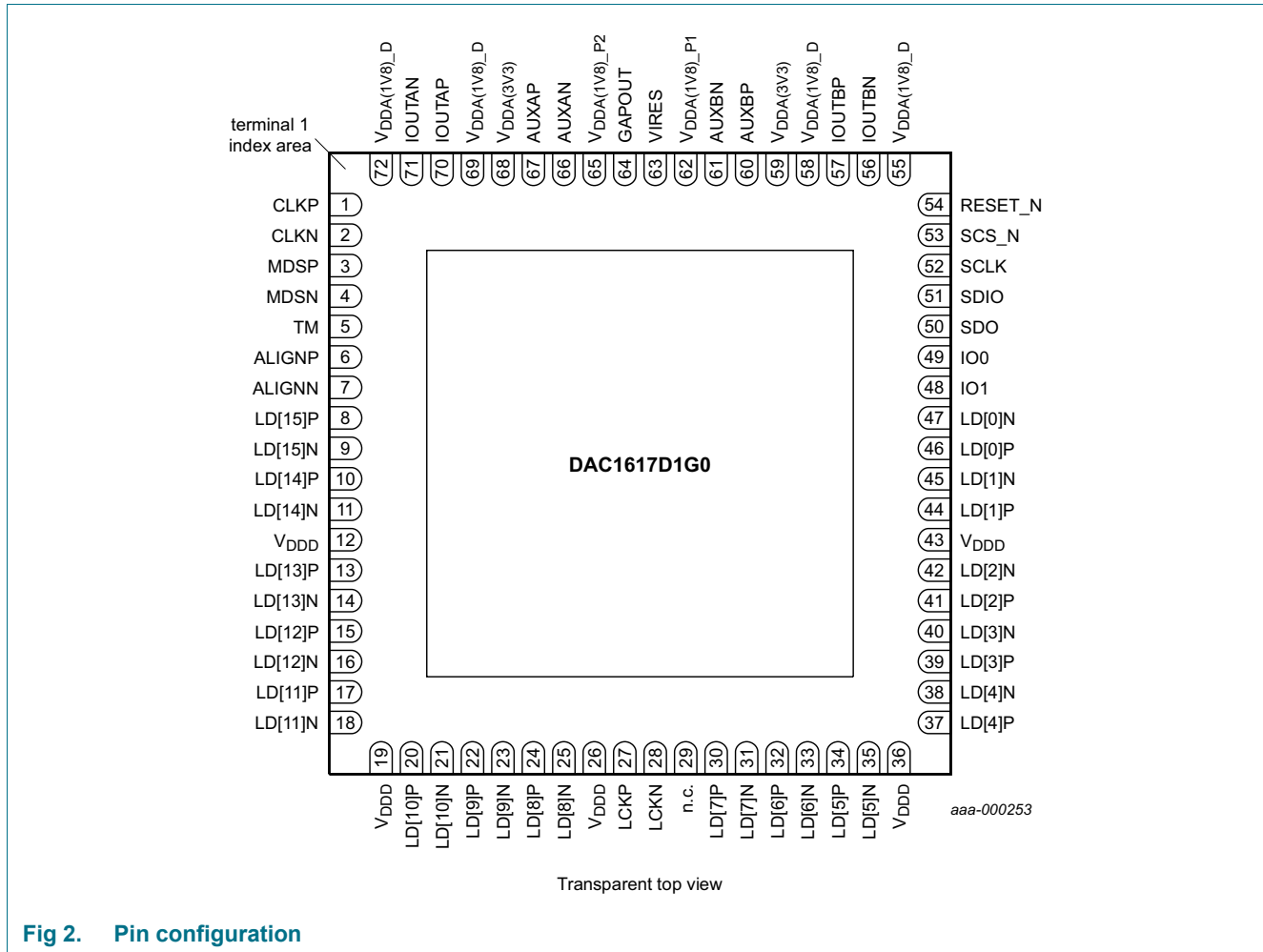


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Type ^[1] | Description |
|---------|-----|---------------------|--|
| CLKP | 1 | I | DAC clock positive input |
| CLKN | 2 | I | DAC clock negative input |
| MDSP | 3 | IO | multi-device synchronization positive signal |
| MDSN | 4 | IO | multi-device synchronization negative signal |
| TM | 5 | I | Test mode selection (connect to GND) |
| ALIGNP | 6 | I | positive input for data alignment |
| ALIGNN | 7 | I | negative input for data alignment |
| LD[15]P | 8 | I | LVDS positive input bit 15 ^[2] |
| LD[15]N | 9 | I | LVDS negative input bit 15 ^[2] |

Table 2. Pin description ...continued

| Symbol | Pin | Type ^[1] | Description |
|-----------------|-----|---------------------|---|
| LD[14]P | 10 | I | LVDS positive input bit 14 ^[2] |
| LD[14]N | 11 | I | LVDS negative input bit 14 ^[2] |
| V _{DD} | 12 | P | digital power supply |
| LD[13]P | 13 | I | LVDS positive input bit 13 ^[2] |
| LD[13]N | 14 | I | LVDS negative input bit 13 ^[2] |
| LD[12]P | 15 | I | LVDS positive input bit 12 ^[2] |
| LD[12]N | 16 | I | LVDS negative input bit 12 ^[2] |
| LD[11]P | 17 | I | LVDS positive input bit 11 ^[2] |
| LD[11]N | 18 | I | LVDS negative input bit 11 ^[2] |
| V _{DD} | 19 | P | digital power supply |
| LD[10]P | 20 | I | LVDS positive input bit 10 ^[2] |
| LD[10]N | 21 | I | LVDS negative input bit 10 ^[2] |
| LD[9]P | 22 | I | LVDS positive input bit 9 ^[2] |
| LD[9]N | 23 | I | LVDS negative input bit 9 ^[2] |
| LD[8]P | 24 | I | LVDS positive input bit 8 ^[2] |
| LD[8]N | 25 | I | LVDS negative input bit 8 ^[2] |
| V _{DD} | 26 | P | digital power supply |
| LCKP | 27 | I | LVDS positive data clock input |
| LCKN | 28 | I | LVDS negative data clock input |
| n.c. | 29 | G | not connected |
| LD[7]P | 30 | I | LVDS positive input bit 7 ^[2] |
| LD[7]N | 31 | I | LVDS negative input bit 7 ^[2] |
| LD[6]P | 32 | I | LVDS positive input bit 6 ^[2] |
| LD[6]N | 33 | I | LVDS negative input bit 6 ^[2] |
| LD[5]P | 34 | I | LVDS positive input bit 5 ^[2] |
| LD[5]N | 35 | I | LVDS negative input bit 5 ^[2] |
| V _{DD} | 36 | P | digital power supply |
| LD[4]P | 37 | I | LVDS positive input bit 4 ^[2] |
| LD[4]N | 38 | I | LVDS negative input bit 4 ^[2] |
| LD[3]P | 39 | I | LVDS positive input bit 3 ^[2] |
| LD[3]N | 40 | I | LVDS negative input bit 3 ^[2] |
| LD[2]P | 41 | I | LVDS positive input bit 2 ^[2] |
| LD[2]N | 42 | I | LVDS negative input bit 2 ^[2] |
| V _{DD} | 43 | P | digital power supply |
| LD[1]P | 44 | I | LVDS positive input bit 1 ^[2] |
| LD[1]N | 45 | I | LVDS negative input bit 1 ^[2] |
| LD[0]P | 46 | I | LVDS positive input bit 0 ^[2] |
| LD[0]N | 47 | I | LVDS negative input bit 0 ^[2] |
| IO1 | 48 | IO | IO port bit 1 |
| IO0 | 49 | IO | IO port bit 0 |
| SDO | 50 | O | SPI data output |

Table 2. Pin description ...continued

| Symbol | Pin | Type ^[1] | Description |
|--------------------------|-----|---------------------|--|
| SDIO | 51 | IO | SPI data input/output |
| SCLK | 52 | I | SPI clock |
| SCS_N | 53 | I | SPI chip select (active LOW) |
| RESET_N | 54 | I | general reset (active LOW) |
| V _{DDA(1V8)_D} | 55 | P | 1.8 V analog power supply (DAC core) |
| IOUTBN | 56 | O | complementary DAC B output current |
| IOUTBP | 57 | O | DAC B output current |
| V _{DDA(1V8)_D} | 58 | P | 1.8 V analog power supply (DAC core) |
| V _{DDA(3V3)} | 59 | P | 3.3 V analog power supply |
| AUXBP | 60 | O | auxiliary DAC B output current |
| AUXBN | 61 | O | complementary auxiliary DAC B output current |
| V _{DDA(1V8)_P1} | 62 | P | 1.8 V analog power supply (PLL) |
| VIRES | 63 | IO | DAC biasing resistor |
| GAPOUT | 64 | IO | band gap input/output voltage |
| V _{DDA(1V8)_P2} | 65 | P | 1.8 V analog power supply (PLL) |
| AUXAN | 66 | O | complementary auxiliary DAC A output current |
| AUXAP | 67 | O | auxiliary DAC A output current |
| V _{DDA(3V3)} | 68 | P | 3.3 V analog power supply |
| V _{DDA1V8_D} | 69 | P | 1.8 V analog power supply (DAC core) |
| IOUTAP | 70 | O | DAC A output current |
| IOUTAN | 71 | O | complementary DAC A output current |
| V _{DDA(1V8)_D} | 72 | P | 1.8 V analog power supply (DAC core) |
| GND | H | G | ground (exposed die pad) |

[1] P: power supply; G: ground; I: input; O: output.

[2] The LVDS input data bus order can be reversed and each element can be swapped between P and N using dedicated registers (see Table 60).

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------|-------------------------------|--|---------------------|------|------|
| $V_{DDA(3V3)}$ | analog supply voltage (3.3 V) | | -0.5 | +4.6 | V |
| V_{DDD} | digital supply voltage | | -0.5 | +2.5 | V |
| $V_{DDA(1V8)}$ | analog supply voltage (1.8 V) | | ^[1] -0.5 | +2.5 | V |
| V_I | input voltage | input pins referenced to GND | -0.5 | +2.5 | V |
| V_O | output voltage | pins IOUTAP, IOUTAN, IOUTBP, IOUTBN, AUXAP, AUXAN, AUXBP and AUXBN referenced to GND | -0.5 | +4.6 | V |
| T_{stg} | storage temperature | | -55 | +150 | °C |
| T_{amb} | ambient temperature | | -40 | +85 | °C |
| T_j | junction temperature | | -40 | +125 | °C |

[1] Connect the analog 1.8 V power supply to pins VDDA1V8_D, VDDA1V8_P1, and VDDA1V8_P2.

8. Thermal characteristics

Table 4. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|---|------------|---------------------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | | ^[1] 16.2 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | | ^[1] 6.7 | K/W |

[1] Value for six-layer board in still air with a minimum of 49 thermal vias.

9. Characteristics

Table 5. Characteristics

$V_{DDA(1V8)} = 1.8\text{ V}$; $V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; Typical values measured at $T_{amb} = +25\text{ °C}$; $R_L = 50\ \Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

| Symbol | Parameter | Conditions | Test [1] | Min | Typ | Max | Unit |
|----------------|--------------------------------|---|----------|------|------|------|------|
| $V_{DDA(3V3)}$ | analog supply voltage (3.3 V) | | C | 3.15 | 3.3 | 3.45 | V |
| V_{DDD} | digital supply voltage | | C | 1.7 | 1.8 | 1.9 | V |
| $V_{DDA(1V8)}$ | analog supply voltage (1.8 V) | | C [2] | 1.7 | 1.8 | 1.9 | V |
| $I_{DDA(3V3)}$ | analog supply current (3.3 V) | Auxiliary DAC on | C | 51 | 55 | 59 | mA |
| I_{DDD} | digital supply current (1.8 V) | $f_s = 983.04\text{ 67}$; $\times 4$ interpolation; no NCO; MDS off | C | 475 | 525 | 585 | mA |
| | | $f_s = 620\text{ Msps}$; $\times 2$ interpolation; NCO on; no MDS | C | 400 | 450 | 500 | mA |
| $I_{DDA(1V8)}$ | analog supply current (1.8 V) | $f_s = 983.04\text{ Msps}$; 1 V (p-p) | C [2] | 207 | 218 | 230 | mA |
| | | $f_s = 620\text{ Msps}$; 1 V (p-p) | C | 207 | 218 | 230 | mA |
| P_{tot} | total power dissipation | $f_s = 983.04\text{ Msps}$; $\times 4$ interpolation; NCO off; MDS off | C | - | 1580 | - | mW |
| | | $f_s = 983.04\text{ Msps}$; $\times 4$ interpolation; 5-bit NCO; MDS off | C | - | 1500 | - | mW |
| | | $f_s = 620\text{ Msps}$; $\times 2$ interpolation; 5-bit NCO; MDS off | - | - | 1370 | - | mW |
| | | power-down using SPI register | C | - | 63 | - | mW |

Clock inputs (pins CLKP, CLKN)

| | | | | | | | |
|-------------------------------|----------------------------------|--------------|---|-----|-----|------|------------|
| $V_{i(\text{clk})\text{dif}}$ | differential clock input voltage | peak-to-peak | C | 150 | - | 1000 | mV |
| R_i | input resistance | | D | - | 200 | - | k Ω |
| C_i | input capacitance | | D | - | 1 | - | pF |

Digital inputs (pins LD[15]P to LD[0]P, LD[15]N to LD[0]N, LCKP and LCKN, ALIGNP and ALIGNN)

| | | | | | | | |
|-------------------|--------------------------------------|---|---|------|-----|------|----------|
| V_i | input voltage | $ V_{\text{gpd}} < 50\text{ mV}^{[3]}$ | C | 825 | - | 1575 | mV |
| V_{idth} | input differential threshold voltage | $ V_{\text{gpd}} < 50\text{ mV}^{[3]}$ | C | -100 | - | +100 | mV |
| R_i | input resistance | | D | - | 100 | - | Ω |
| C_i | input capacitance | | D | - | 0.8 | - | pF |
| | | pins LCKP and LCKN | D | - | 0.9 | - | pF |

Table 5. Characteristics ...continued

$V_{DDA(1V8)} = 1.8\text{ V}$; $V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; Typical values measured at $T_{amb} = +25\text{ }^{\circ}\text{C}$; $R_L = 50\ \Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

| Symbol | Parameter | Conditions | Test [1] | Min | Typ | Max | Unit |
|--|--|--|----------|-------------------|-------|-------------------|-------------------------|
| Digital inputs/outputs (pins MDSN, MDSP) | | | | | | | |
| $V_{O(dif)(p-p)}$ | peak-to-peak differential output voltage | | C | - | 500 | - | mV |
| C_i | input capacitance | between GND and pin MDSN or MDSP | D | - | 0.6 | - | pF |
| R_i | input resistance | | D | - | 100 | - | Ω |
| V_i | input voltage | $ V_{gpd} < 50\text{ mV}^{[3]}$ | C | 825 | - | 1575 | mV |
| V_{idth} | input differential threshold voltage | $ V_{gpd} < 50\text{ mV}^{[3]}$ | C | -100 | - | +100 | mV |
| Digital inputs/outputs (pins SDO, SDIO, SCLK, SCS_N, RESET_N, IO0, IO1) | | | | | | | |
| V_{IL} | LOW-level input voltage | | C | GND | - | $0.3V_{DDD(1V8)}$ | V |
| V_{IH} | HIGH-level input voltage | | C | $0.7V_{DDD(1V8)}$ | - | $V_{DDD(1V8)}$ | V |
| V_{OL} | LOW-level output voltage | pins IO0, IO1, SDO and SDIO | C | GND | - | $0.1V_{DDD(1V8)}$ | V |
| V_{OH} | HIGH-level output voltage | pins IO0, IO1, SDO and SDIO | C | $0.9V_{DDD(1V8)}$ | - | $V_{DDD(1V8)}$ | V |
| I_{IL} | LOW-level input current | maximum VIL | I | -10 | - | +10 | μA |
| I_{IH} | HIGH-level input current | maximum VIL | I | -10 | - | +10 | μA |
| C_i | input capacitance | | D | - | 2.2 | - | pF |
| Analog outputs (pins IOUTAP, IOUTAN, IOUTBP, IOUTBN) | | | | | | | |
| I_{bias} | bias current | DC current | D | - | 2.5 | - | mA |
| $I_{O(fs)}$ | full-scale output current | controlled by the analog GAIN registers (see Table 32) | D | 8.1 | - | 34 | mA |
| | | default value | D | - | 20 | - | mA |
| V_O | output voltage | compliance range | D | 2.3 | - | $V_{DDA(3V3)}$ | V |
| $V_{O(cm)}$ | common-mode output voltage | 1 V (p-p) DAC output | D | - | 3 | - | V |
| | | 2 V (p-p) DAC output | | - | 2.8 | - | V |
| R_o | output resistance | | D | - | 250 | - | k Ω |
| C_o | output capacitance | between pins OUTAN and OUTBN and pins OUTBN and OUTBP | D | - | 5 | - | pF |
| ΔE_O | offset error variation | | D | - | <tdb> | - | ppm/ $^{\circ}\text{C}$ |

Table 5. Characteristics ...continued

$V_{DDA(1V8)} = 1.8\text{ V}$; $V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; Typical values measured at $T_{amb} = +25\text{ }^{\circ}\text{C}$; $R_L = 50\ \Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

| Symbol | Parameter | Conditions | Test [1] | Min | Typ | Max | Unit |
|--|------------------------------------|---|----------|-----|------|-----|-------------------------|
| ΔE_G | gain error variation | | D | - | <td> | - | ppm/ $^{\circ}\text{C}$ |
| INL | integral non-linearity | | D | - | <td> | - | LSB |
| DNL | differential non-linearity | | D | - | <td> | - | LSB |
| Reference voltage output (pin GAPOUT) | | | | | | | |
| $V_{O(ref)}$ | reference output voltage | $T_{amb} = +25\text{ }^{\circ}\text{C}$ | I | - | 1.22 | - | V |
| $I_{O(ref)}$ | reference output current | 1.25 V external voltage | D | - | 40 | - | μA |
| Analog auxiliary outputs (pins AUXAP, AUXAN, AUXBP and AUXBN) | | | | | | | |
| $I_{O(fs)}$ | full-scale output current | auxiliary DAC A; differential outputs | I | - | 3.1 | - | mA |
| | | auxiliary DAC B; differential outputs | I | - | 3.1 | - | mA |
| $V_{O(aux)}$ | auxiliary output voltage | compliance range | D | 0 | - | 2.3 | V |
| LVDS input timing | | | | | | | |
| f_{data} | data rate | $f_{s(max)}$ specification must be respected ($f_s = f_{data} \times \text{interpolation factor}$) | C | - | - | 370 | MHz |
| $t_{sk(clk-D)}$ | skew time from clock to data input | $f_{DATA} = 184.32\text{ MHz}$ | C | 800 | - | 830 | ps |
| | | $f_{DATA} = 245.76\text{ MHz}$ | C | 500 | - | 675 | ps |
| | | $f_{DATA} = 307.2\text{ MHz}$ | C | 300 | - | 520 | ps |
| | | $f_{DATA} = 368.64\text{ MHz}$ | C | 150 | - | 500 | ps |

Table 5. Characteristics ...continued

$V_{DDA(1V8)} = 1.8\text{ V}$; $V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; Typical values measured at $T_{amb} = +25\text{ °C}$; $R_L = 50\ \Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

| Symbol | Parameter | Conditions | Test [1] | Min | Typ | Max | Unit |
|------------|-------------|--|----------|-------|-----|-----|------|
| t_{su} | set-up time | manual tuning mode (see Figure 16); depends on LDCLK_DEL[3:0] | | | | | |
| | | 0000 | C | -300 | - | - | ps |
| | | 0001 | C | -365 | - | - | ps |
| | | 0010 | C | -440 | - | - | ps |
| | | 0011 | C | -520 | - | - | ps |
| | | 0100 | C | -590 | - | - | ps |
| | | 0101 | C | -675 | - | - | ps |
| | | 0110 | C | -750 | - | - | ps |
| | | 0111 | C | -830 | - | - | ps |
| | | 1000 | C | -845 | - | - | ps |
| | | 1001 | C | -845 | - | - | ps |
| | | 1010 | C | -1000 | - | - | ps |
| | | 1011 | C | -1100 | - | - | ps |
| | | 1100 | C | -1220 | - | - | ps |
| | | 1101 | C | -1290 | - | - | ps |
| | | 1110 | C | -1360 | - | - | ps |
| 1111 | C | -1450 | - | - | ps | | |
| t_{hold} | hold time | manual tuning mode (see Figure 15); depends on LDCLK_DEL[3:0]: | | | | | |
| | | 0000 | C | 790 | - | - | ps |
| | | 0001 | C | 870 | - | - | ps |
| | | 0010 | C | 950 | - | - | ps |
| | | 0011 | C | 1055 | - | - | ps |
| | | 0100 | C | 1140 | - | - | ps |
| | | 0101 | C | 1230 | - | - | ps |
| | | 0110 | C | 1360 | - | - | ps |
| | | 0111 | C | 1460 | - | - | ps |
| | | 1000 | C | 1900 | - | - | ps |
| | | 1001 | C | 2075 | - | - | ps |
| | | 1010 | C | 2250 | - | - | ps |
| | | 1011 | C | 2400 | - | - | ps |
| | | 1100 | C | 2560 | - | - | ps |
| | | 1101 | C | 2740 | - | - | ps |
| | | 1110 | C | 2900 | - | - | ps |
| 1111 | C | 3000 | - | - | ps | | |

Table 5. Characteristics ...continued

$V_{DDA(1V8)} = 1.8\text{ V}$; $V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; Typical values measured at $T_{amb} = +25\text{ }^{\circ}\text{C}$; $R_L = 50\ \Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

| Symbol | Parameter | Conditions | Test [1] | Min | Typ | Max | Unit |
|--|-----------------------------|--|----------|------|------------|------|------|
| DAC output timing | | | | | | | |
| $f_{s(max)}$ | sampling rate | | C | 1000 | - | - | MspS |
| t_s | settling time | to $\pm 0.5\text{ LSB}$ | D | - | 20 | - | ns |
| Internal PLL timing | | | | | | | |
| f_s | sampling rate | | D | 50 | - | 1000 | MspS |
| 40-bit NCO frequency range; $f_s = 1000\text{ MspS}$ | | | | | | | |
| f_{NCO} | NCO frequency | two's complement coding | | | | | |
| | | register value = 800000000h | D | - | -500 | - | MHz |
| | | register value = FFFFFFFFh | D | - | -0.9095 | - | mHz |
| | | register value = 000000000h | D | - | 0 | - | Hz |
| | | register value = 000000001h | D | - | +0.9095 | - | mHz |
| | | register value = 7FFFFFFFh | D | - | +499.99909 | - | MHz |
| f_{step} | step frequency | | D | - | 0.9095 | - | mHz |
| Low-power NCO frequency range; $f_s = 1000\text{ MHz}$ | | | | | | | |
| f_{NCO} | NCO frequency | two's complement coding | | | | | |
| | | register value = F800000000h | D | - | -500 | - | MHz |
| | | register value = F800000000h | D | - | -31.25 | - | MHz |
| | | register value = 0000000000h | D | - | 0 | - | Hz |
| | | register value = 0800000000h | D | - | +31.25 | - | MHz |
| | | register value = 7FFFFFFFh | D | - | +468.75 | - | MHz |
| f_{step} | step frequency | | D | - | 31.25 | - | MHz |
| Dynamic performance | | | | | | | |
| SFDR | spurious-free dynamic range | $f_{data} = 245.76\text{ MHz}$; $f_s = 983.04\text{ MspS}$; $BW = f_s / 2$ | I | - | 78 | - | dBc |
| | | $f_o = 20\text{ MHz at } -1\text{ dBFS}$ | | | | | |
| | | $f_{data} = 184.32\text{ MHz}$; $f_s = 737.28\text{ MspS}$; $BW = f_s / 2$ | | | | | |
| | | $f_o = 20\text{ MHz at } -1\text{ dBFS}$ | | | 78 | | dBc |

Table 5. Characteristics ...continued

$V_{DDA(1V8)} = 1.8\text{ V}$; $V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; Typical values measured at $T_{amb} = +25\text{ }^{\circ}\text{C}$; $R_L = 50\text{ }\Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

| Symbol | Parameter | Conditions | Test [1] | Min | Typ | Max | Unit |
|---------------------|--|---|----------|-----|------|-----|--------|
| SFDR _{RBW} | restricted bandwidth spurious-free dynamic range | $f_{data} = 245.76\text{ MHz}$; $f_s = 983.04\text{ Msps}$; $f_o = 150\text{ MHz}$ | | - | | - | dBc |
| | | BW = 100 MHz | | - | 78 | - | dBc |
| | | BW = 180 MHz | | - | 78 | - | dBc |
| IMD3 | third-order intermodulation distortion | $f_{data} = 245.76\text{ MHz}$; $f_s = 983.04\text{ Msps}$; $f_{o1} = 20\text{ MHz}$; $f_{o2} = 21\text{ MHz}$; ×4 interpolation; output level = -1 dBFS | C | - | 75 | - | dBc |
| | | $f_{data} = 245.76\text{ MHz}$; $f_s = 983.04\text{ Msps}$; $f_{o1} = 152\text{ MHz}$; $f_{o2} = 155.1\text{ MHz}$; ×4 interpolation; output level = -1 dBFS | I | - | 75 | - | dBc |
| ACPR | adjacent channel power ratio | WCDMA pattern; $f_s = 983.04\text{ Msps}$; ×4 interpolation; $f_{NCO} = 153.6\text{ MHz}$ | | | | | |
| | | 1 carrier; BW = 5 MHz | C | - | 73 | - | dBc |
| | | 2 carriers; BW = 10 MHz | C | - | 70 | - | dBc |
| | | 4 carriers; BW = 20 MHz | C | - | 68 | - | dBc |
| NSD | noise spectral density | $f_s = 983.04\text{ Msps}$; ×4 interpolation; $f_o = 20\text{ MHz}$ at -1 dBFS | D | - | -158 | - | dBm/Hz |
| | | $f_s = 983.04\text{ Msps}$; ×4 interpolation; $f_o = 153.6\text{ MHz}$ at -1 dBFS | D | - | -155 | - | dBm/Hz |

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] Connect $V_{DDA(1V8)_D}$, $V_{DDA(1V8)_P1}$ and $V_{DDA(1V8)_P2}$ to the same 1.8 V analog power supply. Use dedicated filters for the three power pins.

[3] $|V_{gpd}|$ represents the ground potential difference voltage. This voltage is the result of current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground voltages.

10. Application information

10.1 General description

The DAC1617D1G0 is a dual 16-bit DAC operating up to 1000 Msps. Each DAC consists of a segmented architecture, comprising a 6-bit thermometer subDAC and a 10-bit binary weighted subDAC.

A maximum input LVDS DDR data rate of up to 370 MHz and a maximum output sampling rate of 1000 Msps ensure more flexibility for wide bandwidth and multi-carrier systems. The internal 40-bit NCO of the DAC1617D1G0 simplifies the frequency selection of the system. The DAC1617D1G0 provides x2, x4 or x8 interpolation filters that are useful for removing the undesired images.

Each DAC generates two complementary current outputs on pins IOUTAP and IOUTAN and pins IOUTBP and IOUTBN. These outputs provide a full-scale output current ($I_{O(fs)}$) of up to 34 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

High resolution internal gain, phase and offset control provide outstanding image and Local Oscillator (LO) signal rejection at the system analog modulator output.

Multiple device synchronization enables synchronization of the outputs of multiple DAC devices. MDS guarantees a maximum skew of one output clock period between several devices.

All functions can be set using an SPI interface.

10.2 Serial Peripheral Interface (SPI)

10.2.1 Protocol description

The DAC1617D1G0 serial interface is a synchronous serial communication port ensures easy interface with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both write and read mode.

This interface can be configured as a 3-wire type (pin SDIO as bidirectional pin) or 4-wire type (pins SDIO and SDO as unidirectional pins, input and output port, respectively). In both configurations, SCLK acts as the serial clock and SCS_N as the serial chip select.

Figure 3 shows the SPI protocol. An SCS_N signal follows each read/write operation. A LOW assertion enables it to drive the chip with 2 bytes to 5 bytes, depending on the content of the instruction byte (see Table 7).

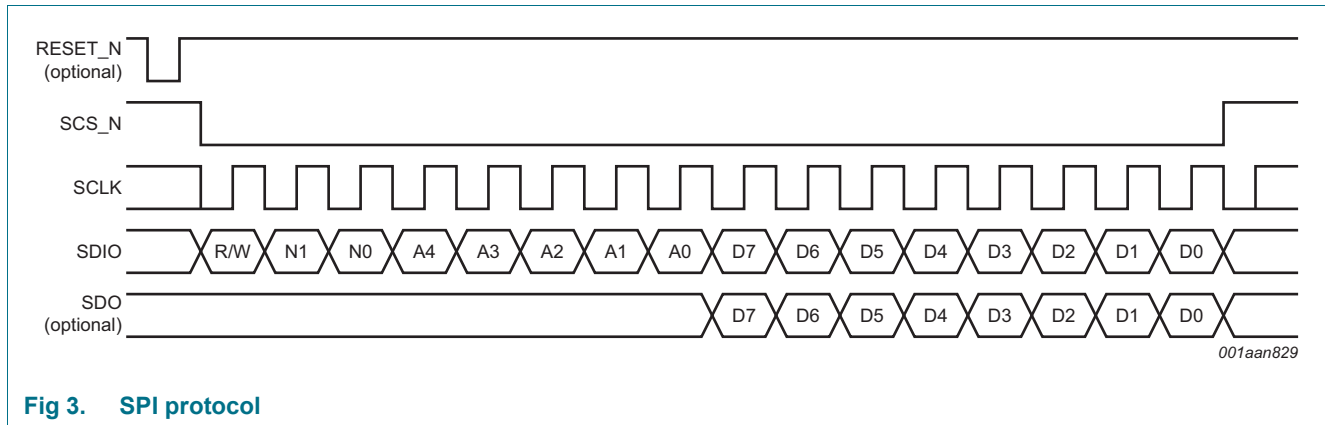


Fig 3. SPI protocol

R/W indicates the mode access (see Table 6)

Table 6. Read or Write mode access description

| R/W | Description |
|-----|----------------------|
| 0 | Write mode operation |
| 1 | Read mode operation |

Table 7 shows the number of bytes to be transferred. N1 and N0 indicate the number of bytes transferred after the instruction byte.

Table 7. Number of bytes transferred

| N1 | N0 | Number of bytes transferred |
|----|----|-----------------------------|
| 0 | 0 | 1 byte |
| 0 | 1 | 2 bytes |
| 1 | 0 | 3 bytes |
| 1 | 1 | 4 bytes |

A[4:0] indicates which register is being addressed. If a multiple transfer occurs, this address concerns the first register. The other registers follow directly in a decreasing order (see Table 21, Table 35 and Table 53).

The DAC1617D1G0 incorporates more than the 32 SPI registers allowed by the address value A[4:0]. It uses three SPI register pages (page_00, page_01, and page_0A), each containing 32 registers. The 32nd register of each page indicates which page is currently addressed (00h, 01h or 0Ah).

10.2.2 SPI timing description

The SPI interface can operate at a frequency up to 15 MHz. The SPI timings are shown in Figure 4.

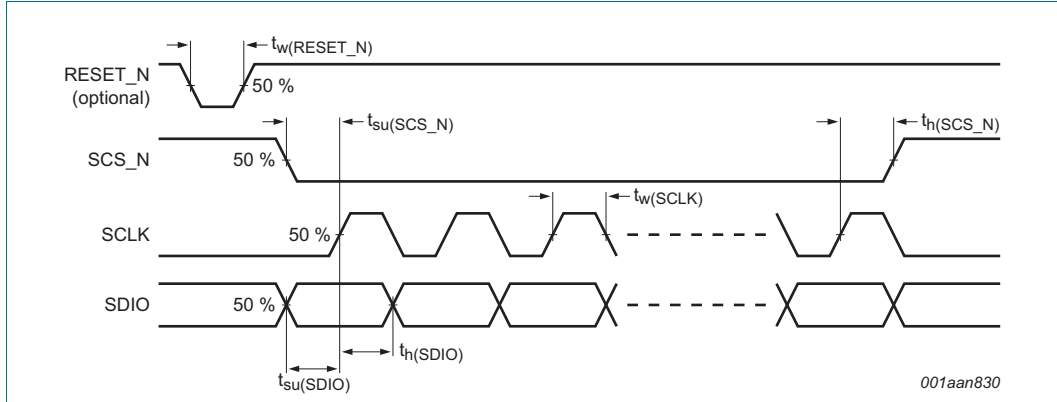


Fig 4. SPI timing diagram

The SPI timing characteristics are given in Table 8.

Table 8. SPI timing characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------------|---------------------|-----|-----|-----|------|
| f_{SCLK} | SCLK frequency | - | - | 25 | MHz |
| $t_w(\text{SCLK})$ | SCLK pulse width | 30 | - | - | ns |
| $t_{su}(\text{SCS_N})$ | SCS_N set-up time | 20 | - | - | ns |
| $t_h(\text{SCS_N})$ | SCS_N hold time | 20 | - | - | ns |
| $t_{su}(\text{SDIO})$ | SDIO set-up time | 10 | - | - | ns |
| $t_h(\text{SDIO})$ | SDIO hold time | 5 | - | - | ns |
| $t_w(\text{RESET_N})$ | RESET_N pulse width | 30 | - | - | ns |

10.3 Power-on sequence

There are three steps for the power-on sequence (see Figure 5):

1. The board is power-on. At the turn-on time, all DAC1617D1G0 supplies have reached their specification ranges.
2. At least 1 μs after the turn-on time pin RESET_N must be released.
3. When the DAC clock and LVDS clock are stable, the SPI configuration is sent to the DAC1617D1G0. Writing 0 in bits RST_DCLK and RST_LCLK of the register MAIN_CNTRL (see Table 54) starts the automatic calibration. 30 μs after this calibration, the DAC1617D1G0 is operational.

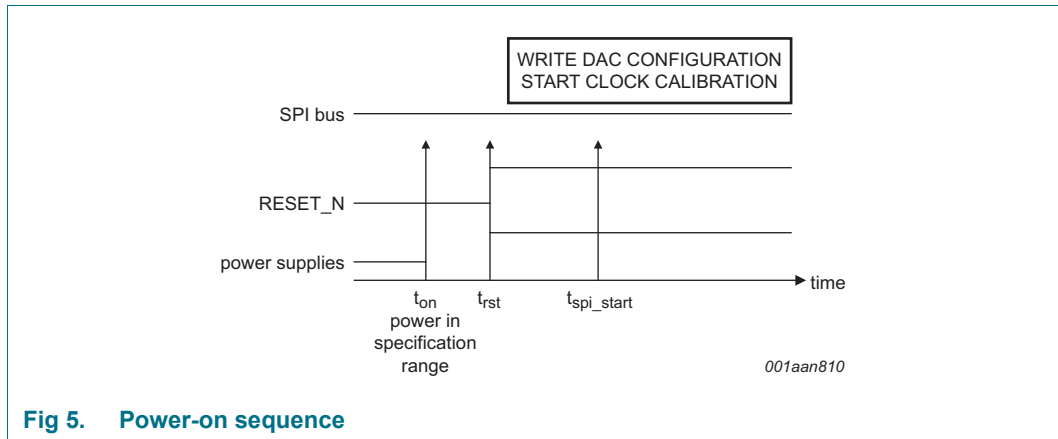


Fig 5. Power-on sequence

10.4 LVDS Data Input Format (DIF) block

The Data Input Formatting (DIF) block captures and resynchronizes data on the LVDS bus with its own LCLKP/LCLKN clock. Each LVDS input buffer has an internal resistance of 100 Ω, so an external resistor is not required. The DIF block includes two subblocks:

- **LVDS receiver:**

Provides high flexibility for the LVDS interface, especially for the PCB layout and the control of the input port polarity and the input port mapping.

- **Data format block:**

Enables the adaptation, which ensures the support of several data encoding modes.

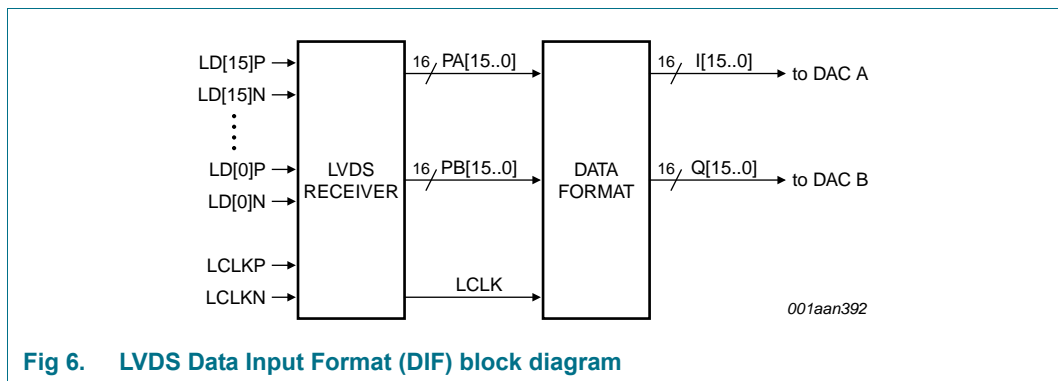


Fig 6. LVDS Data Input Format (DIF) block diagram

10.4.1 Input port polarity

The polarity of each individual LVDS input (LD[15]P to LD[0]P and LD[15]N to LD[0]N) can be changed. This ensures a much easier PCB layout design. The input polarity is controlled with bits LD_POL[15:0] (see Table 59).

10.4.2 Input port mapping

Inverting the order of the LSB and the MSB of the LVDS bus using bit WORD_SWAP in register LD_CNTRL (see Table 60) also simplifies the design of the PCB (see Table 9).

Table 9. Input LVDS bus swapping

| Internal LVDS bus | External LVDS bus (WORD_SWAP = 0) | External LVDS bus (WORD_SWAP = 1) |
|-------------------|-----------------------------------|-----------------------------------|
| LDI[15]P,N | LD[15]P,N | LD[0]P,N |
| LDI[14]P,N | LD[14]P,N | LD[1]P,N |
| LDI[13]P,N | LD[13]P,N | LD[2]P,N |
| LDI[12]P,N | LD[12]P,N | LD[3]P,N |
| LDI[11]P,N | LD[11]P,N | LD[4]P,N |
| LDI[10]P,N | LD[10]P,N | LD[5]P,N |
| LDI[9]P,N | LD[9]P,N | LD[6]P,N |
| LDI[8]P,N | LD[8]P,N | LD[7]P,N |
| LDI[7]P,N | LD[7]P,N | LD[8]P,N |
| LDI[6]P,N | LD[6]P,N | LD[9]P,N |
| LDI[5]P,N | LD[5]P,N | LD[10]P,N |
| LDI[4]P,N | LD[4]P,N | LD[11]P,N |
| LDI[3]P,N | LD[3]P,N | LD[12]P,N |
| LDI[2]P,N | LD[2]P,N | LD[13]P,N |
| LDI[1]P,N | LD[1]P,N | LD[14]P,N |
| LDI[0]P,N | LD[0]P,N | LD[15]P,N |

10.4.3 Input port swapping

The LVDS DDR receiver block internally maps the incoming LVDS data bus into two buses with a single data rate (Figure 7).

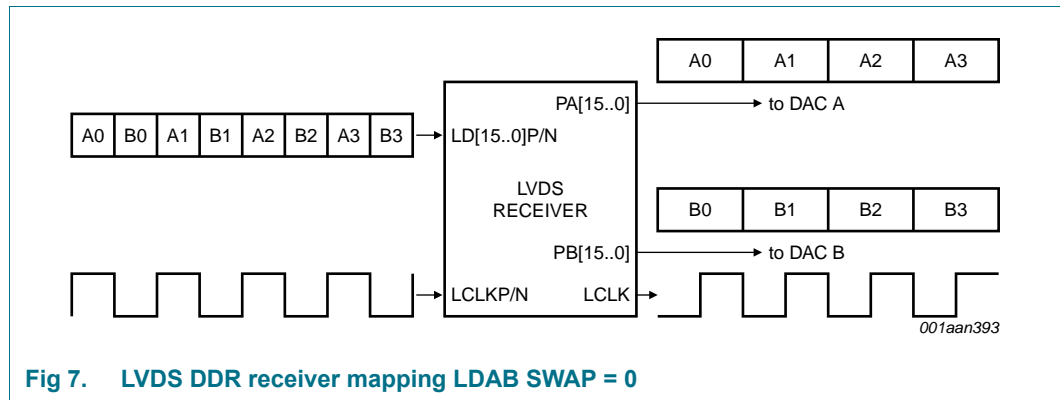
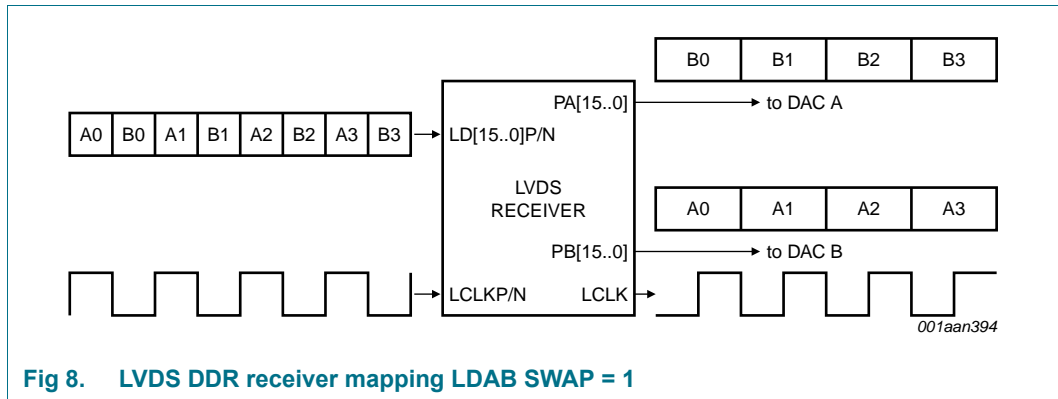


Fig 7. LVDS DDR receiver mapping LDAB SWAP = 0

These two buses can be swapped internally using bit LDAB_SWAP of register LD_CNTRL (see Table 60 and Figure 8).



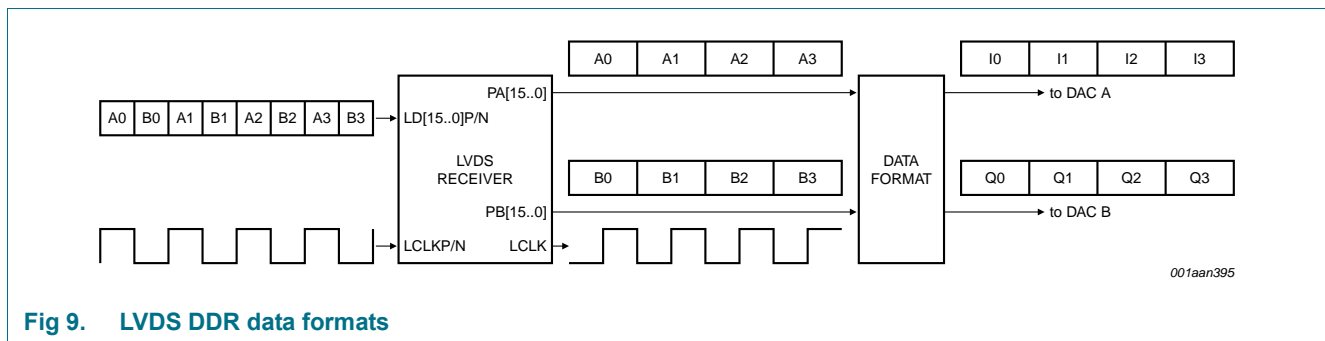
10.4.4 Input port formatting

The LVDS DDR input bus multiplexes two 16-bit streams. The LVDS receiver block demultiplexes these two streams.

The two streams can carry two data formats:

- Folded
- Interleaved

The data format block is in charge of the data format adaptation (see Figure 9).



The DAC1617D1G0 can correctly decode the input stream using bit IQ_FORMAT of register LD_CNTRL (see Table 60), because it can determine which format is used on the LVDS DDR bus.

Table 10 shows the format mapping between the LVDS input data and the data sent to the two DAC channels depending on the data format selected.

Table 10. Folded and interleaved format mapping

| Data format | Data bit mapping |
|------------------------------------|--|
| interleaved format (IQ_FORMAT = 1) | $I_n[15..0] = A_n[15..0]; Q_n[15..0] = B_n[15..0]$ |
| folded format (IQ_FORMAT = 0) | $I_n[15..8] = A_n[15..8]; I_n[7..0] = B_n[15..8]$ $Q_n[15..8] = A_n[7..0]; Q_n[7..0] = B_n[7..0]$ |

10.4.5 Data parity/data enable

The ALIGN pins can be used in several ways:

- As datastream start flag for Multiple Devices Synchronization (see Section 10.13).
- As LVDS data enable which can be used to insert a DC level into the datastream. The SEL_EN bits in register LD_CNTRL (see Table 60) enable the programming of this mode. The DC level for both channels is selected using registers I_DC_LVL and Q_DC_LVL (see Table 62)
- As parity bit for the LD[15:0] to detect disruptions at the LVDS-input port bit PARITYC in register LD_CNTRL (see Table 60) enabling the control of this mode. A Parity error can generate an interrupt (INTR) reported on either IO0 or IO1 pin

10.5 Interrupt controller

The DAC1617D1G0 incorporates an interrupt controller that makes notifying a host-controller in case of an internal event. The INTR-signal can be made available on one of the IO pins. The polarity on the IO pins is programmable.

The internal event that must be tracked and generates an interrupt can be selected using the INTR_EN register (see Table 45). Two types of interrupt sources are considered:

- The ready-indicators (MAQ_RDY_B, MAQ_RDY_A, AUTO_CAL_RDY, and AUTO_DL_RDY; register INTR_FLAGS; see Table 47) notify the host-interface that the corresponding process (invoked by the host interface) has been finalized
- The error flags indicate that a failure has been detected. For example, on the LVDS-interface it is possible to check for parity errors and/or to monitor if the internal timing of the LVDS clock delay has changed since the calibration. Errors like these can result in critical timings within the Clock Domain Interface (CDI) which transfers the data from the LCLK to the DCLK domain

The selected event that has invoked the interrupt can be determined using the INTR_FLAGS register (see Table 47). The flags and the INTR signal are reinitialized by setting the INTR_CLEAR control bit in register INTR_CTRL (see Table 45).

10.6 General-purpose IO pins

The DAC1617D1G0 provides two general-purpose pins, IO0 and IO1. These pins can be used to observe the interrupt signal (INTR) or other internal signals (internal clocks, LVDS data, etc.). These pins can also be used as generic outputs to control external devices.

The internal signals that must be observed on these pins are selected using registers IO_MUX0, IO_MUX1, and IO_MUX2 (see Table 63 and Table 64).

10.7 Input clock

The DAC1617D1G0 operates with two clocks, one for the LVDS DDR interface and one for the DAC core.

10.7.1 LVDS DDR clock

The LVDS DDR clock can be interfaced as shown in Figure 10 because the clock buffer contains a 100 Ω internal resistor.

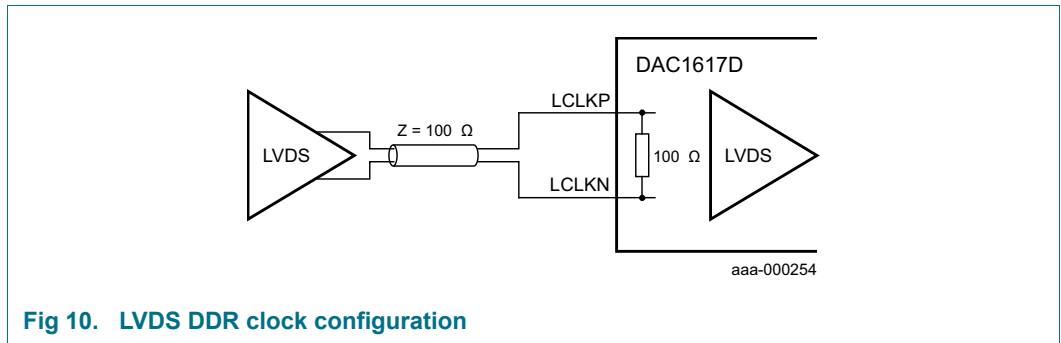


Fig 10. LVDS DDR clock configuration

10.7.2 DAC core clock

The DAC core clock can achieve a frequency of up to 1 Gbps. It includes internal biasing to support both AC-coupling and DC-coupling. The clock can be easily connected to any LVDS, CML or PECL clock sources.

Depending on the interface selected, the hardware configuration varies (see Figure 11 to Figure 13).

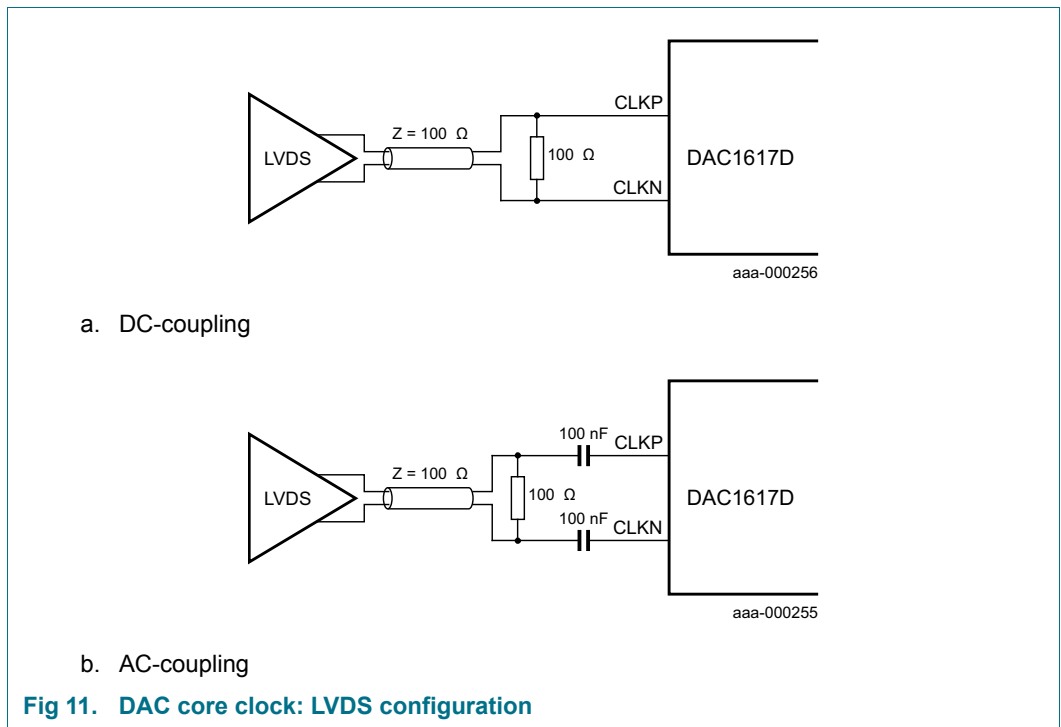
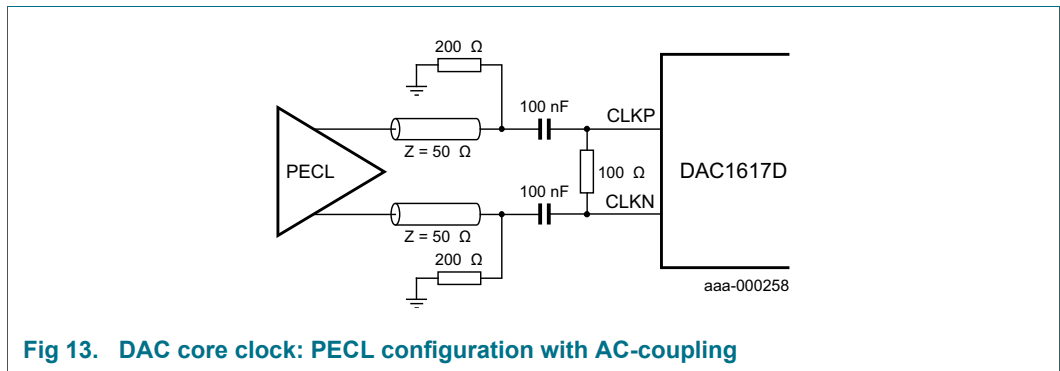
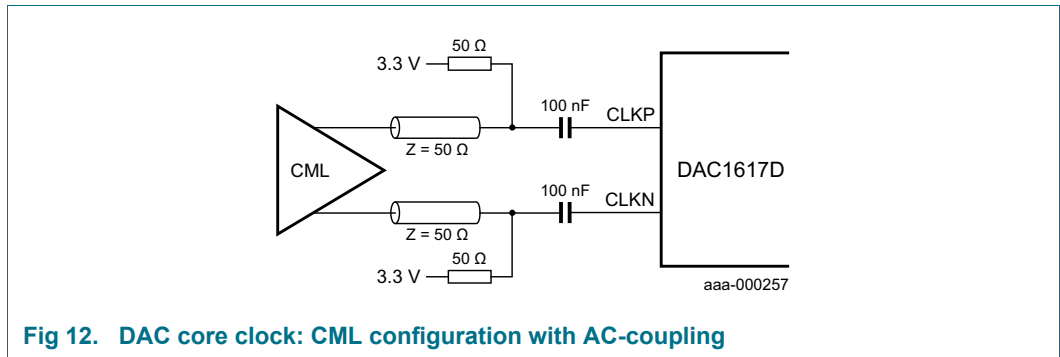


Fig 11. DAC core clock: LVDS configuration



10.8 Timing

The DAC1617D1G0 can operate at an update rate (f_s) of up to 1 Gbps and with an input data rate (f_{data}) of up to 370 MHz.

The sampling position of the LVDS data can be tuned using a 16-step compensation delay clock. An internal clock is generated to define the exact sampling position of the LVDS data (see Figure 14, signals LDCLKPcp and LDCLKNcp) which depends on the compensation delay.

Figure 14 shows how the compensation delay helps to recover the LVDS DDR data on both the A and B paths.

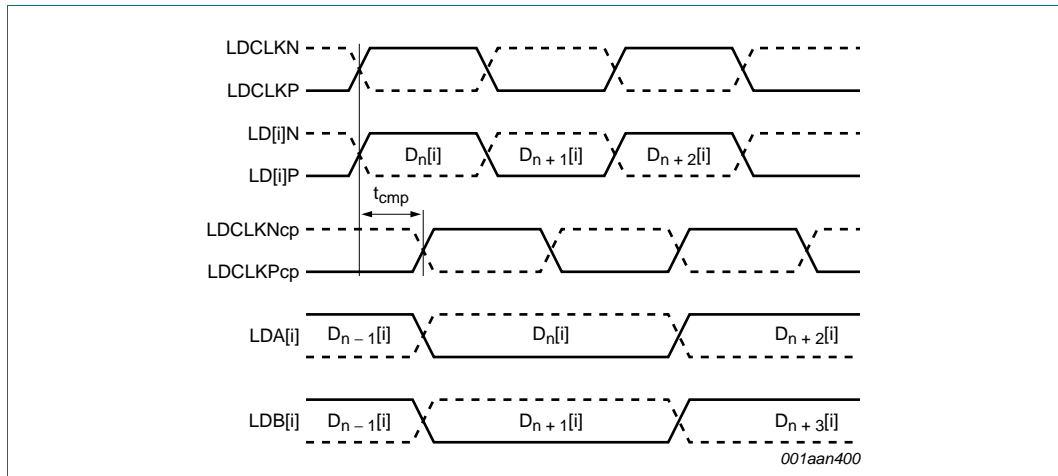


Fig 14. LVDS DDR demux timing (LVDS A and B paths not swapped; LDAB_SWAP = 0)

The compensation delay time (t_{cmp} in Figure 14) can be tuned automatically or manually. Bit CAL_CNTRL of the MAIN_CNTRL register (see Table 54) enables the switching between automatic tuning and manual tuning.

In Automatic tuning mode, the external LVDS data and clock signals are generated using the same reference clock (inside the FPGA). The LDCLK clock is similar to a data bit that toggles each time (the rising edge and falling edge of the LDCLK and LVDS data occur at the same time). In automatic tuning, the internal compensation delay time (t_{cmp}) is defined automatically to compensate the internal DAC1617D1G0 delay time optimally.

The timing requirement in automatic tuning mode is defined in Figure 15 and in Table 5.

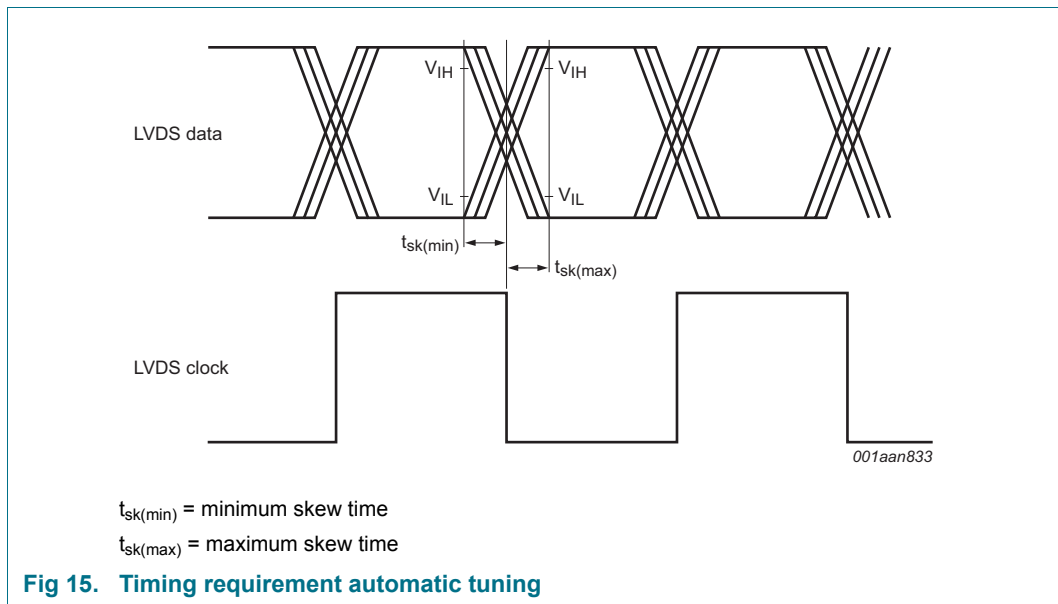


Fig 15. Timing requirement automatic tuning

Use manual tuning mode if the LVDS data and the LDCLK clock signals provided to the DAC1617D1G0 device have a systematic delay. The compensation delay time can be adjusted to compensate for the systematic delay. The compensation delay time (t_{cmp} in Figure 14), can be defined using bits LDCLK_DEL[3:0] of register MAN_LDCLKDEL (see Table 55).

The timing requirement in manual tuning mode is defined in Figure 16 and in Table 5.

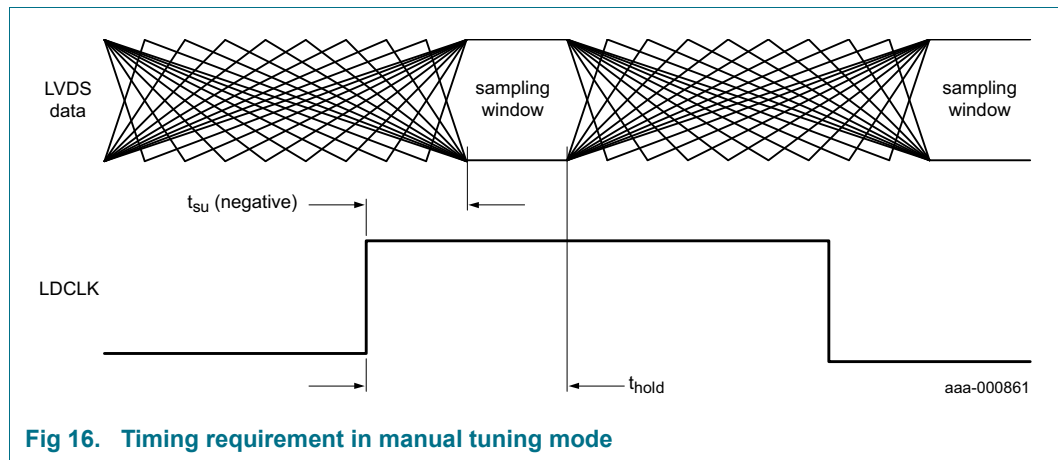


Fig 16. Timing requirement in manual tuning mode

10.9 Operating modes

The DAC1617D1G0 requires two differential clocks:

- The LVDS clock (LDCLKP, LDCLKN) for the LVDS DDR interface
- The data clock (CLKP, CLKN) for the internal PLL and the dual DAC core

In Normal mode, provide both the DAC clock and the LVDS clock to the DAC1617D1G0. Align the ratio frequency between these two clocks needs with selected $\times 2$, $\times 4$ or $\times 8$ interpolation filters. The clocks provided to the DAC1617D1G0 must respect the LVDS input timing and the DAC output timing specifications as defined in Table 5.

In PLL mode, provide the LVDS clock to pins LDCLKP/LDCLKN and pins CLKP/CLKN. Depending on selected interpolation filter, the internal PLL can be set to generate the right DAC core clock frequency internally. The clocks provided to the DAC1617D1G0 pins must respect the LVDS input timing and the DAC output timing specifications as defined in Table 5. The PLL settings must also respect the maximum sampling rate of the PLL (see the sampling rate (f_s) in subsection Internal PLL timing of Table 5).

The main function of the Clock Domain Interface (CDI) is to resynchronize the input data streams to the internal clock the digital processing uses. The CDI also performs the required reformatting of the input datastreams. Set PLL, CDI, and the interpolation filters, which depend on the targeted application accordingly. Section 10.9.1 ($\times 2$), Section 10.9.2 ($\times 4$), and Section 10.9.3 ($\times 8$) explain how to set the DAC1617D1G0 to support the different upsampling modes.

10.9.1 CDI mode 0 (x2 interpolation)

CDI mode 0 (x2 interpolation) is required when the value of the LVDS DDR clock is twice the internal maximum CDI frequency. Table 11 shows examples of applications using an internal PLL or an external clock for the DAC core.

Table 11. CDI mode 0: operating modes examples

| LVDS DDR rate (MHz) | I rate; Q rate (Msps) | CDI mode ^[1] | FIR mode ^[2] | SSBM rate ^[3] (Msps) | DAC rate (Msps) | PLL configuration | | |
|---------------------|-----------------------|-------------------------|-------------------------|---------------------------------|-----------------|--------------------------------------|---------------------------|----------------------------|
| | | | | | | DAC input clock ^[4] (MHz) | PLL status ^[5] | PLL divider ^[6] |
| 320 | 320 | 0 | x2 | 640 | 640 | 320 | enabled | 2 |
| 320 | 320 | 0 | x2 | 640 | 640 | 640 | disabled | n.a. |

[1] Bits CDI_MODE[1:0] of register MISC_CNTRL (see Table 61).

[2] Bits INTERPOLATION[1:0] of register TXCFG (see Table 23).

[3] If a Single Sideband Modulator (SSBM) is used, see bits NCO_ON and MODULATION[2:0] of register TXCFG (see Table 23).

[4] Pins CLKP and CLKN (see Figure 2).

[5] Bit PLL_PD of register PLLCFG (see Table 24).

[6] Bits PLL_DIV[1:0] of register PLLCFG (see Table 24).

10.9.2 CDI mode 1 (x4 interpolation)

CDI mode 1 (x4 interpolation) is required when the values of the LVDS DDR clock and the internal CDI frequency are equal. Table 12 shows examples of applications using an internal PLL or an external clock for the DAC core.

Table 12. CDI mode 1: operating modes examples

| LVDS DDR rate (MHz) | I rate; Q rate (Msps) | CDI mode ^[1] | FIR mode ^[2] | SSBM rate ^[3] (Msps) | DAC rate (Msps) | PLL configuration | | |
|---------------------|-----------------------|-------------------------|-------------------------|---------------------------------|-----------------|--------------------------------------|---------------------------|----------------------------|
| | | | | | | DAC input clock ^[4] (MHz) | PLL status ^[5] | PLL divider ^[6] |
| 250 | 250 | 1 | x4 | 1000 | 1000 | 250 | enabled | 4 |
| 250 | 250 | 1 | x4 | 1000 | 1000 | 1000 | disabled | n.a. |

[1] Bits CDI_MODE[1:0] of register MISC_CNTRL (see Table 61).

[2] Bits INTERPOLATION[1:0] of register TXCFG (see Table 23).

[3] If SSBM is used, see bits NCO_ON and MODULATION[2:0] of register TXCFG (see Table 23).

[4] Pins CLKP and CLKN (see Figure 2).

[5] Bit PLL_PD of register PLLCFG (see Table 24).

[6] Bits PLL_DIV[1:0] of register PLLCFG (see Table 24).

10.9.3 CDI mode 2 (x8 interpolation)

CDI mode 2 (x8 interpolation) is required when the LVDS DDR clock is half the maximum CDI frequency or less. Table 13 shows examples of applications using an internal PLL or an external clock for the DAC core.

Table 13. CDI mode 2: operating modes examples

| LVDS DDR rate (MHz) | I rate; Q rate (Mpsps) | CDI mode ^[1] | FIR mode ^[2] | SSBM rate ^[3] (Mpsps) | DAC rate (Mpsps) | PLL configuration | | |
|---------------------|------------------------|-------------------------|-------------------------|----------------------------------|------------------|--------------------------------------|---------------------------|----------------------------|
| | | | | | | DAC input clock ^[4] (MHz) | PLL status ^[5] | PLL divider ^[6] |
| 125 | 125 | 2 | x8 | 1000 | 1000 | 125 | enabled | 4 |
| 125 | 125 | 2 | x8 | 1000 | 1000 | 1000 | disabled | n.a. |

- [1] Bits CDI_MODE[1:0] of register MISC_CNTRL (see Table 61).
- [2] Bits INTERPOLATION[1:0] of register TXCFG (see Table 23).
- [3] If SSBM is used, see bits NCO_ON and MODULATION[2:0] of register TXCFG (see Table 23).
- [4] Pins CLKP and CLKN (see Figure 2).
- [5] Bit PLL_PD of register PLLCFG (see Table 24).
- [6] Bits PLL_DIV[1:0] of register PLLCFG (see Table 24).

10.10 FIR filters

The DAC1617D1G0 integrates three selectable Finite Impulse Response (FIR) filters which enable the use of the device with x2, x4 or x8 interpolation rates. All three interpolation FIR filters have a stop-band attenuation of at least 80 dBc and a pass-band ripple of less than 0.0005 dB. Table 14 shows the coefficients of the interpolation filters.

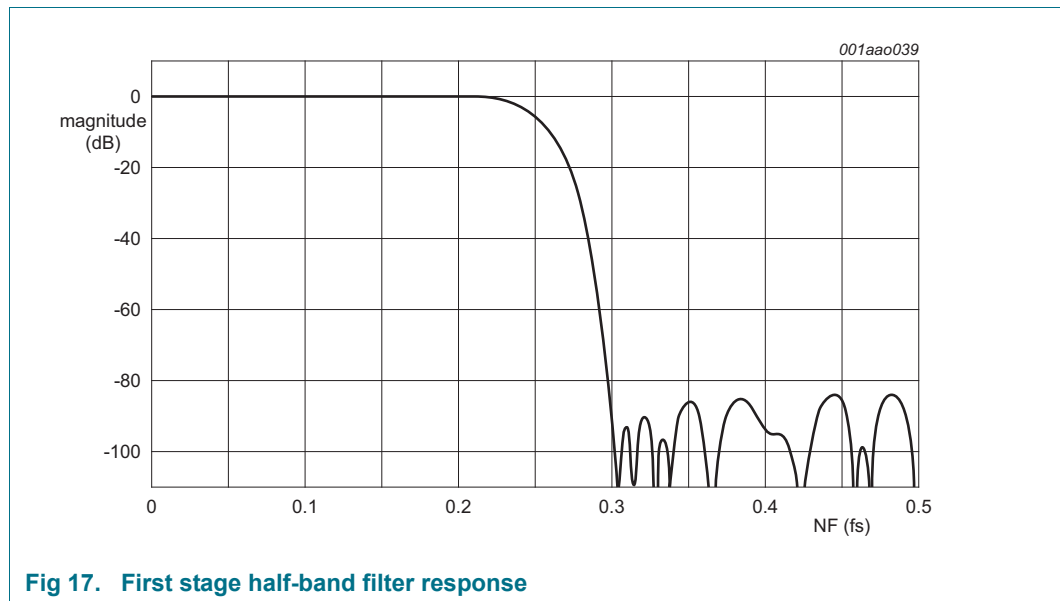


Fig 17. First stage half-band filter response

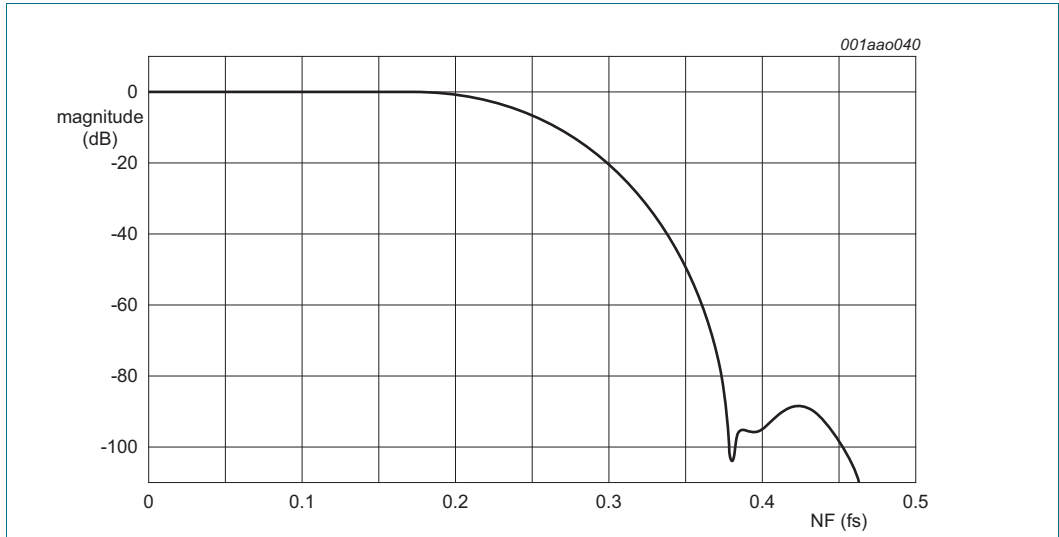


Fig 18. Second stage half-band filter response

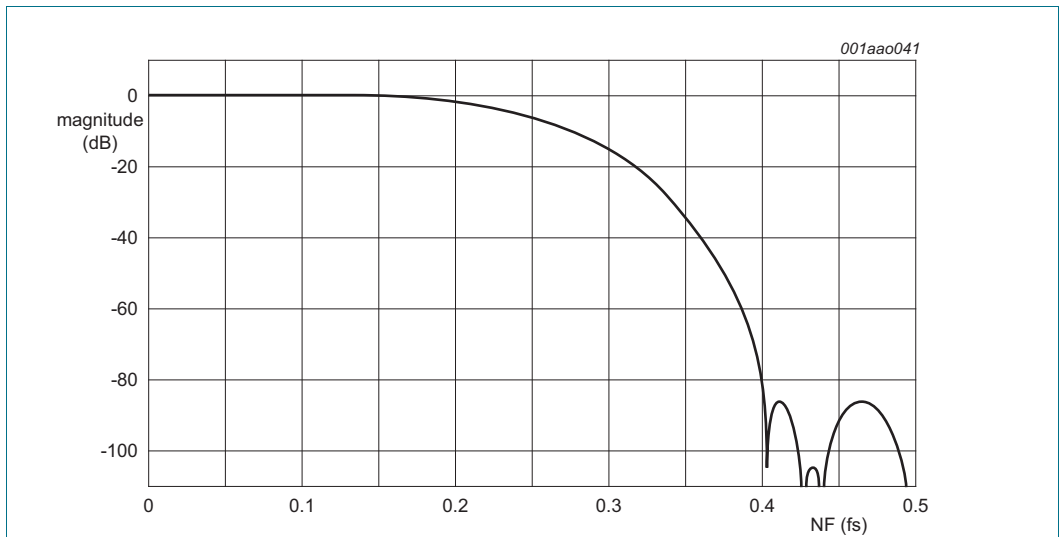


Fig 19. Third stage half-band filter response

Table 14: Interpolation filter coefficients

| First interpolation filter | | | Second interpolation filter | | | Third interpolation filter | | |
|----------------------------|-------|--------|-----------------------------|-------|--------|----------------------------|-------|-------|
| Lower | Upper | Value | Lower | Upper | Value | Lower | Upper | Value |
| - | H(27) | +65536 | H(11) | - | +32768 | H(7) | - | +1024 |
| H(26) | H(28) | +41501 | H(10) | H(12) | +20272 | H(6) | H(8) | +615 |
| H(25) | H(29) | 0 | H(9) | H(13) | 0 | H(5) | H(9) | 0 |
| H(24) | H(30) | -13258 | H(8) | H(14) | -5358 | H(4) | H(10) | -127 |
| H(23) | H(31) | 0 | H(7) | H(15) | 0 | H(3) | H(11) | 0 |
| H(22) | H(32) | +7302 | H(6) | H(16) | +1986 | H(2) | H(12) | +27 |
| H(21) | H(33) | 0 | H(5) | H(17) | 0 | H(1) | H(13) | 0 |
| H(20) | H(34) | -4580 | H(4) | H(18) | -654 | H(0) | H(14) | -3 |

Table 14: Interpolation filter coefficients ...continued

| First interpolation filter | | | Second interpolation filter | | | Third interpolation filter | | |
|----------------------------|-------|-------|-----------------------------|-------|-------|----------------------------|-------|-------|
| Lower | Upper | Value | Lower | Upper | Value | Lower | Upper | Value |
| H(19) | H(35) | 0 | H(3) | H(19) | 0 | - | - | - |
| H(18) | H(36) | +2987 | H(2) | H(20) | +159 | - | - | - |
| H(17) | H(37) | 0 | H(1) | H(21) | 0 | - | - | - |
| H(16) | H(38) | -1951 | H(0) | H(22) | -21 | - | - | - |
| H(15) | H(39) | 0 | - | - | - | - | - | - |
| H(14) | H(40) | +1250 | - | - | - | - | - | - |
| H(13) | H(41) | 0 | - | - | - | - | - | - |
| H(12) | H(42) | -773 | - | - | - | - | - | - |
| H(11) | H(43) | 0 | - | - | - | - | - | - |
| H(10) | H(44) | +456 | - | - | - | - | - | - |
| H(9) | H(45) | 0 | - | - | - | - | - | - |
| H(8) | H(46) | -252 | - | - | - | - | - | - |
| H(7) | H(47) | 0 | - | - | - | - | - | - |
| H(6) | H(48) | +128 | - | - | - | - | - | - |
| H(5) | H(49) | 0 | - | - | - | - | - | - |
| H(4) | H(50) | -58 | - | - | - | - | - | - |
| H(3) | H(51) | 0 | - | - | - | - | - | - |
| H(2) | H(52) | +22 | - | - | - | - | - | - |
| H(1) | H(53) | 0 | - | - | - | - | - | - |
| H(0) | H(54) | -6 | - | - | - | - | - | - |

Equation 1 defines the dependency of the FIR1 output Y(m) on its inputs X(m):

$$Y(m) = \frac{1}{H(27)} \times \sum_{n=0}^{n=54} [H(n):X(m-n)] \tag{1}$$

Equation 2 defines the dependency of the FIR2 output Y(m) on its inputs X(m):

$$Y(m) = \frac{1}{H(11)} \times \sum_{n=0}^{n=22} [H(n):X(m-n)] \tag{2}$$

Equation 3 defines the dependency of the FIR3 output Y(m) on its inputs X(m):

$$Y(m) = \frac{1}{H(7)} \times \sum_{n=0}^{n=14} [H(n):X(m-n)] \tag{3}$$

10.11 Single SideBand Modulator (SSBM)

The SSBM is a quadrature modulator that enables mixing the I data and Q data with the sine and cosine signals generated by the NCO to generate path A and path B (see Figure 20).

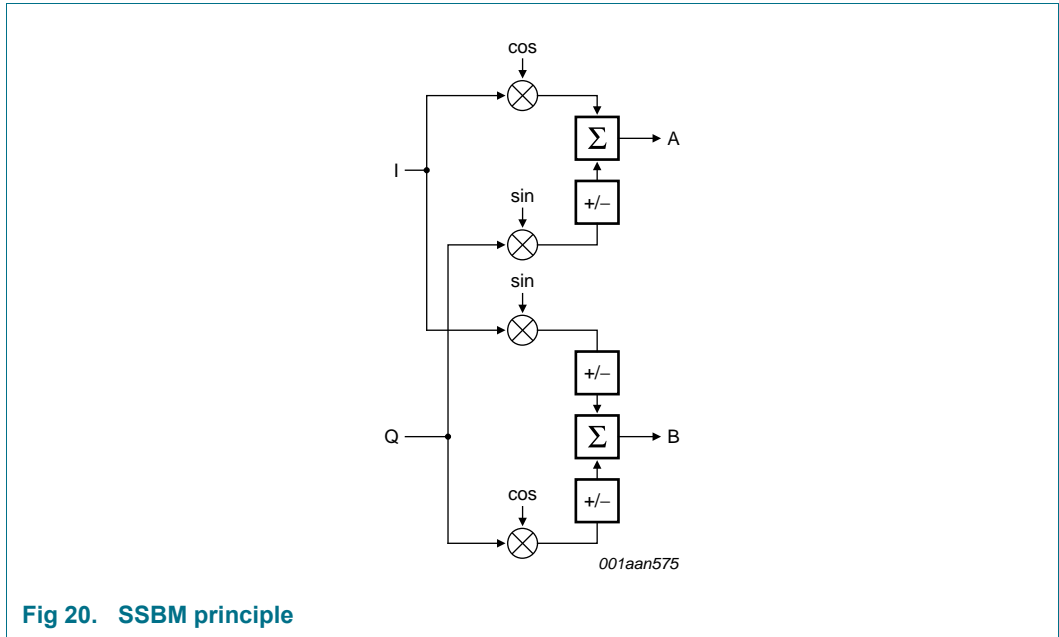


Fig 20. SSBM principle

The frequency of the NCO is programmed over 40 bits. NCO enables inverting the sine component to operate a positive or negative, lower or upper SSB upconversion (see register TXCFG in Table 23).

10.11.1 NCO in 40 bits

When using NCO, the frequency can be set over 40 bits by five registers, FREQNCO_B0 to FREQNCO_B4 (see Table 25).

The frequency is calculated with Equation 4.

$$f_{NCO} = \frac{M \times f_s}{2^{40}} \tag{4}$$

Where:

- M is the two's complement coding representation of FREQ_NCO[39:0]
- f_s is the DAC clock sampling frequency

The default settings are:

- $f_{NCO} = 96$ MHz
- $f_s = 640$ Msps

Registers PHINCO_LSB and PHINCO_MSB over 16 bits from 0° to 360° (see Table 31) can set the phase of the NCO.

10.11.2 NCO low power

The five MSB-bits of register `FREQNCO_B4` (bits `FREQ_NCO[39:35]`; see Table 25) can set the frequency, when using NCO low power (bit `NCO_LP_SEL`; see Table 23).

The frequency is calculated with Equation 5.

$$f_{NCO} = \frac{M \times f_s}{2^5} \tag{5}$$

Where:

- M is the two's complement coding representation of `FREQ_NCO[39:35]`
- f_s is the DAC clock sampling frequency

The five MSB-bits of register `PHINCO_MSB` (see Table 31) can set the phase of the NCO low power.

10.11.3 Complex modulator

The complex modulator upconverts the single side band by mixing NCO signals and I and Q input signals. Table 15 shows the various possibilities set by bits `MODULATION[2:0]` of register `TXCFG` (see Table 23).

The effect of the `MODULATION` parameter is better viewed after mixing the A and B signal with a LO frequency through an IQ modulator:

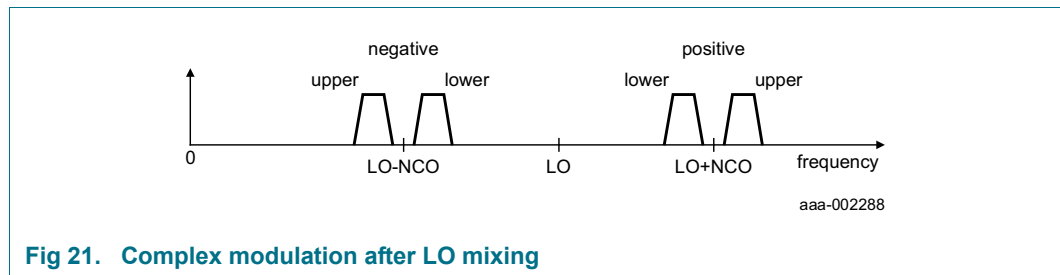


Fig 21. Complex modulation after LO mixing

Table 15. Complex modulator operation mode

| MODULATION[2:0] | Mode | Path A | Path B |
|-----------------|--------------------|---|--|
| 000 | bypass | $I(t)$ | $Q(t)$ |
| 001 | positive upper ssb | $I(t) \times \cos(\omega_{NCO} \times t) - Q(t) \times \sin(\omega_{NCO} \times t)$ | $I(t) \times \sin(\omega_{NCO} \times t) + Q(t) \times \cos(\omega_{NCO} \times t)$ |
| 010 | positive lower ssb | $I(t) \times \cos(\omega_{NCO} \times t) + Q(t) \times \sin(\omega_{NCO} \times t)$ | $I(t) \times \sin(\omega_{NCO} \times t) - Q(t) \times \cos(\omega_{NCO} \times t)$ |
| 011 | negative upper ssb | $I(t) \times \cos(\omega_{NCO} \times t) - Q(t) \times \sin(\omega_{NCO} \times t)$ | $-I(t) \times \sin(\omega_{NCO} \times t) - Q(t) \times \cos(\omega_{NCO} \times t)$ |
| 100 | negative lower ssb | $I(t) \times \cos(\omega_{NCO} \times t) + Q(t) \times \sin(\omega_{NCO} \times t)$ | $-I(t) \times \sin(\omega_{NCO} \times t) + Q(t) \times \cos(\omega_{NCO} \times t)$ |
| others | not defined | - | - |

10.11.4 Minus 3dB

In normal use, a full-scale pattern is also full-scale at the DAC output. Nevertheless, when the I data and Q data come close to full-scale simultaneously, some clipping can occur. The Minus 3dB function (bit MINUS_3DB of register DAC_OUT_CTRL; see Table 28) can be used to reduce the 3 dB gain in the modulator. It retains a full-scale range at the DAC output without added interferers.

10.12 Inverse (sin x) / x

A selectable FIR filter is incorporated to compensate the (sin x) / x effect caused by the roll-off effect of the DAC. This filter has no effect at DC. It introduces a gain for high frequency. The coefficients are represented in Table 16. The filter response is presented in Figure 22.

Table 16. Inversion filter coefficients

| First interpolation filter | | |
|----------------------------|-------|-------|
| Lower | Upper | Value |
| H(1) | H(9) | +1 |
| H(2) | H(8) | -4 |
| H(3) | H(7) | +13 |
| H(4) | H(6) | -51 |
| H(5) | - | +610 |

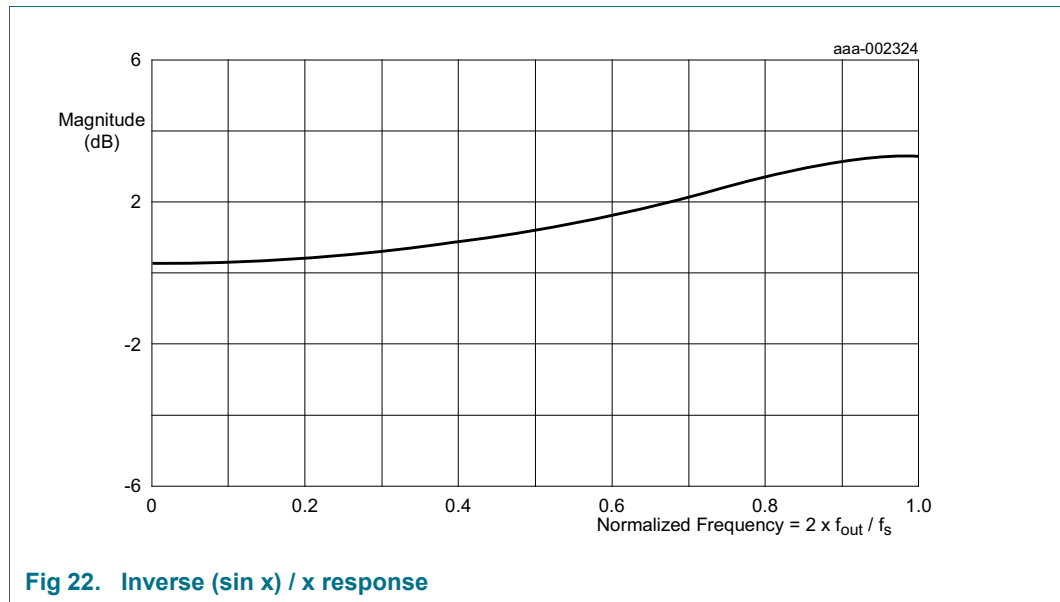


Fig 22. Inverse (sin x) / x response

10.13 Multiple Devices Synchronization (MDS)

Several DAC channels can be sampled synchronously and phase coherently using the MDS feature.

When all DAC slave devices of one system receive the same MDS signal (or at least a synchronous version of this reference) all devices are time-aligned at ±1 DAC clock accuracy at the end of the synchronization process.

10.13.1 MDS concept

The FPGA(s) has(have) to activate the ALIGN pins to identify the LVDS data flow start (see Figure 23).

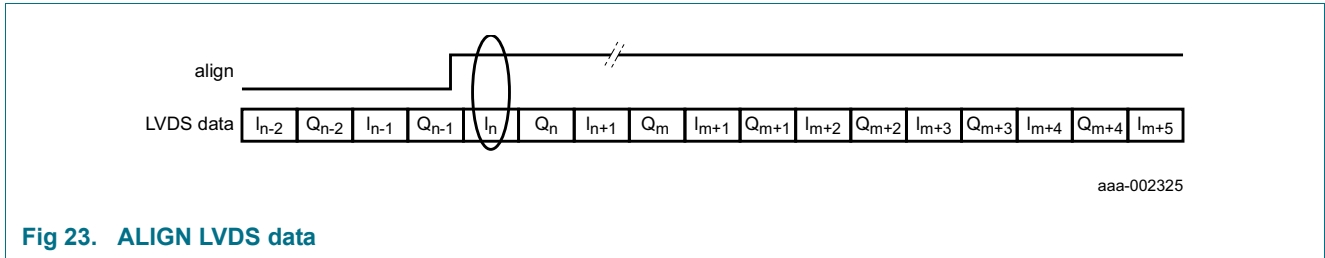


Fig 23. ALIGN LVDS data

The ALIGN signal is used to generate a local reference inside the DAC1617D1G0 which is 'aligned' with the IQ-data.

The DAC1617D1G0 devices use the MDS signals to do the output synchronization (see Figure 24).

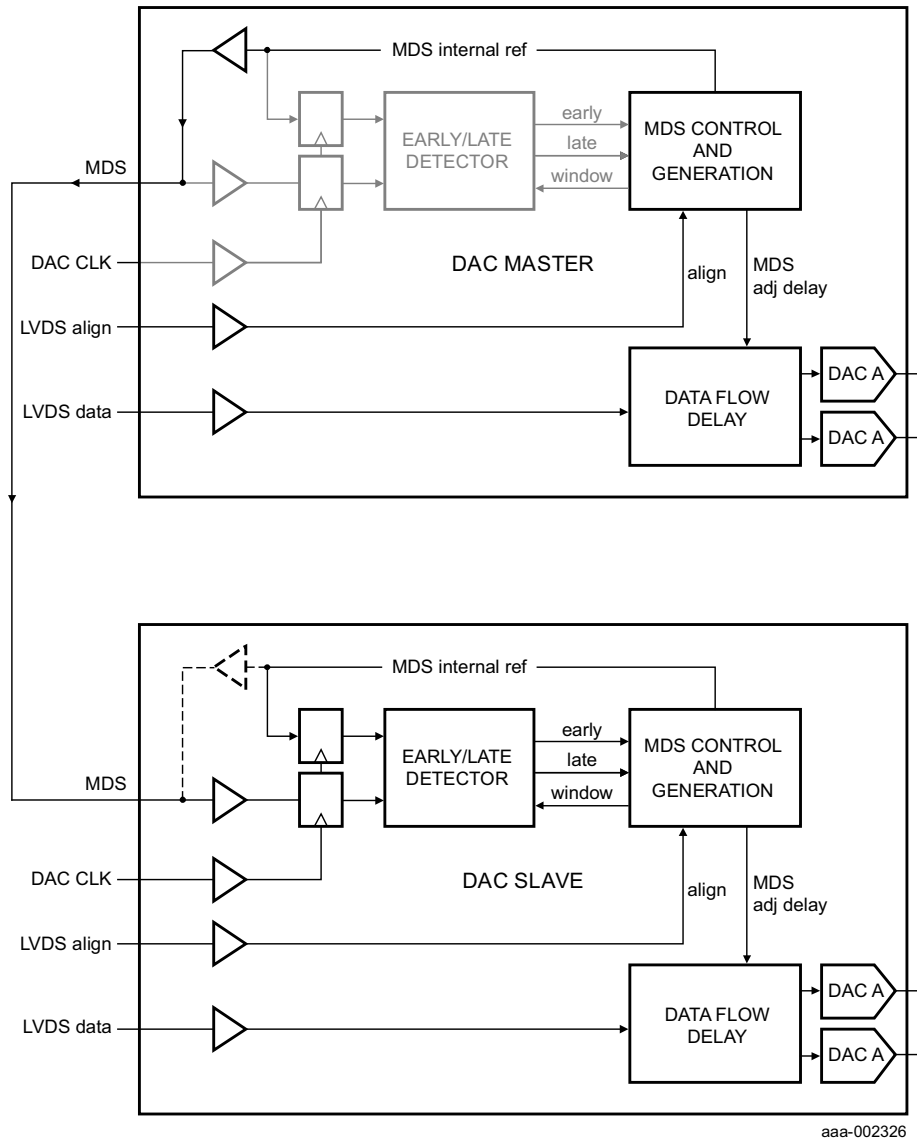


Fig 24. MDS synchronization

The signal detector of the DAC1617D1G0 detects the presence of the MDS signals. Once detected, an internal copy process of this reference starts. The MDS early/late detector block then compares the phase difference of these two signals to align the copy to its reference accurately. The alignment is done inside an "enabling window" that avoids the misinterpretation of the signal edges. This alignment process is done by moving the internal pointer of register MDS_ADJDELAY (see Table 43) (so inserting/removing a delay in data flow). This pointer can have a preset offset. This is specified by register MDS_OFFSET_DLY (see Table 42). Using the MDS_MAN and MDS_MAN_ADJDELAY bits in register MDS_MAN_ADJUSTLY register (see Table 39), the alignment can also be set manually.

During the whole alignment process, the MDS controller tries to adjust the delay to get the internal copy signal aligned to the external MDS signal. Once aligned, the MDS signal is not required anymore. it can be switched off at system level. The alignment is done just in front of the analog DACs cores ensuring the ± 1 DAC clock sample accuracy.

At the end of the MDS process, the MDS circuitry is disabled to avoid any analog disturbances.

The MDS feature can be used in two modes:

- All slaves mode
- Master/slaves mode

The mode can be set using the MD_MASTER bit of register MDS_MAIN (see Table 36).

10.13.1.1 MDS in All slaves mode

In this mode, each device uses its ALIGN pins signal to identify the LVDS data flow start (see Figure 23). The FPGA(s) has(have) to generate these ALIGN signals.

The FPGA is also used to generate the different MDS reference signals to enable the DAC1617D1G0 devices to do the synchronization of the output. Use this mode when two or more DAC1617D1G0 devices must be synchronized.

Figure 25 shows the MDS All slave mode schematic.

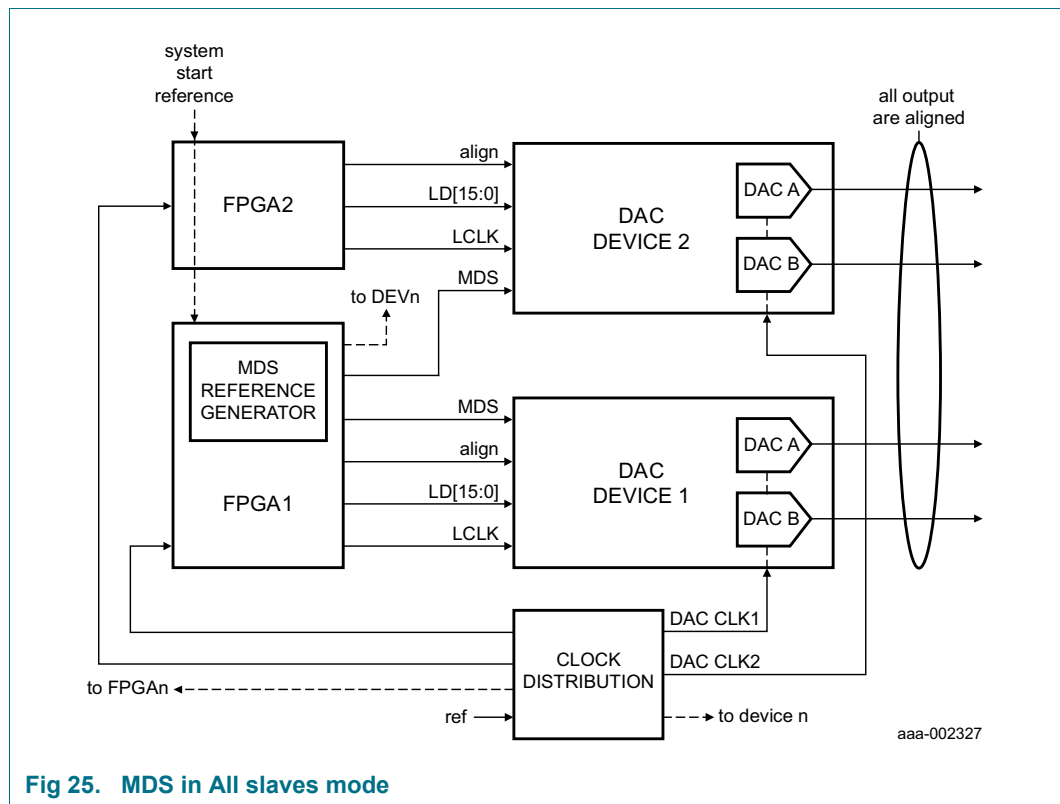


Fig 25. MDS in All slaves mode

10.13.1.2 MDS in Master/slaves mode

In this mode, one DAC1617D1G0 device is used as master, the other one is used as slave. The FPGA(s) still has(have) to provide the ALIGN signal to the DAC devices to identify the LVDS data flow start (see Figure 23). The master generates the reference MDS signal. The slave uses this signal to do the synchronization of the output. This mode is recommended when only two DAC1617D1G0 devices must be synchronized.

Figure 25 shows the MDS Master/slaves mode schematic.

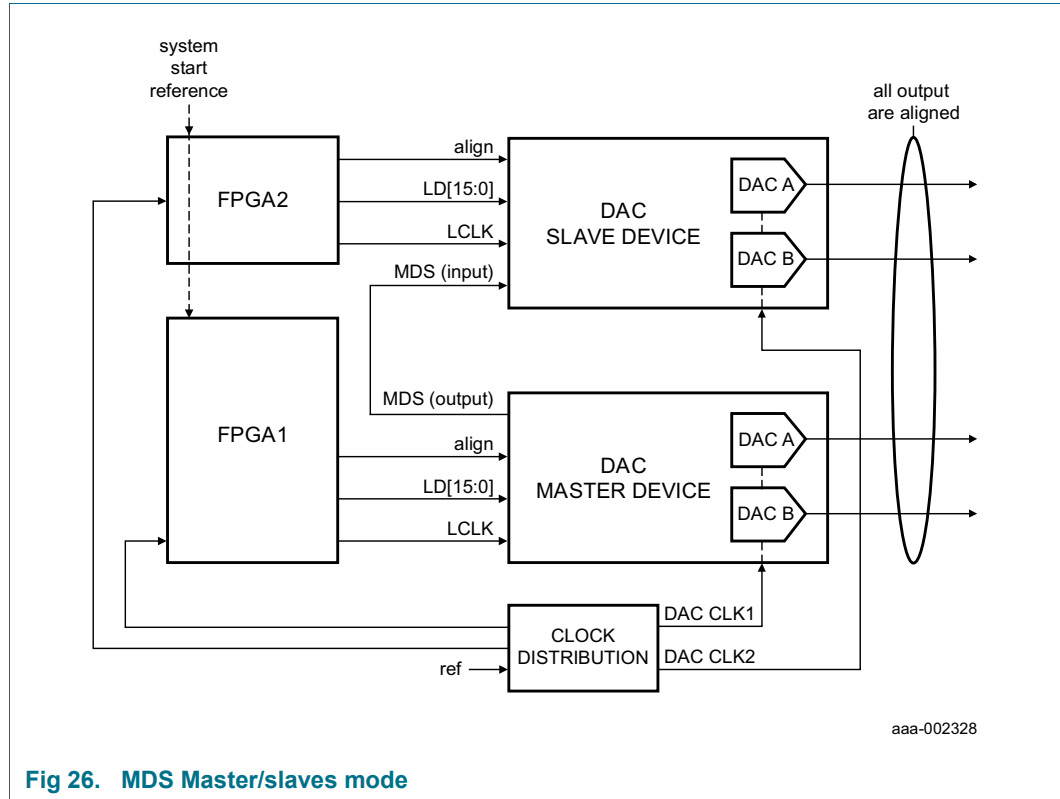


Fig 26. MDS Master/slaves mode

10.13.2 MDS flexibility and constraints

Getting a ± 1 clock period alignment can become very difficult without the MDS feature. There are many sources of misalignment:

- At 1 GHz, two signals with only 15 cm PCB length difference have a 1 clock period skew. So the PCB traces off the FPGA reference clock, the LVDS data/clock, or the DAC clock introduce delay.
- The clock generation circuit can cause delay between the different clocks.
- The most important delay comes from the internal FPGA design that can cause 1 or 2 LVDS clock delays between the different LVDS data patterns.

The DAC1617D1G0 MDS feature compensates these delays when:

- The overall delay compensated by the DAC1617D1G0 remains below ± 64 DAC clock.
- Each FPGA has to activate its ALIGN signal with the beginning of the LVDS data flow start (even if the different ALIGN signals are mis-aligned)

- All slave devices use the MDS signals for the fine alignment. Any misalignment between these signals causes misalignment on the output. Minimize the delay between the different MDS signals to avoid misalignments:
 - In All slave mode: Use a low skew buffer on the FPGA to generate this signal. Use the same PCB length for all MDS signal trace distributions.
 - In Master/slave mode: Minimize the MDS PCB length between the master and the slave (or compensate the introduced MDS PCB delay manually).

10.14 DAC transfer function

The full-scale output current for each DAC is the sum of the two complementary current outputs:

- $I_{OA(fs)} = I_{IOUTAP} + I_{IOUTAN}$
- $I_{OB(fs)} = I_{IOUTBP} + I_{IOUTBN}$

The output current of DAC A depends on the digital input data. Bits DAC_A_DGAIN[11:0] of register DAC_A_DGAIN_LSB (see Table 27) define the gain factor.

$$I_{IOUTAP} = I_{OA(fs)} \times \frac{(DACADGAIN)}{1024} \times \left(\frac{DATA}{65535}\right) \tag{6}$$

$$I_{IOUTAN} = I_{OA(fs)} \times \left(1 - \frac{(DACADGAIN)}{1024} \times \left(\frac{DATA}{65535}\right)\right) \tag{7}$$

The output current of DAC B depends on the digital input data. Bits DAC_B_DGAIN[11:0] of register DAC_B_DGAIN_LSB (see Table 27) define the gain factor.

$$I_{IOUTBP} = I_{OB(fs)} \times \frac{(DACBDGAIN)}{1024} \times \left(\frac{DATA}{65535}\right) \tag{8}$$

$$I_{IOUTBN} = I_{OB(fs)} \times \left(1 - \frac{(DACBDGAIN)}{1024} \times \left(\frac{DATA}{65535}\right)\right) \tag{9}$$

It is possible to define if the DAC1617D1G0 operates with a binary input or a two's complement input (bit CODING; see Table 22).

Table 17 shows the output current as a function of the input data, when $I_{OA(fs)} = I_{OB(fs)} = 20$ mA.

Table 17. DAC transfer function

| Data | I15 to I0/Q15 to Q0 (binary coding) | I15 to I0/Q15 to Q0 (two's complement coding) | IOUTAP/IOUTBP | IOUTAN/IOUTBN |
|-------|--|--|---------------|---------------|
| 0 | 0000 0000 0000 0000 | 1000 0000 0000 0000 | 0 mA | 20 mA |
| ... | ... | ... | ... | ... |
| 32768 | 1000 0000 0000 0000 | 0000 0000 0000 0000 | 10 mA | 10 mA |
| ... | ... | ... | ... | ... |
| 65535 | 1111 1111 1111 1111 | 0111 1111 1111 1111 | 20 mA | 0 mA |

10.15 Full-scale current

10.15.1 Regulation

The DAC1617D1G0 reference circuitry integrates an internal band gap reference voltage which delivers a 1.25 V reference on the GAPOUT pin. Decouple pin GAPOUT using a 100 nF capacitor.

The reference current is generated via an external resistor of 910 Ω (1 %) connected to VIRES. A control amplifier sets the appropriate full-scale current ($I_{OA(fs)}$ and $I_{OB(fs)}$) for both DACs (see Figure 27)).

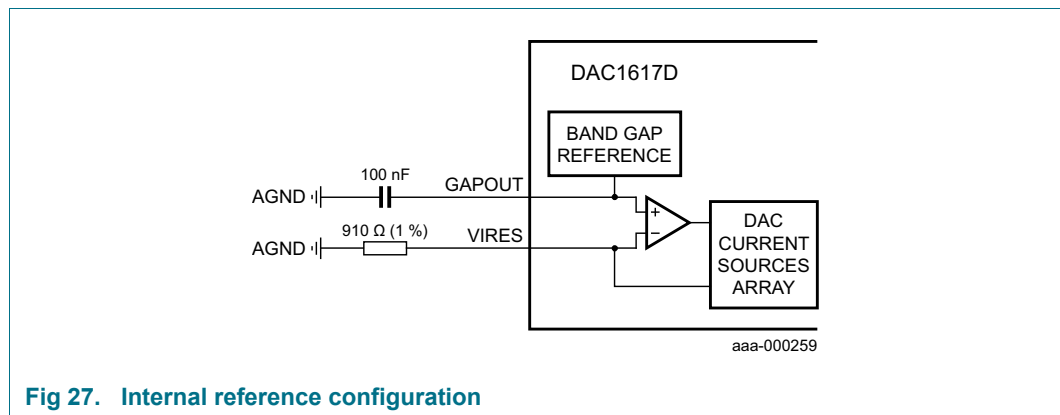


Fig 27. Internal reference configuration

Figure 27 shows the optimal configuration for temperature drift compensation because the band gap reference voltage can be matched to the voltage across the feedback resistor.

Applying an external reference voltage to the non-inverting input pin GAPOUT and disabling the internal band gap reference voltage (bit GAP_PON of the COMMON register; see Table 22) also adjust the DAC current.

10.15.2 Full-scale current adjustment

The default full-scale current ($I_{O(fs)}$) is 20 mA. However, further adjustments, ranging from 8.1 mA to 34 mA, can be made to both DACs independently using the serial interface.

The settings applied to DAC_A_GAIN[9:0] (registers 17h and 18h; see Table 32) define the full-scale current of DAC A:

$$I_{O(fs)} (\mu A) = 8100 + \text{DAC_A_GAIN}[9:0] \times 25.3 \quad (10)$$

The DAC_B_GAIN[9:0] (registers 19h and 1Ah; see Table 32;) define the full-scale current of DAC B:

$$I_{O(fs)} (\mu A) = 8100 + \text{DAC_B_GAIN}[9:0] \times 25.3 \quad (11)$$

10.16 Limiter/clip control

A limiter at the end of the data path saturates the output signal in case the signal does not fit the output range. This feature is activated using the CLIPPING_ENA bit in register DAC_OUT_CTRL (see Table 28).

The clipping level can be programmed using the CLIPPING_LEVEL register (see Table 29.). The output range is limited (or clipped) to between $-128x$ CLIPPING_LEVEL and $+128x$ CLIPPING_LEVEL.

At the DAC analog output, the AC current range is limited to:

$$-\left(\frac{I_{O(FS)}}{2}\right) \times \left(\frac{CLIPPING_LEVEL}{256}\right) \leq I_{IOUT} \leq +\left(\frac{I_{O(FS)}}{2}\right) \times \left(\frac{CLIPPING_LEVEL}{256}\right) \tag{12}$$

10.17 Digital offset adjustment

The DAC1617D1G0 provides digital offset correction (bits DAC_A_OFFSET[15:0] in Table 30). This correction can be used to adjust the common-mode level at the output of each DAC. It adds an offset at the end of the digital part, just before the DACs. Table 18 shows the range of variation of the digital offset.

This offset can be used to remove the LO image at the IQ modulator output.

Table 18. Digital offset adjustment

| DAC_A_OFFSET[15:0] DAC_B_OFFSET[15:0] (two's complement) | Offset applied |
|--|----------------|
| 1000 0000 0000 0000 | -32768 |
| 1000 0000 0000 0001 | -32767 |
| ... | ... |
| 1111 1111 1111 1111 | -1 |
| 0000 0000 0000 0000 | 0 |
| 0000 0000 0000 0001 | +1 |
| ... | ... |
| 0111 1111 1111 1110 | +32766 |
| 0111 1111 1111 1111 | +32767 |

10.18 Analog output

The device has two output channels, producing two complementary current outputs, which enable the reduction of even-order harmonics and noise. The pins are IOUTAP/IOUTAN and IOUTBP/IOUTBN. Connect these pins via a load resistor R_L to the 3.3 V analog power supply ($V_{DDA(3V3)}$).

Figure 28 shows the equivalent analog output circuit of one DAC. This circuit includes a parallel combination of NMOS current sources and associated switches for each segment.

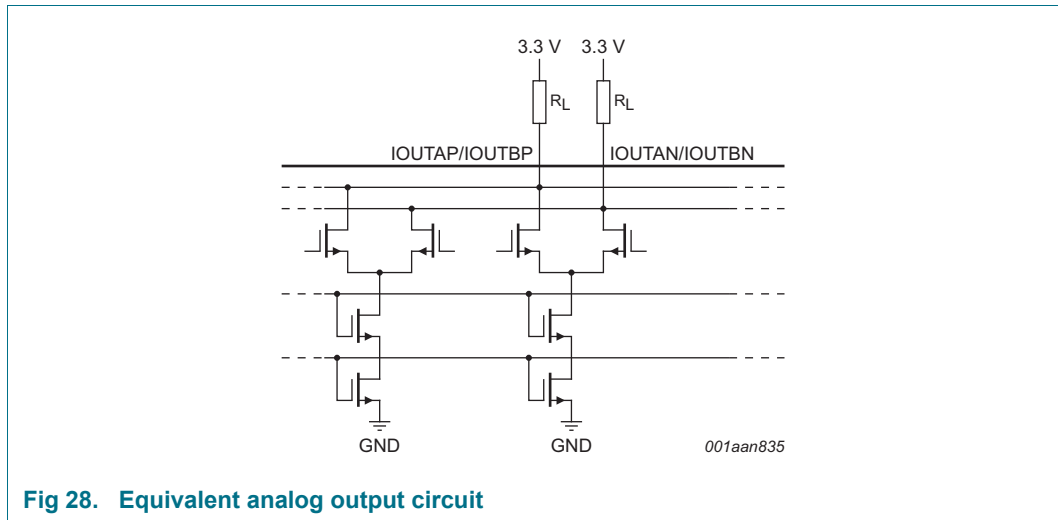


Fig 28. Equivalent analog output circuit

The cascode source configuration increases the output impedance of the source, which improves the dynamic performance of the DAC because there is less distortion.

Depending on the application, the various stages and the targeted performances, the device can be used for an output level of up to 2 V (p-p).

10.19 Auxiliary DACs

The DAC1617D1G0 integrates two auxiliary DACs, which are used to compensate any offset between the DACs and the next stage in the transmission path. Both auxiliary DACs have a 10-bit resolution and are current sources (referenced to ground).

The full-scale output current for each DAC is the sum of the two complementary current outputs:

- $I_{OAUXA(fs)} = I_{AUXAP} + I_{AUXAN}$
- $I_{OAUXB(fs)} = I_{AUXBP} + I_{AUXBN}$

The output current depends on the digital input data set by SPI registers DAC_A_Aux_MSB (bits AUX_A[9:0]) and DAC_B_Aux_MSB (bits AUX_B[9:0]; see Table 33).

$$I_{AUXAP} = I_{OAUXA(fs)} \times \left(\frac{DATAA}{1023} \right) \tag{13}$$

$$I_{AUXAN} = I_{OAUXA(fs)} \times \left(\frac{1023 - DATAA}{1023} \right) \tag{14}$$

$$I_{AUXBP} = I_{OAUXB(fs)} \times \left(\frac{DATAB}{1023} \right) \tag{15}$$

$$I_{AUXBN} = I_{OAUXB(fs)} \times \left(\frac{1023 - DATAB}{1023} \right) \tag{16}$$

Table 19 shows the output current as a function of the auxiliary DACs data DATAA and DATAB in Equation 13 to Equation 16.

Table 19. Auxiliary DAC transfer function

| DATAA; DATAB | AUX_A[9:2]/AUX_A[1:0]; AUX_B[9:0]/AUX_B[1:0] (binary coding) | I _{AUXAP} ; I _{AUXBP} (mA) | I _{AUXAN} ; I _{AUXBN} (mA) |
|--------------|--|--|--|
| 0 | 00 0000 0000 | 0 | 3.1 |
| ... | ... | ... | ... |
| 512 | 10 0000 0000 | 1.55 | 1.55 |
| ... | ... | ... | ... |
| 1023 | 11 1111 1111 | 3.1 | 0 |

10.20 Output configuration

The DAC1617D1G0 supports various output configurations.

The system application must check that for IOUTA/IOUTB output, the output compliance range (V_o) and the common-mode output voltage ($V_{o(cm)}$) specification points are respected to define other configurations.

Similarly, the system application must check that the output compliance range (V_o) specification point is respected for AUXA/AUXB DAC (if used).

The common-mode voltage ($V_{o(cm)}$) value for each IOUTA/IOUTB pin depends on the DC resistor(s) connected to these pins and the IOUT DC sink currents on these pins.

Equation 17 defines the DC sink output current is:

$$I_{O(sink)}(DC) = I_{bias}(DC) + \frac{I_{O(fs)}}{2} \quad (17)$$

Where:

- $I_{O(fs)}$ = full-scale output current
- $I_{bias}(DC)$ = DC bias current

The common-mode voltage ($V_{o(cm)}$) value for each AUXA/AUXB pins depend on the DC resistor(s) connected to these pins and the AUX DC source currents.

Equation 18 defines these AUX DC source currents:

$$I_{O(source)}(DC) = \frac{I_{O(fs)}}{2} \quad (18)$$

Where:

- $I_{O(fs)}$ = full-scale output current

The output compliance range (V_o) of all DAC outputs depends on the AC resistor load connected to the DAC:

$$V_{O(max)} = V_{O(cm)} + \frac{I_{O(fs)}}{2} \times R_{AC} \tag{19}$$

$$V_{O(min)} = V_{O(cm)} - \frac{I_{O(fs)}}{2} \times R_{AC} \tag{20}$$

Where:

- $V_{O(cm)}$ = common-mode output voltage
- $I_{O(fs)}$ = full-scale output current
- R_{AC} = DAC outputs AC resistor load

10.20.1 Basic output configuration

The use of a differentially coupled transformer output (see Figure 29) provides optimum distortion performance. In addition, it helps to match the impedance and provides electrical isolation.

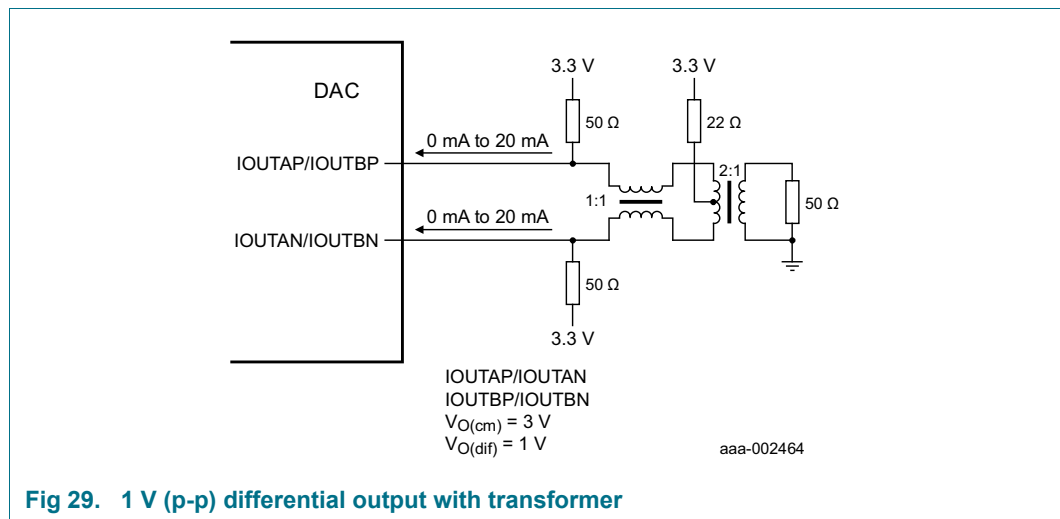


Fig 29. 1 V (p-p) differential output with transformer

The DAC1617D1G0 can operate a differential output of up to 2 V (p-p). In this configuration, connect the center tap of the transformer to a 33 Ω resistor, which is connected to the 3.3 V analog power supply. This adjusts the DC common-mode to around 2.8 V (see Figure 30).

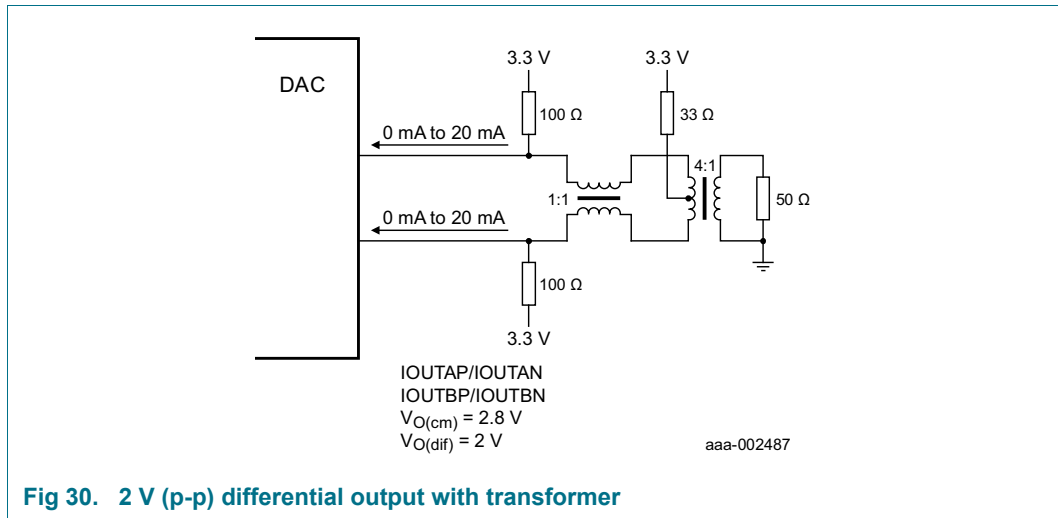


Fig 30. 2 V (p-p) differential output with transformer

10.20.2 Low input impedance IQ-modulator interface

The DAC1617D1G0 can be easily connected to low input impedance IQ-modulators. The image of the local oscillator can be canceled using the digital offset control in the device.

Figure 31 shows an example of a connection between the DAC1617D1G0 and a low input impedance modulator.

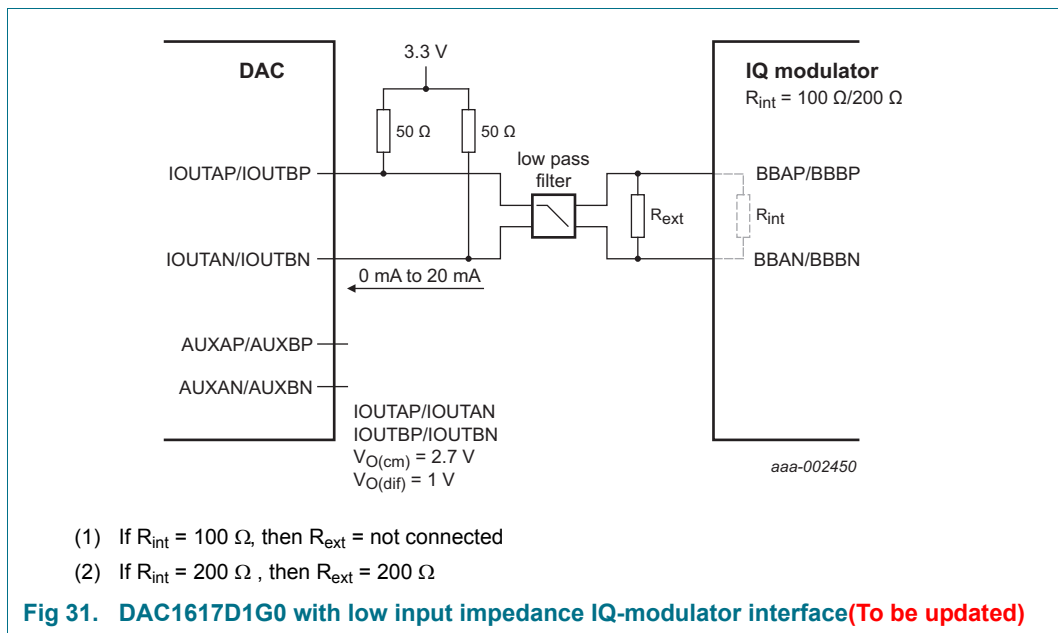


Fig 31. DAC1617D1G0 with low input impedance IQ-modulator interface (To be updated)

10.20.3 IQ-modulator - DC interface

When the system operation requires to keep the DC component of the spectrum, the DAC1617D1G0 can use a DC interface to connect an IQ-modulator. In this case, the image of the local oscillator can be canceled using the digital offset control in the device.

Figure 32 shows an example of a connection to an IQ modulator with a 1.7 V common input level.

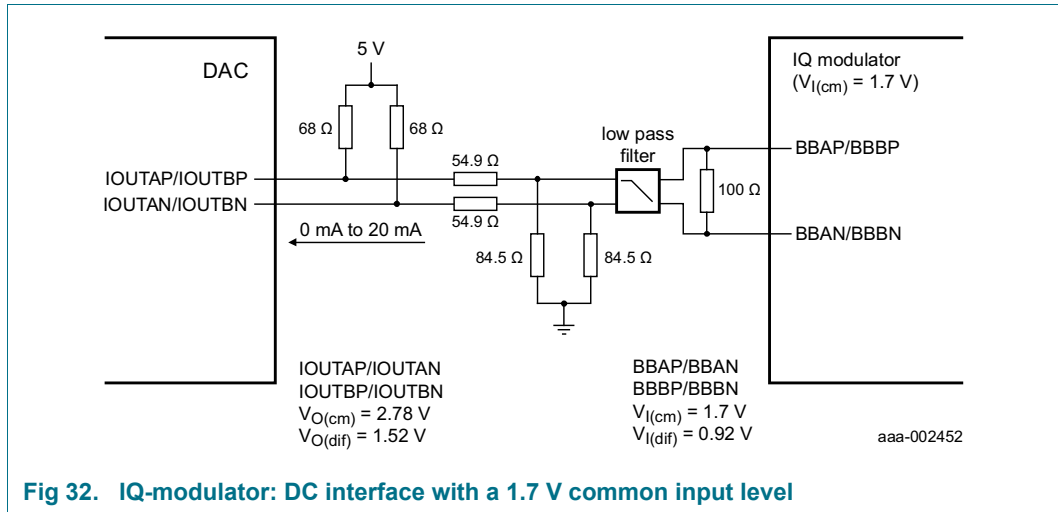
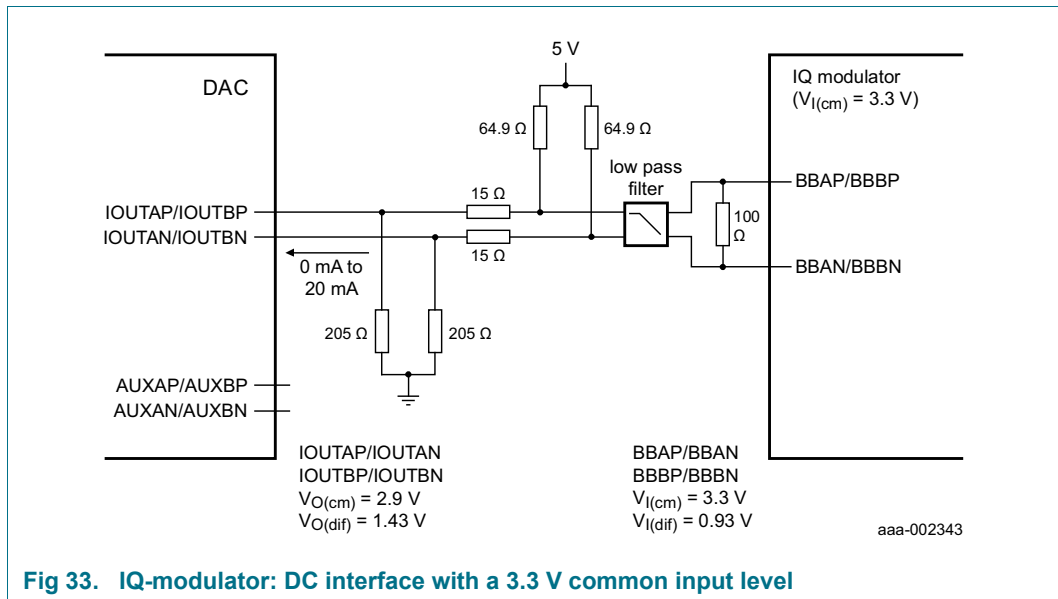
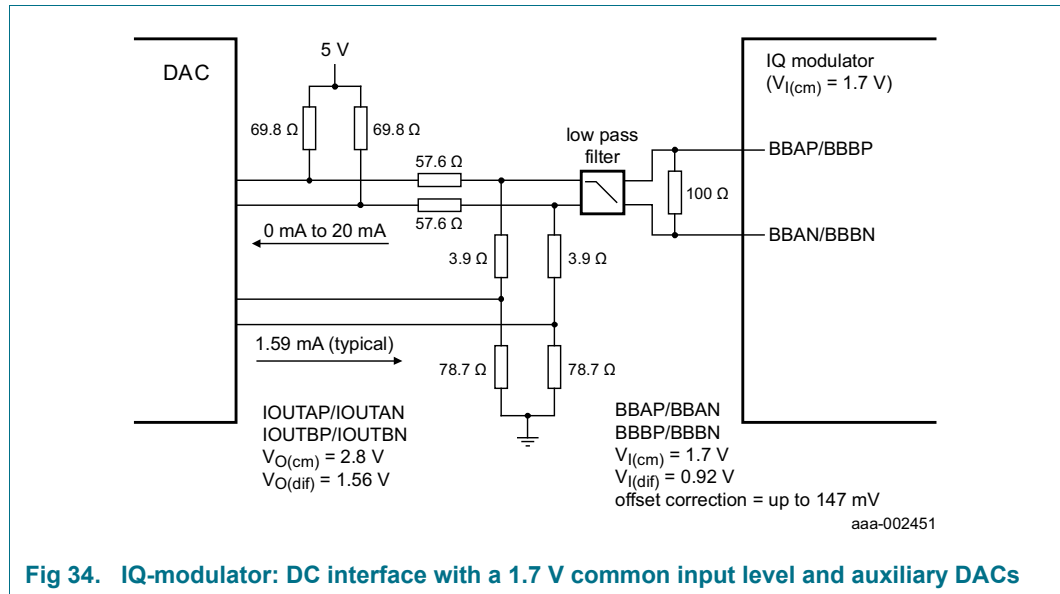


Figure 33 shows an example of a connection to an IQ-modulator with a 3.3 V common input level.



The auxiliary DACs can be used to control the offset within an accurate range or with accurate steps.

Figure 34 shows an example of a connection to an IQ-modulator with a 1.7 V common input level and auxiliary DACs.



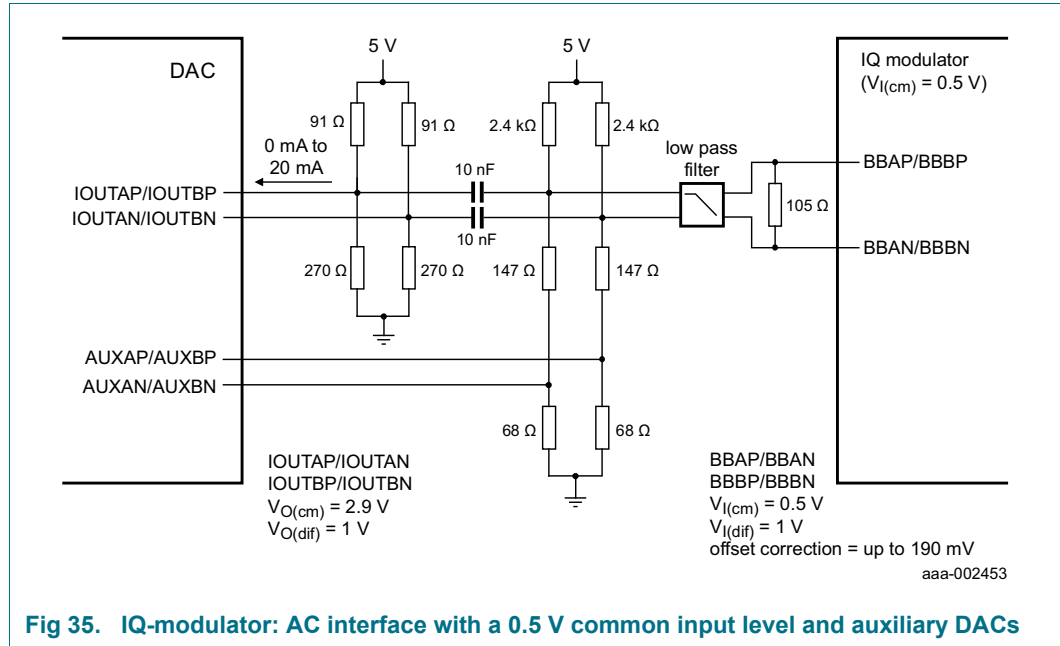
The constraints to adjust the interface are:

- The output compliance range of the DAC
- The output compliance range of the auxiliary DACs
- The input common-mode level of the IQ-modulator
- The range of offset correction

10.20.4 IQ-modulator - AC interface

Use the DAC1617D1G0 AC-coupled when the IQ-modulator common-mode voltage is close to ground. The auxiliary DACs are required for local oscillator cancelation.

Figure 35 shows an example of a connection to an IQ-modulator with a 0.5 V common input level and auxiliary DACs.



10.21 Design recommendations

10.21.1 Power and grounding

Use a separate power supply regulator for the generation of the 1.8 V analog power (pins 65, 62, 55, 69, 72 and 58) and the 1.8 V digital power (pins 12, 19, 36, 26 and 43) to ensure optimal performance.

Also, include individual LC decoupling for the following six sets of power pins:

- $V_{DDA(1V8)}_{P1}$ (pin 62)
- $V_{DDA(1V8)}_{P2}$ (pin 65)
- $V_{DDA(1V8)}$ (pins 55, 69, 72 and 58)
- V_{DD} (pins 12, 19, 26, 36, and 43)
- $V_{DDA(3V3)}$ (pins 59 and 68)

Use at least two capacitors for each power pin decoupling. Locate these capacitors as close as possible to the DAC1617D1G0 power pins.

The die pad is used for both the power dissipation and electrical grounding. Insert several vias (7 × 7 typical) to connect the internal ground plane to the top layer die area.

10.22 Configuration interface

10.22.1 Register description

The DAC1617D1G0 incorporates more than the 32 SPI registers allowed by the address value A[4:0]. It uses three SPI register pages (page_00, page_01, and page_0A), each containing 32 registers. The 32nd register of each page indicates which page is currently addressed (00h, 01h or 0Ah).

Page 00h (see Table 21) is dedicated to the main control of the DAC1617D1G0:

- Mode selection
- NCO control
- Auxiliary DAC control
- Gain/phase/offset control
- Power-down control

Page 01h (see Table 35) is dedicated to:

- Multi-Device Synchronization (MDS)
- DAC analog core control (biasing current, Sleep mode)

Page 0Ah (see Table 53) is dedicated to the LVDS input interface configuration.

10.22.2 SPI start-up sequence

The following SPI sequence shows the list of commands to be used to start the DAC1627D1G25 in interpolation $\times 4$ mode, with NCO frequency = 153.6 MHz ($f_{\text{DAC}} = 983.04$ MHz), PLL bypass mode, and without inverse ($\sin x$) / x . Other start-up sequences can be easily derived from this sequence:

Table 20. SPI start-up sequence

| Step | SPI (address, data) | Comment |
|------|---------------------|--|
| 1 | Write(0x1F, 0x00) | select SPI (page 0) |
| 2 | Write(0x00, 0x47) | reset SPI |
| 3 | Write(0x01, 0x86) | set NCO on with positive upper sideband conversion, interpolation $\times 4$, No inverse ($\sin x$) / x |
| 4 | Write(0x02, 0xA0) | PLL in bypass mode |
| 5 | Write(0x04, 0xFF) | select NCO frequency (FREQ_NCO[7:0]) |
| 6 | Write(0x05, 0xFC) | select NCO frequency (FREQ_NCO[15:8]) |
| 7 | Write(0x06, 0xFF) | select NCO frequency (FREQ_NCO[23:16]) |
| 8 | Write(0x07, 0xFF) | select NCO frequency (FREQ_NCO[31:24]) |
| 9 | Write(0x08, 0x27) | select NCO frequency (FREQ_NCO[39:32]) |
| 10 | Write(0x1F, 0x01) | select SPI (page 1) |
| 11 | Write(0x15, 0x0A) | set DAC_current_6 to 0X0A in order to guaranty good performance over process/temperature/voltage |
| 12 | Write(0x1F, 0x0A) | select SPI (page A) |

Table 20. SPI start-up sequence ...continued

| Step | SPI (address, data) | Comment |
|------|---------------------|--|
| 13 | Write(0x0A, 0x33) | specify LVDS interface setting (no DAC A/B swapping, no parity check, no data enable, ...) |
| 14 | Write(0x0B, 0x01) | set CDI block setting (interpolation $\times 4$, CDI mode) |
| 15 | Write(0x00, 0x00) | release LVDS reset (start of the DAC1617) |

10.22.3 Page 0 register allocation map

Table 21 shows an overview of all registers on page 0 (00h in hexadecimal).

Table 21. Page_00 register allocation map

| Address | Register name | R/W | Bit definition | | | | | | | | Default | |
|---------|-----------------|-----|------------------|------------|-------------|-----------------|-------------------|----------------|--------------------|--------------|--------------|-----|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bin | Hex |
| 0 00h | COMMON | R/W | 3W_SPI | SPI_RST | - | - | - | CODING | IC_PON | GAP_PON | 1000 0111 | 87h |
| 1 01h | TXCFG | R/W | NCO_ON | NCO_LP_SEL | INV_SIN_SEL | MODULATION[2:0] | | | INTERPOLATION[1:0] | | 0000 0001 | 01h |
| 2 02h | PLLCFG | R/W | PLL_BP | PLL_BUF_PD | PLL_PLL_PD | PLL_DIV[1:0] | | PLL_PHASE[1:0] | | PLL_OSC_PD | 1010 0001 | A1h |
| 4 04h | FREQNCO_B0 | R/W | FREQ_NCO[7:0] | | | | | | | | 0110 0110 | 66h |
| 5 05h | FREQNCO_B1 | R/W | FREQ_NCO[15:8] | | | | | | | | 0110 0110 | 66h |
| 6 06h | FREQNCO_B2 | R/W | FREQ_NCO[23:16] | | | | | | | | 0110 0110 | 66h |
| 7 07h | FREQNCO_B3 | R/W | FREQ_NCO[31:24] | | | | | | | | 0010 0110 | 66h |
| 8 08h | FREQNCO_B4 | R/W | FREQ_NCO[39:32] | | | | | | | | 0010 0110 | 26h |
| 9 09h | PH_CORR_CTL0 | R/W | PHASE_COR[7:0] | | | | | | | | 0000 0000 | 00h |
| 10 0Ah | PH_CORR_CTL1 | R/W | PH_COR_ENA | - | - | PHASE_COR[12:8] | | | | | 0000 0000 | 00h |
| 11 0Bh | DAC_A_DGAIN_LSB | R/W | DAC_A_DGAIN[7:0] | | | | | | | | 1101 0100 | 50h |
| 12 0Ch | DAC_A_DGAIN_MSB | R/W | - | - | - | - | DAC_A_DGAIN[11:8] | | | | 0000 1011 | 0Bh |
| 13 0Dh | DAC_B_DGAIN_LSB | R/W | DAC_B_DGAIN[7:0] | | | | | | | | 1101 0100 | 50h |
| 14 0Eh | DAC_B_DGAIN_MSB | R/W | - | - | - | - | DAC_B_DGAIN[11:8] | | | | 0000 0010 | 0Bh |
| 15 0Fh | DAC_OUT_CTRL | R/W | - | - | - | - | A_DGAIN_E | B_DGAIN_E | MINUS_3DB | CLIPPING_ENA | 0000 0000 | 00h |

Table 21. Page_00 register allocation map ...continued

| Address | Register name | R/W | Bit definition | | | | | | | Default | |
|---------|------------------|-----|---------------------|-------|-------|-------|-------|-----------|------------|---------|-----|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bin |
| 16 10h | DAC_CLIPPING | R/W | CLIPPING_LEVEL[7:0] | | | | | | | 1111 | FFh |
| 17 11h | DAC_A_OFFSET_LSB | R/W | DAC_A_OFFSET[7:0] | | | | | | | 0000 | 00h |
| 18 12h | DAC_A_OFFSET_MSB | R/W | DAC_A_OFFSET[15:8] | | | | | | | 0000 | 00h |
| 19 13h | DAC_B_OFFSET_LSB | R/W | DAC_B_OFFSET[7:0] | | | | | | | 0000 | 00h |
| 20 14h | DAC_B_OFFSET_MSB | R/W | DAC_B_OFFSET[15:8] | | | | | | | 0000 | 00h |
| 21 15h | PHINCO_LSB | R/W | PH_NCO[7:0] | | | | | | | 0000 | 00h |
| 22 16h | PHINCO_MSB | R/W | PH_NCO[15:8] | | | | | | | 0000 | 00h |
| 23 17h | DAC_A_GAIN1 | R/W | DAC_A_GAIN[7:0] | | | | | | | 1101 | D8h |
| 24 18h | DAC_A_GAIN2 | R/W | DAC_A_GAIN[9:8] | - | - | - | - | - | - | 0100 | 40h |
| 25 19h | DAC_B_GAIN1 | R/W | DAC_B_GAIN[7:0] | | | | | | | 1101 | D8h |
| 26 1Ah | DAC_B_GAIN2 | R/W | DAC_B_GAIN[9:8] | - | - | - | - | - | - | 0100 | 40h |
| 27 1Bh | DAC_A_AUX_MSB | R/W | AUX_A[9:2] | | | | | | | 1000 | 80h |
| 28 1Ch | DAC_A_AUX_LSB | R/W | AUX_A_PON | - | - | - | - | - | AUX_A[1:0] | 1000 | 80h |
| 29 1Dh | DAC_B_AUX_MSB | R/W | AUX_B[9:2] | | | | | | | 1000 | 80h |
| 30 1Eh | DAC_B_AUX_LSB | R/W | AUX_B_PON | - | - | - | - | - | AUX_B[1:0] | 1000 | 80h |
| 31 1Fh | PAGE_ADDRESS | R/W | - | - | - | - | - | PAGE[2:0] | | 0000 | 00h |

10.22.4 Page 0 bit definition detailed description

The tables in this section contain detailed descriptions of the page 0 registers.

Table 22. Register COMMON (address 00h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|---------|--------|----------|--|
| 7 | 3W_SPI | R/W | | serial interface bus type |
| | | | 0 | 4-wire SPI |
| | | | 1 | 3-wire SPI |
| 6 | SPI_RST | R/W | | serial interface reset |
| | | | 0 | no reset |
| | | | 1 | performs a reset on all registers except address 00h |
| 2 | CODING | R/W | | coding of input word |
| | | | 0 | two's complement coding |
| | | | 1 | unsigned format |
| 1 | IC_PON | R/W | | IC power control |
| | | | 0 | all circuits (digital and analog, except SPI) are in power-down |
| | | | 1 | all circuits (digital and analog, except SPI) are switched on |
| 0 | GAP_PON | R/W | | internal band gap power control |
| | | | 0 | band gap is power-down |
| | | | 1 | internal band gap references are switched on |

Table 23. Register TXCFG (address 01h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------|--------|------------|--|
| 7 | NCO_ON | R/W | | NCO |
| | | | 0 | NCO disabled, the NCO phase is reset to 0 |
| | | | 1 | NCO enabled |
| 6 | NCO_LP_SEL | R/W | | NCO low-power selection |
| | | | 0 | low-power NCO disabled |
| | | | 1 | low-power NCO enabled (frequency and phase given by the five MSB of the registers 06h and 08h, respectively) |
| 5 | INV_SIN_SEL | R/W | | inverse (sin x) / x function selection |
| | | | 0 | disable |
| | | | 1 | enable |
| 4 to 2 | MODULATION[2:0] | R/W | | modulation |
| | | | 000 | dual DAC: no modulation |
| | | | 001 | positive upper single sideband upconversion |
| | | | 010 | positive lower single sideband upconversion |
| | | | 011 | negative upper single sideband upconversion |
| | | | 100 | negative lower single sideband upconversion |
| | | | others | not defined |

Table 23. Register TXCFG (address 01h) bit description ...continued

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------------|--------|-----------|-------------------------|
| 1 to 0 | INTERPOLATION[1:0] | R/W | | interpolation |
| | | | 00 | no interpolation |
| | | | 01 | ×2 interpolation |
| | | | 10 | ×4 interpolation |
| | | | 11 | ×8 interpolation |

Table 24. Register PLLCFG (address 02h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-----------|---|
| 7 | PLL_BP | R/W | | PLL bypass |
| | | | 0 | DAC clock generated by PLL |
| | | | 1 | DAC clock provided via external pins CLKN and CLKP (PLL bypass mode) |
| 6 | PLL_BUF_PD | R/W | | PLL test buffer control |
| | | | 0 | Power-down mode |
| | | | 1 | enabled |
| 5 | PLL_PLL_PD | R/W | | PLL and CKGEN control |
| | | | 0 | Power-down mode |
| | | | 1 | enable |
| 4 to 3 | PLL_DIV[1:0] | R/W | | PLL divider factor |
| | | | 00 | $f_s = 2 \times f_{data}$ |
| | | | 01 | $f_s = 4 \times f_{data}$ |
| | | | 10 | $f_s = 8 \times f$ |
| | | | 11 | undefined |
| 2 to 1 | PLL_PHASE[1:0] | R/W | | PLL phase shift |
| | | | 00 | 0 degrees phase shift of f_s |
| | | | 01 | 120 degrees phase shift of f_s |
| | | | 10 | 240 degrees phase shift of f_s |
| | | | 11 | 240 degrees phase shift of f_s |
| 0 | PLL_OSC_PD | R/W | | PLL oscillator output power-down |
| | | | 0 | Power-down mode |
| | | | 1 | enabled |

Table 25. NCO frequency registers (address 04h to 08h) bit description

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|------------|--------|----------------|--------|-------|--|
| 04h | FREQNCO_B0 | 7 to 0 | FREQ_NCO[7:0] | R/W | | NCO frequency (two's complement coding) |
| | | | | | - | least significant 8 bits for the NCO frequency setting |
| 05h | FREQNCO_B1 | 7 to 0 | FREQ_NCO[15:8] | R/W | - | intermediate 8 bits for the NCO frequency setting |

Table 25. NCO frequency registers (address 04h to 08h) bit description ...continued

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|------------|--------|-----------------|--------|-------|---|
| 06h | FREQNCO_B2 | 7 to 0 | FREQ_NCO[23:16] | R/W | - | intermediate 8 bits for the NCO frequency setting |
| 07h | FREQNCO_B3 | 7 to 0 | FREQ_NCO[31:24] | R/W | - | intermediate 8 bits for the NCO frequency setting |
| 08h | FREQNCO_B4 | 7 to 0 | FREQ_NCO[39:32] | R/W | - | most significant 8 bits for the NCO frequency setting |

Table 26. DAC output phase correction registers (address 09h to 0Ah) bit description

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|--------------|--------|-----------------|--------|----------|---|
| 09h | PH_CORR_CTL0 | 7 to 0 | PHASE_COR[7:0] | R/W | - | DAC output phase correction factor (LSB) least significant 8 bits for the DAC output phase correction factor |
| 0Ah | PH_CORR_CTL1 | 7 | PH_COR_ENA | R/W | 0 | DAC output phase correction control DAC output phase correction disabled |
| | | | | | 1 | DAC output phase correction enabled |
| | | 4 to 0 | PHASE_COR[12:8] | R/W | 00000 | DAC output phase correction factor MSB most significant 5 bits for the DAC output phase correction factor |

Table 27. Digital gain control registers (address 0Bh to 0Eh) bit description

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|-----------------|--------|-------------------|--------|-------|---|
| 0Bh | DAC_A_DGAIN_LSB | 7 to 0 | DAC_A_DGAIN[7:0] | R/W | - | DAC A digital gain control least significant 8 bits for the DAC A digital gain |
| 0Ch | DAC_A_DGAIN_MSB | 3 to 0 | DAC_A_DGAIN[11:8] | | - | most significant 4 bits for the DAC A digital gain |
| 0Dh | DAC_B_DGAIN_LSB | 7 to 0 | DAC_B_DGAIN[7:0] | R/W | - | DAC B digital gain control least significant 8 bits for the DAC B digital gain |
| 0Eh | DAC_B_DGAIN_MSB | 3 to 0 | DAC_B_DGAIN[11:8] | | - | most significant 4 bits for the DAC B digital gain |

Table 28. Register DAC_OUT_CTRL (address 0Fh)

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|-----------|--------|----------|----------------------------|
| 3 | A_DGAIN_E | R/W | | DAC A digital gain control |
| | | | 0 | disable |
| | | | 1 | enable |

Table 28. Register DAC_OUT_CTRL (address 0Fh) ...continued
 Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|--------------|--------|-------|----------------------------|
| 2 | B_DGAIN_E | R/W | | DAC B digital gain control |
| | | | 0 | disable |
| 1 | MINUS_3DB | R/W | 1 | enable |
| | | | 0 | unity gain |
| 0 | CLIPPING_ENA | R/W | 1 | -3 dB gain |
| | | | 0 | disable |
| | | | 1 | enable |

Table 29. Register DAC_CLIPPING (address 10h)
 Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|-------|---|
| 7 to 0 | CLIPPING_LEVEL[7:0] | R/W | - | Digital DAC output clipping level value |

Table 30. Digital offset value registers (address 11h to 14h) bit description
 Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|------------------|--------|--------------------|--------|-------|---|
| 11h | DAC_A_OFFSET_LSB | 7 to 0 | DAC_A_OFFSET[7:0] | R/W | | DAC A digital offset value |
| | | | | | - | least significant 8 bits for the DAC A digital offset |
| 12h | DAC_A_OFFSET_MSB | 7 to 0 | DAC_A_OFFSET[15:8] | | - | most significant 8 bits for the DAC A digital offset |
| | | | | | | |
| 13h | DAC_B_OFFSET_LSB | 7 to 0 | DAC_B_OFFSET[7:0] | R/W | | DAC B digital offset value |
| | | | | | - | least significant 8 bits for the DAC B digital offset |
| 14h | DAC_B_OFFSET_MSB | 7 to 0 | DAC_B_OFFSET[15:8] | | - | most significant 8 bits for the DAC B digital offset |
| | | | | | | |

Table 31. NCO phase offset registers (address 15h to 16h) bit description
 Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|------------|--------|--------------|--------|-------|--|
| 15h | PHINCO_LSB | 7 to 0 | PH_NCO[7:0] | R/W | | NCO phase offset LSB |
| | | | | | - | least significant 8 bits for the NCO phase setting |
| 16h | PHINCO_MSB | 7 to 0 | PH_NCO[15:8] | R/W | | NCO phase offset MSB |
| | | | | | - | most significant 8 bits for the NCO phase setting |

Table 32. Analog gain control registers (address 17h to 1Ah) bit description

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|-------------|--------|-----------------|--------|-------|---------------------------------|
| 17h | DAC_A_GAIN1 | 7 to 0 | DAC_A_GAIN[7:0] | R/W | - | DAC A analog gain control (LSB) |
| 18h | DAC_A_GAIN2 | 7 to 6 | DAC_A_GAIN[9:8] | R/W | - | DAC A analog gain control (MSB) |
| 19h | DAC_B_GAIN1 | 7 to 0 | DAC_B_GAIN[7:0] | R/W | - | DAC B analog gain control (LSB) |
| 1Ah | DAC_B_GAIN2 | 7 to 6 | DAC_B_GAIN[9:8] | R/W | - | DAC B analog gain control (MSB) |

Table 33. Auxiliary DAC registers (address 1Bh to 1Eh) bit description

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|---------------|--------|------------|--------|-------|--|
| 1Bh | DAC_A_AUX_MSB | 7 to 0 | AUX_A[9:2] | R/W | - | most significant 8 bits for auxiliary DAC A |
| 1Ch | DAC_AUX_LSB | 7 | AUX_A_PON | R/W | 0 | off |
| | | | | | 1 | on |
| | | 1 to 0 | AUX_A[1:0] | R/W | - | least significant 2 bits for auxiliary DAC A |
| 1Dh | DAC_B_AUX_MSB | 7 to 0 | AUX_B[9:2] | R/W | - | most significant 8 bits for auxiliary DAC B |
| 1Eh | DAC_B_AUX_LSB | 7 | AUX_B_PON | R/W | 0 | off |
| | | | | | 1 | on |
| | | 1 to 0 | AUX_B[1:0] | R/W | - | least significant 2 bits for auxiliary DAC B |

Table 34. SPI_PAGE register (address 1Fh) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|------------------|
| 2 to 0 | PAGE[2:0] | R/W | - | SPI page address |

10.22.5 Page 1 allocation map

Table 35 shows an overview of all registers on page 1 (01h in hexadecimal).

Table 35. Page 1 register allocation map

| Address | Register name | R/W | Bit definition | | | | | | | | | Default ⁽¹⁾ | |
|---------|-------------------|-----|-----------------------|------------------------|-------------|---------------------|---------------------|---------------------|---------------------|--------------|------|------------------------|-----|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bin | Hex | |
| 0 00h | MDS_MAIN | R/W | MDS_EQCHECK[1:0] | | MDS_RUN | MDS_NCO | MDS_NCO_PULSE | MDS_SREF_DIS | MDS_MASTER | MDS_ENA | 0000 | 04h | |
| 1 01h | MDS_WIN_PERIOD_A | R/W | MDS_WIN_PERIOD_A[7:0] | | | | | | | | | 1000 | 80h |
| 2 02h | MDS_WIN_PERIOD_B | R/W | MDS_WIN_PERIOD_B[7:0] | | | | | | | | | 0100 | 40h |
| 3 03h | MDS_MISCCNTRL0 | R/W | - | - | - | MDS_EVAL_ENA | MDS_PRERUN_E | MDS_PULSEWIDTH[2:0] | | | 0001 | 10h | |
| 4 04h | MDS_MAN_ADJUSTDLY | R/W | MDS_MAN | MDS_MAN_ADJUSTDLY[6:0] | | | | | | | | 0100 | 40h |
| 5 05h | MDS_AUTO_CYCLES | R/W | MDS_AUTO_CYCLES[7:0] | | | | | | | | | 1000 | 80h |
| 6 06h | MDS_MISCCNTRL1 | R/W | MDS_SR_CKEN | MDS_SR_LOCKOUT | MDS_SR_LOCK | MDS_RELOCK | MDS_LOCK_DELAY[3:0] | | | | 0000 | 0Fh | |
| 7 07h | MDS_OFFSET_DLY | RW | - | - | - | MDS_OFFSET_DLY[4:0] | | | | | | 0000 | 00h |
| 8 08h | MDS_ADJDELAY | RW | - | MDS_ADJDELAY[6:0] | | | | | | | | 0000 | 00h |
| 9 09h | MDS_STATUS0 | R | EARLY | LATE | EQUAL | MDS_EQ | EARLY_ERROR | LATE_ERROR | EQUAL_FOUND | MDS_ACTIVE | uuuu | uuu | |
| 10 0Ah | MDS_STATUS1 | R | - | - | ADD_ERR | MDS_EN_PHASE[1:0] | | MDS_PRERUN | MDS_LOCKOUT | MDS_LOCK | uuuu | uuu | |
| 11 0Bh | INTR_CTRL | R/W | - | - | - | - | - | INTR_CLEAR | INTR_MON_DCLK_RANGE | | 0000 | 04h | |
| 12 0Ch | INTR_EN | R/W | MAQB_EN | MAQA_EN | AUTO_DL_EN | AUTO_CAL_EN | FLAG_DL_EN | LCLKSAMP_EN | PARBER_EN | MON_DCLK_EN | 0000 | 00h | |
| 13 0Dh | INTR_FLAGS | R | MAQB_RDY | MAQA_RDY | AUTO_DL_RDY | AUTO_CAL_RDY | FLAG_DL_ERR | LCLKSAMP_ERR | PARBER_ERR | MON_DCLK_ERR | uuuu | uuu | |

Table 35. Page 1 register allocation map ...continued

| Address | Register name | R/W | Bit definition | | | | | | | | Default ⁽¹⁾ | | | |
|---------|---------------|------------------|----------------|-----------|-------------|--------------|----------------|----------|-------------|--------------------|------------------------|--------------|--------------|-----|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bin | Hex | | |
| 14 | 0Eh | DAC_CURRENT_AUX | R/W | - | - | - | - | - | - | DAC_AUX_BIAS[3:0] | | | 0000 0111 | 07h |
| 15 | 0Fh | DAC_CURRENT_0 | R/W | - | - | - | - | - | - | DAC_DIG_BIAS[3:0] | | | 0000 0111 | 07h |
| 16 | 10h | DAC_CURRENT_1 | R/W | - | - | - | - | - | - | DAC_MST_BIAS[3:0] | | | 0000 0111 | 07h |
| 17 | 11h | DAC_CURRENT_2 | R/W | - | - | - | - | - | - | DAC_DRV_BIAS[3:0] | | | 0000 0111 | 07h |
| 18 | 12h | DAC_CURRENT_3 | R/W | - | - | - | - | - | - | DAC_SLV_BIAS[3:0] | | | 0000 0111 | 07h |
| 19 | 13h | DAC_CURRENT_4 | R/W | - | - | - | - | - | - | DAC_CK_BIAS[3:0] | | | 0000 0111 | 07h |
| 20 | 14h | DAC_CURRENT_5 | R/W | - | - | - | - | - | - | DAC_CAS_BIAS[3:0] | | | 0000 0111 | 07h |
| 21 | 15h | DAC_CURRENT_6 | R/W | - | - | - | - | - | - | DAC_COM_BIAS[3:0] | | | 0000 0111 | 07h |
| 22 | 16h | DAC_PON_SLEEP | R/W | DAC_B_PON | DAC_B_SLEEP | DAC_B_COM_PD | DAC_B_BLEED_PD | DAC_A_PD | DAC_A_SLEEP | DAC_A_COM_PD | DAC_A_BLEED_PD | 10111 011 | BBh | |
| 23 | 17h | DAC_CLKDIG_DELAY | R/W | - | - | - | - | - | - | PLL_DIG_DELAY[2:0] | | | 0000 0010 | 02h |
| 31 | 1Fh | PAGE_ADDRESS | R/W | - | - | - | - | - | - | PAGE[2:0] | | | 0000 0000 | 00h |

[1] u = undefined at power-up or after reset.

10.22.6 Page 1 bit definition detailed description

The tables in this section contain detailed descriptions of the page 1 registers.

Table 36. MDS_MAIN register (address 00h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-----------|--|
| 7 to 6 | MDS_EQCHECK[1:0] | R/W | | lock mode |
| | | | 00 | lock when (early = 1 and late = 1) |
| | | | 01 | lock when (early = 1, late = 1 and equal = 1) |
| | | | 10 | lock when equal = 1 |
| | | | 11 | force lock (equal-check = 1) |
| 5 | MDS_RUN | R/W | | evaluation process restart control |
| | | | 0 | no action |
| | | | 1 | (0 ≥ 1) transition restarts evaluation_counter |
| 4 | MDS_NCO | R/W | | NCO synchronization |
| | | | 0 | no action |
| | | | 1 | enable |
| 3 | MDS_NCO_PULSE | R/W | | NCO pulse |
| | | | 0 | no action |
| | | | 1 | manual control NCO tuning |
| 2 | MDS_SREF_DIS | R/W | | internal pulse generation |
| | | | 0 | normal mode |
| | | | 1 | disable |
| 1 | MDS_MASTER | R/W | | MDS mode selection |
| | | | 0 | slave mode |
| | | | 1 | master mode |
| 0 | MDS_ENA | R/W | | MDS function control |
| | | | 0 | disable |
| | | | 1 | enable |

Table 37. MDS window time registers (address 01h to 02h) bit description

Legend: * reset value; <= mandatory value

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|------------------|--------|-----------------------|--------|-------|---------------------------------|
| 01h | MDS_WIN_PERIOD_A | 7 to 0 | MDS_WIN_PERIOD_A[7:0] | R/W | - | determines MDS window LOW time |
| 02h | MDS_WIN_PERIOD_B | 7 to 0 | MDS_WIN_PERIOD_B[7:0] | R/W | - | determines MDS window HIGH time |

Table 38. MDS_MISCCNTRL0 register (address 03h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|--------------|--------|----------|----------------|
| 4 | MDS_EVAL_ENA | R/W | | MDS evaluation |
| | | | 0 | disable |
| | | | 1 | enable |

Table 38. MDS_MISCCNTRL0 register (address 03h) bit description ...continued

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|------------|---|
| 3 | MDS_PRERUN_ENA | R/W | | automatic MDS start-up |
| | | | 0 | no mds_win/mds_ref generation in advance |
| | | | 1 | mds_win/mds_ref run-in before mds_evaluation |
| 2 to 0 | MDS_PULSEWIDTH[2:0] | R/W | | width of MDS (in output clock -periods) |
| | | | 000 | 1 DAC clock period |
| | | | 001 | 2 DAC clock periods |
| | | | 010 to 111 | $(\text{mds_pulsewidth} - 1) \times 4$ DAC clock periods |

Table 39. MDS_MAN_ADJUSTDLY register (address 04h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------------|--------|----------|--|
| 7 | MDS_MAN | R/W | | adjustment delays mode |
| | | | 0 | auto-control adjustment delays |
| | | | 1 | manual control adjustment delays |
| 6 to 0 | MDS_MAN_ADJUSTDLY[6:0] | R/W | | adjustment delay value |
| | | | - | if MDS_MAN = 0 then initial value adjustment delay |
| | | | - | if MDS_MAN = 1 then controls adjustment delay |

Table 40. MDS_AUTO_CYCLES register (address 05h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------------|--------|-------|--|
| 7 to 0 | MDS_AUTO_CYCLES[7:0] | R/W | - | number of evaluation cycles applied for MDS. If set to 255, the IC continuously generates/monitors the MDS pulse |

Table 41. MDS_MISCCNTRL1 register (address 06h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|----------|--|
| 7 | MDS_SR_CKEN | R/W | - | lock mode |
| | | | 0 | free-running MDS_SR_CKEN |
| | | | 1 | MDS_SR_CKEN forced low |
| 6 | MDS_SR_LOCKOUT | R/W | | lockout detector soft reset |
| | | | 0 | MDS_SR_LOCKOUT in use |
| | | | 1 | MDS_SR_LOCKOUT forced low |
| 5 | MDS_SR_LOCK | R/W | | lock detector soft reset |
| | | | 0 | MDS_SR_LOCK in use |
| | | | 1 | MDS_SR_LOCK forced low |
| 4 | MDS_RELOCK | R/W | | relock mode |
| | | | 0 | no action |
| | | | 1 | relock when lockout occurs |
| 3 to 0 | MDS_LOCK_DELAY[3:0] | R/W | - | number of succeeding 'equal' detections until lock |

Table 42. MDS_OFFSET_DLY register (address 07h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|-------|--|
| 4 to 0 | MDS_OFFSET_DLY[6:0] | R/W | - | delay offset for dataflow (two's complement [-16 to 15]) |

Table 43. MDS_ADJDELAY register (address 08h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|-------------------------------|
| 6 to 0 | MDS_ADJDELAY[6:0] | R | - | actual value adjustment delay |

Table 44. MDS status registers (address 09h to 0Ah) bit description

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|-------------|-----|-------------|---|-------|--|
| 09h | MDS_STATUS0 | 7 | EARLY | R | | early signal (sampled) from early-to-late detector |
| | | | | | 0 | false |
| | | 1 | true | | | |
| | | 6 | LATE | R | | late signal (sampled) from early-to-late detector |
| | | | | | 0 | false |
| | | 1 | true | | | |
| | | 5 | EQUAL | R | | equal signal (sampled) from early-to-late detector |
| | | | | | 0 | false |
| | | 1 | true | | | |
| | | 4 | MDS_LOCK | R | | result equal-check |
| | | | | | 0 | false |
| | | 1 | true | | | |
| | | 3 | EARLY_ERROR | R | | adjustment delay maximum value stops the search |
| | | | | | 0 | false |
| 1 | true | | | | | |
| 2 | LATE_ERROR | R | | adjustment delay minimum value stops the search | | |
| | | | 0 | false | | |
| 1 | true | | | | | |
| 1 | EQUAL_FOUND | R | | evaluation logic has detected equal condition | | |
| | | | 0 | false | | |
| 1 | true | | | | | |
| 0 | MDS_ACTIVE | R | | evaluation logic active | | |
| | | | 0 | false | | |
| 1 | true | | | | | |

Table 44. MDS status registers (address 09h to 0Ah) bit description ...continued

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|-------------|--------|-------------------|--------|-------|---|
| 0Ah | MDS_STATUS1 | 5 | ADD_ERR | R | | adjustment delay error detection |
| | | | | | 0 | OK |
| | | | | | 1 | delay offset cannot be applied in available range |
| | | 4 to 3 | MDS_EN_PHASE[1:0] | R | | MDS enable phase |
| | | | | | 00 | enable phase = 0 |
| | | | | | 01 | enable phase = 1 (only for x2) |
| | | | | | 10 | enable phase = 2 (only for x2 and x4) |
| | | | | | 11 | enable phase = 3 (only for x2) |
| | | 2 | MDS_PRERUN | R | | MDS-PRERUN phase active flag |
| | | | | | 0 | false |
| | | | | | 1 | true |
| | | 1 | MDS_LOCKOUT | R | | MDS_LOCKOUT detected flag |
| | | | | | 0 | false |
| | | | | | 1 | true |
| | | 0 | MDS_LOCK | R | | MDS_LOCK flag |
| | | | | | 0 | false |
| | | | | | 1 | true |

Table 45. Interrupt control register (address 0Bh) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|-------|--|
| 3 | INTR_CTRL | R/W | | internal interrupt and flags clearance |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 2 to 0 | INTR_MON_DCLK_RANGE | R/W | | Interrupt condition as related to the DCLK monitoring |
| | | | 00 | mon_dclk_flag when mon_dclk drifts to (1 or 5) (detect small drift) |
| | | | 01 | mon_dclk_flag when mon_dclk drifts to (2 or 4) (detect large drift) |
| | | | 10 | mon_dclk_flag when mon_dclk drifts to (3) (detect maximum drift) |
| | | | 11 | mon_dclk_flag disabled |

Table 46. Interrupt enable register (address 0Ch) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|-------------|--------|-------|---------------------------------------|
| 7 | MAQB_EN | R/W | | acquisition module B interrupt |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 6 | MAQA_EN | R/W | | acquisition module A interrupt |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 5 | AUTO_DL_EN | R/W | | automatic download MTP interrupt |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 4 | AUTO_CAL_EN | R/W | | LVDS automatic calibration interrupt |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 3 | FLAG_DL_EN | R/W | | MTP download error interrupt |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 2 | LCLKSAMP_EN | R/W | | lclk sampling monitor error interrupt |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 1 | PARBER_EN | R/W | | LVDS parity or ber error interrupt |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 0 | MON_DCLK_EN | R/W | | dclk monitor error interrupt |
| | | | 0 | disabled |
| | | | 1 | enabled |

Table 47. INTR_FLAGS register (address 0Dh) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|--------------|--------|-------|-----------------------------------|
| 7 | MAQB_RDY | R | | acquisition module B status |
| | | | 0 | not ready |
| | | | 1 | ready |
| 6 | MAQA_RDY | R | | acquisition module A status |
| | | | 0 | not ready |
| | | | 1 | ready |
| 5 | AUTO_DL_RDY | R | | automatic download MTP status |
| | | | 0 | not ready |
| | | | 1 | ready |
| 4 | AUTO_CAL_RDY | R | | LVDS automatic calibration status |
| | | | 0 | not ready |
| | | | 1 | ready |

Table 47. INTR_FLAGS register (address 0Dh) bit description ...continued
 Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|-------------|--------|-------|---------------------------|
| 3 | FLAG_DL_ERR | R | | error during MTP download |
| | | | 0 | no error |
| | | | 1 | error detected |
| | | | 2 | LCLKSAMP_ERR |
| 0 | no error | | | |
| | | | 1 | error detected |
| | | | 1 | PARBER_ERR |
| 0 | no error | | | |
| | | | 1 | error detected |
| | | | 0 | MON_DCLK_ERR |
| 0 | no error | | | |
| | | | 1 | error detected |

Table 48. Bias current control registers (address 0Eh to 15h) bit description
 Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|-----------------|--------|-------------------|--------|-------|--|
| 0Eh | DAC_CURRENT_AUX | 3 to 0 | DAC_AUX_BIAS[3:0] | R/W | - | bias current control (see Table 49) |
| 0Fh | DAC_CURRENT_0 | 3 to 0 | DAC_DIG_BIAS[3:0] | R/W | - | |
| 10h | DAC_CURRENT_1 | 3 to 0 | DAC_MST_BIAS[3:0] | R/W | - | |
| 11h | DAC_CURRENT_2 | 3 to 0 | DAC_DRV_BIAS[3:0] | R/W | - | |
| 12h | DAC_CURRENT_3 | 3 to 0 | DAC_SLV_BIAS[3:0] | R/W | - | |
| 13h | DAC_CURRENT_4 | 3 to 0 | DAC_CK_BIAS[3:0] | R/W | - | |
| 14h | DAC_CURRENT_5 | 3 to 0 | DAC_CAS_BIAS[3:0] | R/W | - | |
| 15h | DAC_CURRENT_6 | 3 to 0 | DAC_COM_BIAS[3:0] | R/W | - | |

[1] All default values (except for register DAC_current_6) are OK for good performance over Process Voltage and Temperature.

[2] The register DAC_current_6 (address 0X15) must be set to 0X0A.

Table 49. Bias current control table

| BIAS[3:0] | Deviation from nominal current |
|-----------|--------------------------------|
| 0 0 0 0 | -35 % |
| 0 0 0 1 | -30 % |
| 0 0 1 0 | -25 % |
| 0 0 1 1 | -20 % |
| 0 1 0 0 | -15 % |
| 0 1 0 1 | -10 % |
| 0 1 1 0 | -5 % |
| 0 1 1 1 | +0 % (default) |
| 1 0 0 0 | +5 % |
| 1 0 0 1 | +10 % |
| 1 0 1 0 | +15 % |

Table 49. Bias current control table ...continued

| BIAS[3:0] | Deviation from nominal current |
|-----------|--------------------------------|
| 1 0 1 1 | +20 % |
| 1 1 0 0 | +25 % |
| 1 1 0 1 | +30 % |
| 1 1 1 0 | +35 % |
| 1 1 1 1 | +40 % |

Table 50. DAC_PON_SLEEP register (address 16h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|----------------|--------|-------|-----------------------------|
| 7 | DAC_B_PON | R/W | - | DAC B power control |
| | | | 0 | power-down |
| | | | 1 | power on |
| 6 | DAC_B_SLEEP | R | - | DAC B mode selection |
| | | | 0 | normal operation |
| | | | 1 | Sleep mode |
| 5 | DAC_B_COM_PD | R | - | commutator B control |
| | | | 0 | disable (power-down) |
| | | | 1 | enable |
| 4 | DAC_B_BLEED_PD | R | - | DAC B bleed current control |
| | | | 0 | disable (power-down) |
| | | | 1 | enable |
| 3 | DAC_A_PON | R | - | DAC A power control |
| | | | 0 | power-down |
| | | | 1 | power on |
| 2 | DAC_A_SLEEP | R | - | DAC B mode selection |
| | | | 0 | normal operation |
| | | | 1 | Sleep mode |
| 1 | DAC_A_COM_PD | R | - | commutator A control |
| | | | 0 | disable (power-down) |
| | | | 1 | enable |
| 0 | DAC_A_BLEED_PD | R | - | DAC A bleed current control |
| | | | 0 | disable (power-down) |
| | | | 1 | enable |

Table 51. DAC_TEST_8 register (address 17h) bit description

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------------|--------|-------|--|
| 2 to 0 | PLL_DIG_DELAY[2:0] | R/W | - | digital clock delay offset of PLL/CKGEN_DIV8 |

Table 52. SPI_PAGE register (address 1Fh) bit description*Default values are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|------------------|
| 2 to 0 | PAGE[2:0] | R/W | - | SPI page address |

10.22.7 Page A register allocation map

Table 53 shows an overview of all registers on page A (0Ah in hexadecimal).

Table 53. Page_0A register allocation map

| Address | Register name | R/W | Bit definition | | | | | | | | | Default | |
|---------|---------------|-----|------------------------|------------|------------------|------------------|----------------|---------------|------------|-----------|-----------|-----------|-----|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bin | Hex | |
| 0 00h | MAIN_CNTRL | R/W | - | - | - | LD_PD | PD_CNTRL | CAL_CNTRL | RST_DCKL | RST_LCKL | 0000 0011 | 03h | |
| 1 01h | MAN_LDCLKDEL | R/W | - | - | - | - | LDCLK_DEL[3:0] | | | 0000 0000 | 00h | | |
| 2 02h | DBG_LVDS | R/W | - | - | - | - | SBER | RESERVED | | | 0000 0000 | 00h | |
| 4 04h | RST_EXT_LDCLK | R/W | RST_EXT_LCLK_TIME[7:0] | | | | | | | | | 0011 1111 | 3Fh |
| 5 05h | RST_EXT_DCLK | R/W | RST_EXT_DCLK_TIME[7:0] | | | | | | | | | 0010 0000 | 20h |
| 6 06h | DCMSU_PREDIV | R/W | DCMSU_PREDIVIDER[7:0] | | | | | | | | | 0001 1101 | 1Dh |
| 8 08h | LD_POL_LSB | R/W | LD_POL[7:0] | | | | | | | | | 0000 0000 | 00h |
| 9 09h | LD_POL_MSB | R/W | LD_POL[15:8] | | | | | | | | | 0000 0000 | 00h |
| 10 0Ah | LD_CNTRL | R/W | PARITYC | DESCRAMBLE | SEL_EN[1:0] | WORD_SWAP | LDAB_SWAP | IQ_FORMAT | EDGE_LDCLK | 0000 0011 | 03h | | |
| 11 0Bh | MISC_CNTRL | R/W | SR_CDI | RESERVED | I_LEV_CNTRL[1:0] | Q_LEV_CNTRL[1:0] | | CDI_MODE[1:0] | | 0000 0000 | 00h | | |
| 12 0Ch | I_DC_LVL_LSB | R/W | I_DC_LEVEL[7:0] | | | | | | | | | 0000 0000 | 00h |
| 13 0Dh | I_DC_LVL_MSB | R/W | I_DC_LEVEL[15:8] | | | | | | | | | 1000 0000 | 80h |
| 14 0Eh | Q_DC_LVL_LSB | R/W | Q_DC_LEVEL[7:0] | | | | | | | | | 0000 0000 | 00h |
| 15 0Fh | Q_DC_LVL_MSB | R/W | Q_DC_LEVEL[15:8] | | | | | | | | | 1000 0000 | 80h |
| 16 10h | IO_MUX0 | R/W | IO_SELECT0[7:0] | | | | | | | | | 1111 1111 | FFh |

Table 53. Page_0A register allocation map ...continued

| Address | Register name | R/W | Bit definition | | | | | | | | Default | |
|---------|---------------|-----|----------------------|---------------|-------|-----------------|----------|-----------|--------------|-------|---------|-----|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bin | Hex |
| 17 11h | IO_MUX1 | R/W | IO_SELECT1[7:0] | | | | | | | | 1111 | FFh |
| 18 12h | IO_MUX2 | R/W | IO_SELECT1[9:8] | | - | IO_SELECT0[9:8] | | - | | 1111 | FFh | |
| 27 1Bh | TYPE_ID | R | DAC | FRONTEND[1:0] | | DUAL | DSP[1:0] | | BIT_RES[1:0] | | 0011 | 3Ch |
| 28 1Ch | DAC_VERSION | R | DAC_VERSION_ID[7:0] | | | | | | | | 0010 | 29h |
| 29 1Dh | DIG_VERSION | R | DIG_VERSION_ID[7:0] | | | | | | | | 0000 | 04h |
| 30 1Eh | LD_VERSION | R | LVDS_VERSION_ID[7:0] | | | | | | | | 0000 | 09h |
| 31 1Fh | PAGE_ADDRESS | R/W | - | - | - | - | - | PAGE[2:0] | | 0000 | 00h | |

10.22.8 Page A bit definition detailed description

The tables in this section contain detailed descriptions of the page A registers.

Table 54. Register MAIN_CNTRL (address 00h)

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|-----------|--------|----------|---|
| 4 | LD_PD | R/W | | LVDS interface power-down (control possible only when PD_CNTRL = 1) |
| | | | 0 | switched on |
| | | | 1 | switched off |
| 3 | PD_CNTRL | R/W | | power-down modes controlled by |
| | | | 0 | DCMSU block |
| | | | 1 | SPI registers |
| 2 | CAL_CNTRL | R/W | | compensation delay controlled by |
| | | | 0 | DCMSU block (automatic calibration) |
| | | | 1 | SPI registers (manual control) |
| 1 | RST_DCLK | R/W | | reset DCLK |
| | | | 0 | disable |
| | | | 1 | enable |
| 0 | RST_LCLK | R/W | | reset LVDS clock |
| | | | 0 | disable |
| | | | 1 | enable |

Table 55. Register MAN_LDCLKDEL (address 01h)

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-------|---|
| 3 to 0 | LDCLK_DEL[3:0] | R/W | | LVDS clock compensation delay (control only if CAL_CNTRL = 1) |
| | | | - | 4-bit compensation delay for LVDS clock |

Table 56. Register DBG_LVDS (address 02h)

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------|--------|------------|--------------------|
| 3 | SBER | R/W | | simple BER control |
| | | | 0 | no action |
| | | | 1 | simple BER active |
| 2 to 0 | RESERVED | R/W | 000 | reserved |

Table 57. Extension time reset registers (address 04h to 05h) bit description

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|--------------|--------|------------------------|--------|-------|--|
| 04h | RST_EXT_LCLK | 7 to 0 | RST_EXT_LCLK_TIME[7:0] | R/W | - | specifies extension time reset, expressed in LVDS clock periods 8 bits for the extension time reset |
| 05h | RST_EXT_DCLK | 7 to 0 | RST_EXT_DCLK_TIME[7:0] | R/W | - | specify extension time reset, expressed in DCLK periods 8 bits for the extension time reset |

Table 58. Register DCMSU_PREDIV (address 06h)

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------------|--------|-------|---|
| 7 to 0 | DCMSU_PREDIVIDER[7:0] | R/W | - | predivider value for the DCMSU, expressed in LVDS clock period 8 bits for the predivider value |

Table 59. LSB/MSB of polarity registers (address 08h to 09h) bit description

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|------------|--------|--------------|--------|-------|--|
| 08h | LD_POL_LSB | 7 to 0 | LD_POL[7:0] | R/W | - | toggles polarity of corresponding bit pair within LD[7:0] most significant 6 bits for the polarity toggle |
| 09h | LD_POL_MSB | 7 to 0 | LD_POL[15:8] | - | - | most significant 6 bits for the polarity toggle |

Table 60. Register LD_CNTRL (address 0Ah)

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|----------------------|---|
| 7 | PARITYC | R/W | 0 1 | parity check disable enable |
| 6 | DESCRAMBLE | R/W | 0 1 | Descramble control 0 disable descrambling enable descrambling |
| 5 to 4 | SEL_EN[1:0] | R/W | 00 01 10 11 | LDVS data enable LVDS data enable = align signal from channel A LVDS data enable = align signal from channel B LVDS data enable = 0 LVDS data enable = 1 |
| 3 | WORD_SWAP | R/W | 0 1 | reverse order for LVDS path 0 normal operation MSB to LSB order reversed |

Table 60. Register LD_CNTRL (address 0Ah) ...continued
 Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|------------|--------|----------|--|
| 2 | LDAB_SWAP | R/W | | swaps LVDS A and LVDS B paths |
| | | | 0 | normal operation |
| | | | 1 | LVDS A and LVDS B paths are swapped |
| 1 | IQ_FORMAT | R/W | | specify IQ supplied format |
| | | | 0 | folded |
| | | | 1 | interleaved |
| 0 | EDGE_LDCLK | R/W | | specify sampling edge for LVDS data path |
| | | | 0 | falling edge of LDCLK |
| | | | 1 | rising edge of LDCLK |

Table 61. Register MISC_CNTRL (address 0Bh)
 Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-----------|---|
| 7 | SR_CDI | R/W | | CDI block software reset control |
| | | | 0 | no action |
| | | | 1 | perform a software reset on CDI |
| 6 | RESERVED | R/W | 0 | reserved |
| 5 to 4 | I_LEV_CNTRL[1:0] | R/W | | specifies output from CDI for I path |
| | | | 00 | normal operation (CDI data output sent to digital signal processing input) |
| | | | 01 | if LDVS data enable = 1, then normal operation; if LDVS data enable = 0, then digital signal processing input = I_DC_LEVEL register value |
| | | | 10 | digital signal processing input = I_DC_LEVEL |
| | | | 11 | digital signal processing input = I_DC_LEVEL |
| 3 to 2 | Q_LEV_CNTRL[1:0] | R/W | | specifies output from CDI for Q path |
| | | | 00 | normal operation (CDI data output sent to digital signal processing input) |
| | | | 01 | if LDVS data enable = 1, then normal operation; if LDVS data enable = 0, then digital signal processing input = Q_DC_LEVEL register value |
| | | | 10 | digital signal processing input = Q_DC_LEVEL |
| | | | 11 | digital signal processing input = Q_DC_LEVEL |
| 1 to 0 | CDI_MODE[1:0] | R/W | | specifies CDI mode |
| | | | 00 | cdi_mode 0 (x2 mode) |
| | | | 01 | cdi_mode 1 (x4 mode) |
| | | | 10 | cdi_mode 2 (x8 mode) |
| | | | 11 | not used |

Table 62. LDS/MDS of I/Q DC levels registers (address 0Ch to 0Fh) bit description

Default values are shown highlighted.

| Address | Register | Bit | Symbol | Access | Value | Description |
|---------|--------------|--------|------------------|--------|-------|---|
| 0Ch | I_DC_LVL_LSB | 7 to 0 | I_DC_LEVEL[7:0] | R/W | - | I_DC_LEVEL least significant 8 bits for I_DC_LEVEL |
| 0Dh | I_DC_LVL_MSB | 7 to 0 | I_DC_LEVEL[15:8] | | - | most significant 8 bits for I_DC_LEVEL |
| 0Eh | Q_DC_LVL_LSB | 7 to 0 | Q_DC_LEVEL[7:0] | R/W | - | Q_DC_LEVEL least significant 8 bits for Q_DC_LEVEL |
| 0Fh | Q_DC_LVL_MSB | 7 to 0 | Q_DC_LEVEL[15:8] | | - | most significant 8 bits for Q_DC_LEVEL |

Table 63. Register IO_MUX0 and IO_MUX2 (address 10h and 12h)

Default values are shown highlighted.

| IO_SELECT0[9:0] | Signal on pin IO0 | Description |
|-----------------|--------------------------|---|
| 00 0000 0000 | lclk | internal LVDS lclk clock |
| 00 0000 0001 | ringo | internal low frequency oscillator (approximately 1 MHz) |
| 01 0000 nnnn | Ldout_A<nnnn> | internal LVDS data bit of channel A (<nnnn> = 15 to 0; enabling the selection of the bit number to be observed) |
| 10 0000 1111 | AND (Ldout_B bits) | AND result of the 16 LVDS data bits of channel B |
| 10 0001 1111 | OR (Ldout_B bits) | OR result of the 16 LVDS data bits of channel B |
| 10 0010 1111 | AND (Ldout_A bits) | AND result of the 16 LVDS data bits of channel A |
| 10 0011 1111 | OR (Ldout_A bits) | OR result of the 16 LVDS data bits of channel A |
| 11 1100 0000 | $\overline{\text{INTR}}$ | active low interrupt signal |
| 11 1100 0001 | INTR | active high interrupt signal |
| 11 1111 1110 | 1 | set the general-purpose IO to high level |
| 11 1111 1111 | 0 | set the general-purpose IO to low level |

Table 64. Register IO_MUX1 and IO_MUX2 (address 11h and 12h)

Default values are shown highlighted.

| IO_SELECT1[9:0] | Signal on pin IO1 | Description |
|-----------------|--------------------------|--|
| 00 0000 0000 | dclk | internal dclk clock ($f_s / 8$ frequency) |
| 01 0000 nnnn | Ldout_B<nnnn> | internal LVDS data bit of channel B (<nnnn> = 15 to 0; enabling the selection bit number to be observed) |
| 10 0000 1111 | AND (Ldout_B bits) | AND result of the 16 LVDS data bits of channel B |
| 10 0001 1111 | OR (Ldout_B bits) | OR result of the 16 LVDS data bits of channel B |
| 10 0010 1111 | AND (Ldout_A bits) | AND result of the 16 LVDS data bits of channel A |
| 10 0011 1111 | OR (Ldout_A bits) | OR result of the 16 LVDS data bits of channel A |
| 11 1100 0000 | $\overline{\text{INTR}}$ | active low interrupt signal |
| 11 1100 0001 | INTR | active high interrupt signal |
| 11 1111 1110 | 0 | set the general-purpose IO to low level |
| 11 1111 1111 | 1 | set the general-purpose IO to high level |

Table 65. Register TYPE_ID (address 1Bh)

Default values are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------|--------|-----------|------------------------------------|
| 7 | DAC | R | | calibration |
| | | | 0 | uncalibrated device |
| | | | 1 | calibrated device |
| 6 to 5 | FRONTEND | R | 01 | LVDS input interface |
| 4 | DUAL | R | 0 | dual DAC |
| 3 to 2 | DSP | R | | internal digital signal processing |
| | | | 11 | interpolation filter + SSBM |
| | | | 10 | SSBM |
| | | | 01 | interpolation filter |
| | | | 00 | none |
| 1 to 0 | BIT_RES | R | | DAC bit resolution |
| | | | 00 | 16 bits |
| | | | 01 | 14 bits |
| | | | 10 | 12 bits |
| | | | 11 | 10 bits |

Table 66. Register DAC_VERSION (address 1Ch)*Default values are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|-------|-----------------------------------|
| 7 to 0 | DAC_VERSION_ID[7:0] | R | | DAC version number |
| | | | - | 8 bits for the DAC version number |

Table 67. Register DIG_VERSION (address 1Dh)*Default values are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|-------|---------------------------------------|
| 7 to 0 | DIG_VERSION_ID[7:0] | R | | digital version number |
| | | | - | 8 bits for the digital version number |

Table 68. Register LVDS_VERSION (address 1Eh)*Default values are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|----------------------|--------|-------|---|
| 7 to 0 | LVDS_VERSION_ID[7:0] | R | | LVDS receiver version number |
| | | | - | 8 bits for the LVDS receiver version number |

Table 69. Register PAGE_ADD (address 1Fh)*Default values are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|----------------------|
| 2 to 0 | PAGE[2:0] | R/W | | Page address |
| | | | - | current page address |

11. Package outline

HVQFN72: plastic thermal enhanced very thin quad flat package; no leads; 72 terminals; body 10 x 10 x 0.85 mm

SOT813-3

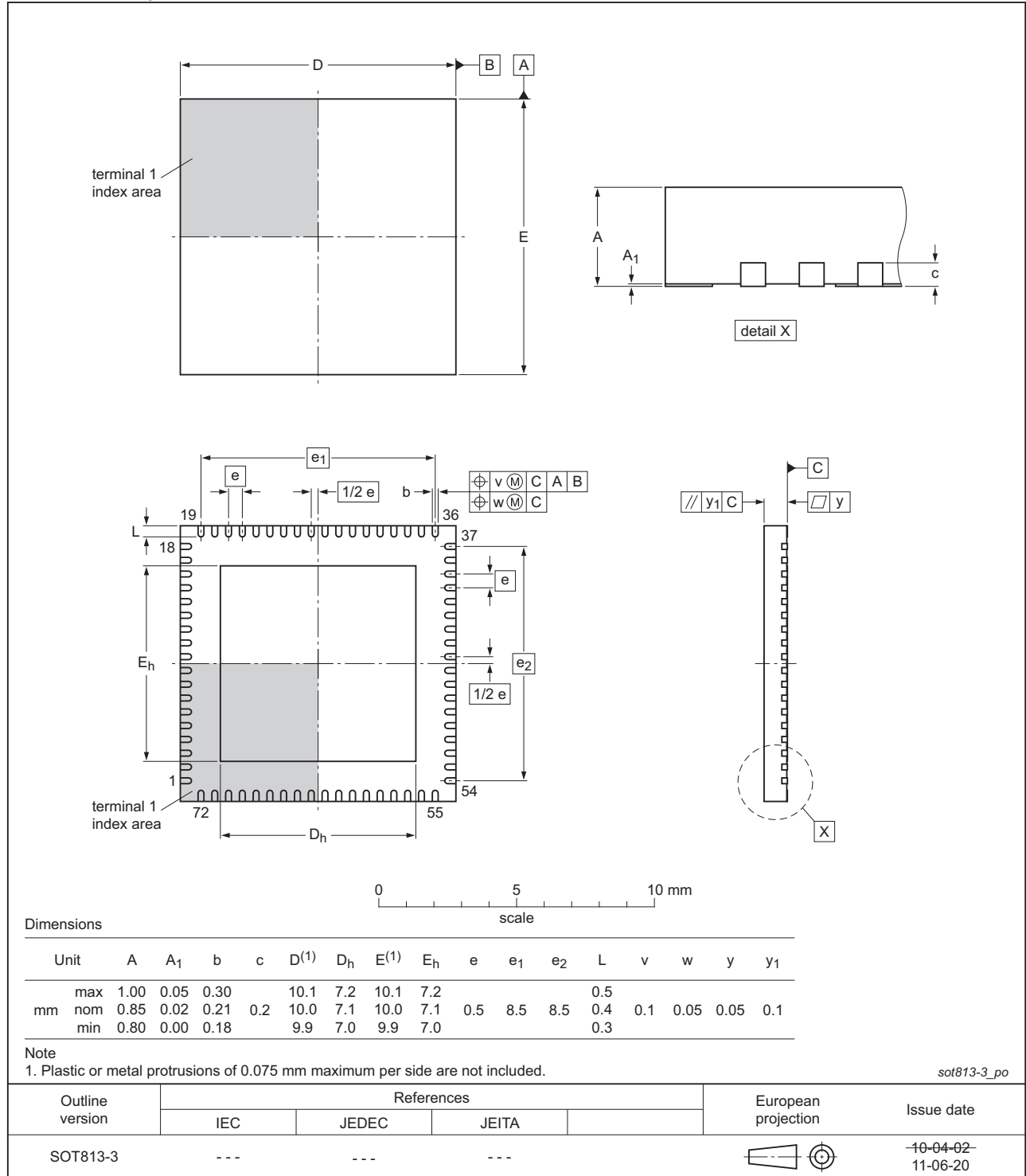


Fig 36. Package outline SOT813-3 (HVQFN72)

12. Abbreviations

Table 70. Abbreviations

| Acronym | Description |
|---------|---|
| BW | BandWidth |
| BWA | Broadband Wireless Access |
| CDI | Clock Domain Interface |
| CDMA | Code Division Multiple Access |
| CML | Current Mode Logic |
| CMOS | Complementary Metal Oxide Semiconductor |
| DAC | Digital-to-Analog Converter |
| EDGE | Enhanced Data rates for GSM Evolution |
| FIR | Finite Impulse Response |
| GSM | Global System for Mobile communications |
| IF | Intermediate Frequency |
| IMD3 | Third Order InterModulation |
| LMDS | Local Multipoint Distribution Service |
| LO | Local Oscillator |
| LVDS | Low-Voltage Differential Signaling |
| NCO | Numerically Controlled Oscillator |
| NMOS | Negative Metal-Oxide Semiconductor |
| PLL | Phase-Locked Loop |
| SFDR | Spurious-Free Dynamic Range |
| SPI | Serial Peripheral Interface |
| WCDMA | Wide band Code Division Multiple Access |
| WLL | Wireless Local Loop |

13. Glossary

13.1 Static parameters

INL — The deviation of the transfer function from a best fit straight line (linear regression computation).

DNL — The difference between the ideal and the measured output value between successive DAC codes.

13.2 Dynamic parameters

Spurious-Free Dynamic Range (SFDR) — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the largest spurious observed (harmonic and non-harmonic, excluding DC component) in the frequency domain.

Decibels relative to full scale (dBFS) — Unit used in a digital system to measure the amplitude level in decibel relative to the maximum peak value.

InterModulation Distortion (IMD) — From a dual-tone digital input sine wave (these two frequencies being close together), the intermodulation distortion products IMD2 and IMD3 (second order and third order components) are defined below.

IMD2 — The ratio between the RMS value of either tone and the RMS value of the worst second order Intermodulation product.

IMD3 — The ratio between the RMS value of either tone and the RMS value of the worst third order Intermodulation product.

Total Harmonic Distortion (THD) — The ratio between the RMS value of the harmonics of the output frequency and the RMS value of the output sine wave. Usually, the calculation of THD is done on the first 5 harmonics.

Signal-to-Noise Ratio (SNR) — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise excluding the harmonics and the DC component.

Restricted BandWidth Spurious-Free Dynamic Range (SFDR_{RBW}) — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise, including the harmonics, in a given bandwidth centered around f_{offset} .

14. Revision history

Table 71. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|---|------------------------|---------------|-------------------|
| DAC1617D1G0 v.3 | 20120702 | Rebranded/updated | - | DAC1617D1G0 v.2 |
| DAC1617D1G0 v.2 | <td> | Preliminary data sheet | - | DAC1617D1G0 v.1.1 |
| Modifications: | <ul style="list-style-type: none"> • Data sheet status changed from Objective to Preliminary. • Text and drawings updated throughout entire data sheet. | | | |
| DAC1617D1G0 v.1.1 | 20110930 | Objective data sheet | - | DAC1617D1G0 v.1 |
| DAC1617D1G0 v.1 | 20110906 | Objective data sheet | - | - |

15. Contact information

For more information or sales office addresses, please visit: <http://www.idt.com>

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