16-Bit, Serial Input, Loop-Powered, 4mA to 20mA DAC

Preliminary Technical Data

AD5421

FEATURES

- 16-Bit Resolution and Monotonicity
- Pin selectable NAMUR Compliant Ranges
  - 4mA to 20mA
  - 3.8mA to 21mA
  - 3.2mA to 24mA
- NAMUR Compliant ALARM Currents
  - Downscale ALARM current = 3.2mA
  - Upscale ALARM Current = 22.8mA/24mA
- 0.05% maximum Total Unadjusted Error (TUE)
- 0.0015% maximum INL Error (15 Bits minimum)
- 5ppm/°C typ Output Drift
- 350uA maximum Quiescent Current
- Flexible SPI Compatible Serial Digital Interface
  - Schmitt Triggered Inputs
- On-Chip Fault Alerts via FAULT pin or ALARM Current
  - Loss of SPI Interface Control
  - SPI Communication Error (Packet Error Check)
  - Programmed Loop Current out of Range
  - Insufficient Loop Voltage
  - Over Temperature
- Automatic Readback of Fault Register on each write cycle
- Slew Rate Control Function
- Gain and Offset Adjust Registers
- On-Chip Reference (10 ppm/°C Max)
- Selectable Regulated Voltage Output
- Loop Voltage Range
  - 5.5V to 52V
- Temperature Range: -40°C to +105°C
- TSSOP Package
- HART® Compatible

APPLICATIONS

- Industrial Process Control
- 4-20mA Loop Powered Transmitter
- Smart Transmitter

GENERAL DESCRIPTION

The AD5421 is a complete, loop powered, digital to 4mA-to-20mA converter, designed to meet the needs of smart transmitter manufacturers in the Industrial Control industry.

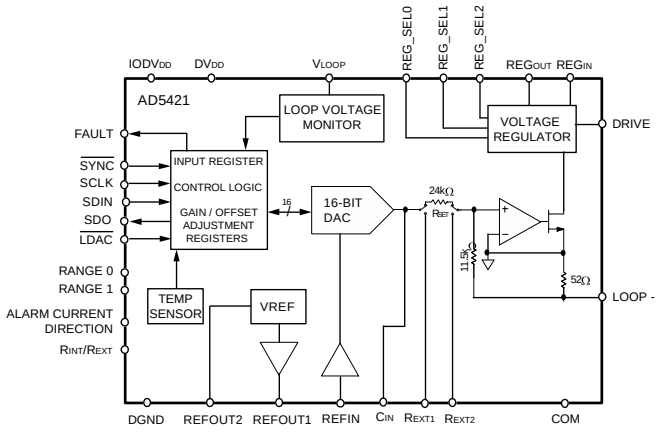

Figure 1. Functional Block Diagram

It provides a high precision, fully integrated, low cost solution in a compact TSSOP package.

The AD5421 includes a regulated voltage output that is used to power itself and other devices in the transmitter. This regulator provides a regulated 1.8V to 12V output voltage. The device also contains precision 1.25V and 2.5V references, The AD5421 thus eliminates the need for a discrete regulator and voltage reference.

The AD5421 can be used with standard HART® FSK protocol communication circuitry without any degradation in specified performance. The high speed serial interface is capable of operating at 20 Mbps and allows for simple connection to commonly-used microprocessors and microcontrollers via a SPI compatible three-wire interface.

The AD5421 is guaranteed monotonic to 16-bits, offers 0.0015% integral nonlinearity, 0.03% offset error and 0.03 % gain error.

The AD5421 is available in a 28 lead TSSOP package and is specified over the extended industrial temperature range of –40°C to +105°C.

Rev. PrN

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REVISION HISTORY

August 9, 2010 — Rev. PrM to Rev. PrN – Preliminary Version Datasheet

Changed DV_{DD} Output Voltage specification to 3.3V typical……Table 1, Page 4
Changed DV_{DD} Short Circuit Current specification to 7mA typical……..Table 1, Page 4
Included “Loop Current Error vs Load Current” specification……..Table 1, Page 4
Changed REGOUT Output Short Circuit Current specification to 23mA typical…Table 1, Page 4
Changes to Fault Thresholds ……...Table 1, Page 5
Changes to V_{LOOP} pin description……..……..…Table 7, Page 11
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SPECIFICATIONS

Loop Voltage = 24V; REFIN= +2.5 V external; R_L = 250Ω; all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					All Ranges
Internal R_{SET}					
Resolution	16			Bits	
Total Unadjusted Error (TUE)[2]	-0.1		+0.1	% FSR	B Version
	-0.05	±0.02	+0.05	% FSR	B Version,.T_A = 25°C
	-0.25		+0.25	% FSR	A Version
	-0.15	±0.1	+0.15	% FSR	A Version,.T_A = 25°C
Relative Accuracy (INL)	-0.006		+0.006	% FSR	
Differential Nonlinearity (DNL)	-1		+1	LSB	Guaranteed monotonic
Offset Error	-0.05		+0.05	% FSR	
	-0.01	±0.005	+0.01	% FSR	T_A = 25°C
Offset Error TC[3]		±5		ppm FSR/°C	
Gain Error	-0.05		+0.05	% FSR	
	-0.02	±0.01	+0.02	% FSR	T_A = 25°C
Gain Error TC[3]		±5		ppm FSR/°C	
Full-Scale Error	-0.05		+0.05	% FSR	
	-0.02	±0.01	+0.02	% FSR	T_A = 25°C
Full-Scale Error TC[3]		±5		ppm FSR/°C	
Zero-Scale Error	-0.05		+0.05	% FSR	
	-0.02	±0.01	+0.02	% FSR	T_A = 25°C
Zero-Scale Error TC[3]		±5		ppm FSR/°C	
Downscale Alarm Current			3.2	mA	All Ranges
Upscale Alarm Current	22.8			mA	4 to 20mA and 3.8 to 21mA Ranges
	24			mA	3.2 to 24mA Range
External R_{SET}					Assumes ideal resistor
Resolution	16			Bits	
Total Unadjusted Error (TUE)[2]	-0.05		+0.05	% FSR	B Version
	-0.025	±0.01	+0.025	% FSR	B Version, T_A = 25°C
	-0.15		+0.15	% FSR	A Version
	-0.075	±0.05	+0.075	% FSR	A Version, T_A = 25°C
Relative Accuracy (INL)	-0.0015		+0.0015	% FSR	
Differential Nonlinearity (DNL)	-1		+1	LSB	Guaranteed monotonic
Offset Error	-0.03		+0.03	% FSR	
	-0.01	±0.005	+0.01	% FSR	T_A = 25°C
Offset Error TC[3]		±3		ppm FSR/°C	
Gain Error	-0.03		+0.03	% FSR	
	-0.02	±0.01	+0.02	% FSR	T_A = 25°C
Gain Error TC[4]		±3		ppm FSR/°C	
Full-Scale Error	-0.03		+0.03	% FSR	
	-0.02	±0.01	+0.02	% FSR	T_A = 25°C
Full-Scale Error TC[3]		±3		ppm FSR/°C	
Zero-Scale Error	-0.03		+0.03	% FSR	
	-0.02	±0.01	+0.02	% FSR	T_A = 25°C
Zero-Scale Error TC[3]		±3		ppm FSR/°C	
Downscale Alarm Current			3.2	mA	All Ranges
Upscale Alarm Current	22.8			mA	4 to 20mA and 3.8 to 21mA Ranges
	24			mA	3.2 to 24mA Range

OUTPUT CHARACTERISTICS[3]					
Loop Compliance Voltage[5]	LOOP- + 5.5			V	REGOUT < 5.5V
	LOOP- +12.5			V	REGOUT = 12V
Loop Current Drift vs. Time		TBD		ppm FSR	Drift after 1000 hours at T_A = 125°C
Loop Current Error vs. load Current		0.8		µA/mA	Loop Current = 12mA , Load Current from REGOUT = 5 mA
Resistive Load	0		TBD	Ω	See figure TBD for a load line graph
Inductive Load		50		mH	
Power Supply Sensitivity			0.5	µA/V	Loop Current = 12mA
Output Impedance		50		MΩ	
Output TC		±5		ppm FSR/°C	Loop Current = 12mA, Internal R_{SET}
		±3		ppm FSR/°C	Loop Current = 12mA, External R_{SET}
Output Noise (0.1 Hz to 10Hz)		3		µA p-p	
Output Noise (500 Hz to 10 kHz)		1		mVp-p	HART® bandwidth. Measured across 500Ω load
Noise Spectral Density		TBD		nA/√Hz	@ 1kHz
		TBD		nA/√Hz	@ 10 kHz
REFERENCE INPUT/OUTPUT					
Reference Input[3]					
Reference Input Voltage[6]		2.5		V	For specified performance
DC Input Impedance	5	10		MΩ	
Reference Output					
REFOUT1					
Output Voltage	2.498	2.5	2.502	V	@T_A = 25°C
Temperature Coefficient		2	10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[3]		3		µV p-p	
Noise Spectral Density[3]		TBD		nV/√Hz	@ 1 kHz
		TBD		nV/√Hz	@ 10kHz
Output Voltage Drift vs. Time[3]		TBD		ppm	Drift after 1000 hours at T_A = 125°C
Capacitive Load[3]			TBD	nF	
Load Current[3,7]		0.5		mA	
Short Circuit Current[3]		1		mA	
Power Supply Sensitivity[3]		TBD		µV/V	
Thermal Hysteresis[3]		TBD		ppm	
Load Regulation[3]		TBD		V/mA	
Output Impedance		0.5		Ω	
REFOUT2					
Output Voltage	1.248	1.25	1.252	V	@T_A = 25°C
Output Impedance		100		kΩ	
REG_{OUT} OUTPUT					Voltage Regulator Output
Output Voltage	1.8		12	V	See Table 7
Output Voltage Accuracy		±2		%	
Externally Available Current[3,7]	3.15			mA	Assuming 4mA flowing in the Loop and during HART® Communications
Short Circuit Current		23mA			
Line Regulation[3]		1		mV/V	
Load Regulation[3]		15		mV/mA	
Inductive Load			50	mH	
Capacitive Load	2	10		µF	
ADC Accuracy					
Die Temperature		±5		°C	
V_{LOOP} – COM Voltage		±1		V	

DV_{DD} OUTPUT					Can be over-driven up to 5.5V
Output Voltage		3.3		V	
Externally Available Current[3,7]	4			mA	
Short Circuit Current		7		mA	
Load Regulation		TBD		mV/mA	
DIGITAL INPUTS[3]					SCLK, $\overline{SYNC}$, SDIN, $\overline{LDAC}$
V_{IH}, Input High Voltage	0.7 * $IODV_{DD}$			V	
V_{IL}, Input Low Voltage			0.3 * $IODV_{DD}$	V	
Hysteresis	100			mV	
Input Current	-1		+1	µA	Per pin
Pin Capacitance		10		pF	Per pin
DIGITAL OUTPUTS [3]					
SDO					
V_{OL}, Output Low Voltage			0.4	V	
V_{OH}, Output High Voltage	$IODV_{DD}$ - 0.5			V	
High Impedance Leakage Current	-1		+1	µA	
High Impedance Output Capacitance		5		pF	
FAULT					
V_{OL}, Output Low Voltage			0.4	V	
V_{OH}, Output High Voltage	$IODV_{DD}$ - 0.5			V	
FAULT Thresholds					
I_{LOOP} Under		I_{LOOP} – 5% FSR			
I_{LOOP} Over		I_{LOOP} + 5% FSR			
TEMP 140°C		140		°C	Fault is removed when temp ≥ 125°C
TEMP 100°C		100		°C	Fault is removed when temp ≥ 85°C
V_{LOOP} 6V		0.3		V	Fault is removed when V_{LOOP} ≥ 0.4V
V_{LOOP} 12V		0.6		V	Fault is removed when V_{LOOP} ≥ 0.7V
POWER REQUIREMENTS					
REG_{IN}	5.5		52	V	With respect to LOOP-
$IODV_{DD}$	1.7		5.5	V	With respect to COM
Quiescent Current		250	350	µA	

[1] Temperature range: -40°C to +105°C; typical at +25°C.
[2] Total Unadjusted Error is the total measured error (Offset error + Gain error + Linearity error) after factory calibration of the AD5421. System level total error may be reduced using the offset and gain registers.
[3] Guaranteed by design and characterization, Not production tested.

[5] The voltage between LOOP- and REGIN must be 5.5V or greater
[6] The AD5421 is factory calibrated with an external 2.5V reference connected to REFIN
[7] This is the current that the output is capable of sourcing. The load current originates from the loop and therefore contributes to the total current consumption figure.

Loop Voltage = 24V; REFIN= REFOUT (2.5V Internal reference); R_L = 250Ω; all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Table 2

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Internal R_{SET}					All Ranges
Total Unadjusted Error (TUE)	-0.15		+0.15	% FSR	
Relative Accurcy (INL)	-0.006		+0.006	% FSR	
Offset Error	-0.05		+0.05	% FSR	
Gain Error	-0.08		+0.08	% FSR	
Full-Scale Error	-0.08		+0.08	% FSR	
Output TC		±10		ppm/°C	Loop Current = 12mA
Output Noise (500 Hz to 10 kHz)		1.5		mVp-p	HART® bandwidth. Measured across 500Ω load
External R_{SET}					Assumes ideal resistor, All Ranges
Total Unadjusted Error (TUE)	-0.075		+0.075	% FSR	
Relative Accuracy(INL)	-0.0015		-0.0015	% FSR	
Offset Error	-0.03		+0.03	% FSR	
Gain Error	-0.05		+0.05	% FSR	
Full-Scale Error	-0.05		+0.05	% FSR	
Output TC		±8		ppm/°C	Loop Current = 12mA
Output Noise (500 Hz to 10 kHz)		1.5		mVp-p	HART® bandwidth. Measured across 500Ω load

[1] Specifications guaranteed by characterization, not production tested

AC PERFORMANCE CHARACTERISTICS

Loop Voltage = 24V; REFIN= +2.5 V external; R_L = 250Ω; all specifications T_{MIN} to T_{MAX}.

Table 3.

Parameter[1]		Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Current Settling Time	1	ms typ	To 0.1% FSR, C_{IN} = open circuit
	2	ms typ	To 0.1% FSR, C_{IN} = 20nF
	TBD	ms typ	To 0.1% FSR ,C_{IN} = 20nF, H_L = 50mH
Slew Rate	TBD	mA/µs typ	C_{IN} = open circuit
	TBD	mA/µs typ	C_{IN} = 20nF
	TBD	mA/µs typ	C_{IN} = 20nF, H_L = 50mH
AC Loop Voltage Sensitivity	1	µA/V typ	1200 Hz to 2200 Hz
Power-up Glitch	TBD	nA-s	
	TBD	nA-s	R_L = 1Ω

[1] Temperature range: -40°C to +105°C; typical at +25°C.

TIMING CHARACTERISTICS

Loop Voltage = 24V; REFIN= +2.5 V external; R_L = 250Ω; all specifications T_{MIN} to T_{MAX}.

Table 4.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	62.5	ns min	SCLK cycle time
t_2	25	ns min	SCLK high time
t_3	25	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	20	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	25	µs min	Minimum $\overline{SYNC}$ high time
t_7	10	ns min	Data setup time
t_8	10	ns min	Data hold time
t_9	20	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ falling edge
t_{10}	2	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{11}	20	ns min	$\overline{LDAC}$ pulse width low
t_{12}	60	ns max	SCLK rising edge to SDO valid ($C_{L\ SDO}$ = 15 pF)
t_{13}	10	ns min	$\overline{SYNC}$ falling edge to SCLK rising edge setup time
t_{14}	5	µs max	$\overline{SYNC}$ rising edge to SDO tri-state ($C_{L\ SDO}$ = 15 pF)

Table 5. SPI Watchdog Timeout Periods

T0	T1	T2		Unit	Description
0	0	0	50	ms typ	
0	0	1	100	ms typ	
0	1	0	500	ms typ	
0	1	1	1000	ms typ	
1	0	0	2000	ms typ	
1	0	1	3000	ms typ	
1	1	0	4000	ms typ	
1	1	1	5000	ms typ	

[1] Guaranteed by characterization. Not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2 and Figure 3.

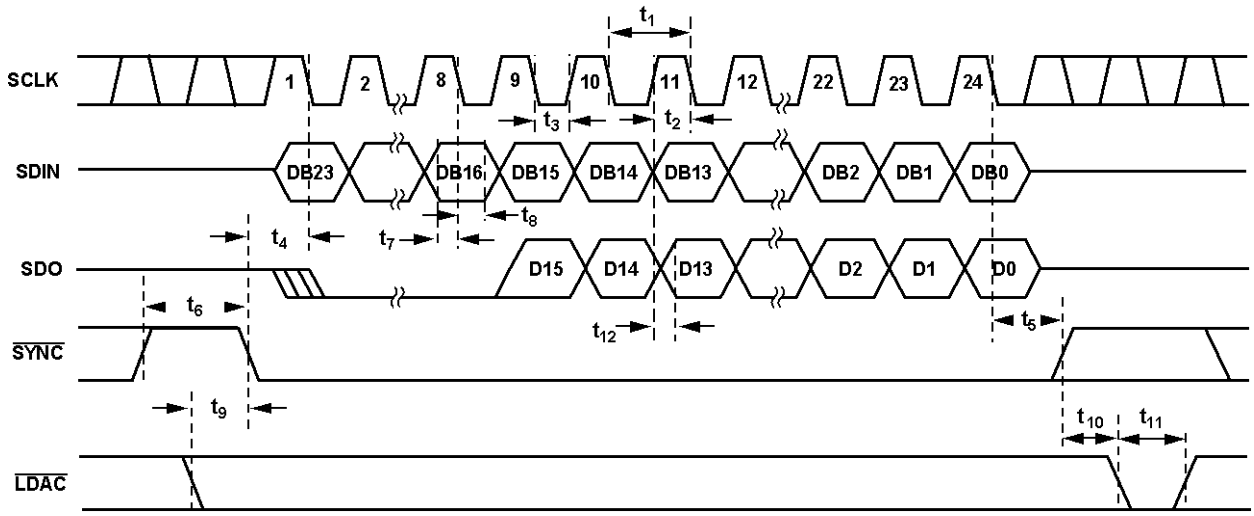


Figure 2. Serial Interface Timing Diagram

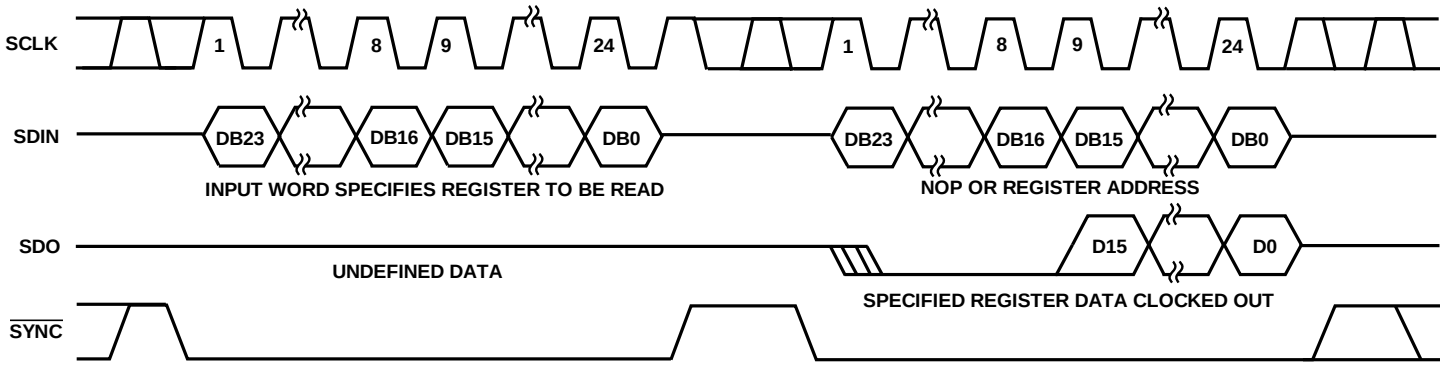


Figure 3. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.
Transient currents of up to 100 mA do not cause SCR latch-up.

Table 6.

Parameter	Rating
REG_{IN}/REG_{OUT} to COM	–0.3 V to +60 V
Digital Inputs to COM	
RANGE0,RANGE1,ALARM CURRENT DIRECTION, R_{INT}/R_{EXT},REG_SEL0,REG_SEL1, REG_SEL2	–0.3 V to DV_{DD}+ 0.3 V or +7 V (whichever is less)
SCLK,SDIN,$\overline{SYNC}$,$\overline{LDAC}$	–0.3 V to $IODV_{DD}$+ 0.3 V or +7 V (whichever is less)
Digital Outputs to COM	–0.3 V to DV_{DD} + 0.3 V or +7V (whichever is less)
REFIN/REFOUT1/REFOUT2 to COM	–0.3 V to +7 V
V_{LOOP} to COM	-0.3V to +60V
LOOP- to COM	+0.3V to –5V
DV_{DD} to COM	-0.3V to +7V
$IODV_{DD}$ to COM	-0.3V to +7V
$R_1/R_2/C_{IN}$ to COM	-0.3V to REG_{OUT}
Operating Temperature Range (T_A)	
Industrial	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature (T_J max)	125°C
TSSOP Package	
θ_{JA} Thermal Impedance	32°C/W
θ_{JC} Thermal Impedance	9°C/W
Power Dissipation	(T_J max – T_A)/ θ_{JA}
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

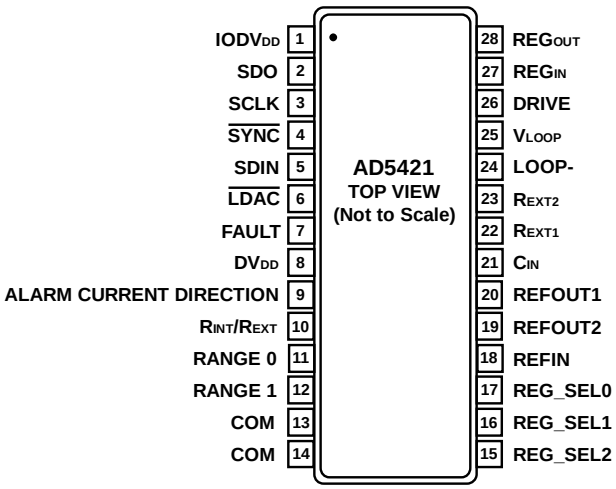


Figure 4. TSSOP Pin Configuration

Table 7. Pin Function Descriptions

TSSOP Pin No.	Mnemonic	Description
1	$IODV_{DD}$	Digital interface supply pin. Digital thresholds are referenced to the voltage applied to this pin. A voltage between 1.8V and 5.5V can be connected.
2	SDO	Serial Data Output. Used to clock data from the serial register. Data is clocked out on the rising edge and valid on the falling edge of SCLK.
3	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 16 MHz.
4	$\overline{SYNC}$	Active Low Frame Synchronisation Input. This is the frame synchronization signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred on the falling edge of SCLK. The Input shift register data is latched on the rising edge of $\overline{SYNC}$.
5	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
6	$\overline{LDAC}$	Active Low Load DAC Input. This is used to update the DAC register and consequently, the output current. When tied permanently low, the DAC register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the input register is updated, but the output update is held off until the falling edge of $\overline{LDAC}$. The $\overline{LDAC}$ pin should not be left unconnected.
7	FAULT	Active High Fault Alert Pin, This pin is asserted high when a fault is detected. Detectable faults are loss of SPI interface control, communication error(PEC), Loop current out of range, insufficient loop voltage and over temperature.
8	DV_{DD}	3V Digital power supply output, DV_{DD} should be decoupled to COM with a 100 nF capacitor. DV_{DD} can supply up to 4mA of current.
9	ALARM CURRENT DIRECTION	Digital Input Pin. Alarm Current Direction Select. This is used to select whether the Alarm current is upscale (22.8mA / 24mA) or downscale (3.2mA). Connecting this pin to DV_{DD} selects an upscale Alarm current (22.8mA / 24mA), connecting this pin to COM selects a downscale Alarm current (3.2mA). See Features section for further details.
10	R_{INT}/R_{EXT}	Digital Input Pin. Current setting resistor select. With this pin connected to DV_{DD} the internal current setting resistor is selected. With this pin connected to COM the external current setting resistor is selected. An external resistor can be connected between the R_{EXT1} and R_{EXT2} pins.
11 12	RANGE 0 RANGE 1	Digital input pins. These two pins select the loop current range.
13, 14	COM	Ground reference pin for the AD5421.
N/A	DNC	Do not connect to these pins

RANGE1	RANGE0	Loop Range
COM	COM	4mA to 20mA
COM	DV_{DD}	3.8mA to 21mA
DV_{DD}	COM	3.2mA to 24mA
DV_{DD}	DV_{DD}	3.8mA to 21mA

TSSOP Pin No.	Mnemonic	Description
15	REG_SEL2	Digital input pins. These three pins select the regulator output (REG_{OUT}) voltage.
16	REG_SEL1	
17	REG_SEL0	
18	REFIN	Reference Voltage Input. V_{REFIN} = 2.5 V for specified performance.
19	REFOUT2	Internal Reference Voltage Output. REFOUT = 1.25 V ± 2 mV @ 25°C.
20	REFOUT1	Internal Reference Voltage Output. REFOUT = 2.5 V ± 2 mV @ 25°C.
21	C_{IN}	External capacitor connection and HART FSK input. An external capacitor connected from C_{IN} to COM implements an output slew rate control function. HART FSK signalling can also be coupled through a capacitor to this pin. See Features section for further details.
22	R_{EXT1}	Connection for external current setting resistor. An external precision resistor may be connected between these pins for improved performance over temperature.
23	R_{EXT2}	
24	LOOP-	Loop Current Return Pin.
25	V_{LOOP}	Voltage input pin. Voltage input range is 0V to +2.5V. The voltage applied to this pin is digitised to 8 bits which are available in the Fault register. This pin can be used for general purpose voltage monitoring but is intended to be used for monitoring the loop supply voltage. Connecting the loop voltage to this pin via a 20:1 resistive divider allows the AD5421 to monitor and feedback the loop voltage. The AD5421 will also alert if the loop voltage is close to the minimum operating value. See Features section for further details.
26	DRIVE	Gate connection for external depletion mode mosfet. See Features section for further details.
27	REG_{IN}	Voltage regulator input, the loop voltage can be connected directly to this pin or alternatively to reduce on-chip power dissipation an external pass transistor can be connected here to standoff the loop voltage. See the Connecting the AD5421section for further details.
28	REG_{OUT}	Voltage regulator output, pin selectable value between 1.8V and 12V via the VS0, VS1 and VS2 pins.
EPAD	COM	The exposed paddle should be connected to the same potential as the COM pin and to a copper plane for optimum thermal performance

REG_SEL2	REG_SEL1	REG_SEL0	REG_{OUT}
COM	COM	COM	1.8V
COM	COM	DV_{DD}	2.5V
COM	DV_{DD}	COM	3V
COM	DV_{DD}	DV_{DD}	3.3V
DV_{DD}	COM	COM	5V
DV_{DD}	COM	DV_{DD}	9V
DV_{DD}	DV_{DD}	COM	12V

THEORY OF OPERATION

The AD5421 is an integrated device designed for use in loop-powered 4-20 mA smart transmitter applications. The AD5421, in a single chip provides a 16-bit DAC and current amplifier for digital control of the loop current, A voltage regulator to power the entire transmitter, a voltage reference, Fault alert functions, Flexible SPI compatible serial interface, Gain and offset adjust registers and other features and functions. Further details on the features of the AD5421 are described below.

SERIAL INTERFACE

The AD5421 is controlled over a versatile 3-wire serial interface that operates at clock rates up to 20 MHz. It is compatible with SPI, QSPI, MICROWIRE and DSP standards. Figure 2 shows the timing diagram. The interface will operate with both a continuous or non-continuous gated burst clock.
The write sequence begins with a falling edge of the $\overline{\text{SYNC}}$ signal, data is clocked in on the SDIN data line on the falling edge of SCLK. On the on the rising edge of $\overline{\text{SYNC}}$ the 24 bits of data are latched, also at this time the data is transfered to the addressed register and the programmed function is executed (a change in DAC output or mode of operation). If packet error checking on the SPI interface is required using cyclic redundancy codes, a further 8 bits must be written to the AD5421 making a 32 bit serial interface. In this case 32 bits are written to the AD5421 before $\overline{\text{SYNC}}$ is brought back high.

Input Shift Register

The input shift register is 24 bits wide (32 bits wide if CRC error checking of the data is required). Data is loaded into the device MSB first as a 24/32-bit word under the control of a serial clock input, SCLK. The input register consists of an 8-bit address/command byte, a 16-bit data word and an optional 8-bit CRC as shown in Table 9 and Table 10.The Address byte decoding is described in Table 8.

Table 8. Address/Command Word Functions

Address/Command Byte	Function
00000001	Write to Dac Register
00000010	Write to Control Register
00000011	Write to Offset Adjust Register
00000100	Write to Gain Adjust Register
00000101	Load DAC
00000110	Force Alarm Current
00000111	Reset
00001000	Initiate V_{LOOP} / TEMP Measurement
00001001	No Operation
10000001	Read Dac Register
10000010	Read Control Register
10000011	Read Offset Adjust Register
10000100	Read Gain Adjust Register
10000101	Read Fault Register

Readback

To be able to readback a register, bit D11 of the Control register must be set to logic 1 to disable the automatic readback of the Fault register.

Table 9. Input Shift Register

MSB																							LSB
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADDRESS/COMMAND BYTE								DATA WORD															

Table 10. Input Shift Register with CRC

MSB			LSB
D31 D24	D23 D8	D7 D0	
ADDRESS/COMMAND BYTE	DATA WORD	CRC	

DAC REGISTER

The Dac register is a read/write register and is addressed as outlined in Table 8. The data programmed to the dac register determines the loop current as shown by the transfer function equations below and in Table 12.

Table 11. Dac Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-Bit Data															

Ideal Output Transfer Function

The transfer function describing the relationship between the data programmed to the dac register and the loop current is expressed by the following three equations;

For the 4mA to 20mA output range, the loop current can be expressed as:

$$I_{LOOP} = \left[\frac{16mA}{2^N}\right] \times D + 4mA$$

For the 3.8mA to 21mA output range, the loop current can be expressed as:

$$I_{LOOP} = \left[\frac{17.2mA}{2^N}\right] \times D + 3.8mA$$

And for the 3.2mA to 24mA output range, the loop current can be expressed as:

$$I_{LOOP} = \left[\frac{20.8mA}{2^N}\right] \times D + 3.2mA$$

Where:
D is the decimal value of the Data register.
N is the bit resolution of the DAC, 16 in this case.

Table 12.Ideal Loop Current to Data register code relationship (Gain = 65536 , Offset = 0)

Dac Register Code	4mA to 20mA Range	3.8mA to 21mA Range	3.2mA to 24mA Range
0x0000	4 mA	3.8 mA	3.2 mA
0x0001	4.00024 mA	3.80026 mA	3.2003 mA
…	…	…	…
0x7FFF	11.9997 mA	12.39974 mA	13.5997 mA
0x8000	12 mA	12.4 mA	13.6 mA
…	…	…	…
0xFFFE	19.9995 mA	20.99947 mA	23.9994 mA
0xFFFF	19.9997 mA	20.99974 mA	23.9997 mA

CONTROL REGISTER

The Control register is a read/write register and is addressed as outlined in Table 8. The data programmed to the Control register determines the mode of operation of the AD5421.

Table 13. Control Register

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SPI Watchdog Timeout			SPI Watchdog	Auto Fault Readback	Alarm on SPI Fault	Set Min Loop Current	Select ADC Input	On-chip ADC	Internal Reference	V_{LOOP} Fault Alert					
T0	T1	T2													

Table 14. Control Register Bit Descriptions

Control Bit	Description			
SPI Watchdog Timeout	These three bits allow the user to program the watchdog timeout period. The watchdog timer is reset on a valid write to any one of the AD5421's registers or on writing a NOP.			
	T0	**T1**	**T2**	**Timeout Period**
	0	0	0	50 ms
	0	0	1	100 ms
	0	1	0	500 ms
	0	1	1	1 second (Default)
	1	0	0	2 seconds
	1	0	1	3 seconds
	1	1	0	4 seconds
	1	1	1	5 seconds
SPI Watchdog	0	The SPI watchdog timer is enabled (Default)		
	1	The SPI watchdog is disabled		
Auto Fault Readback	0	On each write operation the Fault register contents are clocked out on the SDO pin (Default)		
	1	Fault register contents are not automatically clocked out on SDO pin. (Fault register can be addressed for readback)		
Alarm on SPI	0	If an SPI fault is detected (Watchdog timer times out) the SPI fault bit of the Fault register and the FAULT pin will be set		

Control Bit		Description
Fault		and the loop current will be forced to the Alarm value (Default)
	1	If an SPI fault is detected (Watchdog timer times out) the SPI fault bit of the Fault register and the FAULT pin will be set. The loop current will not be forced to the Alarm value.
Set Min Loop Current	0	Normal Operation (Default)
	1	The loop current is set to its minimum possible value so that the total current flowing in the loop consists only of the operating current of the AD5421 and the load current of the REG_{OUT} pin.
Select ADC Input	0	The on-chip ADC measures the voltage connected at the V_{LOOP} pin (Default).
	1	The on-chip ADC measures the temperature of the AD5421 die.
On-chip ADC	0	On-chip ADC is disabled (Default)
	1	On-chip ADC is enabled
Power Down Internal Reference	0	Internal voltage referenced is powered-up (Default)
	1	Internal voltage reference is powered-down and an external voltage reference source is required.
V_{LOOP} Fault Alert	0	The Fault pin will not be set if the V_{LOOP} – COM voltage falls to approx. 0.3V. The V_{LOOP} 6V bit of the Fault register will be set.
	1	If the V_{LOOP} – COM voltage falls to approx. 0.3V the Fault pin will be set as well as the V_{LOOP} 6V bit of the Fault register

FAULT REGISTER

The Fault register is a read only register and is addressed as outlined in Table 8. The bits in the fault register alert to a range of possible fault conditions. If any one of the fault bits are activated the fault pin will also be activated.

Table 15. Fault Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SPI	PEC	I_{LOOP} Over	I_{LOOP} Under	Temp 140°C	Temp 100°C	V_{LOOP} 6V	V_{LOOP} 12V	8-bit V_{LOOP} / Temperature Value							

Table 16. Fault Register Bit Descriptions

Fault Alert	Fault Pin Set	Alarm Current	Description
SPI	Yes	Yes, if bit D10 of the Control register is cleared.	This bit is set high to alert to the loss of the SPI interface signalling, the fault is alerted if there is no valid communication to the AD5421 over the SPI interface for more than the user defined timeout period. The occurence of this fault will also force the loop current to the Alarm value (if bit D10 of the Control register is at logic 0). The Alarm current direction is determined by the state of the ALARM CURRENT DIRECTION pin.
PEC (Packet Error Check)	Yes	No	This bit is set high to alert to an error in the SPI communication, the error is detected using Cyclic Redundancy Code (CRC) error detection. See Features section for further details.
I_{LOOP} Under	Yes	No	This bit is set high to alert to an error in the loop current, the fault is alerted if the actual loop current is less than the programmed loop current.
I_{LOOP} Over	Yes	No	This bit is set high to alert to an error in the loop current, the fault is alerted if the actual loop current is greater than the programmed loop current.
Temp 100°C	No	No	This bit is set high to alert to an increasing temperature of the AD5421. This bit is set if the die temperature of the AD5421 exceeds approx. 100°C, this bit will be cleared when the temperature returns below approx. 85°C
Temp 140°C	Yes	No	This bit is set high to alert to an over temperature fault. This bit is set if the die temperature of the AD5421 exceeds approx. 140°C, this bit will be cleared when the temperature returns below approx. 125°C
V_{LOOP} 12V	No	No	This bit is set high to alert that the voltage between the V_{LOOP} and COM pins has fallen below approx. 0.6V (Representing a 12V loop supply voltage with 20:1 resistor divider connected at V_{LOOP}), this bit will be cleared when the voltage returns above approx. 0.7V
V_{LOOP} 6V	Yes	No	This bit is set high to alert that the voltage between the V_{LOOP} and COM pins has fallen below approx. 0.3V (Representing a 6V loop supply voltage with 20:1 resistor divider connected at V_{LOOP}), this bit will be cleared when the voltage returns above approx. 0.4V.

Fault Alert	Fault Pin Set	Alarm Current	Description
V_{LOOP} / Temperature Value	N/A	N/A	8-bit representation of V_{LOOP} – COM voltage or AD5421 die temperature, selected by D8 of the control register

8-bit value	V_{LOOP} – COM Voltage	Die Temperature (°C)
0 0 0 0 0 0 0 0	0 Volts	300
	…	…
1 1 1 1 1 1 1 1	2.49 Volts	-55

The transfer function equations for the measurement of V_{LOOP} – COM and the die temperature are respectively:

$$V_{LOOP} - COM = \left(\frac{2.5}{256}\right) * D$$

$$Die\ Temperature = 125 - 1.771 * (D - 128)$$

Where;

D is the 8-bit digital code returned from the on-chip ADC

OFFSET ADJUST REGISTER

The Offset adjust register is a read/write register and is addressed as outlined in Table 8.

Table 17. Offset Adjust Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-Bit Offset Adjust Data															

Table 18. Offset Adjust Register adjustment range

Offset Adjust Register Data	Digital Adjustment (LSBs)
65535	+ 32767
65534	+ 32766
…	…
32769	+ 1
32768 (Default)	0
32767	- 1
…	…
1	- 32767
0	- 32768

GAIN ADJUST REGISTER.

Table 19. Gain Adjust Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-Bit Gain Adjust Data															

Table 20. Gain Adjust Register adjustment range

Gain Adjust Register Data	Loop Current (mA)
65535 (Default)	DAC Register Data
65534	$\left(DAC\ Register\ Data / 65536\right) \times 65534$
…	…
32769	$\left(DAC\ Register\ Data / 65536\right) \times 32769$
32768	$\left(DAC\ Register\ Data / 65536\right) \times 32768$
32767	$\left(DAC\ Register\ Data / 65536\right) \times 32767$
…	…
1	$\left(DAC\ Register\ Data / 65536\right) \times 1$
0	0

When the Offset adjust and Gain adjust register values are taken into account the transfer equations become;

For the 4mA to 20mA output range, the loop current can be expressed as:

$$I_{LOOP} = \left[\frac{\left(16mA/2^N\right) * Gain}{2^N}\right] * D + 4mA + \left[\left(\frac{16mA}{2^N}\right) * (Offset - 32768)\right]$$

For the 3.8mA to 21mA output range, the loop current can be expressed as:

$$I_{LOOP} = \left[\frac{\left(17.2mA/2^N\right) * Gain}{2^N}\right] * D + 3.8mA + \left[\left(\frac{17.2mA}{2^N}\right) * (Offset - 32768)\right]$$

And, for the 3.2mA to 24mA output range, the loop current can be expressed as:

$$I_{LOOP} = \left[\frac{\left(20.8mA/2^N\right) * Gain}{2^N}\right] * D + 3.2mA + \left[\left(\frac{20.8mA}{2^N}\right) * (Offset - 32768)\right]$$

Where:
D is the decimal value of the Data register.
N is the bit resolution of the DAC, 16 in this case.
Gain is the decimal value of the Gain Adjust Register
Offset is the decimal value of the Offset Adjust Register

FEATURES

FAULT ALERTS

The AD5421 provides a number of fault alert features. All of the faults are alerted to the controller via the FAULT pin and the Fault register, in the case of a loss of communications between the AD5421 and the micro-controller (SPI fault), the AD5421 will program the loop current to an alarm value. If the controller detects that the FAULT pin has been set high, it should then read the Fault register to determine the cause of the fault.

SPI Fault

The SPI Fault is alerted if there is no valid communication to any register on the SPI bus for more than a user defined period, the user can program the time period in the Control register, The SPI Fault bit alerts to the fault on the SPI bus. As this fault is caused by a loss of communication between the controller and the AD5421 the loop current will also be forced to the alarm value, the direction of the alarm current (downscale or upscale) is selected via the ALARM CURRENT DIRECTION pin.

Packet Error Check

To verify that data has been received correctly in noisy environments, the AD5421 offers the option of error checking based on an 8-bit cyclic redundancy check. Packet error checking is enabled by writing to the AD5421 with a 32 bit serial frame where the least significant 8 bits is the frame check sequence.. The device controlling the AD5421 should generate the 8-bit frame check sequence using the polynomial :

$$C(x) = X^8 + X^2 + X + 1$$

This is appended to the end of the data word and 32 data bits are sent to the AD5421 before taking $\overline{SYNC}$ high. If the check is valid the data will be accepted. If the error check fails, the FAULT pin will be asserted and the PEC bit of the Fault register will be set. After the Fault register is read the PEC bit will be reset low and the FAULT pin will return low.
In the case of data reads, if the AD5421 is addressed with a 32 bit frame, it will generate the 8 bit frame check sequence and append it to the end of the 24 bit data stream to create a 32 bit data stream.

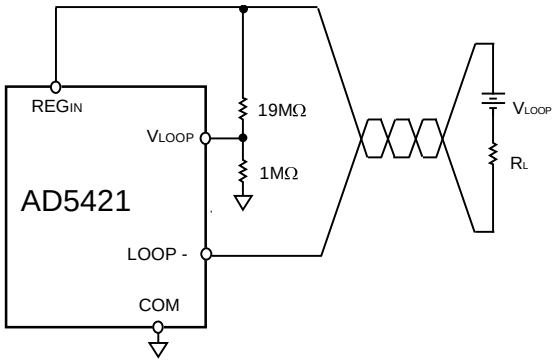


Figure 5. Resistor Divider Connection At V_{LOOP} pin

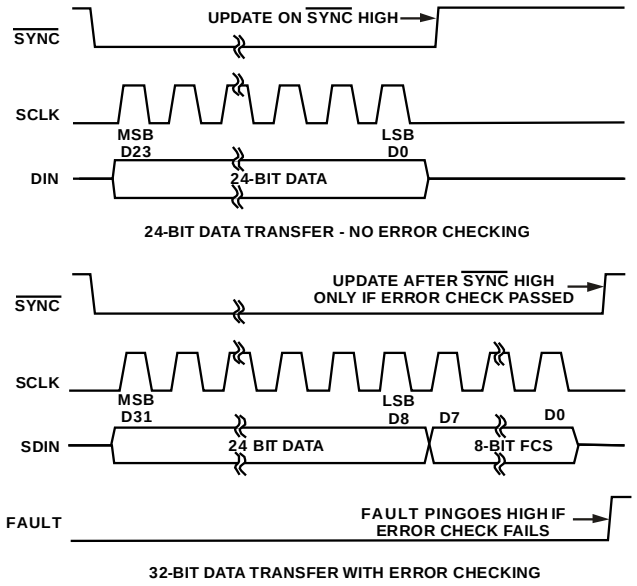


Figure 6. PEC Timing

Current Loop Fault

The current loop (I_{LOOP}) fault is alerted if the actual loop current is not within ±2%FSR of the programmed loop current. For example, if a loop current of 10 mA is programmed, the measured loop current must be within the range 9.8 mA to 10.2mA, otherwise a current loop fault will be alerted. If the loop current is less than that programmed the *I_{LOOP}Under* bit of the control register will be set, if the loop current is greater than that programmed the *I_{LOOP}OVER* bit of the control register will be set. The FAULT pin will be set to logic high in either case.

Over-Temperature Fault

There are two over temperature alert bits in the Fault register, *TEMP 100°C* and *TEMP 140°C*. If the die temperature of the AD5421 exceeds either 100°C or 140°C the relevant bit will be set, in the case of TEMP 140°C, the FAULT pin will be set to logic high.

Loop Voltage Fault

There are two Loop Voltage alert bits in the fault register, *V_{LOOP}12V* and *V_{LOOP}6V,* If the voltage between the V_{LOOP} and COM pins falls below 0.6V (corresponding to a 12V loop supply value) the *V_{LOOP}12V* bit is set, this bit is cleared when the voltage returns above 0.7V, similarly if the voltage between the V_{LOOP} and COM pins falls below 0.3V (corresponding to a 6V loop supply value) the *V_{LOOP}6V* bit is set, this bit is cleared once tha voltage returns above 0.4V. In the case of the V_{LOOP}12V alert, the FAULT pin will be set to logic high. Figure 5 demonstrates how a resistor divider enables the monitoring of the loop supply with the V_{LOOP} input. The recommended resistor divider consists of a 1MΩ and a 19MΩ resistor providing a 20:1 ratio allowing the 2.5V input range of the V_{LOOP} pin monitor up to 50V loop supplies. With a 20:1 divider ratio the preset 6V and 12V alert bits in the Fault register will alert to a loop supply at

their stated values. Inserting other divider ratios will mean that the fault bits will alert at values that are not equal to 6V and 12V.

ON-CHIP ADC

The AD5421 contains an on-chip ADC used to measure and feedback to the FAULT register either the temperature of the die or the voltage between the V_{LOOP} and COM pins. Bit D8 (Select ADC Input) of the Control Register selects which parameter is to be converted. A conversion is initiated with command byte 00001000 (This is necessary only if auto fault readback is disabled). This command byte powers-on the ADC and performs the conversion. A read of the Fault register reads the conversion result. If auto readback of the Fault register is required the ADC must first be powered-up by setting bit D7 (On-Chip ADC) of the Control register.

VOLTAGE REGULATOR

The on-chip voltage regulator provides a regulated voltage to supply the AD5421 and the remainder of the transmitter circuitry. The output voltage is selected by the states of three digital input pins. The output voltage range is from 1.8V to 12V and is set as outlined in Table 21. The regulator output is accessed at the REG_{OUT} pin.

Table 21. Setting the Voltage Regulator Output

REG_SEL0	REG_SEL1	REG_SEL2	Regulated Output Voltage
COM	COM	COM	1.8V
COM	COM	DV_{DD}	2.5V
COM	DV_{DD}	COM	3.0V
COM	DV_{DD}	DV_{DD}	3.3V
DV_{DD}	COM	COM	5.0V
DV_{DD}	COM	DV_{DD}	9.0V
DV_{DD}	DV_{DD}	COM	12.0V

LOOP CURRENT SLEW RATE CONTROL

The rate of change of the loop current can be controlled by connecting an external capacitor between the C_{IN} pin and COM, this will reduce the rate of change of the loop current. The output resistance of the DAC (R_{DAC}) together with capacitor (C_{SLEW}) generate a time constant that determines the response of the loop current, see Figure 7.

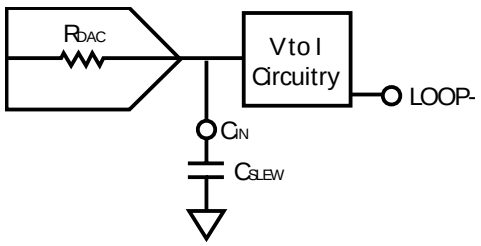


Figure 7.Slew Capacitor Circuit

The resistance of the DAC is typically 15.22 kΩ for the 4mA to 20mA and 3.8mA to 21mA loop current ranges, the DAC resistance changes to 16.11kΩ when the 3.2mA to 24mA loop current range is selected.

The time constant of the circuit is expressed as;

$$\tau = R_{DAC} * C_{SLEW}$$

Taking 5 time constants as the required time to reach final value, C_{SLEW} can be determined as follows for a desired response time, *T*;

$$C_{SLEW} = \frac{T}{5 * R_{DAC}}$$

Where;
T is the desired time for the output current to reach its final value
R_{DAC} is the resistance of the DAC core which has a value of 15.22kΩ or 16.11kΩ depending on the selected loop current range.

For a response time of 5ms;

$$C_{SLEW} = \frac{5ms}{5 * 15220} \approx 66nF$$

For a response time of 10ms;

$$C_{SLEW} = \frac{10ms}{5 * 15220} \approx 130nF$$

The responses for both of these configurations are shown in Figure 8.

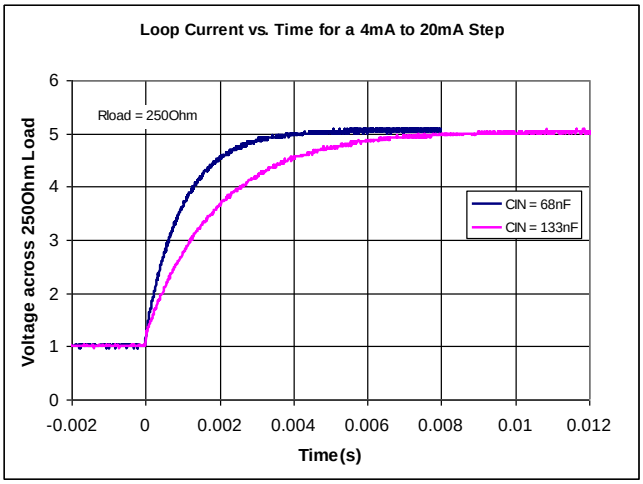


Figure 8. 4mA to 20mA step

The C_{IN} pin can also be used as a coupling input for HART FSK signalling. The HART signal must be ac coupled to the C_{IN} input. The capacitor through which the HART signal is coupled must be considered in the above calculations where the total capacitance is C_{SLEW} + C_{HART}. For further details on HART communications refer to the HART Communications section.

POWER-ON DEFAULT

The AD5421 will power-on with zero-code loaded to all registers and with the loop current set at 3.2mA or 22.8mA/24mA (depending on the state of the alarm current direction pin and selected range), it will stay in this state until it is programmed with a new value. The SPI watchdog timer is enabled by default with a timeout period of 1 second, if there is no communication with the AD5421 within 1 second of power-on the Fault pin will be set.

HART COMMUNICATIONS

The AD5421 can be interfaced to a HART modem to enable HART digital communications over the two wire loop connection. Figure 9 shows how the modem FSK output is connected to the AD5421.

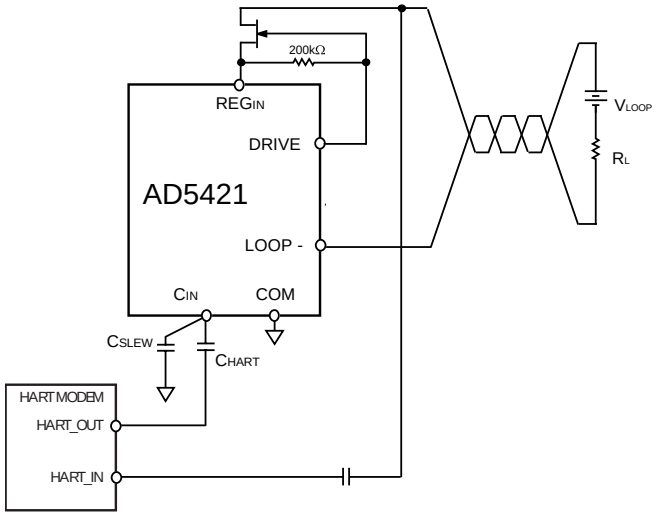


Figure 9. Connecting a HART modem to the AD5421

To achieve a 1mAp-p FSK current signal on the loop, the voltage at the C_{IN} pin must be 111mVp-p. Assuming a 500mVp-p output from the HART modem, this means the signal must be attenuated by a factor of 4.5. The following equation can be used to calculate the values of the capacitors C_{HART} and C_{SLEW}.

$$4.5 = \frac{C_{HART} + C_{SLEW}}{C_{HART}}$$

From this equation the ratio of C_{HART} to C_{SLEW} is 1 to 3.5. This ratio of the capacitor values will set the amplitude of the HART FSK signal on the loop, the absolute values of the capacitors will set the response time of the loop current, and also the bandwidth presented to the HART signal input at the C_{IN}.pin. The bandwidth must pass frequencies from 500Hz to 10kHz, The two capacitors and the internal impedance, R_{DAC} form a highpass filter, the 3dB Frequency of which should be less than. 500Hz. The 3dB frequency can be calculated as follows ;

$$F_{3dB} = \frac{1}{2 * \pi * R_{DAC} * (C_{HART} + C_{SLEW})}$$

From this equation, to achieve a 500Hz high pass 3dB frequency cut off, the combined values of C_{HART} and C_{SLEW} should be 21nF. The final values for the capacitors are C_{HART} = 4.7nF and C_{SLEW} = 16.3nF to ensure the correct HART signal amplitude on the current loop.

APPLICATION DIAGRAM

Figure 10 below shows a typical connection diagram for the AD5421 configured in a HART capable smart transmitter. The temperature coefficient of the on-chip current setting resistor is typically 16ppm/°C, if greater accuracy over temperature is required, an external, precision, low TC resistor may be connected (R1). To reduce power dissipation on the chip a depletion mode, mosfet (T1) such as a DN2540 or BSP129 can be connected between the loop voltage and the AD5421. In cases where a low loop voltage is used, T1 does not need to be inserted and the loop voltage can connect directly to REG_{IN}. All of the interface signal lines are shown connected to the microcontroller, to reduce the number of interface signal lines, the $\overline{LDAC}$ signal may be connected to COM and the SDO and FAULT lines may be left unconnected, this will however disable the use of the fault alert features.

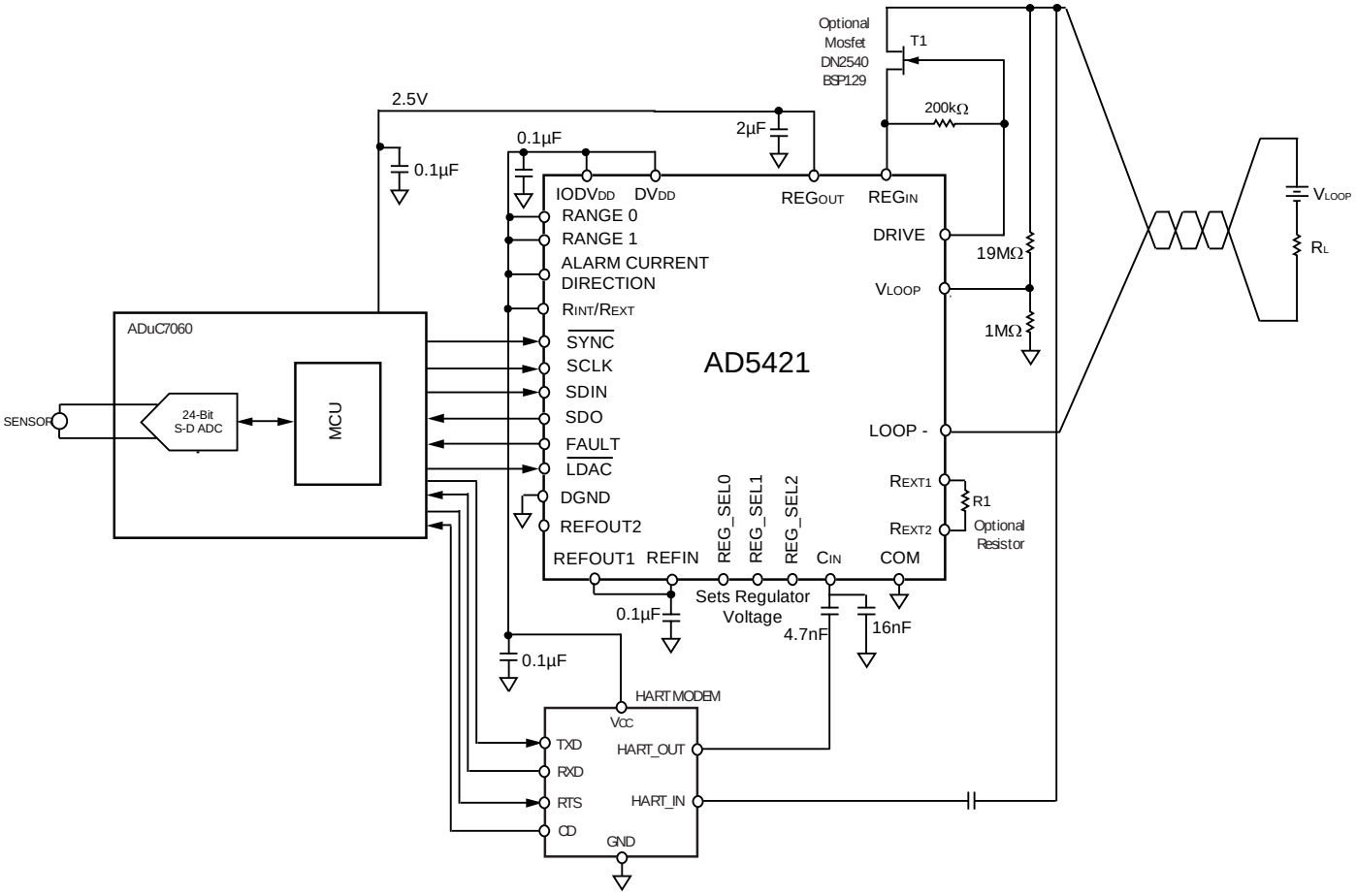


Figure 10. AD5421 Application Diagram

THERMAL AND SUPPLY CONSIDERATIONS

The AD5421 is designed to operate at a maximum junction temperature of 125°C. It is important that the device is not operated under conditions that causes the junction temperature to exceed this value, this ensures reliable and specified operation over the lifetime of the product. Excessive junction temperature can occur if the AD5421 experiences elevated voltages across its terminals while regulating the loop current at a high value. The resulting junction temperature will depend on the ambient temperature. Table 22 outlines the bounds of operation at maximum ambient temperature and maximum supply voltage. This information is displayed graphically in Figure 11 and Figure 12. These graphs assume that the exposed paddle is connected to a copper plane of approx. 6cm^2

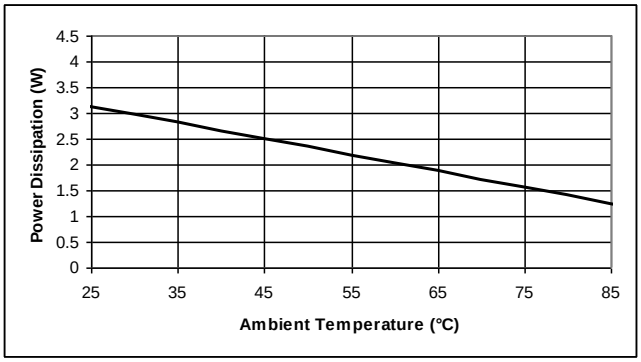


Figure 11. Maximum Power Dissipation vs. Ambient temperature

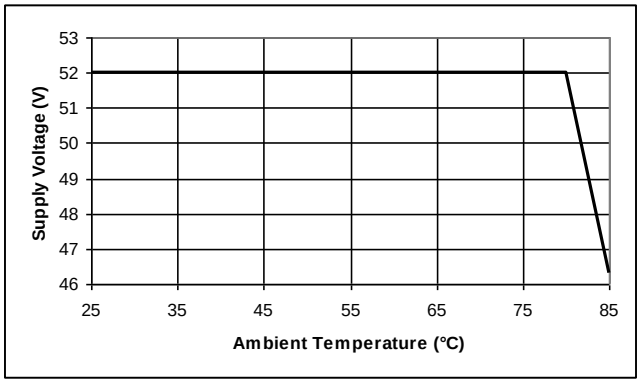
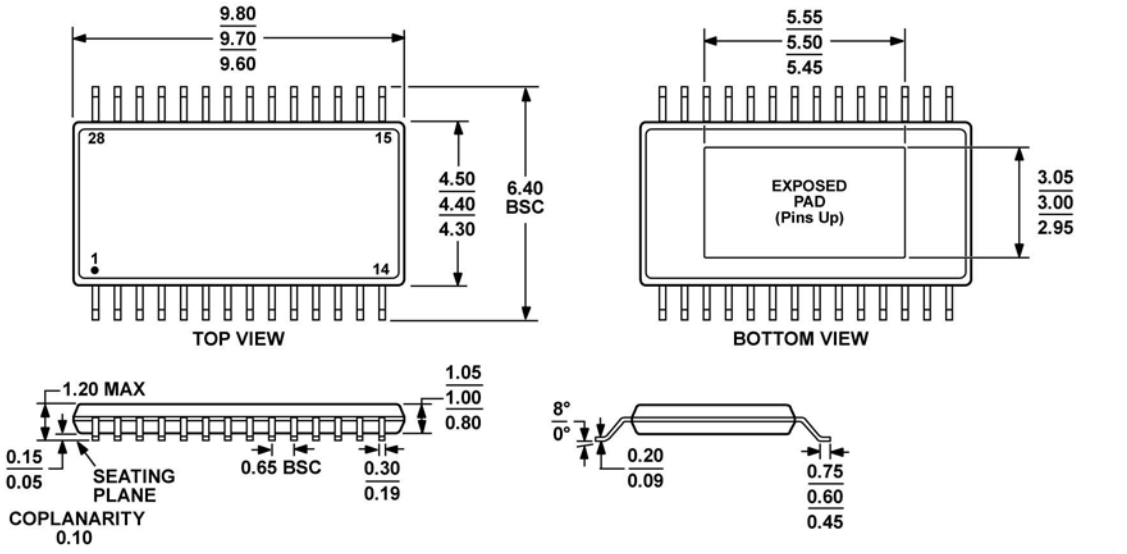


Figure 12. Maximum Supply Voltage vs. Ambient Temperature

Table 22. Thermal and Supply Considerations (External Mosfet not connected)

Parameter	Description	28-Lead TSSOP Package
Maximum Power Dissipation	Maximum permitted power dissipation when operating at an ambient temperature of 105°C	$\frac{T_J\ max - T_A}{\theta_{JA}} = \frac{125-105}{32} = 625\ \text{mW}$
Maximum Ambient Temperature	Maximum permitted ambient temperature when operating from a supply of 52V, while regulating a loop current of 22.8mA.	$T_J\ max - P_D \times \theta_{JA} =$ $125 - (52 \times 0.0228) \times 32 =$ 87°C
Maximum Supply Voltage	Maximum permitted supply voltage when operating at an ambient temperature of 105°C, while regulating a loop current of 22.8mA	$\frac{T_J max - T_A}{I_{LOOP} \times \theta_{JA}} = \frac{125-105}{0.0228 \times 32} = 27\ \text{V}$

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AET

Figure 13. 28-Lead Thin Shrink Small Outline Package, Exposed Pad [TSSOP_EP]
(RE-28-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	TUE	Temperature Range	Package Description	Package Option
AD5421BREZ	0.05%	-40°C to +105°C	28-Lead TSSOP_EP	RE-28-2
AD5421AREZ	0.15%	-40°C to +105°C	28-Lead TSSOP_EP	RE-28-2

PR09128-0-8/10(PrN)