Rev 0; 4/05

Triple NV Low Step Size Variable Resistor Plus Memory

DS3906

General Description

The DS3906 is intended for low resistance, small step-size applications. It contains three nonvolatile (NV), low-temperature coefficient, variable digital resistors that are capable of ohm and subohm increments when used in parallel with a fixed external resistor. All three of the DS3906's resistors have 64 positions (plus a high-Z state) with a pseudo-log response cleverly chosen to have a linear equivalent resistance when paired with an external resistor (see graphs below). The DS3906 also contains 16 bytes of user EEPROM that, in addition to the resistors, are controlled through an I²C™-compatible serial interface. Three address pins allow up to eight DS3906s to be placed on the same I²C bus.

The DS3906 can also be factory cutomized to provide a variety of transfer functions depending on user requirements. Contact mixedsignal.apps@dalsemi.com for additional information.

Applications

Low Ohm, Fine Resolution Driver Control for LED Display Panels

Low Ohm, Fine Resolution Instrumentation Control

Typical Operating Circuit appears at end of data sheet.

Features

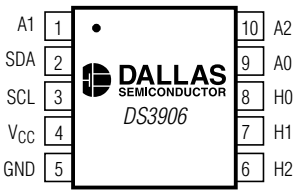
- **Three Programmable Resistors for Low Step-Size Applications (Ohm and Subohm)**
- **Resistor Settings are NV**
- **16-Byte NV User Memory (EEPROM)**
- **I²C-Compatible Serial Interface**
- **Up to 8 Devices Can be Multidropped on the Same I²C Bus**
- **Low Power Consumption**
- **Wide Operating Voltage (2.7V to 5.5V)**
- **Operating Temperature Range: -40°C to +85°C**

Ordering Information

PART	TEMP RANGE	PACKAGE
DS3906U	-40°C to +85°C	10-Pin µSOP
DS3906U+	-40°C to +85°C	10-Pin µSOP

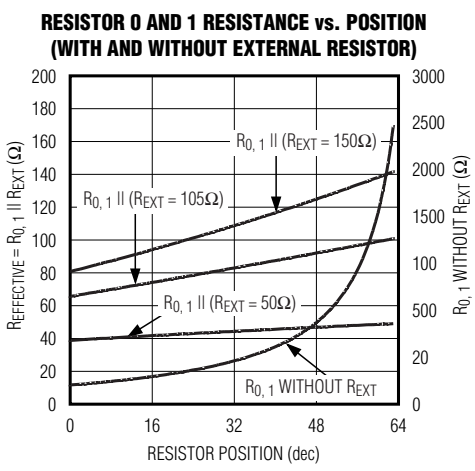
+Denotes lead-free package.
Add "/T&R" for Tape-and-Reel orders

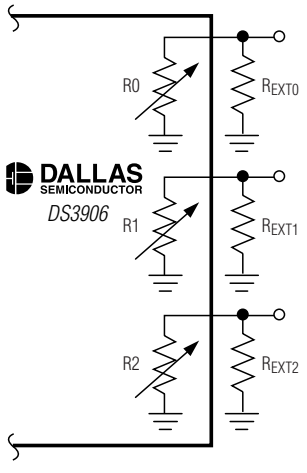
Pin Configuration

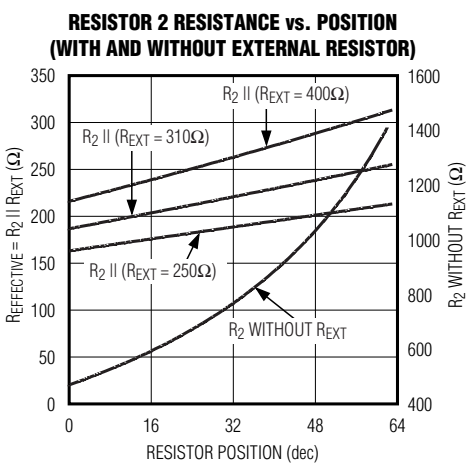


10-PIN µSOP

Resistor Plots







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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Triple NV Low Step Size Variable Resistor Plus Memory

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC}, SDA, SCL, and H0-H2 Pins
Relative to Ground.....-0.5V to +6.0V
Voltage on A0, A1, and A2
Relative to Ground .....-0.5V to V_{CC} + 0.5V, not to exceed +6.0V
Resistor Current 5mA

Operating Temperature Range .....-40°C to +85°C
EEPROM Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....See J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.7		+5.5	V
Input Logic 1	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		-0.3		0.3 x V_{CC}	V
Resistor Inputs	H0, H1, H2	V_{CC} = 2.7V to 5.5V	-0.3		+5.5	V
Resistor Current	I_R				5	mA

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current (Note 2)	I_{STBY}	3V		130		µA
		5V		160	250	
Input Leakage for All Pins	I_L	(Note 3)	-1.0		+1.0	µA
Low-Level Output Voltage (SDA)	$V_{OL\ SDA}$	3mA sink current	0		0.4	V
		6mA sink current	0		0.6	
I/O Capacitance	$C_{I/O}$				10	pF

ANALOG RESISTOR CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resistor Tolerance		From nominal values in Table 3	-20		+20	%
INL		(Note 4)	-2		+2	LSB
DNL		(Note 4)	-0.5		+0.5	LSB
Temperature Coefficient		At position 3Fh (Note 8)		60		ppm/°C
Resistor High-Z	R_{HIGH-Z}		5.5			MΩ
Resistors		Guaranteed monotonic by design				

AC ELECTRICAL CHARACTERISTICS (See Figure 2)

(V_{CC} = +2.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 5)	0		400	kHz
Bus Free Time Between Stop and Start Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) Start Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Set-up Time	$t_{SU:DAT}$		100			ns
Start Set-up time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 6)	$20 + 0.1C_B$		300	ns
SDA and SCL Fall Time	t_F	(Note 6)	$20 + 0.1C_B$		300	ns
Stop Set-up Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 6)			400	pF
EEPROM Write Time	t_{WR}	(Note 7)			20	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Writes		0°C to +70°C. The room temperature specification is at least 4x better than specification over 0°C to +70°C.	50,000			

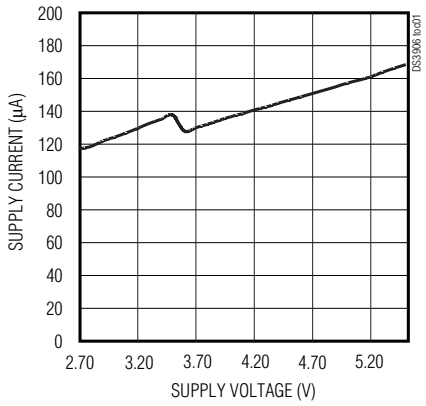
Note 1: All voltages referenced to ground.
Note 2: I_{STBY} is specified with SDA = SCL = V_{CC}, resistor pins floating, and inputs tied to V_{CC} or GND.
Note 3: The DS3906 will not obstruct the SDA and SCL lines if V_{CC} is switched off as long as the voltages applied to these input do not violate their minimum and maximum input voltage levels.
Note 4: Tested with external resistor of 87Ω for R_0 and R_1 and 258Ω for R_2 at 25°C.
Note 5: Timing shown is for fast mode (400kHz) operation. This device is also backward compatible with I^2C standard mode timing.
Note 6: C_B—total capacitance of one bus line in picofarads.
Note 7: The EEPROM write time begins after a stop condition occurs.
Note 8: Guaranteed by design.

Triple NV Low Step Size Variable Resistor Plus Memory

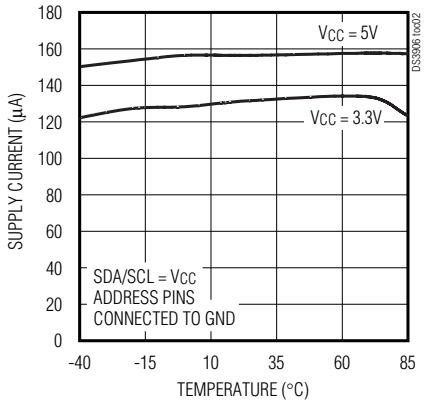
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

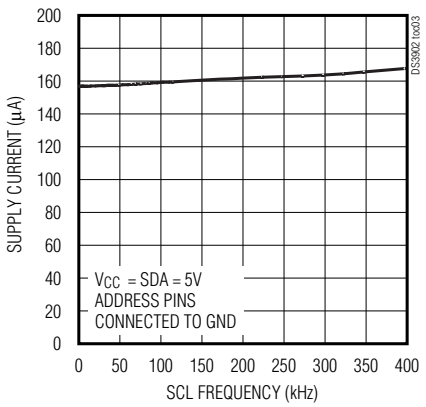
SUPPLY CURRENT vs. SUPPLY VOLTAGE



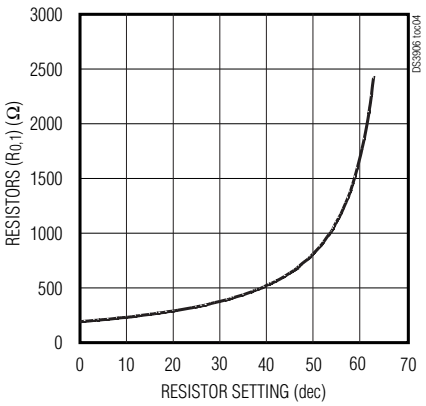
SUPPLY CURRENT vs. TEMPERATURE



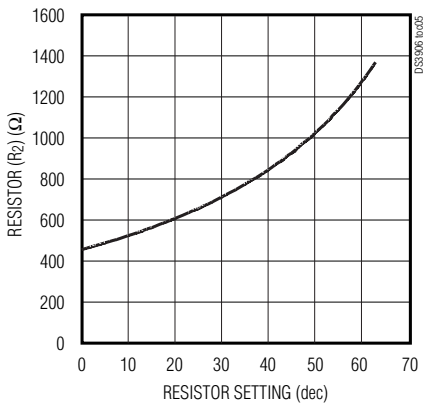
SUPPLY CURRENT vs. SCL FREQUENCY



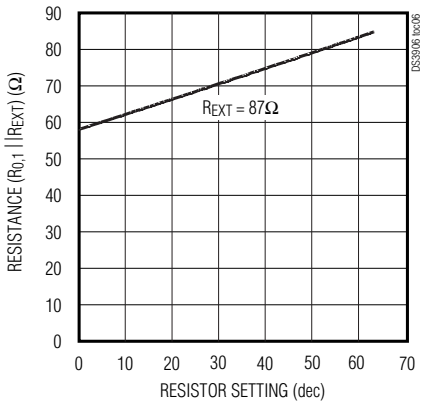
RESISTORS ($R_{0,1}$) vs. RESISTOR SETTING



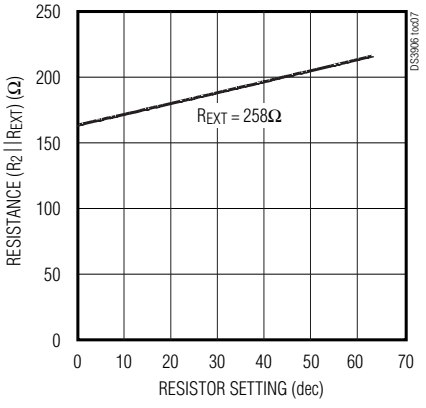
RESISTOR R_2 vs. RESISTOR SETTING



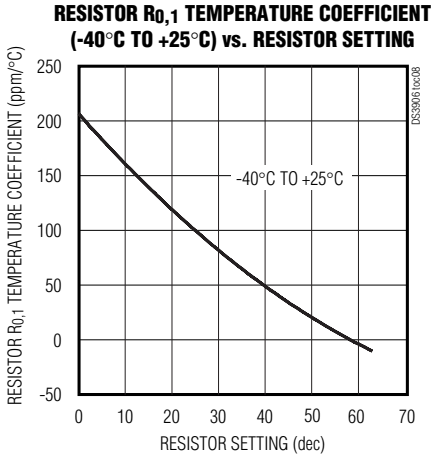
RESISTANCE ($R_{0,1}$ ||R_{EXT}) vs. RESISTOR SETTING



RESISTANCE (R_2 ||R_{EXT}) vs. RESISTOR SETTING



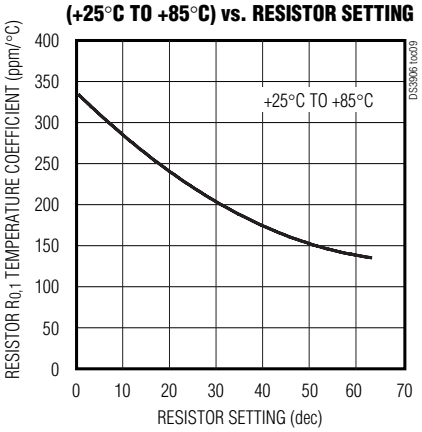
RESISTOR $R_{0,1}$ TEMPERATURE COEFFICIENT (-40°C TO +25°C) vs. RESISTOR SETTING



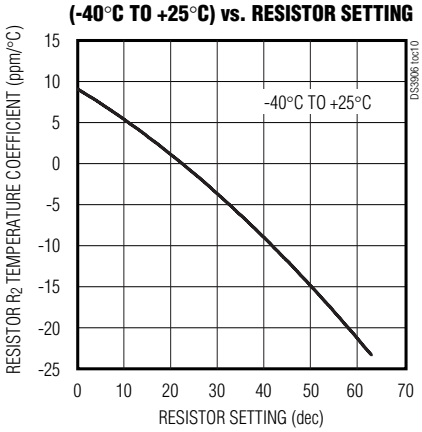
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

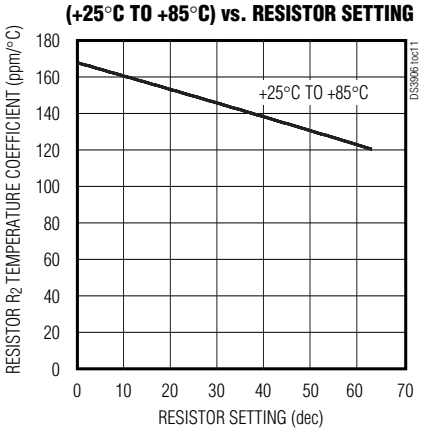
RESISTOR $R_{0,1}$ TEMPERATURE COEFFICIENT (+25°C TO +85°C) vs. RESISTOR SETTING



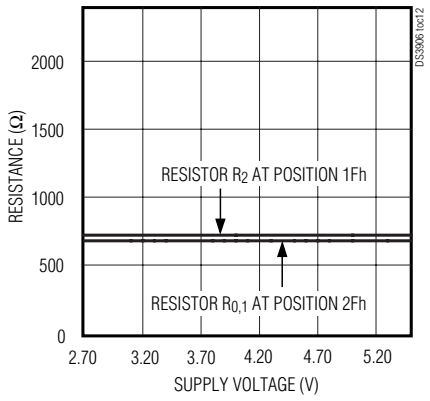
RESISTOR R_2 TEMPERATURE COEFFICIENT (-40°C TO +25°C) vs. RESISTOR SETTING



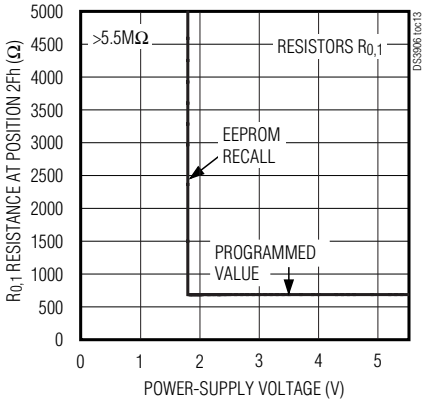
RESISTOR R_2 TEMPERATURE COEFFICIENT (+25°C TO +85°C) vs. RESISTOR SETTING



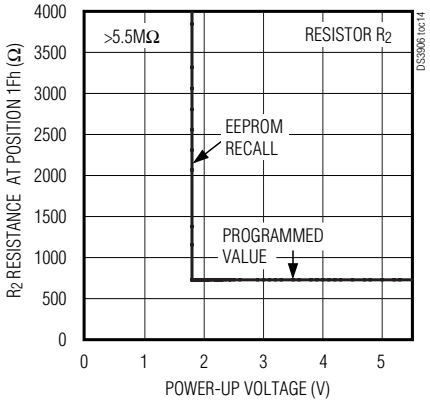
RESISTANCE vs. SUPPLY VOLTAGE



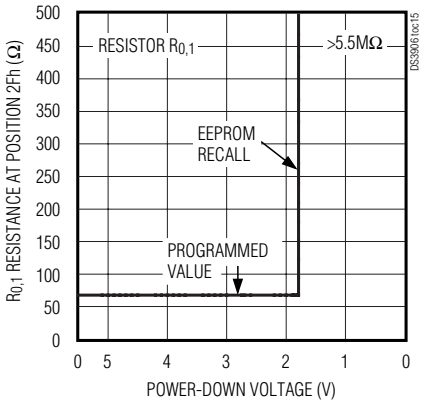
$R_{0,1}$ RESISTANCE AT POSITION 2Fh vs. POWER-UP VOLTAGE



R_2 RESISTANCE AT POSITION 1Fh vs. POWER-UP VOLTAGE



$R_{0,1}$ RESISTANCE AT POSITION 2Fh vs. POWER-UP VOLTAGE

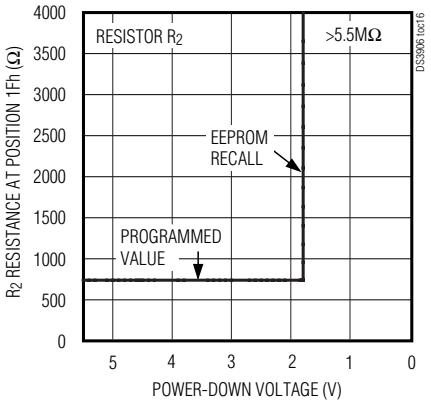


Triple NV Low Step Size Variable Resistor Plus Memory

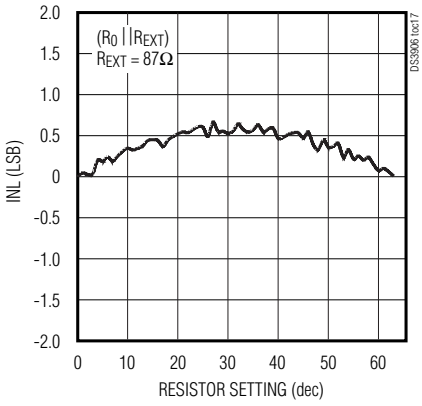
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

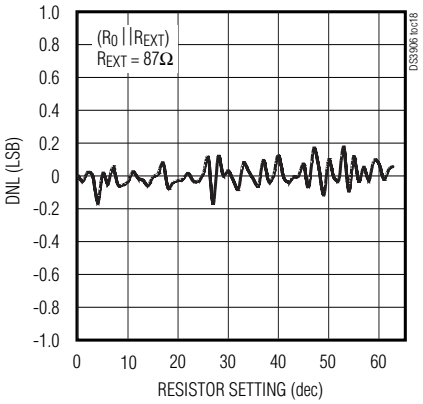
R_2 RESISTANCE AT POSITION 1Fh vs. POWER-UP VOLTAGE



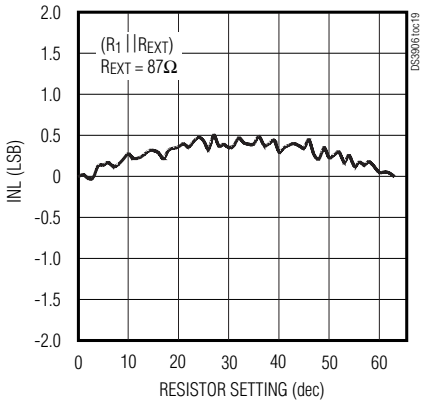
INL vs. RESISTOR SETTING FOR (R_0 ||R_{EXT})



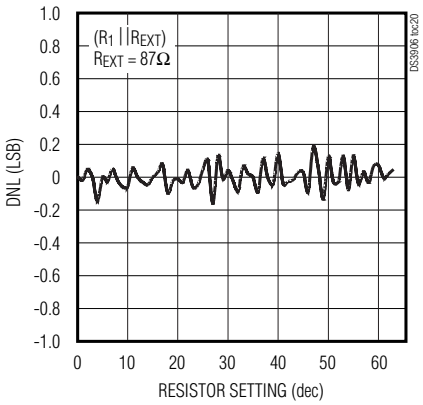
DNL vs. RESISTOR SETTING FOR (R_0 ||R_{EXT})



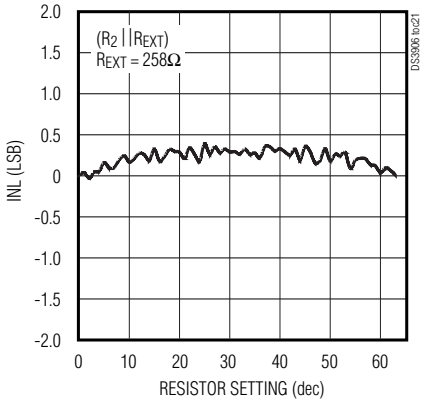
INL vs. RESISTOR SETTING FOR (R_1 ||R_{EXT})



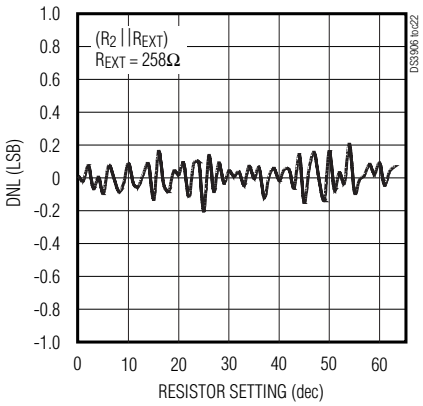
DNL vs. RESISTOR SETTING FOR (R_1 ||R_{EXT})



INL vs. RESISTOR SETTING FOR (R_2 ||R_{EXT})



DNL vs. RESISTOR SETTING FOR (R_2 ||R_{EXT})

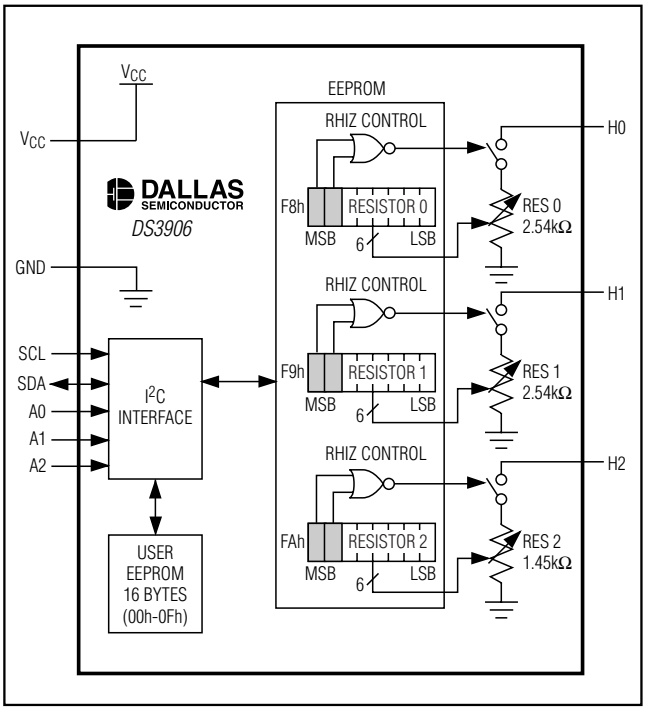


Triple NV Low Step Size Variable Resistor Plus Memory

Pin Description

PIN	NAME	FUNCTION
1	A1	I^2C Address Input. Inputs A0, A1, and A2 determine the I^2C slave address of the device.
2	SDA	I^2C Serial Data Open-Drain Input/Output
3	SCL	I^2C Serial Clock Input
4	V_{CC}	Power Supply Voltage
5	GND	Ground
6	H2	High Terminal of Resistor 2
7	H1	High Terminal of Resistor 1
8	H0	High Terminal of Resistor 0
9	A0	I^2C Address Input. Inputs A0, A1, and A2 determine the I^2C slave address of the device.
10	A2	

Block Diagram



Detailed Description

The DS3906 contains three variable resistors plus a user EEPROM. The block diagram illustrates these in addition to the registers that control the resistors. The following sections provide detailed information about the DS3906.

Memory Organization

The DS3906 contains 16 bytes of User EEPROM plus 3 NV resistor registers. Refer to Table 1. Communication with the memory/registers is achieved through the I^2C-compatible serial interface and is described in subsequent sections.

Resistor Registers/Settings

Each of the three resistors in the DS3906 has its own control register used to set the resistor position. Refer to the block diagram and Table 2. Each resistor has 64 positions plus a high impedance state. The nominal resistance values for each position is listed in Table 3. Resistors 0 and 1 have the same full-scale resistance, which is different than resistor 2. As shown in Table 3, the resistors have a pseudo-log response (resistance vs. position) when used without an external parallel resistor. Valid resistor settings are 00h to 3Fh. Writing a value greater than 3Fh to any of the resistor registers

makes the corresponding resistor go High-Z. Plots for both resistor sizes are shown on the front page of this data sheet. It can be seen that, when an external resistor is connected in parallel with the DS3906's resistors, the effective resistance is linear and capable of achieving sub-ohm and ohm steps.

The resistor settings are stored in EEPROM memory. It is important to point out that the DS3906 EEPROM is organized in 2-byte pages. This is transparent when reading from the device or when performing single byte writes. However, this limits the maximum number of bytes that can be written in one I^2C transaction to two. Furthermore, the multiple byte writes must begin on even memory addresses (00h, 02h, ..., F8h, etc). Additional information is provided later in the *I^2C Communication* section . Example communication transactions are provided in Figure 3.

Table 1. DS3906 Memory Map

ADDRESS	TYPE	NAME	FUNCTION	FACTORY DEFAULT
00h to 0Fh	EEPROM	User memory	16 bytes of general-purpose user EEPROM.	00h
F8h	EEPROM	Resistor 0	Resistor 0-2 settings. See Table 2 and the *Resistor Registers/Settings* section.	3Fh
F9h	EEPROM	Resistor 1		3Fh
FAh	EEPROM	Resistor 2		3Fh
FBh-FFh	Reserved			

Table 2. DS3906 Resistor Registers

ADDRESS	VARIABLE RESISTOR	POSITION 3FH RESISTANCE (kΩ)	NUMBER OF POSITIONS*
F8h	Resistor 0	2.54	64 (00h to 3Fh) + High-Z
F9h	Resistor 1	2.54	
FAh	Resistor 2	1.45	

** Writing a value greater than 3Fh to any of the resistor registers makes the corresponding resistor go High-Z. Position 3Fh is the maximum position.*

Table 3. DS3906 Resistor Settings (without external resistor)

POSITION		NOMINAL RESISTOR VALUES WITHOUT EXT RESISTOR (25°C)	
Dec	Hex	Resistors 0, 1	Resistor 2
0	00	175.0	469.7
1	01	178.8	476.4
2	02	182.7	483.2
3	03	186.8	490.1
4	04	190.9	497.2
5	05	195.2	504.4
6	06	199.6	511.7
7	07	204.2	519.2
8	08	208.9	526.8
9	09	213.7	534.6
10	0A	218.8	542.5
11	0B	223.9	550.6
12	0C	229.3	558.8
13	0D	234.9	567.3
14	0E	240.6	575.9
15	0F	246.6	584.6
16	10	252.8	593.6
17	11	259.2	602.8
18	12	265.9	612.1
19	13	272.8	621.7
20	14	280.0	631.5
21	15	287.5	641.5
22	16	295.3	651.7
23	17	303.5	662.2
24	18	312.0	672.9
25	19	320.8	683.8
26	1A	330.1	695.0
27	1B	339.8	706.5
28	1C	350.0	718.3
29	1D	360.7	730.3
30	1E	371.9	742.7
31	1F	383.7	755.4

POSITION		NOMINAL RESISTOR VALUES WITHOUT EXT RESISTOR (25°C)	
Dec	Hex	Resistors 0, 1	Resistor 2
32	20	396.1	768.4
33	21	409.1	781.7
34	22	422.9	795.4
35	23	437.5	809.4
36	24	452.9	823.9
37	25	469.3	838.7
38	26	486.7	853.9
39	27	505.2	869.6
40	28	525.0	885.7
41	29	546.1	902.3
42	2A	568.8	919.4
43	2B	593.1	936.9
44	2C	619.2	955.1
45	2D	647.5	973.7
46	2E	678.1	993.0
47	2F	711.4	1012.8
48	30	747.7	1033.3
49	31	787.5	1054.5
50	32	831.3	1076.4
51	33	879.6	1099.0
52	34	933.3	1122.4
53	35	993.4	1146.6
54	36	1060.9	1171.7
55	37	1137.5	1197.7
56	38	1225.0	1224.7
57	39	1326.0	1252.7
58	3A	1443.8	1281.7
59	3B	1583.0	1311.9
60	3C	1750.0	1343.3
61	3D	1954.2	1376.0
62	3E	2209.4	1410.1
63	3F	2537.5	1445.6

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External Resistor Selection/Considerations

Using an external resistor in parallel with any of the DS3906's resistors makes the effective resistance linear with small increments from position to position. Typical values for the external resistors are 87Ω for Resistor 0 and 1 and 258Ω for Resistor 2. The effective resistance will be the most linear when these values are used. Of course these values may be tweaked to achieve the desired step size and range. The effects of changing R_{EXT} is shown on the front page. Likewise, a series resistor may be used to further customize the desired response. If the DS3906's transfer function does not meet the applications needs, contact the factory at the email address provided on the front page to inquire about custom resistance values.

I²C Slave Address and Address Pins

The DS3906's I²C slave address is determined by the state of the A0, A1, and A2 address pins as shown in Figure 1. Address pins tied to GND result in a '0' in the corresponding bit position in the slave address. Conversely, address pins tied to V_{CC} result in a '1' in the corresponding bit positions. I²C communication is described in detail in the following section.

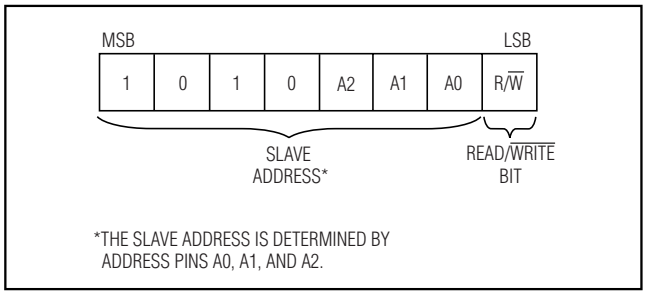

Figure 1. DS3906 Slave Address Byte

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses, start and stop conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between stop and start conditions when both SDA and SCL are inactive and in their logic high states. When the bus is idle it often initiates a low power mode for slave devices.

Start Condition: A start condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a start condition. See the timing diagram for applicable timing.

Stop Condition: A stop condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a stop condition. See the timing diagram for applicable timing.

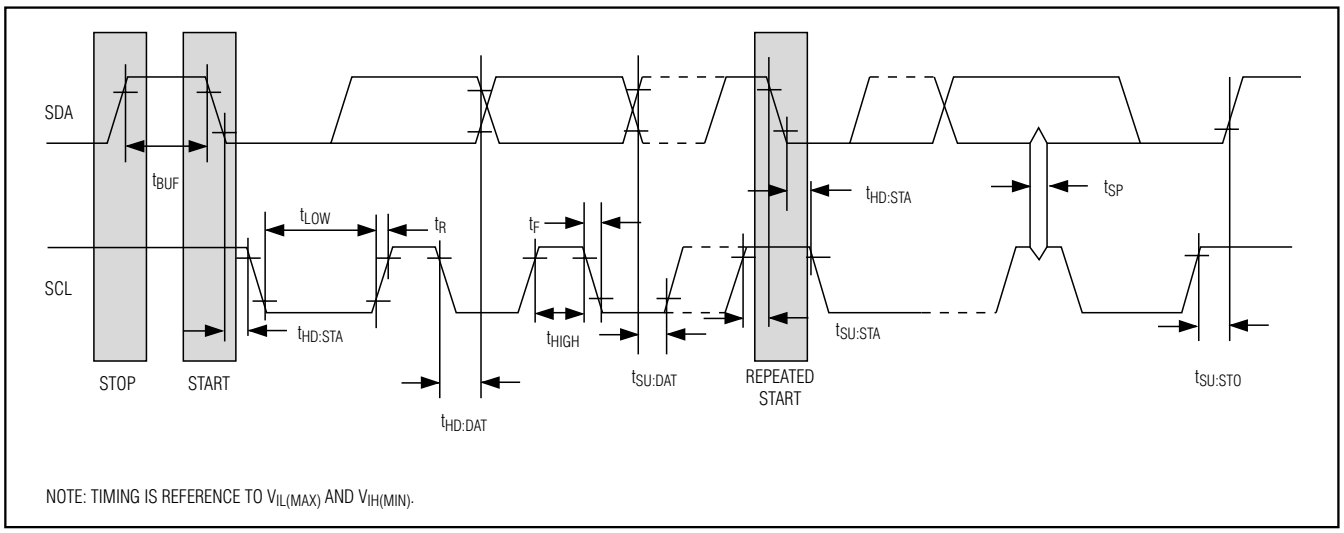

Figure 2. I²C Timing Diagram

Repeated Start Condition: The master can use a repeated start condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated start condition is issued identically to a normal start condition, See the timing diagram for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (see Figure 2). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end a write operation, the master must release the SDA bus line for the proper amount of setup time (see Figure 2) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 2) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminated communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a start condition. The slave address byte contains the slave address in the most significant 7-bits and the R/$\overline{W}$ bit in the least significant bit.

The DS3906's slave address is determined by the state of the A0, A1, and A2 address pins as shown in Figure 1. Address pins tied to GND result in a '0' in the corresponding bit position in the slave address. Conversely, address pins tied to V_{CC} result in a '1' in the corresponding bit positions.

When the R/$\overline{W}$ bit is 0 (such as in A0h), the master is indicating it writes data to the slave. If R/$\overline{W}$ = 1, (A1h in this case), the master is indicating it wants to read from the slave.

If an incorrect slave address is written, the DS3906 assumes the master is communicating with another I²C device and ignore the communication until the next start condition is sent.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a Single Byte to a Slave: The master must generate a start condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data and generate a stop condition. Remember the master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: The DS3906 is capable of writing up to 2 bytes (1-page or row) in a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 2-byte page. Pages begin on even addresses (00h, 02h, 04h, etc). Attempts to write more than 2 bytes of memory without at once without sending a stop condition between pages results in the address counter wrapping around to the beginning of the present row.

To write multiple bytes to a slave in one transaction, the master generates a start condition, writes the slave address byte (R/$\overline{W}$ =0), writes the memory address (must be even), writes two data bytes, and generates a stop condition. Remember the master must read the slave's acknowledgement during all byte write operations.

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Acknowledge Polling: Any time an EEPROM page is written, the DS3906 requires the EEPROM write time (t_W) after the stop condition to write the contents of the page to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS3906, which allows communication to continue as soon as the DS3906 is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

EEPROM Write Cycles: When EEPROM writes occur, the DS3906 internally writes the whole EEPROM page (2-bytes) even if only a single byte write was performed. Writes that do not modify all 2 bytes on the page are valid and do not corrupt any of other bytes on the same page. Because the whole page is written, even bytes on the page that were not modified during the transaction are still subject to a write cycle. The DS3906's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature. It is capable of handling many additional writes at room temperature.

Reading a Single Byte from a Slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a start condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a stop condition. However, since requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a start condition, writes the slave address byte (R/$\overline{W}$ =0), writes the memory address where it desires to read, generates a repeated start condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a stop condition.

See Figure 3 for a read example using the repeated start condition to specify the starting memory location.

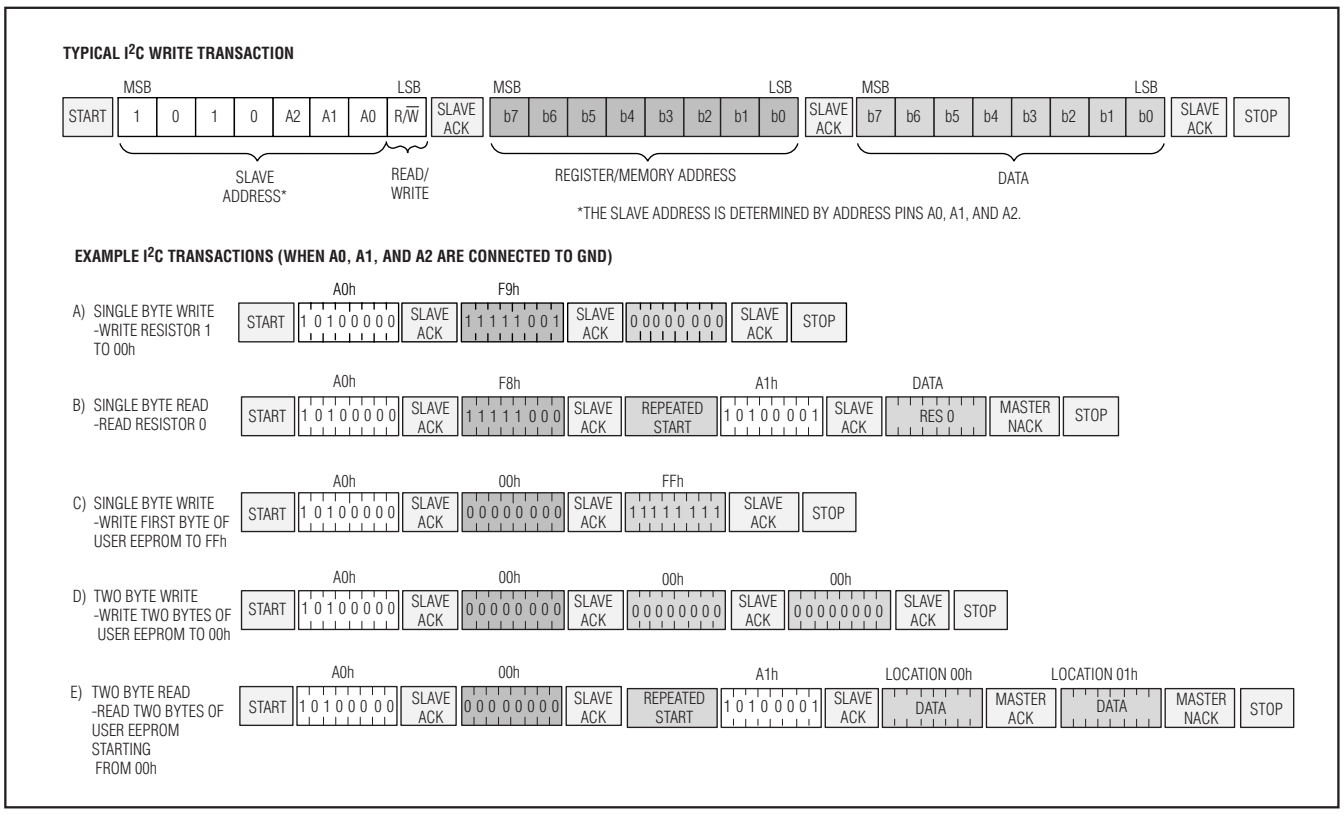


Figure 3. I²C Communication Examples

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and generates a stop condition.

Application Information

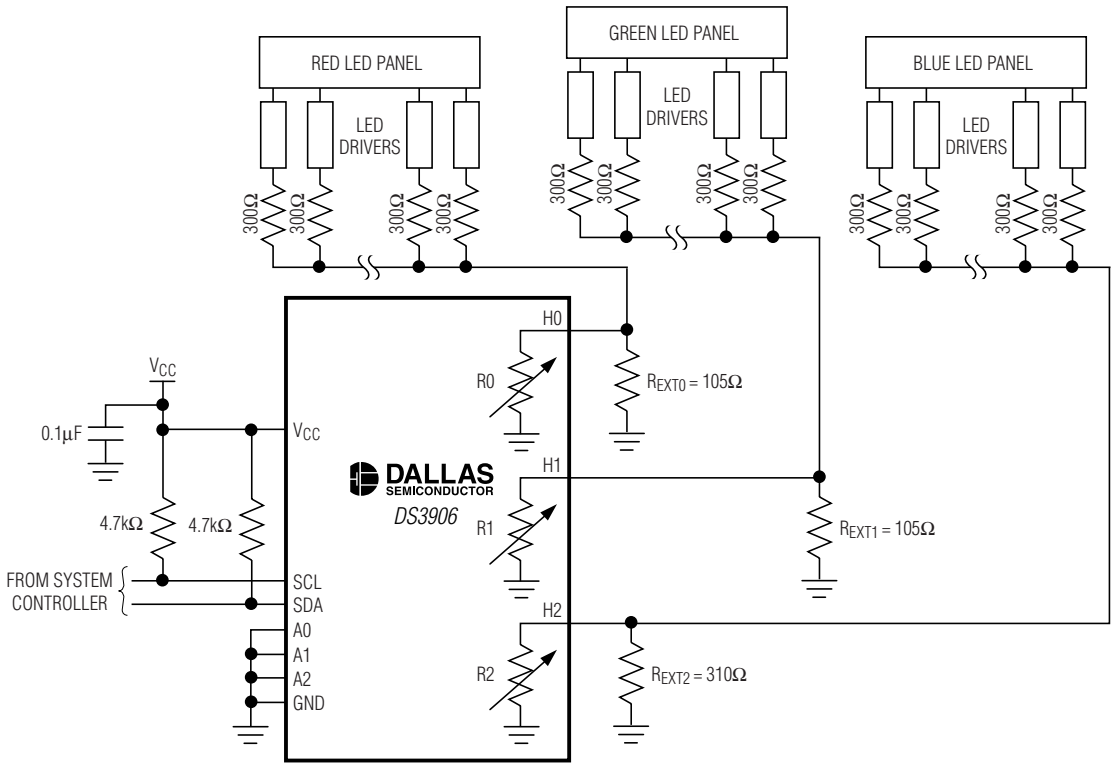
Power Supply Decoupling

To achieve best results, it is highly recommended that a decoupling capacitor is used on the I.C. power supply pins. Typical values of decoupling capacitors are 0.01µF and 0.1µF. Use a high-quality, ceramic, surface-mount capacitor, and mount it as close as possible to the V_{CC} and GND pins of the I.C. to minimize lead inductance.

High Resistor Terminal Voltage

It is permissible to have a voltage on the resistor-high terminals that is higher than the voltage connected to V_{CC}. For instance, connecting V_{CC} to 3.0V while one or more of the resistor high terminals are connected to 5.0V allows a 3V system to control a 5V system. The 5.5V maximum still applies to the limit on the resistor high terminals regardless of the voltage present on V_{CC}.

Typical Operating Circuit



DESIGN NOTES:
1. IN THIS APPLICATION A NUMBER OF LED DRIVERS ARE SET USING THE DS3906'S VARIABLE RESISTORS.
2. THE PARALLEL COMBINATION OF THE DS3906 VARIABLE RESISTOR R0 AND 105Ω (R_{EXT0}) IS EQUIVALENT TO A VARIABLE RESISTOR WITH LINEAR STEP INCREMENTS OF 0.6Ω RANGING FROM 66Ω TO 101Ω. THE SAME APPLIES FOR RESISTOR 1 (R1). THE PARALLEL COMBINATION OF R2 AND 310Ω (R_{EXT2}) IS EQUIVALENT TO A VARIABLE RESISTOR WITH LINEAR STEP INCREMENTS OF 1Ω RANGING FROM 187Ω TO 255Ω.
3. VALUES LARGER THAN THE SHOWN EXTERNAL RESISTORS (R_{EXT0}, R_{EXT1}, AND R_{EXT2}) RESULT IN LARGER STEP INCREMENTS AND RESISTOR VALUES LOWER THAN THE SHOWN VALUES RESULT IN SMALLER STEP INCREMENTS. REFER TO THE RESISTOR TABLES AND COMPUTE EQUIVALENT RESISTANCE TO FIND OUT THE RANGES.

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Chip Topology

TRANSISTOR COUNT: 16,200

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.