

**Digitally Controlled Potentiometer (XDCP™)**

**FEATURES**

- **Solid-state potentiometer**
- **3-wire serial interface**
- **100 wiper tap points**
  - Wiper position stored in nonvolatile memory and recalled on power-up
- **99 resistive elements**
  - Temperature compensated
  - End to end resistance,  $\pm 20\%$
  - Terminal voltages,  $\pm 5V$
- **Low power CMOS**
  - $V_{CC} = 5V$
  - Active current, 3mA max.
  - Standby current, 750 $\mu A$  max.
- **High reliability**
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- **X9C102 = 1k $\Omega$**
- **X9C103 = 10k $\Omega$**
- **X9C503 = 50k $\Omega$**
- **X9C104 = 100k $\Omega$**
- **Packages**
  - 8 Ld SOIC and 8 Ld PDIP
- **Pb-free plus anneal available (RoHS compliant)**

**DESCRIPTION**

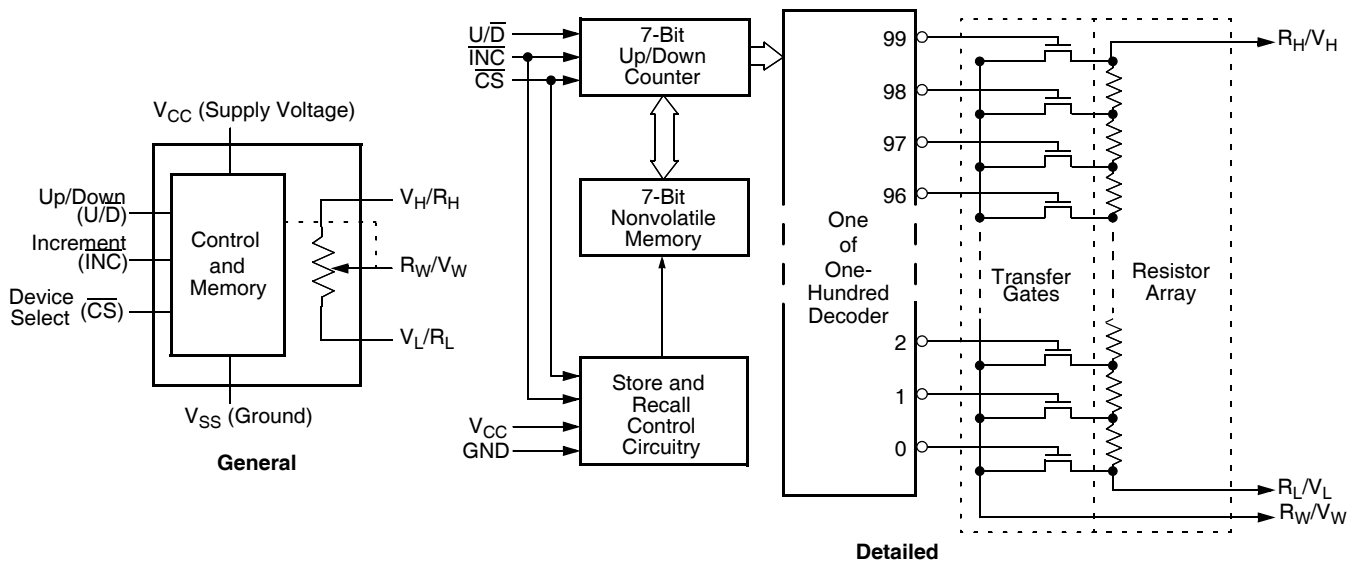
The X9Cxxx are Intersil digitally controlled (XDCP) potentiometers. The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a three-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the  $\overline{CS}$ ,  $\overline{U/D}$ , and  $\overline{INC}$  inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

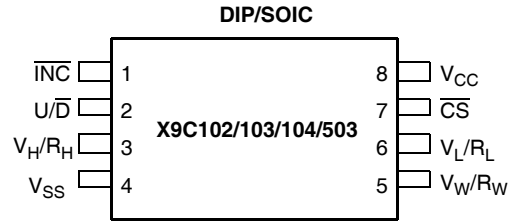
- control
- parameter adjustments
- signal processing

**BLOCK DIAGRAM**



# X9C102, X9C103, X9C104, X9C503

## PIN CONFIGURATION



## ORDERING INFORMATION

| PART NUMBER           | PART MARKING | R <sub>TOTAL</sub><br>(kΩ) | TEMPERATURE RANGE<br>(°C) | PACKAGE             | PKG. DWG. # |
|-----------------------|--------------|----------------------------|---------------------------|---------------------|-------------|
| X9C102P               | X9C102P      | 1                          | 0 to 70                   | 8 Ld PDIP           | MDP0031     |
| X9C102PZ (Note)       | X9C102P Z    |                            | 0 to 70                   | 8 Ld PDIP (Pb-free) | MDP0031     |
| X9C102PI              | X9C102P I    |                            | -40 to 85                 | 8 Ld PDIP           | MDP0031     |
| X9C102PIZ (Note)      | X9C102P ZI   |                            | -40 to 85                 | 8 Ld PDIP (Pb-free) | MDP0031     |
| X9C102S*, **          | X9C102S      |                            | 0 to 70                   | 8 Ld SOIC           | MDP0027     |
| X9C102SZ* (Note)      | X9C102S Z    |                            | 0 to 70                   | 8 Ld SOIC (Pb-free) | MDP0027     |
| X9C102SI*, **         | X9C102S I    |                            | -40 to 85                 | 8 Ld SOIC           | MDP0027     |
| X9C102SIZ*, ** (Note) | X9C102S ZI   |                            | -40 to 85                 | 8 Ld SOIC (Pb-free) | MDP0027     |
| X9C103P               | X9C103P      | 10                         | 0 to 70                   | 8 Ld PDIP           | MDP0031     |
| X9C103PZ (Note)       | X9C103P Z    |                            | 0 to 70                   | 8 Ld PDIP (Pb-free) | MDP0031     |
| X9C103PI              | X9C103P I    |                            | -40 to 85                 | 8 Ld PDIP           | MDP0031     |
| X9C103PIZ (Note)      | X9C103P ZI   |                            | -40 to 85                 | 8 Ld PDIP (Pb-free) | MDP0031     |
| X9C103S*, **          | X9C103S      |                            | 0 to 70                   | 8 Ld SOIC           | MDP0027     |
| X9C103SZ*, ** (Note)  | X9C103S Z    |                            | 0 to 70                   | 8 Ld SOIC (Pb-free) | MDP0027     |
| X9C103SI*, **         | X9C103S I    |                            | -40 to 85                 | 8 Ld SOIC           | MDP0027     |
| X9C103SIZ*, ** (Note) | X9C103S ZI   |                            | -40 to 85                 | 8 Ld SOIC (Pb-free) | MDP0027     |
| X9C503P               | X9C503P      | 50                         | 0 to 70                   | 8 Ld PDIP           | MDP0031     |
| X9C503PZ (Note)       | X9C503P Z    |                            | 0 to 70                   | 8 Ld PDIP (Pb-free) | MDP0031     |
| X9C503PI              | X9C503P I    |                            | -40 to 85                 | 8 Ld PDIP           | MDP0031     |
| X9C503PIZ (Note)      | X9C503P ZI   |                            | -40 to 85                 | 8 Ld PDIP (Pb-free) | MDP0031     |
| X9C503S*              | X9C503S      |                            | 0 to 70                   | 8 Ld SOIC           | MDP0027     |
| X9C503SZ* (Note)      | X9C503S Z    |                            | 0 to 70                   | 8 Ld SOIC (Pb-free) | MDP0027     |
| X9C503SI*, **         | X9C503S I    |                            | -40 to 85                 | 8 Ld SOIC           | MDP0027     |
| X9C503SIZ*, ** (Note) | X9C503S ZI   |                            | -40 to 85                 | 8 Ld SOIC (Pb-free) | MDP0027     |
| X9C104P               | X9C104P      | 100                        | 0 to 70                   | 8 Ld PDIP           | MDP0031     |
| X9C104PI              | X9C104P I    |                            | -40 to 85                 | 8 Ld PDIP           | MDP0031     |
| X9C104PIZ (Note)      | X9C104P ZI   |                            | -40 to 85                 | 8 Ld PDIP (Pb-free) | MDP0031     |
| X9C104S*, **          | X9C104S      |                            | 0 to 70                   | 8 Ld SOIC           | MDP0027     |
| X9C104SZ*, ** (Note)  | X9C104S Z    |                            | 0 to 70                   | 8 Ld SOIC (Pb-free) | MDP0027     |
| X9C104SI*, **         | X9C104S I    |                            | -40 to 85                 | 8 Ld SOIC           | MDP0027     |
| X9C104SIZ*, ** (Note) | X9C104S ZI   |                            | -40 to 85                 | 8 Ld SOIC (Pb-free) | MDP0027     |

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

\*Add "T1" suffix for tape and reel.

\*\*Add "T2" suffix for tape and reel.

**PIN DESCRIPTIONS**

| Pin | Symbol                                | Brief Description  |
|-----|---------------------------------------|--|
| 1   | $\overline{\text{INC}}$               | <b>Increment</b> . The $\overline{\text{INC}}$ input is negative-edge triggered. Toggling $\overline{\text{INC}}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the $\text{U}/\overline{\text{D}}$ input.   |
| 2   | $\text{U}/\overline{\text{D}}$        | <b>Up/Down</b> . The $\text{U}/\overline{\text{D}}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.  |
| 3   | $\text{R}_\text{H}/\text{V}_\text{H}$ | <b><math>\text{R}_\text{H}/\text{V}_\text{H}</math></b> . The high ( $\text{V}_\text{H}/\text{R}_\text{H}$ ) terminals of the X9C102/103/104/503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. The terminology of $\text{V}_\text{H}/\text{R}_\text{H}$ and $\text{V}_\text{L}/\text{R}_\text{L}$ references the relative position of the terminal in relation to wiper movement direction selected by the $\text{U}/\overline{\text{D}}$ input and not the voltage potential on the terminal. |
| 4   | $\text{V}_\text{SS}$                  | <b><math>\text{V}_\text{SS}</math></b>   |
| 5   | $\text{V}_\text{W}/\text{R}_\text{W}$ | <b><math>\text{V}_\text{W}/\text{R}_\text{W}</math></b> . $\text{V}_\text{W}/\text{R}_\text{W}$ is the wiper terminal, and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.   |
| 6   | $\text{R}_\text{L}/\text{V}_\text{L}$ | <b><math>\text{R}_\text{L}/\text{V}_\text{L}</math></b> . The low ( $\text{V}_\text{L}/\text{R}_\text{L}$ ) terminals of the X9C102/103/104/503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. The terminology of $\text{V}_\text{H}/\text{R}_\text{H}$ and $\text{V}_\text{L}/\text{R}_\text{L}$ references the relative position of the terminal in relation to wiper movement direction selected by the $\text{U}/\overline{\text{D}}$ input and not the voltage potential on the terminal.  |
| 7   | $\overline{\text{CS}}$                | <b><math>\overline{\text{CS}}</math></b> . The device is selected when the $\overline{\text{CS}}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{\text{CS}}$ is returned HIGH while the $\overline{\text{INC}}$ input is also HIGH. After the store operation is complete the X9C102/103/104/503 device will be placed in the low power standby mode until the device is selected once again.   |
| 8   | $\text{V}_\text{CC}$                  | <b><math>\text{V}_\text{CC}</math></b>   |

**ABSOLUTE MAXIMUM RATINGS**

Temperature under bias ..... -65°C to +135°C  
 Storage temperature ..... -65°C to +150°C  
 Voltage on  $\overline{CS}$ ,  $\overline{INC}$ ,  $U/\overline{D}$  and  $V_{CC}$   
 with respect to  $V_{SS}$  ..... -1V to +7V  
 Voltage on  $V_H/R_H$  and  $V_L/R_L$   
 referred to  $V_{SS}$  ..... -8V to +8V  
 $\Delta V = |V_H/R_H - V_L/R_L|$   
 X9C102 ..... 4V  
 X9C103, X9C503, and X9C104 ..... 10V  
 Lead temperature (soldering, 10 seconds) ..... +300°C  
 $I_W$  (10 seconds) ..... 8.8mA  
 Power rating X9C102 ..... 16mW  
 Power rating X9C103/104/503 ..... 10mW

**COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

| Temperature | Min.  | Max.  |
|-------------|-------|-------|
| Commercial  | 0°C   | +70°C |
| Industrial  | -40°C | +85°C |

| Supply Voltage ( $V_{CC}$ ) | Limits  |
|-----------------------------|---------|
| X9C102/103/104/503          | 5V ±10% |

**POTENTIOMETER CHARACTERISTICS** (Over recommended operating conditions unless otherwise stated.)

| Symbol                          | Parameter                           | Limits |                     |      | Unit              | Test Conditions/Notes                   |
|---------------------------------|-------------------------------------|--------|---------------------|------|-------------------|---|
|                                 |                                     | Min.   | Typ.                | Max. |                   |   |
| $R_{TOTAL}$                     | End to end resistance variation     | -20    |                     | +20  | %                 |   |
| $V_{VH/RH}$                     | $V_H$ terminal voltage              | -5     |                     | +5   | V                 |   |
| $V_{VL/RL}$                     | $V_L$ terminal voltage              | -5     |                     | +5   | V                 |   |
| $I_W$                           | Wiper current                       | -4.4   |                     | 4.4  | mA                |   |
| $R_W$                           | Wiper resistance                    |        | 40                  | 100  | $\Omega$          | Wiper Current = ±1mA                    |
|                                 | Noise <sup>(5)</sup>                |        | -120                |      | dBV               | Ref. 1kHz                               |
|                                 | Resolution                          |        | 1                   |      | %                 |   |
|                                 | Absolute linearity <sup>(1)</sup>   | -1     |                     | +1   | MI <sup>(3)</sup> | $V_{W(n)(actual)} - V_{W(n)(expected)}$ |
|                                 | Relative linearity <sup>(2)</sup>   | -0.2   |                     | +0.2 | MI <sup>(3)</sup> | $V_{W(n+1)(actual)} - [V_{W(n)} + MI]$  |
|                                 | RTOTAL temperature coefficient      |        | ±300 <sup>(5)</sup> |      | ppm/°C            | X9C103/503/104                          |
|                                 | RTOTAL temperature coefficient      |        | ±600 <sup>(5)</sup> |      | ppm/°C            | X9C102                                  |
|                                 | Ratiometric temperature coefficient |        | ±20                 |      | ppm/°C            |   |
| $C_H/C_L/C_W$<br><sup>(5)</sup> | Potentiometer capacitances          |        | 10/10/25            |      | pF                | See Circuit #3, Macro Model             |

- Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage =  $[V_{W(n)(actual)} - V_{W(n)(expected)}] = \pm 1$  MI Maximum.  
 (2) Relative linearity is a measure of the error in step size between taps =  $V_{W(n+1)} - [V_{W(n)} + MI] = +0.2$  MI.  
 (3) 1 MI = Minimum Increment =  $R_{TOT}/99$   
 (4) Typical values are for  $T_A = +25^\circ C$  and nominal supply voltage.  
 (5) This parameter is not 100% tested.

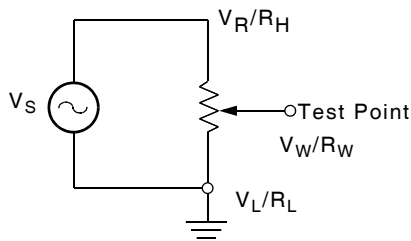
**D.C. OPERATING CHARACTERISTICS** (Over recommended operating conditions unless otherwise specified.)

| Symbol         | Parameter   | Limits |                     |          | Unit    | Test Conditions   |
|----------------|---|--------|---------------------|----------|---------|---|
|                |   | Min.   | Typ. <sup>(4)</sup> | Max.     |         |   |
| $I_{CC}$       | $V_{CC}$ active current   |        | 1                   | 3        | mA      | $\overline{CS} = V_{IL}$ , $U/\overline{D} = V_{IL}$ or $V_{IH}$ and $\overline{INC} = 0.4V$ to $2.4V$ @ max. $t_{CYC}$ |
| $I_{SB}$       | Standby supply current  |        | 200                 | 750      | $\mu A$ | $\overline{CS} = V_{CC} - 0.3V$ , $U/\overline{D}$ and $\overline{INC} = V_{SS}$ or $V_{CC} - 0.3V$                     |
| $I_{LI}$       | $\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ input leakage current |        |                     | $\pm 10$ | $\mu A$ | $V_{IN} = V_{SS}$ to $V_{CC}$   |
| $V_{IH}$       | $\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ input HIGH voltage    | 2      |                     |          | V       |   |
| $V_{IL}$       | $\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ input LOW voltage     |        |                     | 0.8      | V       |   |
| $C_{IN}^{(5)}$ | $\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ input capacitance     |        | 10                  |          | pF      | $V_{CC} = 5V$ , $V_{IN} = V_{SS}$ , $T_A = 25^\circ C$ , $f = 1MHz$   |

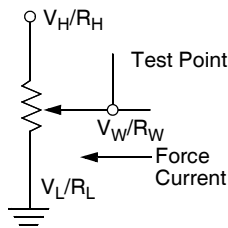
**ENDURANCE AND DATA RETENTION**

| Parameter         | Min.    | Unit                              |
|-------------------|---------|-----------------------------------|
| Minimum endurance | 100,000 | Data changes per bit per register |
| Data retention    | 100     | years                             |

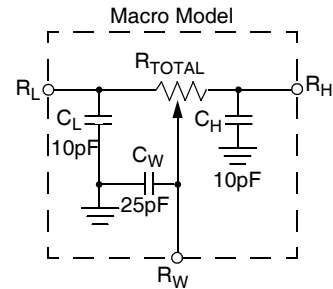
**Test Circuit #1**



**Test Circuit #2**



**Test Circuit #3**



**A.C. CONDITIONS OF TEST**

|                           |          |
|---------------------------|----------|
| Input pulse levels        | 0V to 3V |
| Input rise and fall times | 10ns     |
| Input reference levels    | 1.5V     |

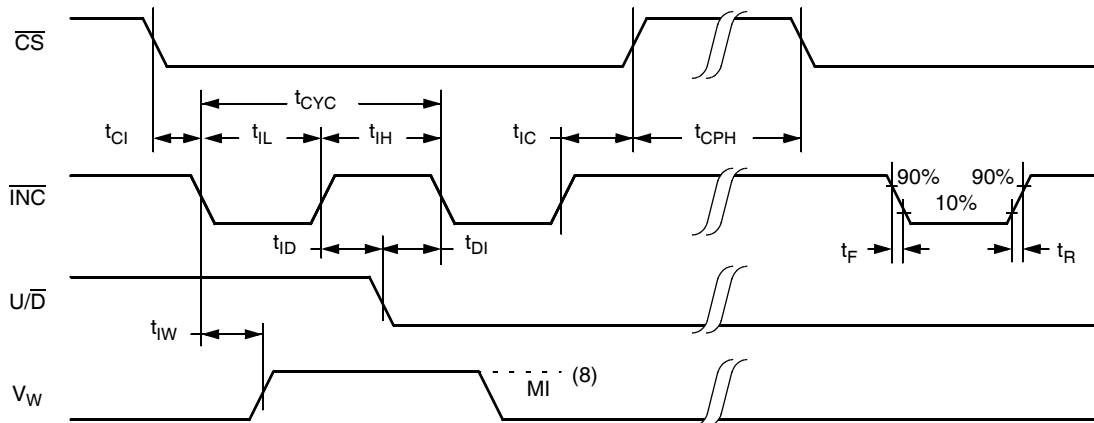
**A.C. OPERATING CHARACTERISTICS** (Over recommended operating conditions unless otherwise specified)

| Symbol             | Parameter   | Limits |                     |      | Unit    |
|--------------------|---|--------|---------------------|------|---------|
|                    |   | Min.   | Typ. <sup>(6)</sup> | Max. |         |
| $t_{CI}$           | $\overline{CS}$ to $\overline{INC}$ setup             | 100    |                     |      | ns      |
| $t_{ID}$           | $\overline{INC}$ HIGH to $U/\overline{D}$ change      | 100    |                     |      | ns      |
| $t_{DI}$           | $U/\overline{D}$ to $\overline{INC}$ setup            | 2.9    |                     |      | $\mu$ s |
| $t_{iL}$           | $\overline{INC}$ LOW period                           | 1      |                     |      | $\mu$ s |
| $t_{iH}$           | $\overline{INC}$ HIGH period                          | 1      |                     |      | $\mu$ s |
| $t_{iC}$           | $\overline{INC}$ inactive to $\overline{CS}$ inactive | 1      |                     |      | $\mu$ s |
| $t_{CPH}$          | $\overline{CS}$ deselect time (STORE)                 | 20     |                     |      | ms      |
| $t_{CPH}$          | $\overline{CS}$ deselect time (NO STORE)              | 100    |                     |      | ns      |
| $t_{iW}^{(5)}$     | $\overline{INC}$ to $V_W/RW$ change                   |        | 100                 |      | $\mu$ s |
| $t_{CYC}$          | $\overline{INC}$ cycle time                           | 2      |                     |      | $\mu$ s |
| $t_R, t_F^{(5)}$   | $\overline{INC}$ input rise and fall time             |        |                     | 500  | $\mu$ s |
| $t_{PU}^{(5)}$     | Power-up to wiper stable                              |        | 500                 |      | $\mu$ s |
| $t_R V_{CC}^{(5)}$ | $V_{CC}$ power-up rate                                | 0.2    |                     | 50   | V/ms    |

**POWER-UP AND DOWN REQUIREMENTS**

At all times, voltages on the potentiometer pins must be less than  $\pm V_{CC}$ . The recall of the wiper position from nonvolatile memory is not in effect until the  $V_{CC}$  supply reaches its final value. The  $V_{CC}$  ramp rate spec is always in effect.

**A.C. TIMING**



- Notes: (6) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.
- (7) This parameter is periodically sampled and not 100% tested.
- (8) MI in the A.C. timing diagram refers to the minimum incremental change in the  $V_W$  output due to a change in the wiper position.

**DETAILED PIN DESCRIPTIONS**

**$R_H/V_H$  and  $R_L/V_L$**

The high ( $V_H/R_H$ ) and low ( $V_L/R_L$ ) terminals of the X9C102/103/104/503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. The terminology of  $V_H/R_H$  and  $V_L/R_L$  references the relative position of the terminal in relation to wiper movement direction selected by the  $U/\bar{D}$  input and not the voltage potential on the terminal.

**$R_W/V_W$**

$V_W/R_W$  is the wiper terminal, and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

**Up/Down ( $U/\bar{D}$ )**

The  $U/\bar{D}$  input controls the direction of the wiper movement and whether the counter is incremented or decremented.

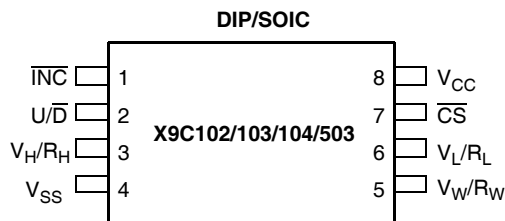
**Increment ( $\bar{INC}$ )**

The  $\bar{INC}$  input is negative-edge triggered. Toggling  $\bar{INC}$  will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the  $U/\bar{D}$  input.

**Chip Select ( $\bar{CS}$ )**

The device is selected when the  $\bar{CS}$  input is LOW. The current counter value is stored in nonvolatile memory when  $\bar{CS}$  is returned HIGH while the  $\bar{INC}$  input is also HIGH. After the store operation is complete the X9C102/103/104/503 device will be placed in the low power standby mode until the device is selected once again.

**PIN CONFIGURATION**



**PIN NAMES**

| Symbol      | Description               |
|-------------|---------------------------|
| $V_H/R_H$   | High Terminal             |
| $V_W/R_W$   | Wiper Terminal            |
| $V_L/R_L$   | Low Terminal              |
| $V_{SS}$    | Ground                    |
| $V_{CC}$    | Supply Voltage            |
| $U/\bar{D}$ | Up/Down Control Input     |
| $\bar{INC}$ | Increment Control Input   |
| $\bar{CS}$  | Chip Select Control Input |
| NC          | No Connection             |

**PRINCIPLES OF OPERATION**

There are three sections of the X9Cxxx: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for  $t_{1W}$  ( $\bar{INC}$  to  $V_W/R_W$  change). The  $R_{TOTAL}$  value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

**INSTRUCTIONS AND PROGRAMMING**

The  $\overline{INC}$ ,  $U/\overline{D}$  and  $\overline{CS}$  inputs control the movement of the wiper along the resistor array. With  $\overline{CS}$  set LOW the device is selected and enabled to respond to the  $U/\overline{D}$  and  $\overline{INC}$  inputs. HIGH to LOW transitions on  $\overline{INC}$  will increment or decrement (depending on the state of the  $U/\overline{D}$  input) a seven-bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever  $\overline{CS}$  transitions HIGH while the  $\overline{INC}$  input is also HIGH.

The system may select the X9Cxxx, move the wiper, and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep  $\overline{INC}$  LOW while taking  $\overline{CS}$  HIGH. The new wiper position will be maintained until changed by the system or until a power-down/up cycle recalled the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference: system parameter changes due to temperature drift, etc...

The state of  $U/\overline{D}$  may be changed while  $\overline{CS}$  remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

**MODE SELECTION**

| $\overline{CS}$ | $\overline{INC}$ | $U/\overline{D}$ | Mode                         |
|-----------------|------------------|------------------|------------------------------|
| L               |                  | H                | Wiper Up                     |
| L               |                  | L                | Wiper Down                   |
|                 | H                | X                | Store Wiper Position         |
| H               | X                | X                | Standby Current              |
|                 | L                | X                | No Store, Return to Standby  |
|                 | L                | H                | Wiper Up (not recommended)   |
|                 | L                | L                | Wiper Down (not recommended) |

**SYMBOL TABLE**

| WAVEFORM | INPUTS                      | OUTPUTS                       |
|----------|-----------------------------|-------------------------------|
|          | Must be steady              | Will be steady                |
|          | May change from Low to High | Will change from Low to High  |
|          | May change from High to Low | Will change from High to Low  |
|          | Don't Care: Changes Allowed | Changing: State Not Known     |
|          | N/A                         | Center Line is High Impedance |



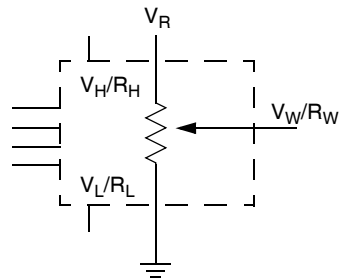
**PERFORMANCE CHARACTERISTICS**

Contact the factory for more information.

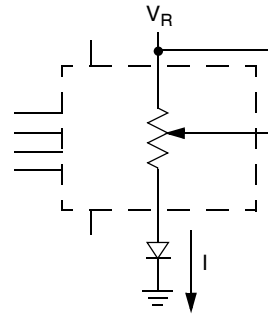
**APPLICATIONS INFORMATION**

Electronic digitally controlled (XCDP) potentiometers provide three powerful application advantages; (1) the variability and reliability of a solid-state potentiometer, (2) the flexibility of computer-based digital controls, and (3) the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

**Basic Configurations of Electronic Potentiometers**



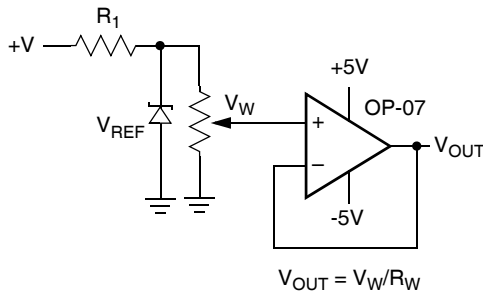
Three terminal potentiometer; variable voltage divider



Two terminal variable resistor; variable current

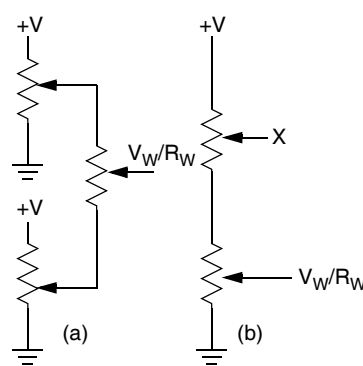
**Basic Circuits**

**Buffered Reference Voltage**

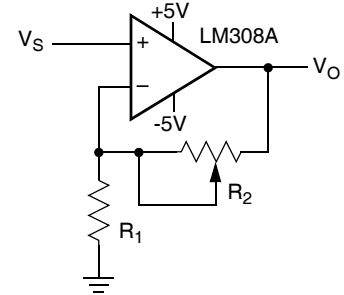


$$V_{OUT} = V_W/R_W$$

**Cascading Techniques**

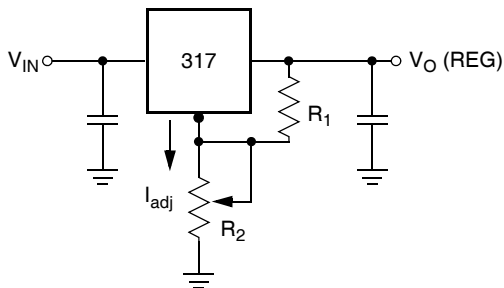


**Noninverting Amplifier**



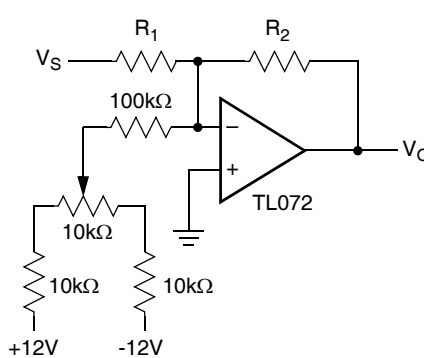
$$V_O = (1 + R_2/R_1)V_S$$

**Voltage Regulator**

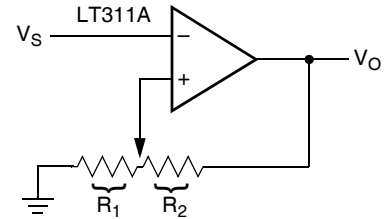


$$V_O (REG) = 1.25V (1 + R_2/R_1) + I_{adj} R_2$$

**Offset Voltage Adjustment**



**Comparator with Hysteresis**

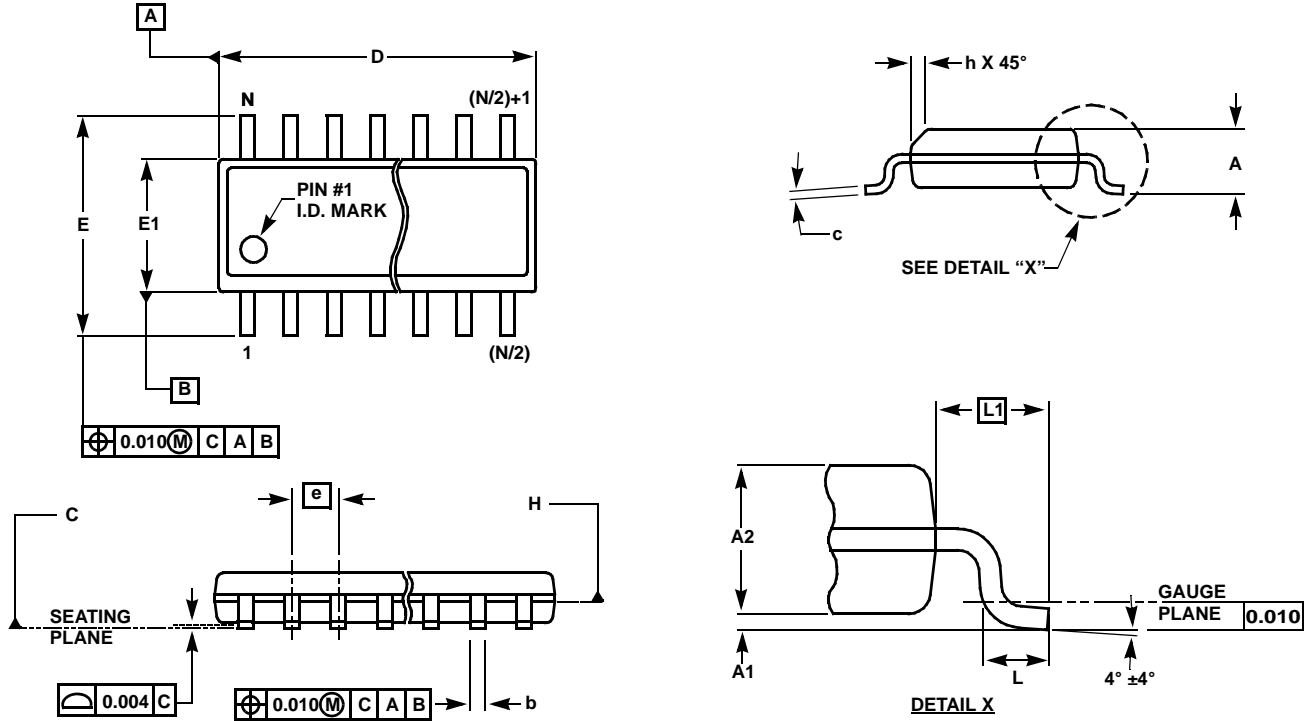


$$V_{UL} = \{R_1/(R_1 + R_2)\} V_O(max)$$

$$V_{LL} = \{R_1/(R_1 + R_2)\} V_O(min)$$

(for additional circuits see AN115)

**Small Outline Package Family (SO)**



**MDP0027**

**SMALL OUTLINE PACKAGE FAMILY (SO)**

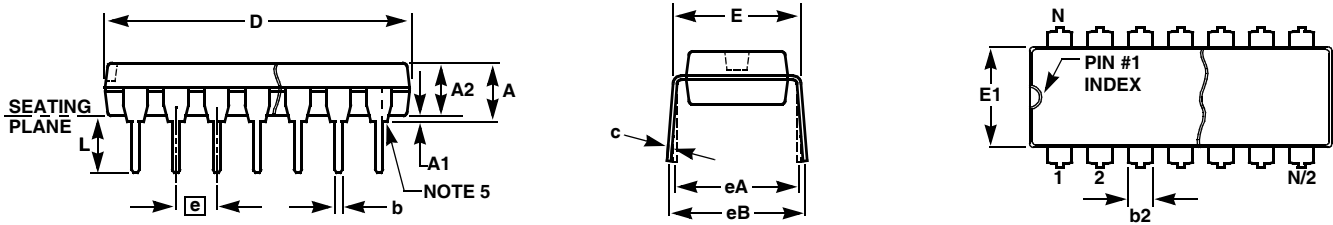
| SYMBOL | SO-8  | SO-14 | SO16<br>(0.150") | SO16 (0.300")<br>(SOL-16) | SO20<br>(SOL-20) | SO24<br>(SOL-24) | SO28<br>(SOL-28) | TOLERANCE   | NOTES |
|--------|-------|-------|------------------|---------------------------|------------------|------------------|------------------|-------------|-------|
| A      | 0.068 | 0.068 | 0.068            | 0.104                     | 0.104            | 0.104            | 0.104            | MAX         | -     |
| A1     | 0.006 | 0.006 | 0.006            | 0.007                     | 0.007            | 0.007            | 0.007            | $\pm 0.003$ | -     |
| A2     | 0.057 | 0.057 | 0.057            | 0.092                     | 0.092            | 0.092            | 0.092            | $\pm 0.002$ | -     |
| b      | 0.017 | 0.017 | 0.017            | 0.017                     | 0.017            | 0.017            | 0.017            | $\pm 0.003$ | -     |
| c      | 0.009 | 0.009 | 0.009            | 0.011                     | 0.011            | 0.011            | 0.011            | $\pm 0.001$ | -     |
| D      | 0.193 | 0.341 | 0.390            | 0.406                     | 0.504            | 0.606            | 0.704            | $\pm 0.004$ | 1, 3  |
| E      | 0.236 | 0.236 | 0.236            | 0.406                     | 0.406            | 0.406            | 0.406            | $\pm 0.008$ | -     |
| E1     | 0.154 | 0.154 | 0.154            | 0.295                     | 0.295            | 0.295            | 0.295            | $\pm 0.004$ | 2, 3  |
| e      | 0.050 | 0.050 | 0.050            | 0.050                     | 0.050            | 0.050            | 0.050            | Basic       | -     |
| L      | 0.025 | 0.025 | 0.025            | 0.030                     | 0.030            | 0.030            | 0.030            | $\pm 0.009$ | -     |
| L1     | 0.041 | 0.041 | 0.041            | 0.056                     | 0.056            | 0.056            | 0.056            | Basic       | -     |
| h      | 0.013 | 0.013 | 0.013            | 0.020                     | 0.020            | 0.020            | 0.020            | Reference   | -     |
| N      | 8     | 14    | 16               | 16                        | 20               | 24               | 28               | Reference   | -     |

Rev. L 2/01

**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

**Plastic Dual-In-Line Packages (PDIP)**



**MDP0031**

**PLASTIC DUAL-IN-LINE PACKAGE**

| SYMBOL | PDIP8 | PDIP14 | PDIP16 | PDIP18 | PDIP20 | TOLERANCE     | NOTES |
|--------|-------|--------|--------|--------|--------|---------------|-------|
| A      | 0.210 | 0.210  | 0.210  | 0.210  | 0.210  | MAX           |       |
| A1     | 0.015 | 0.015  | 0.015  | 0.015  | 0.015  | MIN           |       |
| A2     | 0.130 | 0.130  | 0.130  | 0.130  | 0.130  | ±0.005        |       |
| b      | 0.018 | 0.018  | 0.018  | 0.018  | 0.018  | ±0.002        |       |
| b2     | 0.060 | 0.060  | 0.060  | 0.060  | 0.060  | +0.010/-0.015 |       |
| c      | 0.010 | 0.010  | 0.010  | 0.010  | 0.010  | +0.004/-0.002 |       |
| D      | 0.375 | 0.750  | 0.750  | 0.890  | 1.020  | ±0.010        | 1     |
| E      | 0.310 | 0.310  | 0.310  | 0.310  | 0.310  | +0.015/-0.010 |       |
| E1     | 0.250 | 0.250  | 0.250  | 0.250  | 0.250  | ±0.005        | 2     |
| e      | 0.100 | 0.100  | 0.100  | 0.100  | 0.100  | Basic         |       |
| eA     | 0.300 | 0.300  | 0.300  | 0.300  | 0.300  | Basic         |       |
| eB     | 0.345 | 0.345  | 0.345  | 0.345  | 0.345  | ±0.025        |       |
| L      | 0.125 | 0.125  | 0.125  | 0.125  | 0.125  | ±0.010        |       |
| N      | 8     | 14     | 16     | 18     | 20     | Reference     |       |

Rev. B 2/99

**NOTES:**

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

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