DATA SHEET

PCA9544

4-channel I^2C multiplexer and interrupt controller

Product specification
Supersedes data of 1999 Apr 01

1999 Oct 07

Philips
Semiconductors

4-channel I²C multiplexer and interrupt controller PCA9544

FEATURES

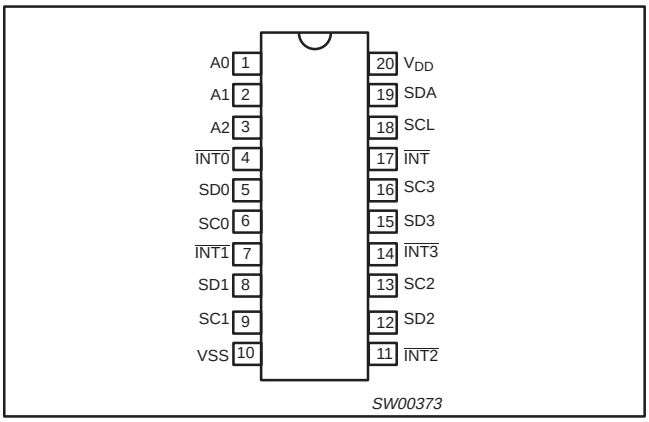
- 1-of-4 bi-directional translating multiplexer
- Channel selection via I²C bus
- Operating supply voltage 2.5 to 3.6 V
- Operating temperature range 0°C to 70°C
- Power-up with all multiplexer channels deselected
- 3 address pins, allowing up to 8 devices on the I²C bus
- Low on resistance

DESCRIPTION

The PCA9544 is a 1-of-4 bi-directional translating multiplexer, controlled via the I²C bus. The SCL/SDA upstream pair fans out to four SCx/SDx downstream pairs, or channels. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register. Four interrupt inputs, one for each of the SCx/SDx downstream pair, are provided. One interrupt output, which acts as an AND of the four interrupt inputs, is provided. All I/O pins are 5 V tolerant.

The pass gates of the multiplexer are constructed such that the V_{DD} pin can be used to limit the maximum high voltage which will be passed by the PCA9544. This allows the use of different bus voltages on each SCx/SDx pair, so that 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors can pull the bus up to the desired voltage level for this channel.

PIN CONFIGURATION



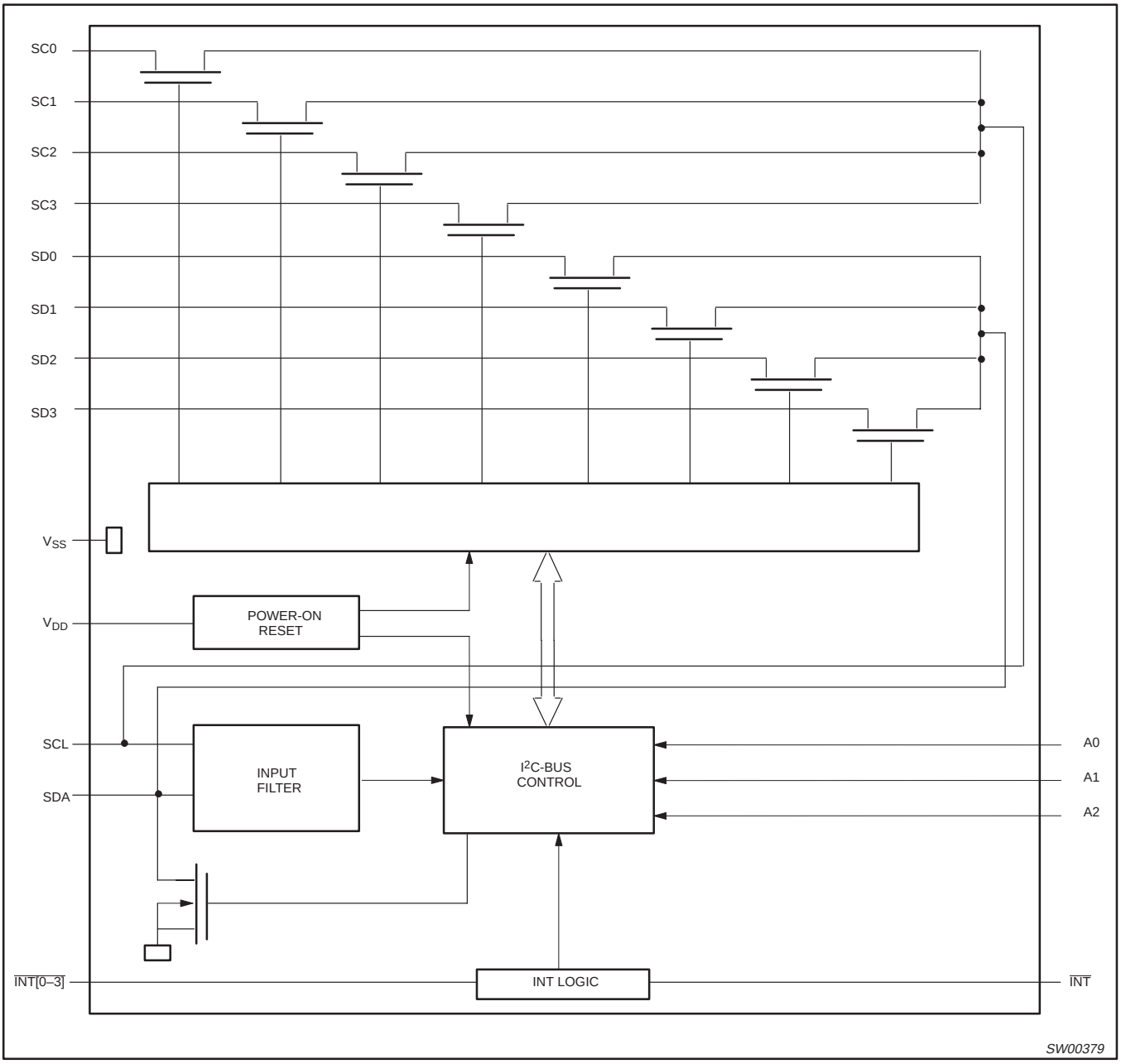
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	A0	Address input 0
2	A1	Address input 1
3	A2	Address input 2
4	$\overline{INT0}$	Interrupt input 0
5	SD0	Serial data 0
6	SC0	Serial clock 0
7	$\overline{INT1}$	Interrupt input 1
8	SD1	Serial data 1
9	SC1	Serial clock 1
10	VSS	Supply ground
11	$\overline{INT2}$	Interrupt input 2
12	SD2	Serial data 2
13	SC2	Serial clock 2
14	$\overline{INT3}$	Interrupt input 3
15	SD3	Serial data 3
16	SC3	Serial clock 3
17	$\overline{INT}$	Interrupt output
18	SCL	Serial clock line
19	SDA	Serial data line
20	V_{DD}	Supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic TSSOP	0°C to +70°C	PCA9544 PW DH	SOT360-1

BLOCK DIAGRAM

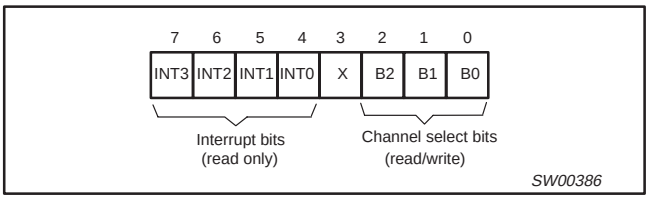


CHANNEL SELECTION

A SC0x/SD0x downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9544 has been addressed. The 3 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a stop condition has been placed on the I²C bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

CONTROL BYTE								SELECTED CHANNEL
7	6	5	4	3	2	1	0	
X	X	X	X	X	0	X	X	none
X	X	X	X	X	1	0	0	0 (SC0/SD0)
X	X	X	X	X	1	0	1	1 (SC1/SD1)
X	X	X	X	X	1	1	0	2 (SC2/SD2)
X	X	X	X	X	1	1	1	3 (SC3/SD3)

CONTROL REGISTER



POWER-ON RESET

During power-up, the control register defaults to all zeroes causing all the channels to be deselected.

INTERRUPT HANDLING

The PCA9544 provides 4 interrupt inputs, one for each channel and one open drain interrupt output. When an interrupt is generated by any device, it will be detected by the PCA9544 and the interrupt output will be driven LOW. The channel need not be active for detection of the interrupt. A bit is also set in the control byte. Bits 4 – 7 of the control byte correspond to channels 0 – 3 of the PCA9544, respectively. Therefore, if an interrupt is generated by any device connected to channel 2, then bit 6 will be set in the control register. Likewise, an interrupt on any device connected to channel 3 would cause bit 7 of the control register to be set. The master can then address the PCA 9544 and read the contents of the control byte to determine which channel contains the device generating the interrupt. The master can then reconfigure the PCA9544 to select this channel, and locate the device generating the interrupt and clear it. The interrupt clears when the device originating the interrupt clears.

It should be noted that more than one device can be providing an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

7	6	5	4	3	2	1	0	INTERRUPTING CHANNEL
0	0	0	1	X	X	X	X	0 (SC0/SD0)
0	0	1	0	X	X	X	X	1 (SC1/SD1)
0	1	0	0	X	X	X	X	2 (SC2/SD2)
1	0	0	0	X	X	X	X	3 (SC3/SD3)

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see FIgure 1).

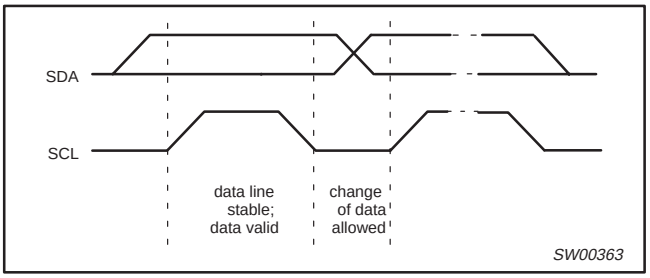


Figure 1. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 2).

System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 3).

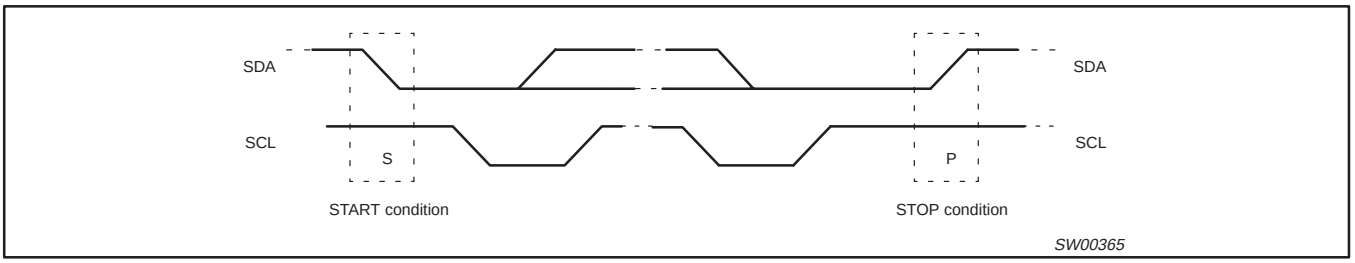


Figure 2. Definition of start and stop conditions

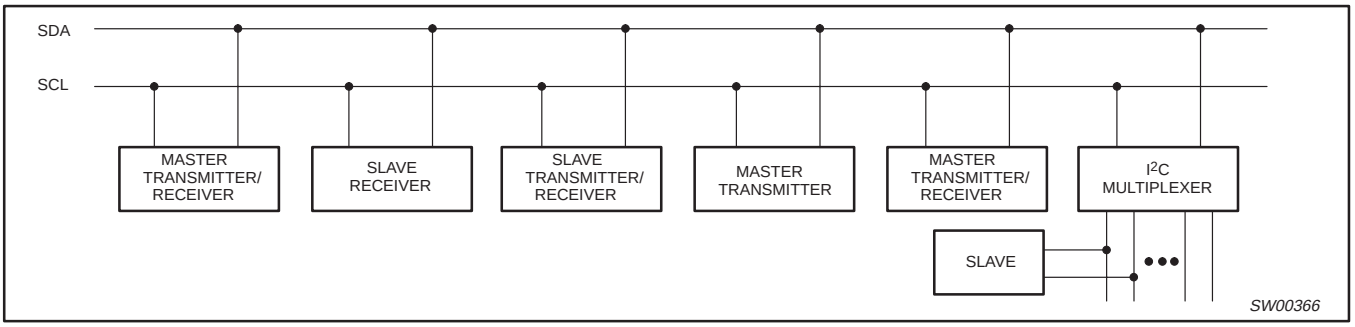


Figure 3. System configuration

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

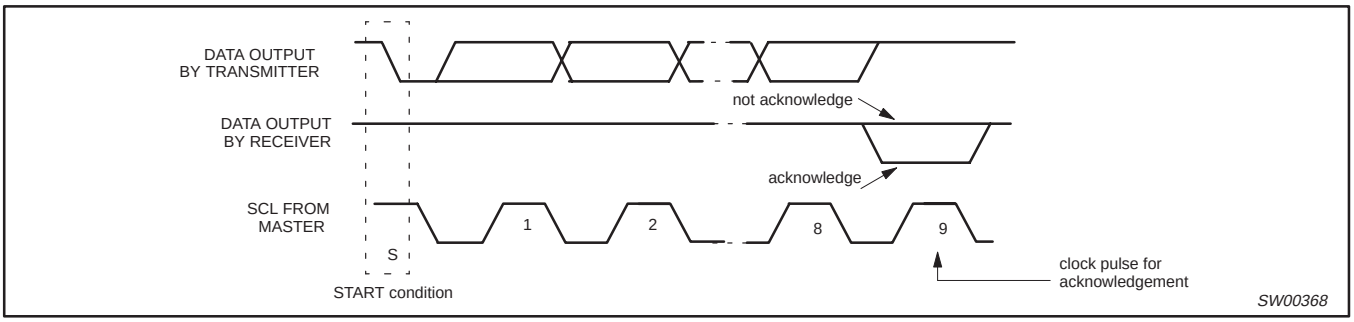


Figure 4. Acknowledgement on the I²C-bus

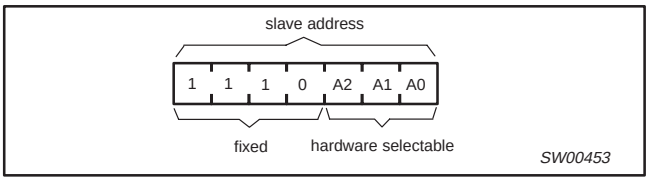


Figure 5. Slave address

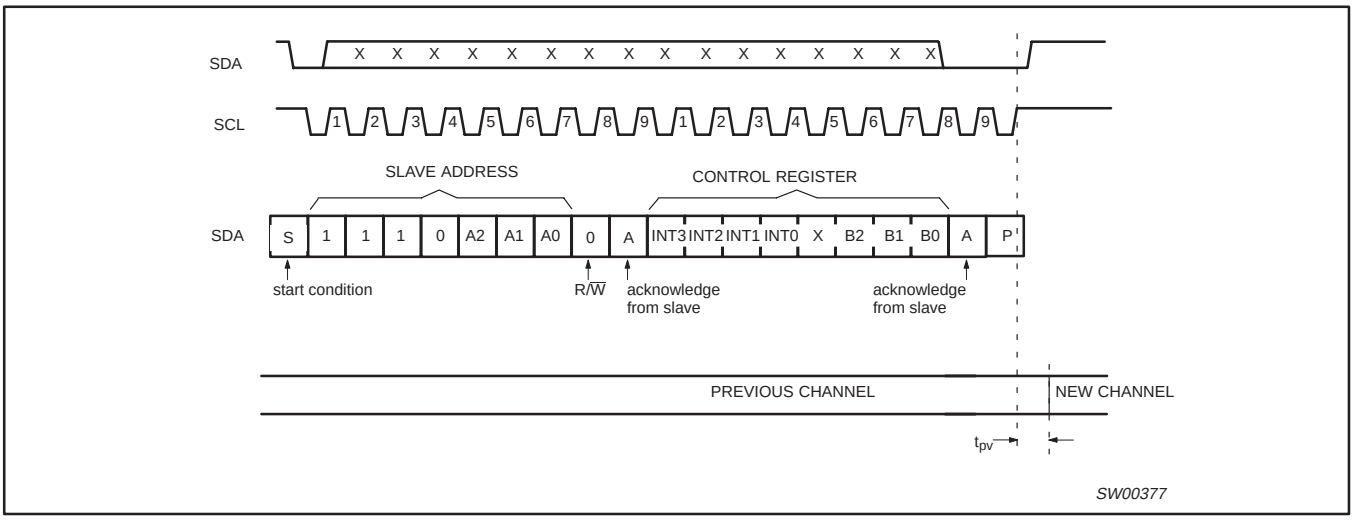


Figure 6. WRITE control register

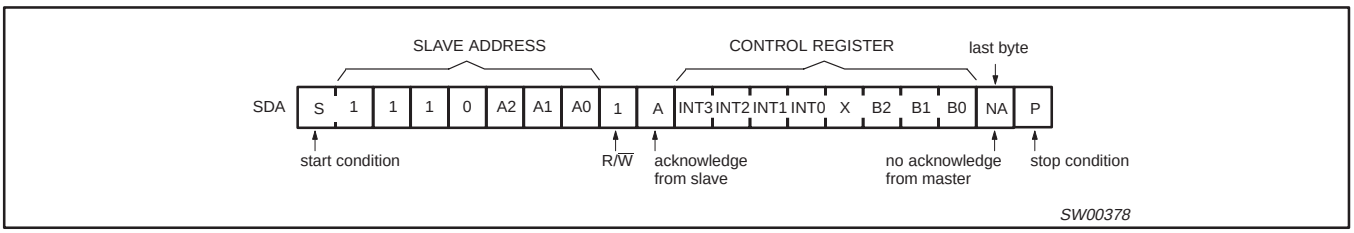


Figure 7. READ control register

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{DD}	DC supply voltage		–0.5 to +7.0	V
V_I	DC input voltage		–0.5 to +7.0	V
I_I	DC input current		±20	mA
I_O	DC output current		±25	mA
I_{DD}	Supply current		±100	mA
I_{SS}	Supply current		±100	mA
P_{tot}	total power dissipation		400	mW
T_{stg}	Storage temperature range		–60 to +150	°C
T_{amb}	Operating ambient temperature		0 to +70	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.

DC CHARACTERISTICS

V_{DD} = 2.5 to 3.6 V; V_{SS} = 0 V; T_{amb} = 0°C to +70°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply						
VDDQn ≤ V_{DD}	Supply voltage		2.5		3.6	V
I_{DD}	Supply current	Operating mode; V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	–	20	100	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}	–	2.5	100	µA
V_{POR}	Power-on reset voltage	V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}	–	1.3	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		–0.5	–	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	–	6	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
		V_{OL} = 0.6 V	6	–	–	
I_L	Leakage current	V_I = V_{DD} or V_{SS}	–1	–	+1	µA
C_i	Input capacitance	V_I = V_{SS}	–	–	13	pF
Select inputs A0 to A2 / $\overline{INT0}$ to $\overline{INT3}$						
V_{IL}	LOW level input voltage		–0.5	–	+0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	–	V_{DD} + 0.5	V
I_{LI}	Input leakage current	pin at V_{DD} or V_{SS}	–1	–	+1	µA
Pass Gate						
R_{ON}	Switch resistance	V_{CC} = 3.67 V, V_O = 0.4 V, I_O = 15 mA	5	20	30	Ω
		V_{CC} = 2.3 to 2.7 V, V_O = 0.4V, I_O = 10 mA	7	26	55	
V_{Pass}	Switch output voltage	V_{swin} = V_{DD} = 3.3 V; I_{swout} = –100 µA		2.2		V
		V_{swin} = V_{DD} = 3.0 to 3.6 V; I_{swout} = –100 µA	1.6		2.8	
		V_{swin} = V_{DD} = 2.5 V; I_{swout} = –100 µA		1.5		
		V_{swin} = V_{DD} = 2.3 to 2.7 V; I_{swout} = –100 µA	1.1		2.0	
I_L	Leakage current	V_I = V_{DD} or V_{SS}	–1	–	+1	µA
INT Output						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
I_L	Leakage current	V_I = V_{DD} or V_{SS}	–1	–	+1	µA

AC CHARACTERISTICS

SYMBOL	PARAMETER	STANDARD-MODE I²C-BUS		FAST-MODE I²C-BUS		UNIT
		MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay from SDA to SD_n or SCL to SC_n		0.3[1]		0.3[1]	ns
f_{SCL}	SCL clock frequency	0	100	0	400	KHz
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
$t_{HD:STA}$	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7	–	0.6		µs
$t_{HD:DAT}$	Data hold time: for CBUS compatible masters for I²C-bus devices	 5.0 0[2]	 – –	 – 0[2]	 – 0.9[3]	 µs µs
$t_{SU:DAT}$	Data set-up time	250	–	100[4]	–	ns
$t_{SU:STO}$	Set-up time for STOP condition	–	1000	–	300	ns
t_r	Rise time of both SDA and SCL signals	–	300	–	300	ns
t_f	Fall time of both SDA and SCL signals	4.0	–	0.6	–	µs
C_b	Capacitive load for each bus line		400	–	400	pF
$\overline{INT}$						
t_{iv}	$\overline{INTn}$ to $\overline{INT}$ active valid time		4		4	µs
t_{ir}	$\overline{INTn}$ to $\overline{INT}$ inactive delay time		2		2	µs
L_{pwr}	LOW level pulse width rejection or $\overline{INTn}$ inputs	1		1		ns
H_{pwr}	HIGH level pulse width rejection or $\overline{INTn}$ inputs	500		500		ns

NOTES:
1. Pass gate propagation delay is calculated from the 20Ω typical R_{ON} and and the 15pF load capacitance.
2. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIH_{min} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A fast-mode I²C bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU:DAT} \geq 250$ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU:DAT} = 1000 + 250 = 1250$ns (according to the standard-mode I²C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF.

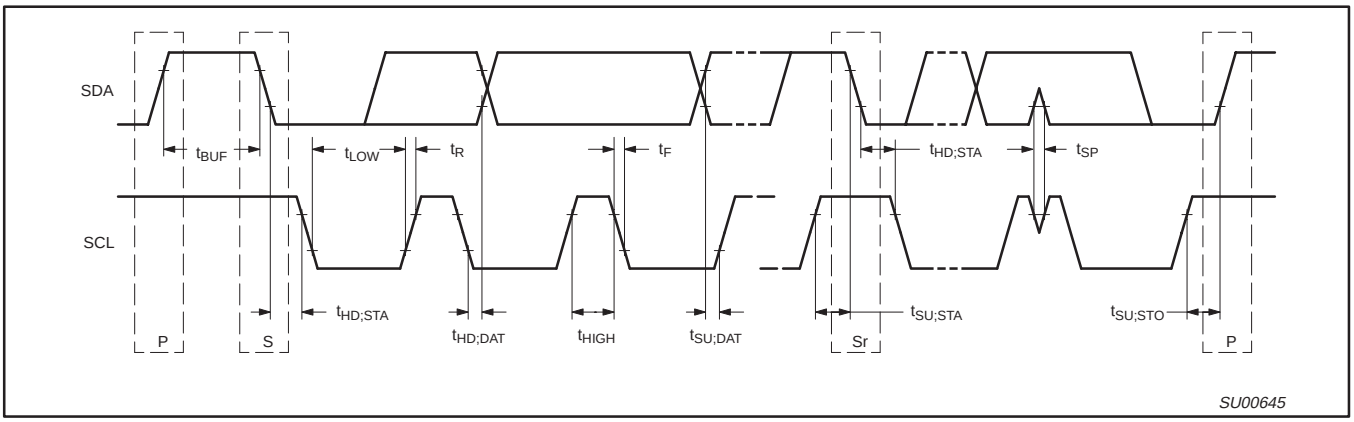
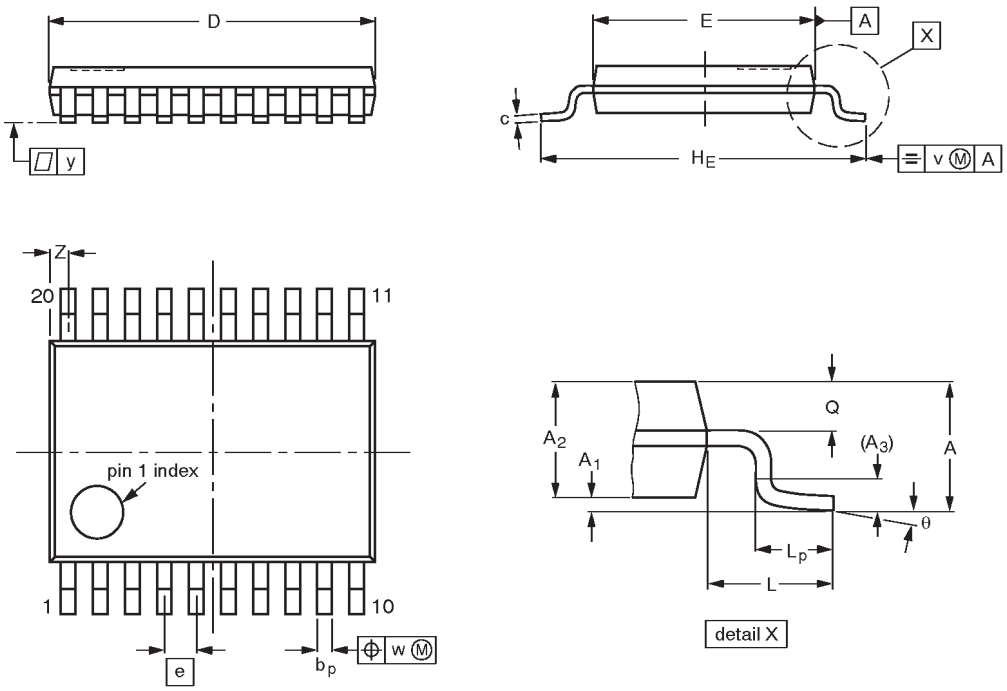
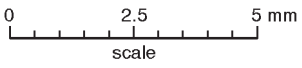


Figure 8. Definition of timing on the I²C-bus

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

NOTES

4-channel I²C multiplexer and interrupt controller PCA9544

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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