National Semiconductor

Not Intended For New Designs

Comlinear CLC561
Wideband, Low Distortion DriveR-*Amps*

General Description

The CLC561 is a wideband dc coupled, amplifier that combines high output drive and low distortion. At an output of +24dBm ($10V_{pp}$ into 50Ω), the –3dB bandwidth is 150MHz. As illustrated in the table below, distortion performance remains excellent even when amplifying high-frequency signals to high output power levels.

Typical Distortion Performance

Output Power	20MHz 2nd	20MHz 3rd	50MHz 2nd	50MHz 3rd	100MHz 2nd	100MHz 3rd
10dBm	– 59	– 62	– 52	– 60	– 35	– 49
18dBm	– 52	– 48	– 45	– 46	– 30	– 36
24dBm	– 50	– 41	– 36	– 32	– 40	– 30

With the output current internally limited to 250mA, the CLC561 is fully protected against shorts to ground and can, with the addition of a series limiting resistor at the output, withstand shorts to the ±15V supplies.

The CLC561 has been designed for maximum flexibility in a wide variety of demanding applications. The two resistors comprising the feedback network set both the gain and the output impedance, without requiring the series backmatch resistor needed by most op amps. This allows driving into a matched load without dropping half the voltage swing through a series matching resistor. External compensation allows user adjustment of the frequency response. The CLC561 is specified for both maximally flat frequency response and 0% pulse overshoot compensations.

The combination of wide bandwidth, high output power, and low distortion, coupled with gain, output impedance and frequency response flexibility, makes the CLC561 ideal for waveform generator applications. Excellent stability driving capacitive loads yields superior performance driving ADC's, long transmission lines, and SAW devices. A companion part, the CLC560, offers superior pulse fidelity for high accuracy dc coupled applications.

The CLC561 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

CLC561AI -25°C to +85°C 24-pin
CLC561A8C -55°C to +85°C 24-pin plastic SOIC
Contact factory for other packages and DESC SMD number.

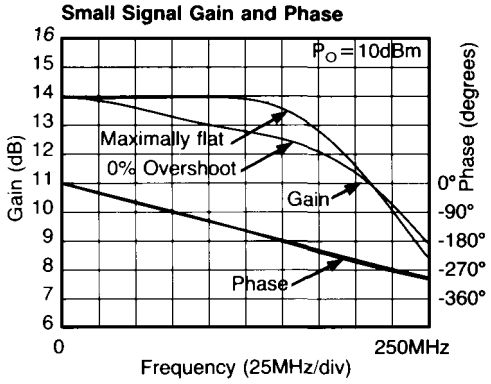
Features

- 150MHz bandwidth at +24dBm output
- Low distortion (2nd/3rd: -59/-62dBc @ 20MHz and 10dBm)
- Output short circuit protection
- -43dB feedthrough at 30MHz
- User-definable output impedance, gain, and compression
- Internal current limiting

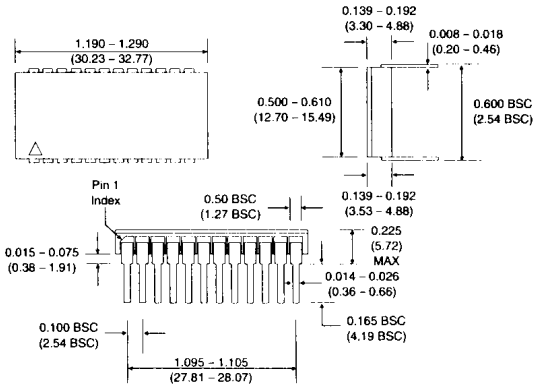
Applications

- Output amplification
- Arbitrary waveform generation
- ATE systems
- Cable/line driving
- Function generators
- SAW drivers
- Flash A/D driving and testing

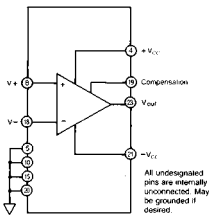
Small Signal Gain and Phase



Package Dimensions



Pinout



Electrical Characteristics ($A_V = +10$, $V_{CC} = \pm 15V$, $R_f = 410\Omega$, $R_g = 40\Omega$, $R_O = 50\Omega$, $R_L = 50\Omega$)

NOTES TO THE ELECTRICAL SPECIFICATIONS

The electrical characteristics shown here apply to the specific test conditions shown above (see also Figure 1 in description of operation). The CLC561 provides an equivalent, non-zero, output impedance determined by the external resistors. The signal gain to the load is therefore load dependent. **The signal gain shown above ($A_V = +10$) is the no load gain.** The actual gain to the matching 50 ohm load used in these specifications is half of this (+5).

The CLC561 requires an external compensation capacitor. Unless otherwise noted, this has been set to 10.5pF for the frequency domain specifications (yielding a maximally flat frequency response) and 12.5pF for the time domain specifications (yielding a 0% small signal pulse overshoot response).

Parameters preceded by an * are the final electrical test parameters and are 100% tested at 25°C on all versions. The A8C (military) grade part is also 100% tested at -55°C and 125°C case temperature.

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Case Temperature	CLC561A8	+25°C	−55°C	+25°C	+125°C		
Case Temperature	CLC561AI	+25°C	−25°C	+25°C	+ 85°C		
FREQUENCY DOMAIN (Maximally Flat Compensation)							
-3dB bandwidth							
*maximally flat compensation	$V_{OUT}<2V_{pp}$ (+10dBm)	215	>175	>185	>175	MHz	SSBW
0% overshoot compensation	$V_{OUT}<2V_{pp}$ (+10dBm)	210	>170	>180	>170	MHz	
large signal bandwidth	$V_{OUT}<10V_{pp}$ (+24dBm)	150	>145	>135	>120	MHz	FPBW
(see Frequency Response vs. Output Power plot)							
gain flatness	$V_{OUT}<2V_{pp}$ (+10dBm)						
* peaking	0.1 - 50MHz	0	<0.50	<0.40	<0.50	dB	GFPL
* peaking	>50MHz	0	<1.75	<0.75	<1.00	dB	GFPH
* roll off	at 100MHz	0.1	<1.00	<0.75	<1.00	dB	GFR
group delay	to 100MHz	2.9	—	—	—	ns	GD
linear phase deviation	to 100MHz	0.6	<1.7	<1.2	<1.7	°	LPD
return loss (see discussion of R_X)	to 100MHz	−15	<−11	<−11	<−11	dB	RL
DISTORTION (Maximally Flat Compensation)							
2nd harmonic distortion							
*24dBm ($10V_{pp}$):	20MHz	−50	<−38	<−40	<−38	dBc	HD2HL
*	50MHz	−36	<−29	<−29	<−22	dBc	HD2HM
	100MHz	−40	<−25	<−25	<−25	dBc	HD2HH
*18dBm ($5V_{pp}$):	20MHz	−52	<−42	<−44	<−42	dBc	HD2ML
*	50MHz	−45	<−30	<−35	<−30	dBc	HD2MM
*	100MHz	−30	<−22	<−25	<−25	dBc	HD2MH
*10dBm ($2V_{pp}$):	20MHz	−59	<−48	<−52	<−48	dBc	HD2LL
*	50MHz	−52	<−36	<−40	<−40	dBc	HD2LM
*	100MHz	−35	<−27	<−28	<−28	dBc	HD2LH
3rd harmonic distortion							
*24dBm ($10V_{pp}$):	20MHz	−41	<−34	<−34	<−30	dBc	HD3HL
*	50MHz	−32	<−26	<−26	<−21	dBc	HD3HM
	100MHz	−30	<−24	<−24	<−24	dBc	HD3HH
*18dBm ($5V_{pp}$):	20MHz	−48	<−40	<−44	<−44	dBc	HD3ML
*	50MHz	−46	<−37	<−37	<−35	dBc	HD3MM
	100MHz	−36	<−30	<−30	<−30	dBc	HD3MH
*10dBm ($2V_{pp}$):	20MHz	−62	<−54	<−57	<−57	dBc	HD3LL
*	50MHz	−60	<−49	<−52	<−49	dBc	HD3LM
	100MHz	−49	<−45	<−45	<−45	dBc	HD3LH
2-tone 3rd order intermod intercept[1]	20MHz	38	>36	>36	>36	dBm	IM3L
	50MHz	35	>32	>32	>32	dBm	IM3M
	100MHz	29	>27	>27	>23	dBm	IM3H

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Electrical Characteristics ($A_V = +10$, $V_{CC} = \pm 15V$, $R_f = 410\Omega$, $R_g = 40\Omega$, $R_O = 50\Omega$, $R_L = 50\Omega$)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Case Temperature	CLC561A8	+25°C	−55°C	+25°C	+125°C		
Case Temperature	CLC561AI	+25°C	−25°C	+25°C	+ 85°C		
TIME DOMAIN (0% Overshoot Compensation)							
rise and fall time							
2V step		1.5	<2.0	<1.9	<2.0	ns	TRS
10V step		2.4	<2.8	<2.8	<3.4	ns	TRL
settling time to 0.5% (time<1μs)	5V step	7	<12	<12	<15	ns	TS
long term thermal tail (time>1μs)	5V step	1.5	<2.0	<2.0	<2.0	%	SE
slew rate	$10V_{pp}$, 175MHz	3300	>3000	>2900	>2500	V/μs	SR
overshoot	2V step						
maximally flat compensation		5	<13	<10	<13	%	OSMF
0% overshoot compensation		0	<5	<3	<5	%	OSZO
EQUIVALENT INPUT NOISE							
voltage	>100KHz	2.1	<2.5	<2.5	<2.5	$nV/\sqrt{Hz}$	VN
inverting current	>100KHz	34	<40	<40	<45	$pA/\sqrt{Hz}$	ICN
non-inverting current	>100KHz	2.8	<4.5	<4.5	<5.0	$pA/\sqrt{Hz}$	NCN
noise floor	>100KHz	−159	<−157	<−157	<−157	dBm/(1Hz)	SNF
integrated noise	1kHz to 200MHz	35	<45	<45	<45	μV	INV
noise figure	>100KHz	15	<17	<17	<17	dB	NF
STATIC, DC							
*input offset voltage		2.0	<14.0	<5.0	<15.0	mV	VIO
average temperature coefficient		35	<100	—	<100	μV/°C	DVIO
*non-inverting bias current		5.0	<35	<20	<20	μA	IBN
average temperature coefficient		20	<175	—	<100	nA/°C	DIBN
*inverting bias current		10.0	<50	<30	<50	μA	IBI
average temperature coefficient		100	<200	—	<200	nA/°C	DIBI
*power supply rejection ratio (DC)		57	>54	>54	>52	dB	PSRR
*supply current	no load	50	<60	<60	<65	mA	ICC
MISCELLANEOUS							
open loop current gain	(± 2% tolerance)	10.0	—	—	—	mA/mA	G
average temperature coefficient		+0.02	<+.03	—	<+.02	%/°C	DG
inverting input resistance	(±5% tolerance)	14.0	—	—	—	Ω	RIN
average temperature coefficient		+.02	<+.025	—	<+.025	Ω/°C	DRIN
non-inverting input resistance		700	>200	>400	>400	KΩ	RNI
non-inverting input capacitance	to 100MHz	2.7	<3.5	<3.5	<3.5	pF	CNI
output voltage range @ 150mA	load current	±10.5	—	>±10.0	—	V	VO
output current limit		210	<250	<250	<250	mA	OCL

Absolute Maximum Ratings

V_{cc} (reversed supplies will destroy part)	±20V
differential input voltage	±3V
common mode input voltage	$\pm V_{cc}$
junction temp. (see thermal model)	+175°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	±300°C
output current (internally limited)	±250mA

Recommended Operating Conditions

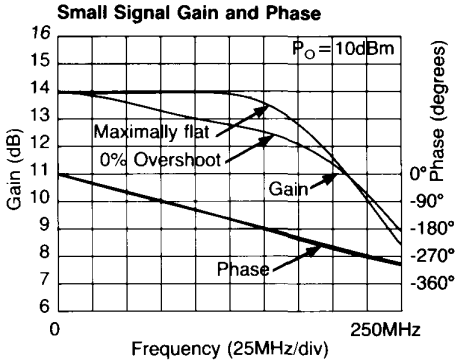
$\pm V_{CC}$	±10 to ±15
I_{out}	≤±200mA
common mode input voltage	$< \pm(\lvert V_{CC}\rvert - 6)V$
output impedance	25Ω to 200Ω
gain range (no-load voltage gain)	+5 to +80
case temp. AI	−25°C to +85°C
A8	−55°C to +125°C

NOTES:

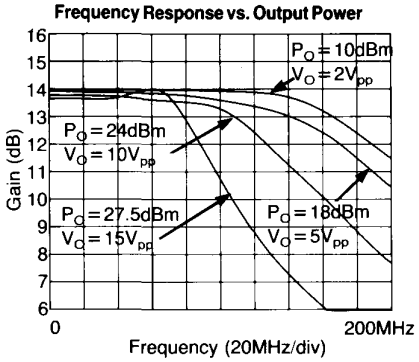
1. Test tones are set ±100kHz of indicated frequency.

Typical Performance Characteristics (T_A = 25° C. Circuit of Figure 1 unless otherwise specified)

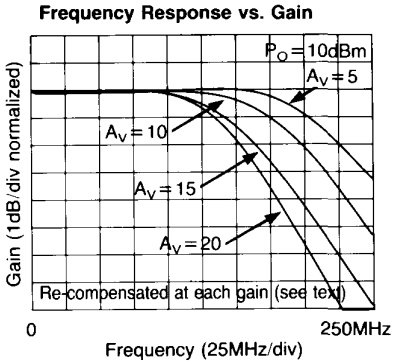
Small Signal Gain and Phase



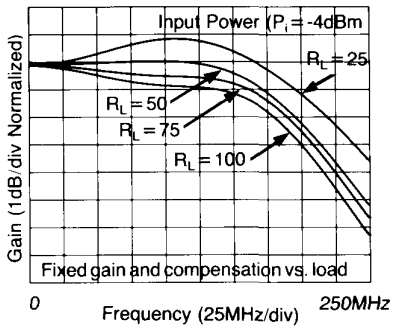
Frequency Response vs. Output Power



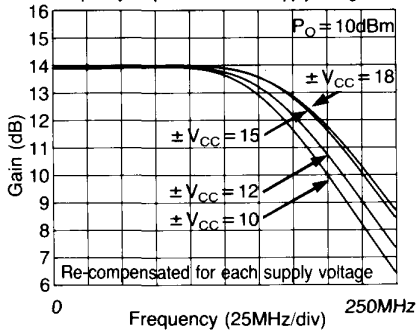
Frequency Response vs. Gain



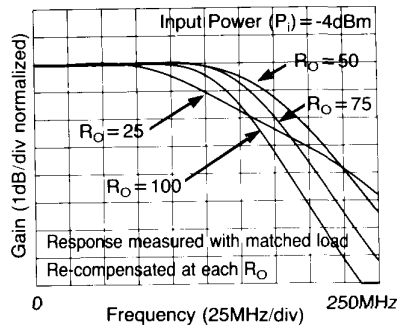
Frequency Response vs. Load Impedance (R_L)



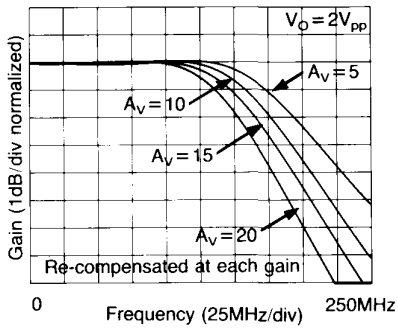
Frequency Response vs. Power Supply Voltages



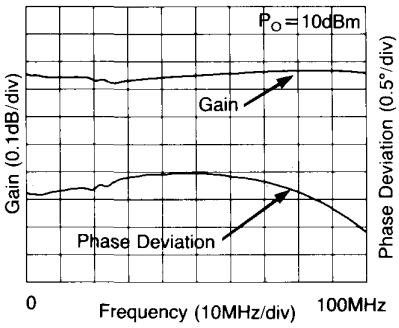
Frequency Response vs. Output Impedance (R_O)



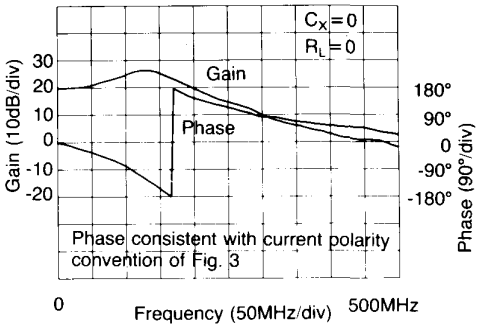
Frequency Response vs. Gain with R_O = R_L = 75Ω



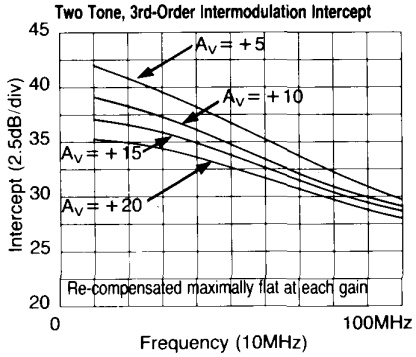
Gain Flatness and Deviation from Linear Phase



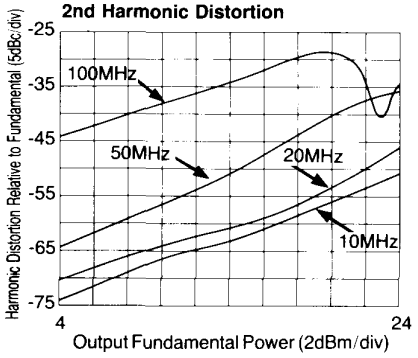
Internal Current Gain and Phase



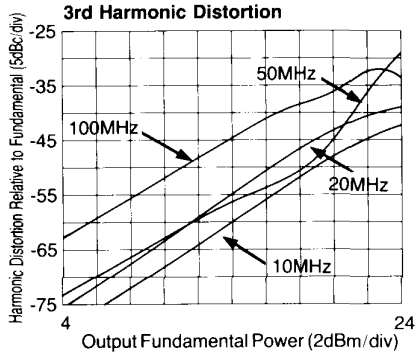
Two Tone, 3rd-Order Intermodulation Intercept



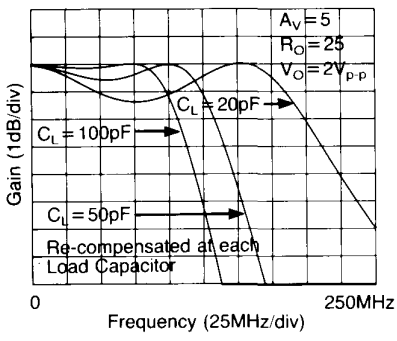
2nd Harmonic Distortion



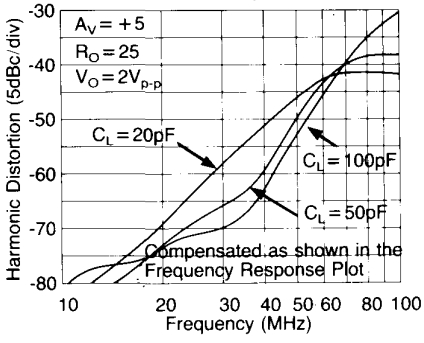
3rd Harmonic Distortion



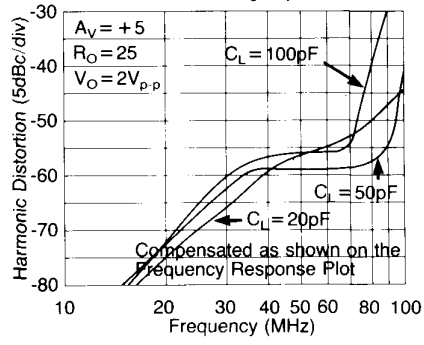
Frequency Response Driving a Capacitive Load



2nd Harmonic Distortion Driving a Capacitive Load

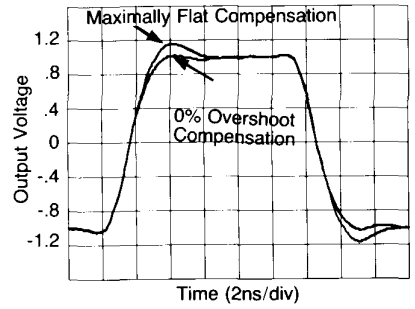


3rd Harmonic Distortion Driving a Capacitive Load

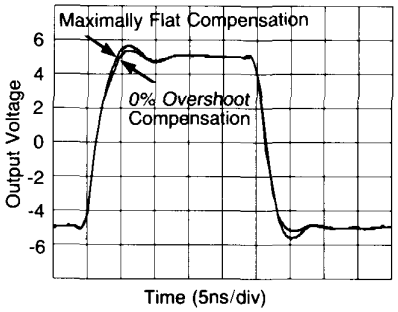


Typical Performance Characteristics (T_A = 25° C. Circuit of Figure 1 unless otherwise specified)

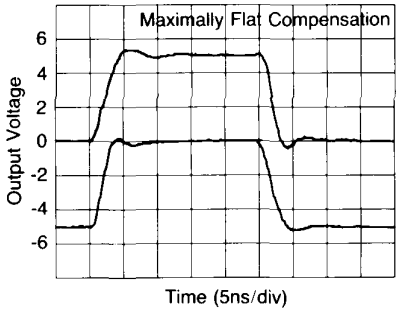
Small Signal Pulse Response



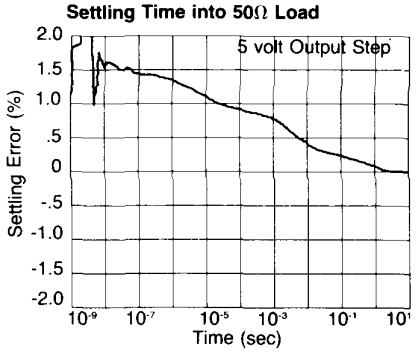
Large Signal Pulse Response



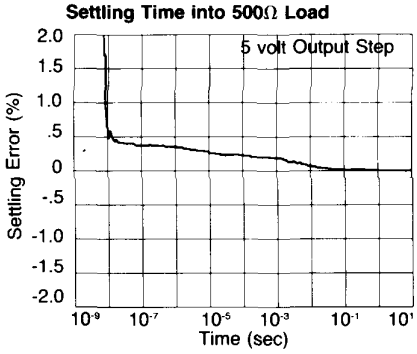
Uni-polar Pulse Response



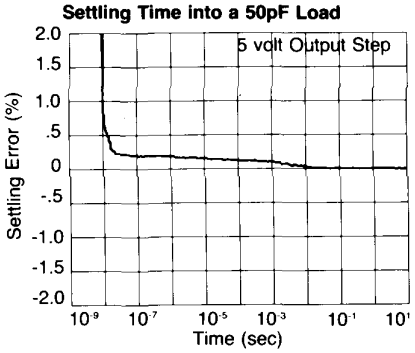
Settling Time into 50Ω Load



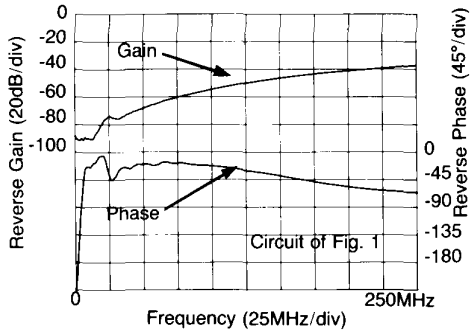
Settling Time into 500Ω Load



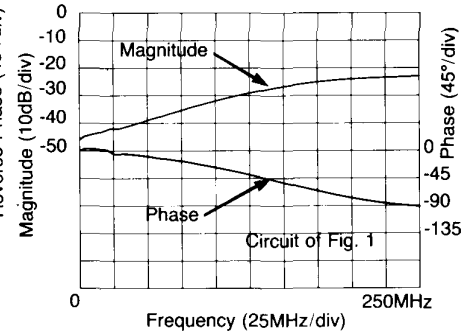
Settling Time into a 50pF Load



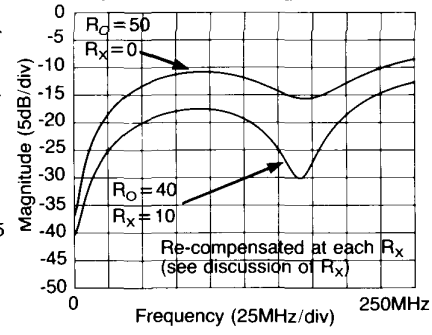
Reverse Transmission Gain and Phase (S_{12})



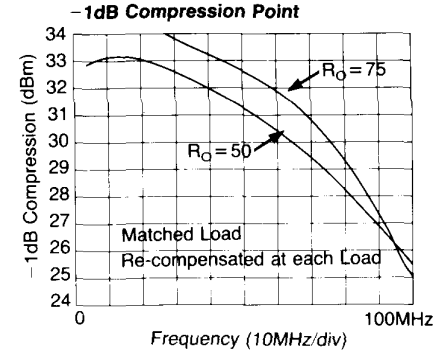
Input Return Loss (S_{11})



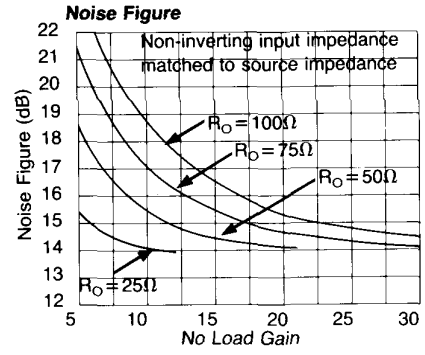
Output Return Loss (S_{22})



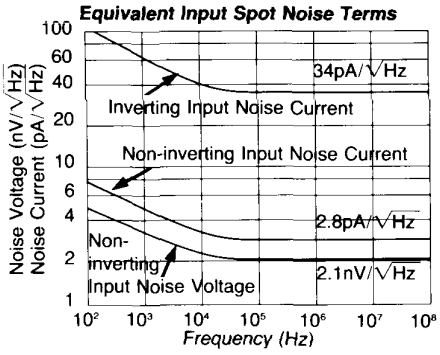
−1dB Compression Point



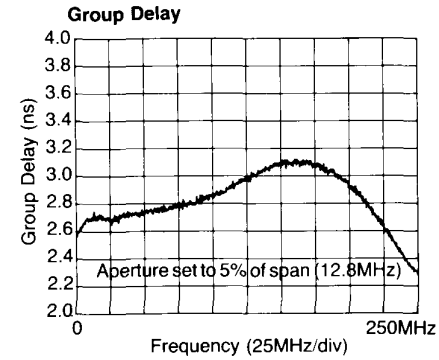
Noise Figure



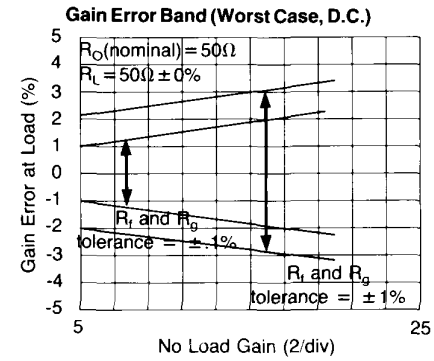
Equivalent Input Spot Noise Terms



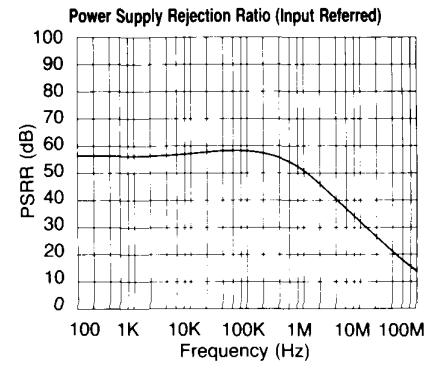
Group Delay



Gain Error Band (Worst Case, D.C.)



Power Supply Rejection Ratio (Input Referred)



SUMMARY DESIGN EQUATIONS AND DEFINITIONS

$R_f = (G + 1) R_o - A_V R_i$ — R_f – Feedback resistor from output to inverting input

$R_g = \frac{R_f - R_o}{A_v - 1}$ — R_g – Gain setting resistor from inverting input to ground

$C_x = \frac{1}{\frac{R_o}{300\left(1 - \frac{2}{R_g}\right)} - .08}$ — C_x – External compensation capacitor from output to pin 19 (in pF)

Where:

R_o – Desired equivalent output impedance
A_v – Non-inverting input to output voltage gain with no load
G – Internal current gain from inverting input to output = 10 ± 1%
R_i – Internal inverting input impedance = 14Ω ± 5%

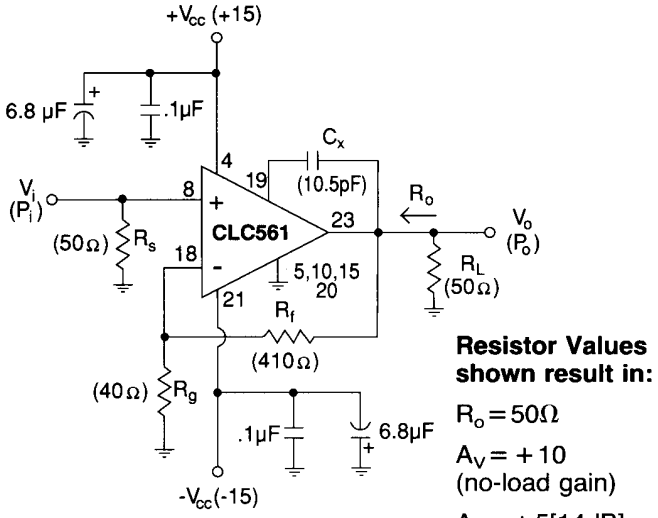
and

R_s – Non-inverting input termination resistor
R_L – Load Resistor
A_L – Voltage gain from non-inverting input to load resistor

CLC561 Description of Operation

Looking at the circuit of Figure 1 (the topology and resistor values used in setting the data sheet specifications), the CLC561 appears to bear a strong external resemblance to a classical op amp. As shown in the simplified block diagram of Figure 2, however, it differs in several key areas. Principally, the error signal is a current into the inverting input (current feedback) and the forward gain from this current to the output is relatively low, but very well controlled, current gain. The CLC561 has been intentionally designed to have a low internal gain and a current mode output in order that an equivalent output impedance can be achieved without the series matching resistor more commonly required of low output impedance op amps. Many of the benefits of a high loop gain have, however, been retained through a very careful control of the CLC561's internal characteristics.

The feedback and gain setting resistors determine both the output impedance and the gain. R_f predominately sets the output impedance (R_o), while R_g predominately determines the no load gain (A_v). Solving for the required R_f and R_g, given a desired R_o and A_v, yields the design equations shown below. Conversely, given an R_f and R_g, the performance equations show that both R_f and R_g play a part in setting R_o and A_v. Independent R_o and A_v adjustment would be possible if the inverting input impedance (R_i) were 0 but, with $R_i = 14\Omega$ as shown in the specification listing, independent gain and output impedance setting is not directly possible.



Resistor Values shown result in:

$R_o = 50\Omega$

$A_V = +10$ (no-load gain)

$A_L = +5$[14dB] (gain to 50Ω load)

Figure 1: Test Circuit

Design Equations

$R_f = (G+1) R_o - A_V R_i$

$R_g = \frac{R_f - R_o}{A_v - 1}$

Where:

G≡forward current gain (=10)
R_i≡inverting node input resistance (=14Ω)
R_o≡desired output impedance
A_v≡desired non-inverting voltage gain with no load

Performance Equations

$R_o = \frac{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}{G + 1 + \frac{R_i}{R_g}}$

$A_v = 1 + \frac{R_f}{R_g}\left[\frac{G - \frac{R_i}{R_f}}{G + 1 + \frac{R_i}{R_g}}\right]$

Simplified Circuit Description

Looking at the CLC561's simplified schematic in Figure 2, the amplifier's operation may be described. Going from the non-inverting input at pin 8 to the inverting input at pin 18, transistors Q1 - Q4 act as an open loop unity gain buffer forcing the inverting node voltage to follow the non-inverting voltage input.

Transistors Q3 and Q4 also act as a low impedance (14Ω looking into pin 18) path for the feedback error current. This current, (i_{err}), flows through those transistors into a very well defined current mirror having a gain of 10 from this error current to the output. The current mirror outputs act as the amplifier output.

The input stage bias currents are supply voltage independent. Since these set the bias level for the whole part, relatively constant performance over supply voltage is achieved. A current sense in the error current leg of the 10X current mirror feeds back to the bias current setup providing a current shutdown feature when the output current approaches 250mA.

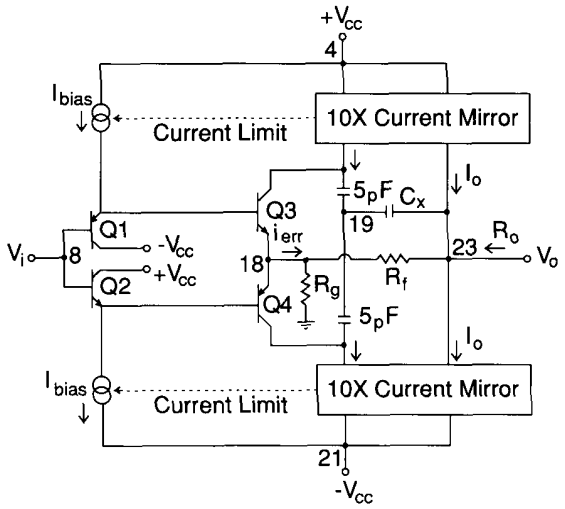
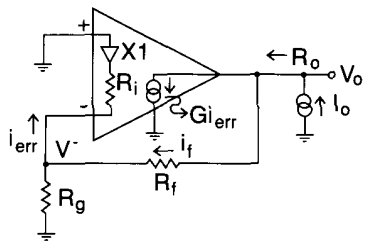


Figure 2: Simplified Circuit Diagram

Developing the Performance Equations

The CLC561 is intended to provide both a controllable voltage gain from input to output as well as a controllable output impedance. It is best to treat these two operations separately with no load in place. Then, with the no-load gain and output impedance determined, the gain to the load will simply be the no-load gain attenuated by the voltage divider formed by the load and the equivalent output impedance.

Figure 3 steps through the output impedance development using an equivalent model of Figure 2. Offering an equivalent, non-zero, output impedance into a matched load allows the CLC561 to operate at lower internal voltage swings for a given desired swing at the load. This allows higher voltage swings to be delivered at the load for a given power supply voltage at lower distortion levels than an equivalent op amp needing to generate twice the voltage swing actually desired at the matched load. This improved distortion is specified and tested over a wide range as shown in the specification listing.



Get both V_o and I_o into terms of just the error current, i_{err}, using

$V- = i_{err} R_i$ and

$$i_f = i_{err} + \frac{V-}{R_g} = i_{err}\left(1 + \frac{R_i}{R_g}\right)$$

$$V_o = V- + i_f R_f = i_{err}\left[R_i + R_f\left(1 + \frac{R_i}{R_g}\right)\right]$$

$$V_o = i_{err}\left[R_f + R_i\left(1 + \frac{R_f}{R_g}\right)\right]$$

and

$$I_o = Gi_{err} + i_f = i_{err}\left[G + 1 + \frac{R_i}{R_g}\right]$$

then

$$R_o \equiv \frac{V_o}{I_o} = \frac{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}{G + 1 + \frac{R_i}{R_g}}$$

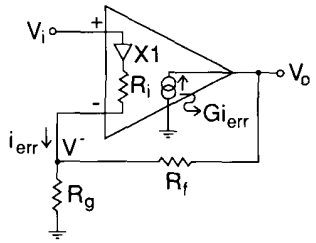
note that $R_o\Big|_{R_i=0} = \frac{R_f}{G+1}$

Figure 3: Output Impedance Derivation

Note that the R_o expression simplifies considerably if $R_i = 0$. Also note that if the forward current gain were to go to infinity, the output impedance would go to 0. This would be the normal op amp topology with a very high internal gain. **The CLC561 achieves a non-zero R_o by setting the internal forward gain to be a low, well controlled, value.**

Developing the No-Load Gain Expression

Taking the output impedance expression as one constraint setting the external resistor values, we now need to develop the no-load voltage gain expression from the non-inverting input to the output as the other constraint. Figure 4 shows the derivation of the no load gain.



No load gain

$$A_v \equiv \frac{V_o}{V_i}$$

Recognize that [taking V_i positive]

$$V_o = V^- + Gi_{err} R_f$$

Solving for V^- from two directions

$$V^- = V_i - i_{err} R_i = (G+1)\, i_{err} R_g$$

solving for i_{err} from this

$$i_{err} = \frac{V_i}{(G+1) R_g + R_i}$$

then

$$V^- = V_i - \frac{V_i R_i}{(G+1) R_g + R_i}$$

and, substituting for V^- and i_{err} in the original V_o expression

$$V_o = V_i - \frac{V_i R_i}{(G+1) R_g + R_i} + \frac{GR_f V_i}{(G+1) R_g + R_i}$$

which simplifies to

$$V_o = V_i \left[1 + \frac{GR_f - R_i}{(G+1) R_g + R_i} \right]$$

pulling an $\frac{R_f}{R_g}$ out of the fraction

$$A_v \equiv \frac{V_o}{V_i} = 1 + \frac{R_f}{R_g} \left[\frac{G - \frac{R_i}{R_f}}{G+1+\frac{R_i}{R_g}} \right]$$

note that $A_v \Big|_{R_i=0} = 1 + \frac{R_f}{R_g} \left(\frac{G}{G+1} \right)$

Figure 4: Voltage Gain Derivation

Note again that if $R_i = 0$ this expression would simplify considerably. Also, if G were very large the voltage gain expression would reduce to the familiar non-inverting op amp gain equation. These two performance equations, shown below, provide a means to derive the design equations for R_f and R_g given a desired no load gain and output impedance. The details of that derivation may be found in Application Note OA-10.

Performance Equations

$$R_o = \frac{R_f + R_i \left(1 + \frac{R_f}{R_g}\right)}{G+1+\frac{R_i}{R_g}}$$

$$A_v = 1 + \frac{R_f}{R_g} \left[\frac{G - R_i/R_f}{G+1+R_i/R_g} \right]$$

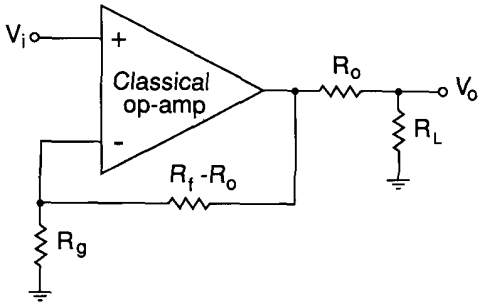
Design Equations

$$R_f = (G+1) R_o - A_v R_i$$

$$R_g = \frac{R_f - R_o}{A_v - 1}$$

Equivalent Model

Given that the physical feedback and gain setting resistors have been determined in accordance with the design equations shown above, an equivalent model may be created for the gain to the load where the amplifier block is taken as a standard op amp. Figure 5 shows this analysis model and the resulting gain equation to the load.



$$\frac{V_o}{V_i} = \left(1 + \frac{R_f - R_o}{R_g}\right) \frac{R_L}{R_L + R_o}$$

Substituting in for R_f and R_g with their design equation yields

$$\frac{V_o}{V_i} = A_v \frac{R_L}{R_L + R_o} = A_L \text{ (gain to load)}$$

Figure 5: Equivalent Model

This model is used to generate the DC error and noise performance equations. As with any equivalent model, the primary intent is to match the external *terminal characteristics recognizing that the model* distorts the internal currents and voltages. In this case, the model would incorrectly predict the output *pin voltage swing for a given swing* at the load. But it does provide a simplified means of getting to the external terminal characteristics.

External Compensation Capacitor (C_x)

As shown in the test circuit of Figure 1, the CLC561 requires an external compensation capacitor from the output to pin 19. The recommended values described here assume that a maximally flat frequency response into a matched load is desired. The required C_x varies widely with the desired value of output impedance and to a lesser degree on the desired gain. Note from *Figure 2, the simplified* internal schematic, that the actual total compensation (C_t) is the series combination of C_x and the internal *10pF from pin 19 to the compensation nodes. The* total compensation (C_t) is developed in two steps as shown below.

$$C_1 = \frac{300}{R_o} \left(1 - \frac{2.0}{R_g}\right) \text{ pF intermediate equation}$$

$$C_t = \frac{C_1}{1 + (.02)\, C_1} \text{ pF total compensation}$$

With this total value derived, the required external C_x is developed by backing out the effect of the internal 10pF. This, and an expression for the external C_x without the intermediate steps are shown below.

$$C_x = \frac{10\ C_t}{10 - C_t}$$

or

$$C_x = \frac{1}{\frac{R_o}{300\left(1-\frac{2}{R_g}\right)} - .08}\ \text{pF}$$

The plot of Figure 6 shows the required C_x vs. gain for several desired output impedances using the equations shown above. Note that for lower R_o's, C_x can get very large. But, since the total compensation is actually the series combination of C_x and 10pF, going to very high C_x's is increasingly ineffective as the total compensation is only slightly changed. This, in part, sets the lower limits on allowable R_o.

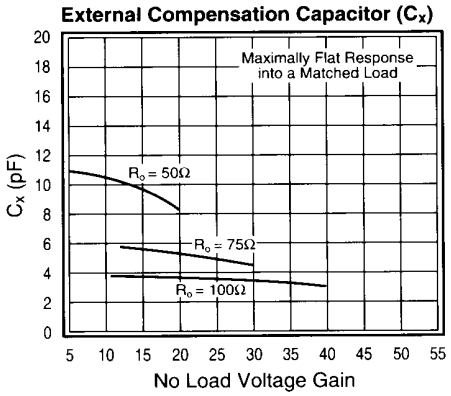


Figure 6: External Compensation Capacitance (C_x)

A 0% small signal overshoot response can be achieved by increasing C_x slightly from the maximally flat value. Note that this applies only for small signals due to slew rate effects coming into play for large, fast edge rates.

Beyond the nominal compensation values developed thus far, this external C_x provides a very flexible means for tailoring the frequency response under a wide variety of gain and loading conditions. It is oftentimes useful to use a small adjustable cap in development to determine a C_x suitable to the application, then fixing that value for production. An excellent 5pF to 20pF trimmer cap for this is a Sprague-Goodman part #GKX20000.

When the CLC561 is used to drive a capacitive load, such as an ADC or SAW device, the load will act to compensate the response along with C_x. Generally, considerably lower C_x values are required than the earlier development would indicate. This is advantageous in that a low R_o would be desired to drive a capacitive load which, without the compensating effect of load itself, would otherwise require very large C_x values.

Gain and Output Impedance Range

Figure 7 shows a plot of the recommended gain and output impedances for the CLC561. Operation outside of this region is certainly possible with some degradation in performance. Several factors contribute to set this range. At very low output impedances, the required value of feedback resistor becomes so low as to excessively load the output causing a rapid degradation in distortion. The maximum R_o was set somewhat arbitrarily at 200Ω. This allows the CLC561 to drive into a 2:1 step down transformer matching to a 50Ω load. (This offers some advantages from a distortion standpoint. See Application Note OA-10 for details.)

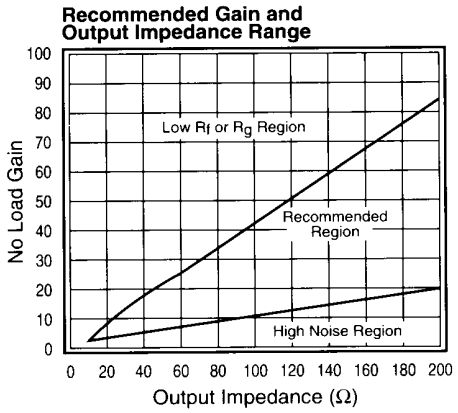


Figure 7: Recommended Gain and Output Impedance Range

For a given R_o, the minimum gain shown in Figure 7 has been set to keep the equivalent input noise voltage less than $4nV/\sqrt{Hz}$. Generally, the equivalent input noise voltage decreases with higher signal gains. The high gain limit has been set by targeting a minimum R_g of 10Ω or a minimum R_f of 100Ω.

Amplifier Configurations (Additional discussion in Application Note OA-10)

The CLC561 is intended for a fixed, non-inverting, gain configuration as shown in Figure 1. The CLC560 offers the better pulse fidelity with its improved thermal tail in the pulse response (vs. the CLC561). Due to its low internal forward gain, the inverting node **does not** present a low impedance, or virtual ground, node. Hence, in an inverting configuration, the signal's source impedance will see a finite load whose value depends on the output loading. Inverting mode operation can be best achieved using a wideband, unity gain buffer with low output impedance, such as the CLC110, to isolate the source from this varying load. A DC level can, however, be summed into the inverting node to offset the output either for offset correction or signal conditioning. Application Note OA-10 describes this and a composite amplifier structure that enhances the DC and gain accuracy characteristics of the CLC561.

Accuracy Calculations

Several factors contribute to limit the achievable CLC561 accuracy. These include the DC errors, noise effects, and the impact internal amplifier characteristics have on the signal gain. Both the output DC error and noise model may be developed using the equivalent model of Figure 5. Generally, non-inverting input errors show up at the output with the same gain as the input signal, while the inverting current errors have a gain of simply $(R_f - R_o)$ to the output voltage (neglecting the R_o to R_L attenuation).

Output DC offset:

The DC error terms shown in the specification listing along with the model of Figure 5 may be used to estimate the output DC offset voltage and drift. Each term shown in the specification listing can be of either polarity. While the equations shown below are for output offset voltage, the same equation may be used for the drift with each term replaced by its temperature drift value shown in the specification listing.

Output DC offset

$$V_{os} = \left(I_{bn} \cdot R_s \pm V_{io}\right) \cdot \left(1 + \frac{R_f - R_o}{R_g}\right) \pm I_{bi}\,(R_f - R_o)$$

Where: $I_{bn} \equiv$ non-inverting bias current
$I_{bi} \equiv$ inverting bias current
$V_{io} \equiv$ input offset voltage

An example calculation for the circuit of Figure 1 using typical 25°C DC error terms and $R_s = 25\Omega$ $R_L = 50\Omega$ yields

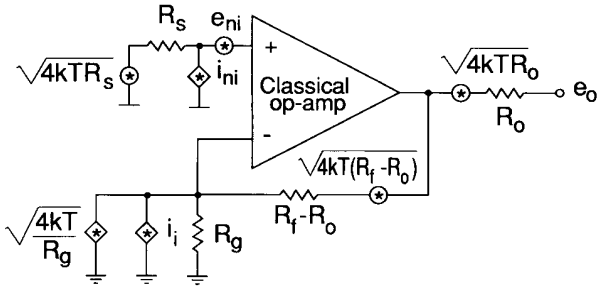
$$V_o\Big|_{DC} = [(5\mu A \cdot 25\Omega \pm 2.0mV)\,10 \pm 10\mu A(360\Omega)]\,\tfrac{1}{2} = \pm 12.4\,mV$$

(attenuation between R_o and R_L)

Recall that the source impedance, R_s, includes both the terminating and signal source impedance and that the actual DC level to the load includes the voltage divider between R_o and R_L. Also note that for the CLC561, as well as for all current feedback amplifiers, the non-inverting and inverting bias currents do not track each other in either magnitude or polarity. Hence, there is no meaning in an offset current specification, and source impedance matching to cancel bias currents is ineffective.

Noise Analysis:

Although the DC error terms are in fact random, the calculation shown above assumes they are all additive in a worst case sense. The effect of all the various noise sources are combined as a root sum of squared terms to get an overall expression for the spot noise voltage. The circuit of Figure 8 shows the equivalent circuit with all the various noise voltages and currents included along with their gains to the output.



Where:	Gain to e_o
e_{ni} – non-inverting input voltage noise	A_v
i_{ni} – non-inverting input current noise	$A_v R_s$
i_i – inverting input current noise	$R_f - R_o$
$\sqrt{4kTR_s}$ – source resistance voltage noise	A_v
$\sqrt{4kT/R_g}$ – gain setting resistor noise current	$R_f - R_o$
$\sqrt{4kT(R_f - R_o)}$ – feedback resistor voltage noise	1
$\sqrt{4kTR_o}$ – output resistor voltage noise	1

Figure 8

To get an expression for the equivalent output noise voltage, each of these noise voltage and current terms must be taken to the output through their appropriate gains and combined as the root sum of squares.

$$e_o = \sqrt{(e_{ni}^2 + (i_{ni}R_s)^2 + 4kTR_s)\,A_v^2 + i_i^2(R_f - R_o)^2 \cdots + 4kT(R_f - R_o)\,A_v + 4kTR_o}$$

Where the $4kT(R_f - R_o)A_v$ term is the combined noise power of R_g and $R_f - R_o$.

It is often more useful to show the noise as an equivalent input spot noise voltage where every term shown above is reflected to the input. This allows a direct measure of the input signal to noise ratio. This is done by dividing every term inside the radical by the signal voltage gain squared. This, and an example calculation for the circuit of Figure 1, are shown below. Note that R_L may be neglected in this calculation.

$$e_n = \sqrt{e_{ni}^2 + (i_{ni}R_s)^2 + 4kTR_s + \frac{i_i^2(R_f - R_o)^2}{A_v^2} + \cdots + \frac{4kT(R_f - R_o)}{A_v} + \frac{4kTR_o}{A_v^2}}$$

For the circuit of Figure 1, the equivalent input noise voltage may be calculated using the data sheet spot noises and $R_s = 25\Omega$, $R_L = \infty$. Recall that $4kT = 16E{-}21J$. All terms cast as $(nV/\sqrt{Hz})^2$

$$e_n = \sqrt{(2.1)^2 + (.07)^2 + (.632)^2 + (1.22)^2 + (.759)^2 + (.089)^2}$$

$$= 2.62nV/\sqrt{Hz}$$

Gain Accuracy (DC):
A classical op amp's gain accuracy is principally set by the accuracy of the external resistors. The CLC561 also depends on the internal characteristics of the forward current gain and inverting input impedance. The performance equations for A_v and R_o along with the Thevinin model of Figure 5 are the most direct way of assessing the absolute gain accuracy. Note that internal temperature drifts will decrease the absolute gain slightly as the part warms up. Also note that the parameter tolerances affect both the signal gain and output impedance. The gain tolerance to the load must include both of these effects as well as any variation in the load. The impact of each parameter shown in the performance equations on the gain to the load (A_L) is shown below.

Increasing current gain G	Increases A_L
Increasing inverting input R_i	Decreases A_L
Increasing R_f	Increases A_L
Increasing R_g	Decreases A_L

Applications Suggestions

Driving a capacitive load:
The CLC561 is particularly suitable for driving a capacitive load. Unlike a classical op amp (with an inductive output impedance), the CLC561's output impedance, while starting out real at the programmed value, goes somewhat capacitive at higher frequencies. This yields a very stable performance driving a capacitive load. The overall response is limited by the (1/RC) bandwidth set by the CLC561's output impedance and the load capacitance. It is therefore advantageous to set a low R_o with the constraint that extremely low R_f values will degrade the distortion performance. $R_o = 25\Omega$ was selected for the data sheet plots. Note from distortion plots into a capacitive load that the CLC561 achieves better than 60dBc THD (10 bits) driving $2V_{pp}$ into a 50pF load through 30MHz.

Improving the output impedance match vs. frequency – Using R_x:
Using the loop gain to provide a non-zero output impedance provides a very good impedance match at low frequencies. As shown on the Output Return Loss plot, however, this match degrades at higher frequency. Adding a small external resistor in series with the output, R_x, as part of the output impedance (and adjusting the programmed R_o accordingly) provides a much better match over frequency. Figure 9 shows this approach.

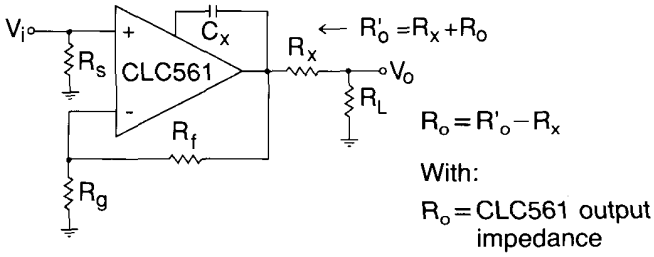


Figure 9

Increasing R_x will decrease the achievable voltage swing at the load. A minimum R_x should be used consistent with the desired output match. As discussed in the thermal analysis discussion, R_x is also very useful in limiting the internal power under an output shorted condition.

Interpreting the Slew Rate:
The slew rate shown in the data sheet applies to the voltage swing at the load for the circuit of Figure 1. Twice this value would be required of a low output impedance amplifier using an external matching resistor to achieve the same slew rate at the load.

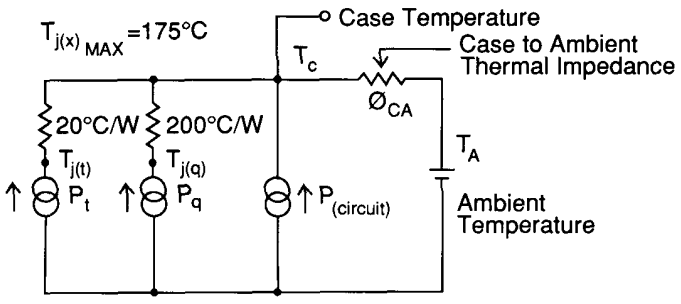
Layout Suggestions:
The fastest fine scale pulse response settling requires careful attention to the power supply de-coupling. Generally, the larger electrolytic capacitor ground connections should be as near the load ground (or cable shield connection) as is reasonable, while the higher frequency ceramic de-coupling caps should be as near the CLC561's supply pins as possible to a low inductance ground plane.

Evaluation Boards and Encased Versions:
An evaluation board (showing a good high frequency layout) for the CLC561 is available. This board may be ordered as part #730019. In addition, encased versions of the CLC561 are also available. These are modular amplifiers similar to Comlinear's other E-series parts.

Thermal Analysis and Protection

A thermal analysis of a chip and wire hybrid is directed at determining the maximum junction temperature of all the internal transistors. From the total internal power dissipation, a case temperature may be developed using the ambient temperature and the case to ambient thermal impedance. Then, each of the dominant power dissipating paths are considered to determine which has the maximum rise above case temperature.

The thermal model and analysis steps are shown below. As is typical, the model is cast as an electrical model where the temperatures are voltages, the power dissipators are current sources, and the thermal impedances are resistances. Refer to the summary design equations and Figure 1 for a description of terms.



$I_o = V_o/R_{eq}$ total output current

with $R_{eq} = R_L \parallel \left[\frac{R_f A_L}{A_L - 1}\right]$ total load

$I_t = \frac{1}{2}(I_o + \sqrt{I_o^2 + (.06)^2}$ total internal output stage current

$P_t = I_t \cdot (V_{cc} - V_o - .7 - 15.3\Omega \cdot I_t)$ output stage power

$P_q = .2 \cdot I_t \cdot (V_{cc} - 1.4 - 17.3\Omega \cdot I_t)$
power in hottest internal junction prior to output stage

$P_{circuit} = 1.3 \cdot V_{cc} \cdot (2 \cdot I_t - I_o + 19.2mA) - P_t - P_q$
power in remainder of circuit [note $V_{cc} = |-V_{cc}|$]

Note that the P_t and P_q equations are written for positive V_o. Absolute values of $-V_{cc}$, V_o, and I_o should be used for a negative going V_o since we are only interested in delta V's. For bipolar swings, the two powers for each output polarity are developed as shown above then ratioed by the duty cycle. Having the total internal power, as well as its component parts, the maximum junction temperature may be computed as follows.

$T_c = T_A + (P_q + P_T + P_{circuit}) \cdot \emptyset_{CA}$ Case Temperature

$\emptyset_{CA} = 35°C/W$ for the CLC561 with no heatsink in still air

$T_j(t) = T_c + P_t \cdot 20°C/W$
output transistor junction temperature

$T_j(q) = T_c + P_q \cdot 200°C/W$
hottest internal junction temperature

The Limiting Factor for Output Power is Maximum Junction Temperature

Reducing θ_{ca} through either heatsinking and/or airflow can greatly reduce the junction temperatures. One effective means of heatsinking the CLC561 is to use a thermally conductive pad under the part from the package bottom to a top surface ground plane on the component side. Tests have shown a θ_{ca} of 24°C/W in still air using a "Sil-Pad" available from Bergquist (800-347-4572) as Comlinear part #550006.

As an example of calculating the maximum internal junction temperatures, consider the circuit of Figure 1 driving ±2.5V, 50% duty cycle, square wave into a 50Ω load.

$R_{eq} = 50\Omega \parallel \left[\frac{410\Omega \cdot 5}{5-1}\right] = 45.6\Omega$

$I_o = 2.5V/(45.6\Omega) = 54.9mA$

$I_T = \frac{1}{2}(54.9mA + \sqrt{(54.9mA)^2 + (.06)^2}) = 68.1mA$

$P_T = 68.1mA[15 - 2.5 - .7 - 15.3\Omega \cdot 68.1mA] = 733mW$
total power in both sides of the output stage

$P_q = .2 \cdot 68.1mA[15 - 1.4 - 17.3\Omega \cdot 68.1mA] = 169mW$
total power in both sides of hottest junctions prior to output stage

$P_{circuit} = 1.3 \cdot (15) \cdot [2 \cdot 68.1mA - 54.9mA + 19.2mA] - 733mW - 169mW = 1.058W$
power in the remainder of circuit

With these powers and $T_A = 25°C$ and $\emptyset_{ca} = 35°C/W$

$T_c = 25°C + (.733 + .169 + 1.058) \cdot 35 = 94°C$
case temperature

From this, the hottest internal junctions may be found as

$T_j(t) = 94°C + \frac{1}{2}(.733) \cdot 20 = 101°C$ output stage

$T_j(q) = 94°C + \frac{1}{2}(.169) \cdot 200 = 111°C$
hottest internal junction

Note that ½ of the total P_T and P_q powers were used here since the 50% duty cycle output splits the power evenly between the two halves of the circuit whereas the total powers were used to get case temperature.

Even with the output current internally limited to 250mA, the CLC561's short circuiting capability is principally a thermal issue. Generally, the CLC561 can survive short duration shorts to ground without any special effort. For protection against shorts to the ±15 volt supply voltages, it is very useful to reduce some of the voltage across the output stage transistors by using some external output resistance, R_x, as shown in Figure 9. Application Note OA-10 discusses this in detail.

Evaluation Board

An evaluation board (part number 730019) for the CLC561 is available.

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