Introduction

This purpose of this application note in conjunction with the VSC8201 Datasheet is to provide information to assist in the design and lay-out of the VSC8201 Gigabit Ethernet Transceiver.

Power Supply Organization and Decoupling

The VSC8201 requires a 3.3v and a 1.5v power supply source for operation using GMII, MII or TBI MAC interfaces. In RGMII and RTBI modes, an additional 2.5v supply is needed as specified by the RGMI/RTBI standard. The VSC8201 can be powered using the following options:

- 2 separate supplies, 3.3v and 1.5v respectively.
- A single 3.3v supply. This is done by using the optional on-chip regulator control circuit, which drives a simple external series pass type supply regulator (MOSFET) to generate the 1.5v core power supply.

PCB Power Plane Organization

It is recommended that the PCB power plane(s) in a system be divided into four separate regions:

Table 1: Power Supply Plane Regions

PCB Power Plane	*Description*	Nominal Supply Voltage	Current[a]		LQFP Supply Names[b]
			Typ	Max	
V+IO	Digital Input/Output buffer supply	3.3v/2.5v	8mA	11mA	VDDIO
V+A33	Filtered analog 3.3v supply	3.3v	101mA	111mA	TXVDD, VDDREC33, VDDPLL33
V+A15	Filtered analog 1.5v supply	1.5v	41mA	48mA	VDDREC15, VDDPLL15
V+DIG	Digital core supply	1.5v	350mA	423mA	VDDDIG

a. Test conditions: Room temperature (25^{o}C), 1000BASE-T data, full duplex, minimum IPG, 64-byte packets, RGMII MAC active, excluding regulator power dissipation but including external twisted pair termination; all worst case current figures have all nominal power supplies scaled by +5%.
b. Refer VSC8201 Datasheet to correlate supply names with part pin numbers.

Power Supply Filtering and Decoupling

For best performance, each power supply region should contain capacitors for both bulk decoupling and for local high-frequency decoupling. This is summarized in the following tables:

Table 2: Power Supply Decoupling for separate 3.3v and 1.5v Power Supplies

PCB Power Plane	Bulk Decoupling required	Local Decoupling Required
V+IO	1 pair of 22uF, 1uF	Four 0.1uF capacitors
V+A33	1 pair of 22uF, 1uF and 1 10uF	Two 0.1 uF capacitors
V+A15	1 pair of 2.2uF, 1uF	One 0.1 uF capacitor
V+DIG	1 pair of 22uF, 1uF	Four 0.1uF capacitors

Table 3: Power Supply Decoupling for single 3.3v Supply and Optional fixed 1.5v Regulator

PCB Power Plane	Bulk Decoupling required	Local Decoupling Required
V+IO	1 pair of 22uF, 1uF	Four 0.1uF capacitors
V+A33	1 pair of 22uF, 1uF and 1 10 uF	Two 0.1uF capacitors
V+A15	1 pair of 2.2uF, 1uF	One 0.1 uF capacitor
V+DIG	2.2uF	Four 0.1uF capacitors

The following figure shows the proposed layout for the local decoupling capacitors. The figure is approximately drawn to scale for standard 0603 size capacitors. Vias to the power and ground planes immediately in the vicinity of the capacitors provide a low inductive path and aid in heat dissipation.

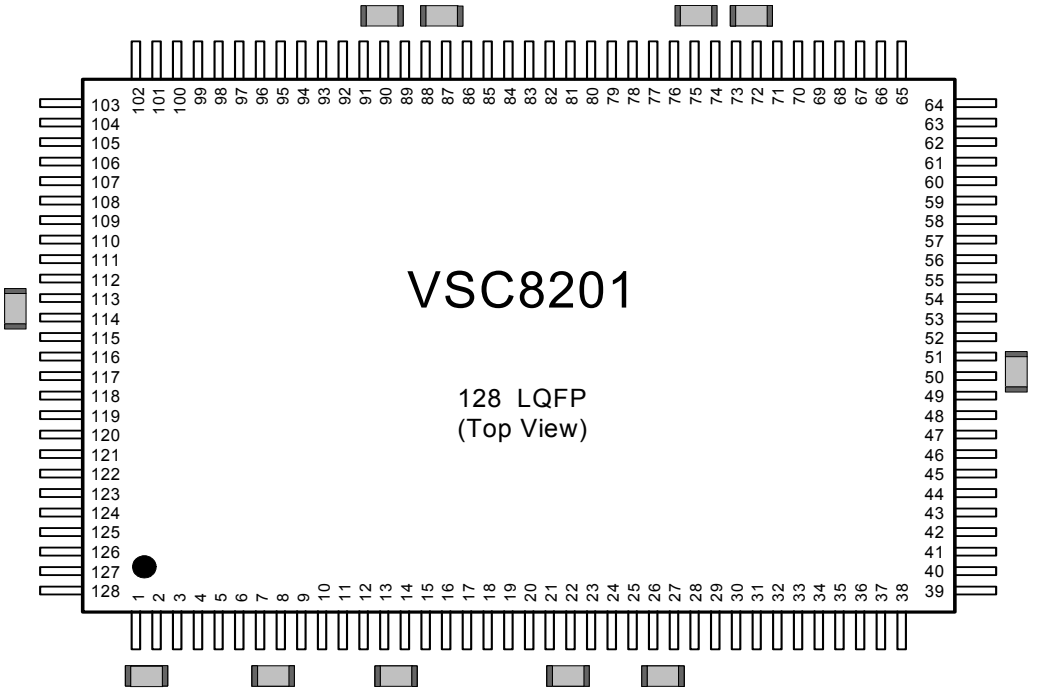


Figure 1: Local High-Frequency decoupling Capacitor Layout - LQFP package

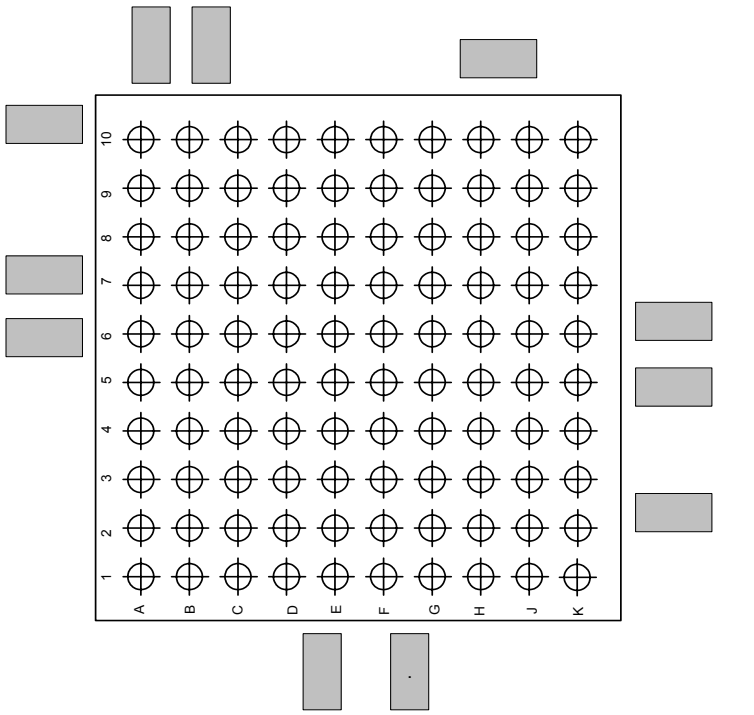


Figure 2: Local High-Frequency decoupling Capacitor Layout - LBGA package

In addition, a ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and the local decoupling capacitors.

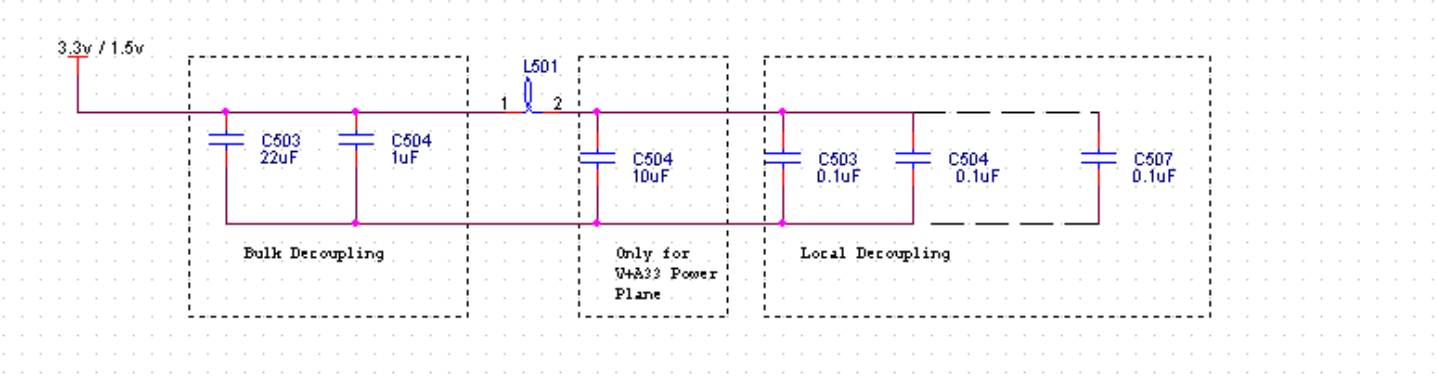


Figure 3: Power Supply Decoupling Schematic

The beads should be chosen to have the following characteristics:

- Current Rating of at least 150% of the maximum current of the power supply.
- Impedance of 80 to 100W at 100Mhz.

Recommended beads are:

- Panasonic EXCELSA39 or similar.
- Steward HI 1206N101R-00 or similar.

Since all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. For this reason, it is recommended that system designers provide and option to replace the ferrite beads with zero-ohm resistors, once thorough evaluation of system performance is completed.

PCB Chassis ground Region

To isolate the board from the ESD events and to provide a common-mode noise ground path, a separate chassis ground region should be allocated. This should provide an electrical connection to the external chassis and the shield ground to discharge common-mode noise through a 75-ohm resistor and a single 1000pF 2kV capacitor. See “VSC8201 System Schematic” in the datasheet.

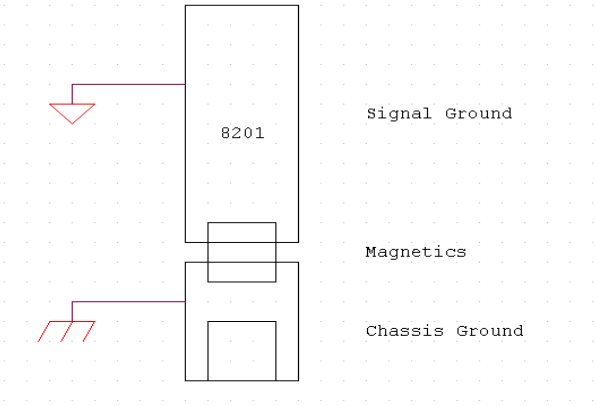


Figure 4: Ground Plane Layout

Key points

- The chassis ground and the PCB ground should have as much separation as possible. 45 mils or greater is recommended.
- There should be no power or ground plane beneath the primary and secondary coils of the transformer.

Regulator Circuit

For systems with a single power supply, the VSC8201 provides an option to generate the 1.5v supply from the 3.3v supply by using the on chip regulator. The internal regulator is enabled by having a 10k pull-up on the REG_EN pin.

To use the Regulator the following additional components are required:

- FET device, similar to Fairchild FDT439N.
- For decoupling, two 0.0047uF capacitors with 10% tolerance or better. NPO, X7R or X5R are all acceptable.

Systems with single 3.3v,+/-10% Wake on LAN supply

The following figure shows the circuit for generating the 1.5v supply using a 3.3v,+/-10% supply

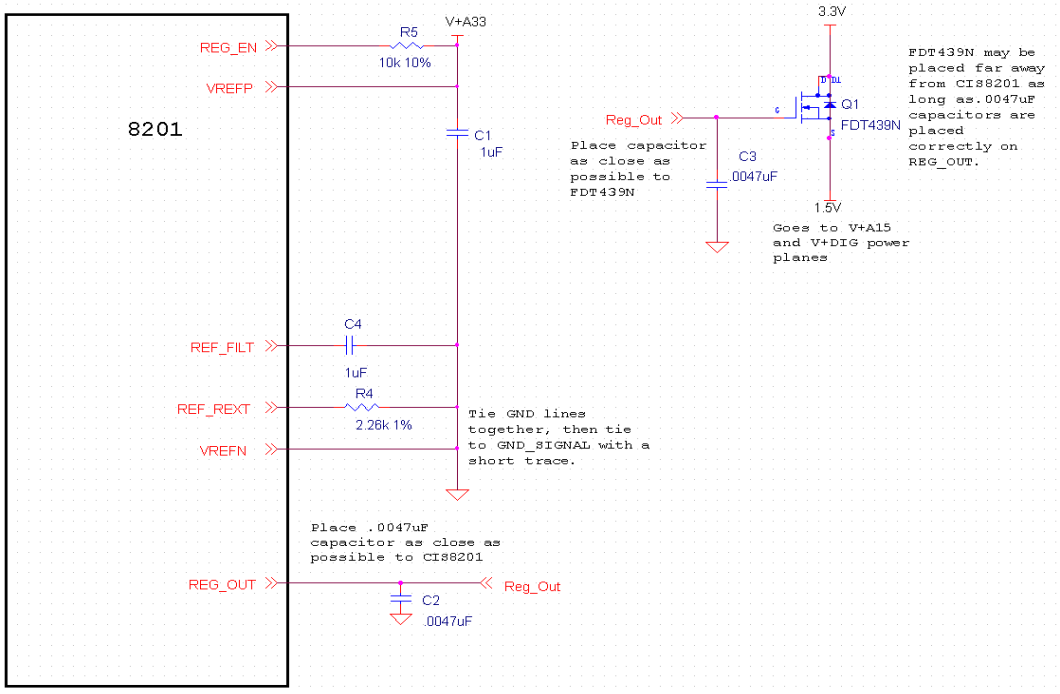


Figure 5: Regulator Circuit using 3.3v, +/-10% supply

Key points

- Place a 0.0047uF capacitor as close to REG_OUT as possible.
- Place a 0.0047uF capacitor as close to the FET as possible.
- Tie the GND line together with VREFN, capacitor connected to REF_FILT, resistor R4 (See figure above) and then connect to a common ground.
- VREFP should be connected to the analog 3.3v plane i.e. V+A33.

Using ActiPHY™ Power Management

The VSC8201 supports a new power saving mode called ActiPHY™, particularly suited to power saving applications like laptop computers with wake on LAN capability.[1]

When in ActiPHY™ mode the PHY is in one of two power down states and has the ability to detect valid signal energy levels at the media pins and convey it to the station manager.

1. Refer VSC8201 Datasheet.

The following tasks are required to be done by the station manager to use the power saving ActiPHY™ feature:

1. Setting the squelch level:
   As per IEEE standard 802.3 MII register 22:11 and 22:10 set the squelch levels for 10Base-T operation. In addition to the 10BASE-T squelch level control, the VSC8201 uses these bits to control the ActiPHY™ squelch levels. This is summarized in the following table:

Table 4: 10BASE-T/ActiPHY™ squelch levels

Register Bit Setting 22:11:10	10BASE-T/ActiPHY™ squelch level
00	Normal Squelch
01	Low squelch
10	High squelch
11	Reserved

2. Enabling the interrupt pin:
   The VSC8201 conveys the valid signal detect signal via the MDINT# pin. In order to enable the MDINT# pin the station manager must set the MII register 25:15.

3. Enabling the ActiPHY™ signal detect interrupt:
   In ActiPHY™ mode MII register 25:13 i.e. the link state-change interrupt mask also acts as the ActiPHY™ signal detect interrupt mask. This bit should be set to enable the ActiPHY™ signal detect interrupt. When a valid signal level is detected an interrupt occurs and register 26:13 is set by the VSC8201 PHY. The MDINT# pin is pulled low.

4. Setting the PHY in ActiPHY™ mode:
   The station manager can put the VSC8201 in ActiPHY™ mode by setting MII register 23:5. On setting register 23:5 the PHY goes in one of the following power down states depending upon the state of the MII register 18:0

Table 5:

Register Bit Setting 18:0	Power down state	Power dissipation[a]
0	PLL disabled - 125MHz clock not available on CLK125 pin	
1	PLL enabled - 125MHz clock available on CLK125 pin	

a. Power dissipation figures are currently unavailable.

5. Coming out of ActiPHY™ mode:
   The station manager responds to the interrupt signal by clearing the ActiPHY™ enable bit i.e. clears the register 23:5. When this bit is cleared, all blocks of the PHY are powered up and the PHY reverts back to auto-negotiation and tries to establish a link. The station manager should read MII register 26 to reset the interrupt status register.

Design for Signal Integrity

Many high speed signal pins on the VSC8201 have rise/fall times of the order of 0.7 to 2.4 ns. Because of these fast rise/fall times, interconnects should be treated as transmission lines rather than simple lumped element connections. Use of transmission lines with a basic understanding of line matching will reduce signal reflections which degrades overall performance of the part.

Theory

In order to apply correct impedance matching/termination techniques it is important to know about the types of interconnects used on the PC board. There are 2 kinds of traces on a PC Board.

- In case the signal transmission line is sandwiched between the dielectric material of the board and 2 conducting planes it is called a stripline.

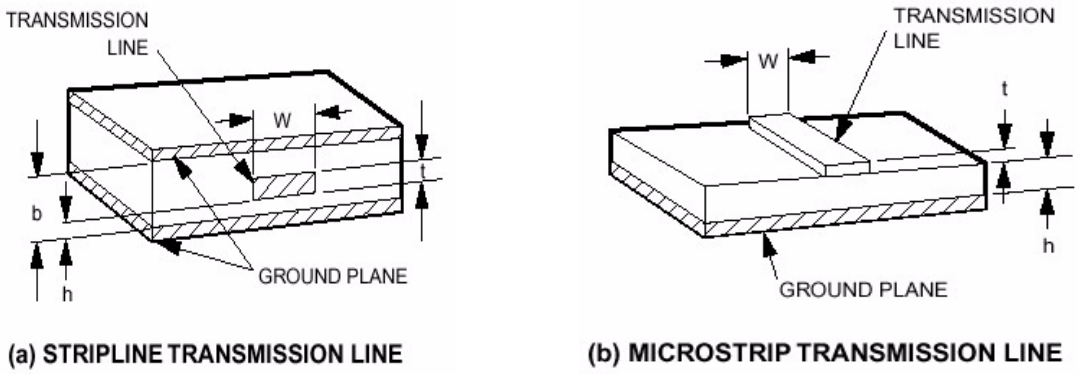


Figure 6: Transmission Lines

- A signal transmission line that has one side open to air and dielectric material and a conducting plane beneath it, is called a microstrip.

Impedance of a transmission line is determined by the relative dielectric constant ε_r of the PC board material, thickness of the dielectric h ,the width w and the thickness of the transmission line t .

Characteristic impedance of the microstrip is calculated using the approximation:

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \cdot \ln\left[\frac{5.98 \cdot h}{0.8w + t}\right] \Omega$$

The propagation delay for the microstrip is:

$$t_{pd} = (85) \cdot \sqrt{0.475\varepsilon_r + 0.67} \text{ ps/ft}$$

Characteristic impedance of the stripline is calculated using the equation:

$$Z_o = \frac{60}{\sqrt{\varepsilon_r}} \cdot \ln\left[\frac{4 \cdot b}{0.67\pi(0.8w + t)}\right] \Omega$$

where b is the distance between the planes above and below the stripline. The above formula is used when the stripline is equidistant from the above and below planes.

The propagation delay of the strip line is:

$$t_{pd} = (85) \cdot \sqrt{\varepsilon_r} \text{ ps/in}$$

If the length of the line L such that:

$$L(in) < \frac{Rise - time(ps)}{Propagation - delay\left(\frac{ps}{inch}\right)} \times \frac{1}{6}$$

Then the line must be considered a transmission line and proper termination techniques be employed.

Assuming a dielectric constant of 4.4 for FR-4, we get t_{pd}=141ps for a microstrip line. If the rise time of the signal is 0.7ns then a trace with length L greater the 0.827 inch should be considered a transmission line.

The 2 most common termination techniques are as follows:

- Place a resistor equal to the characteristic impedance of the line in series with and close to the signal source. This is called series termination or source termination.
- Place a resistor equal to the characteristic impedance of the line between ground and the end of the signal trace. This is called end termination.

The common value for the characteristic impedance of a transmission line is 50Ω.

High Speed signals of VSC8201

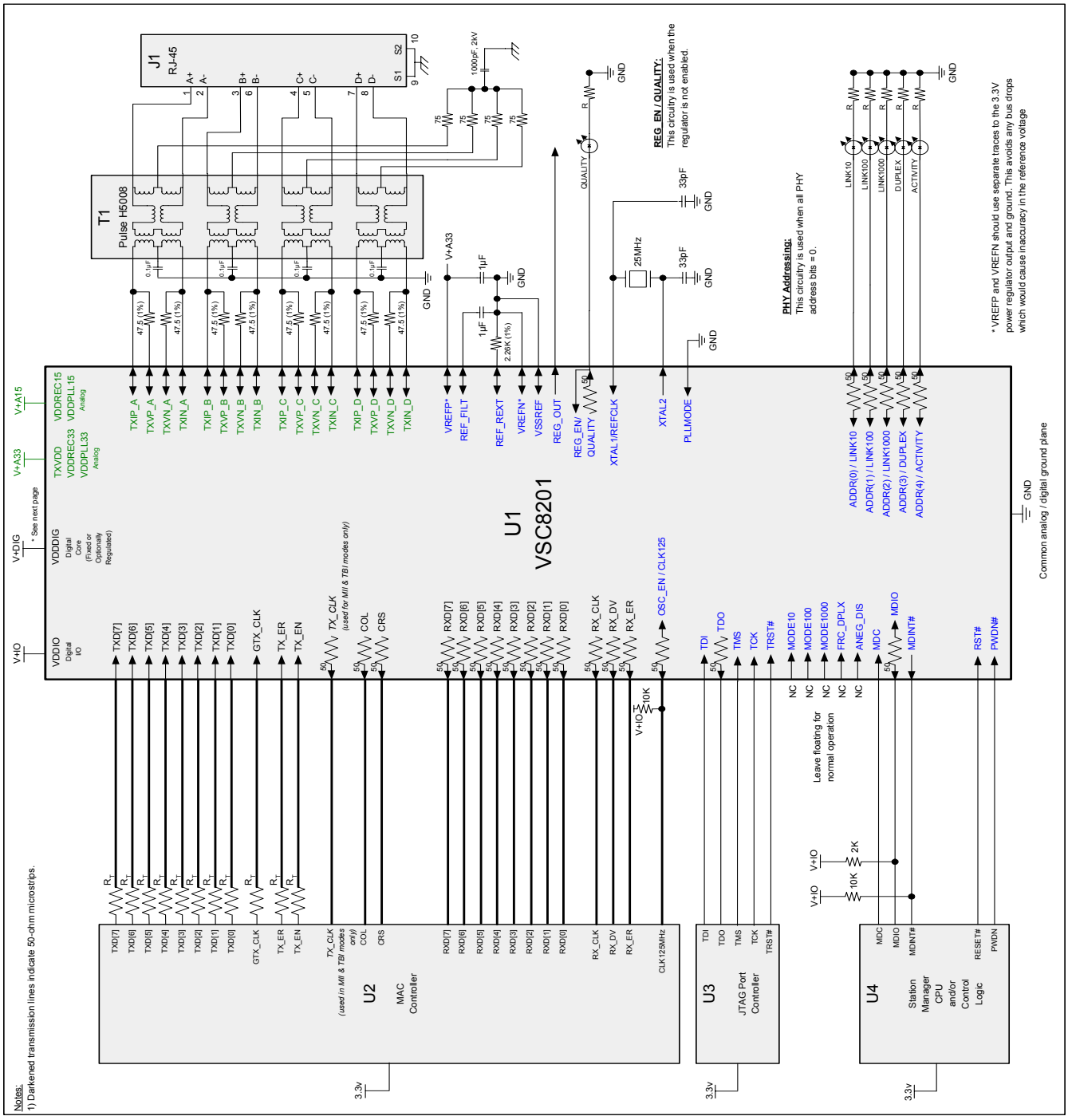


Figure 7: VSC8201 System Schematic

MAC Transmit and Receive Interface Pins

These signals on these pins have rise/fall times of about 0.7 to 1 ns. To adequately accommodate these signals on a PCB, it is recommended that the traces be designed as either a microstrip or stripline transmission lines with a characteristic impedance of 50Ω. It is also important that an unbroken ground plane exist above and/or below these signals.

For the MAC transmit interface, if the output resistance of the corresponding pins on the MAC side is less than 50Ω, additional series termination resistor should be placed close to the MAC device.

For the VSC8201 MAC receive interface, each pin is self-calibrating to an output resistance of 50Ω. Thus, external series termination resistors are not required as long as the characteristic impedance of the trace is 50Ω.

As shown in the previous section, for a rise time of 0.7 ns, the minimum length of a microstrip for it to be considered a transmission line is 0.827 inches (for standard FR4 material with dielectric constant of 4.4). Hence above mentioned series termination considerations are important only if the microstrip length is greater than 0.827 inches.

For most cases the MAC can be placed close to the PHY's MAC interface pins.

Twisted-Pair Interface pins

As the interface to external CAT-5 cable, these pins are organized in four differential pairs for each port.These are labelled "TXIP_x" and "TXIN_x", where 'x' is the particular pair within a single cable. When routing these pairs on a PCB, they must be routed using transmission lines with a characteristic impedance of 50Ω, and the traces for each differential pair must be routed symmetrically as close to each other as possible. By keeping the differential pairs together on the board, the result is the required 100-ohm differential impedance for each twisted pair.

Other Impedance Controlled pins

The following signals have 50 ohm integrated series termination resistors and therefore should be routed using 50Ω transmission lines:

- ADDR(0)/LINK10
- ADDR(1)/LINK100
- ADDR(2)/LINK1000
- ADDR(3)/DUPLEX
- ADDR(4)/ACTIVITY
- MODE10
- MODE100
- MODE1000
- TDO
- OSC_EN/CLK125
- REG_EN/QUALITY
- MDIO

Other Board Layout Considerations

- Place the RJ-45, transformer and the PHY device as close as possible to each other.
- All traces that run from the transformer to the RJ-45 should be matched in length and be as short as possible.
- Keep a continuous ground plane underneath the high speed MAC Tx/Rx data signal traces. These traces should be of equal length and be as short as possible.

Special RGMII Implementation Using a Single 3.3V Supply

This section addresses designers who wish to use the VSC8201 Single Port Gigabit Ethernet PHY in RGMII interface mode at an interface voltage of 3.3V, rather than the standard[1] 2.5V.

VSC8201's RGMII Interface Description

The VSC8201 PHY is designed, as per the RGMII version 1.2a specification, to support RGMII operation at a 2.5v I/O supply. In addition to the RGMII requirements specified by the standard, the PHY also has an internal clock delay feature (enabled by setting MII Register 23.8) that adds an internal delay of ~2ns to the RXC and the TXC signals when operating at 2.5v. This feature eliminates the need for PCB trace delays or 2ns buffers in the path of the RXC and TXC traces.

Due to customer interest in using the VSC8201 PHY in RGMII interface mode with a single 3.3v supply, Vitesse has characterized the RGMII I/O timing of the PHY under this condition in the following two configurations:

- Standard RGMII Implementation (i.e. with RXC and TXC trace delays on the PCB)
- RGMII Implementation using the Internal Clock Delay feature.

Since the VSC8201 PHY was not specifically designed for RGMII operation with a 3.3v I/O supply, certain accommodations must be made to the board layout in order to ensure a robust interface. The VSC8201 PHY complies with the I/O timing requirements specified in the RGMII version 1.2a specification. No special board layout considerations other than those mentioned in the standard are required for this implementation.

RGMII Implementation using the Internal Clock Delay feature with 3.3v I/O Supply

With a 3.3v I/O supply, the worst case internal delay added to the TXC signal is around 3ns. If the TXC, TD[3:0], and TX_CTL traces are length matched on the PCB, then the PHY may mis-latch data under the worst case TXC delay conditions, resulting in packet errors at the MAC/PHY transmit interface. Due to this it is important to follow the guidelines mentioned in the section below during board layout.

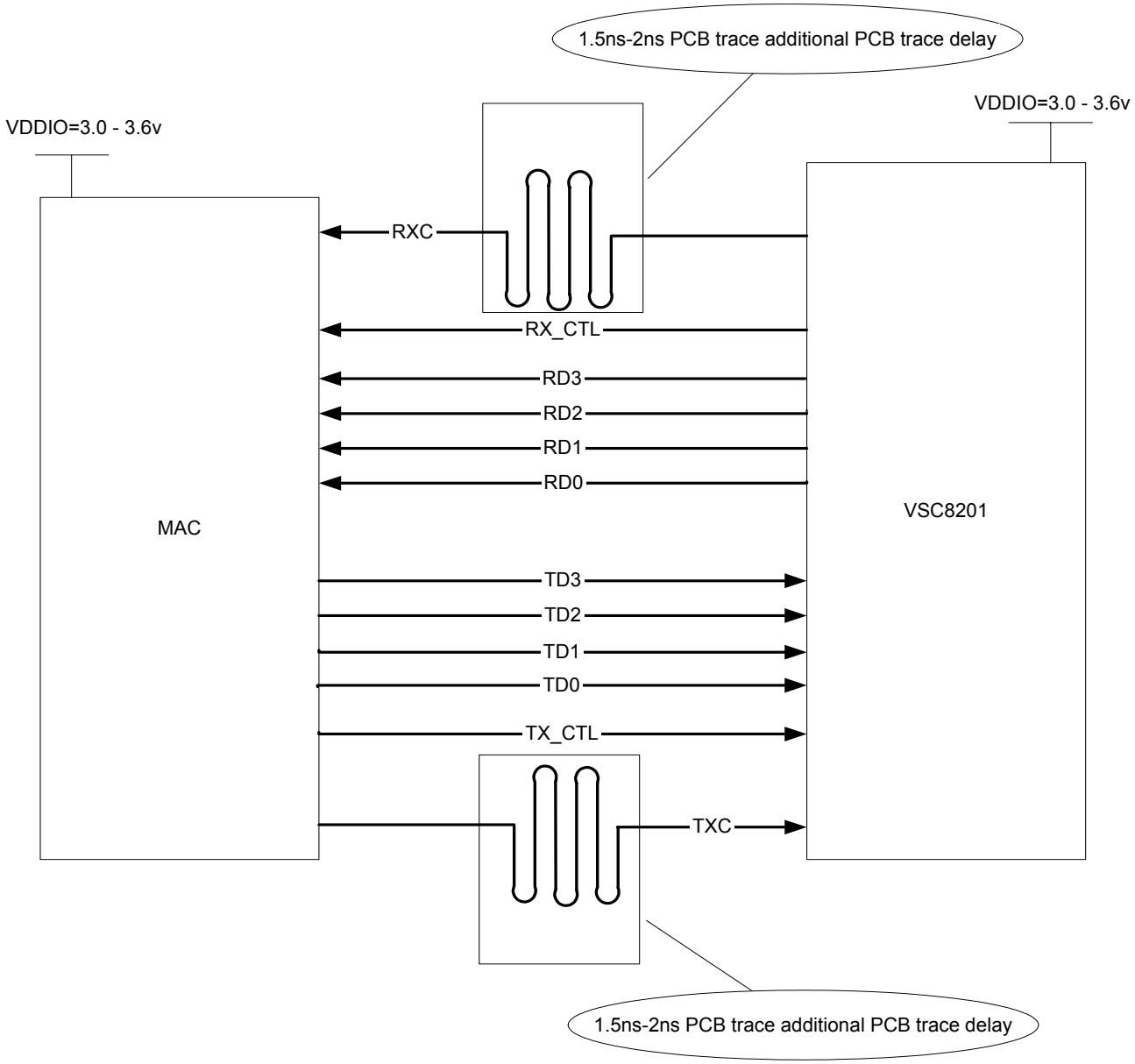
1. RGMII Version 1.2a

RGMII Single 3.3v Supply Implementation Methods

Method I - Standard RGMII Implementation

In this mode the Internal Clock Delay feature of the PHY is not enabled. See MII Register 23.8 for more information.

Board Layout



Benefits

- Does not require an external 2.5v supply, thereby reducing overall system cost.

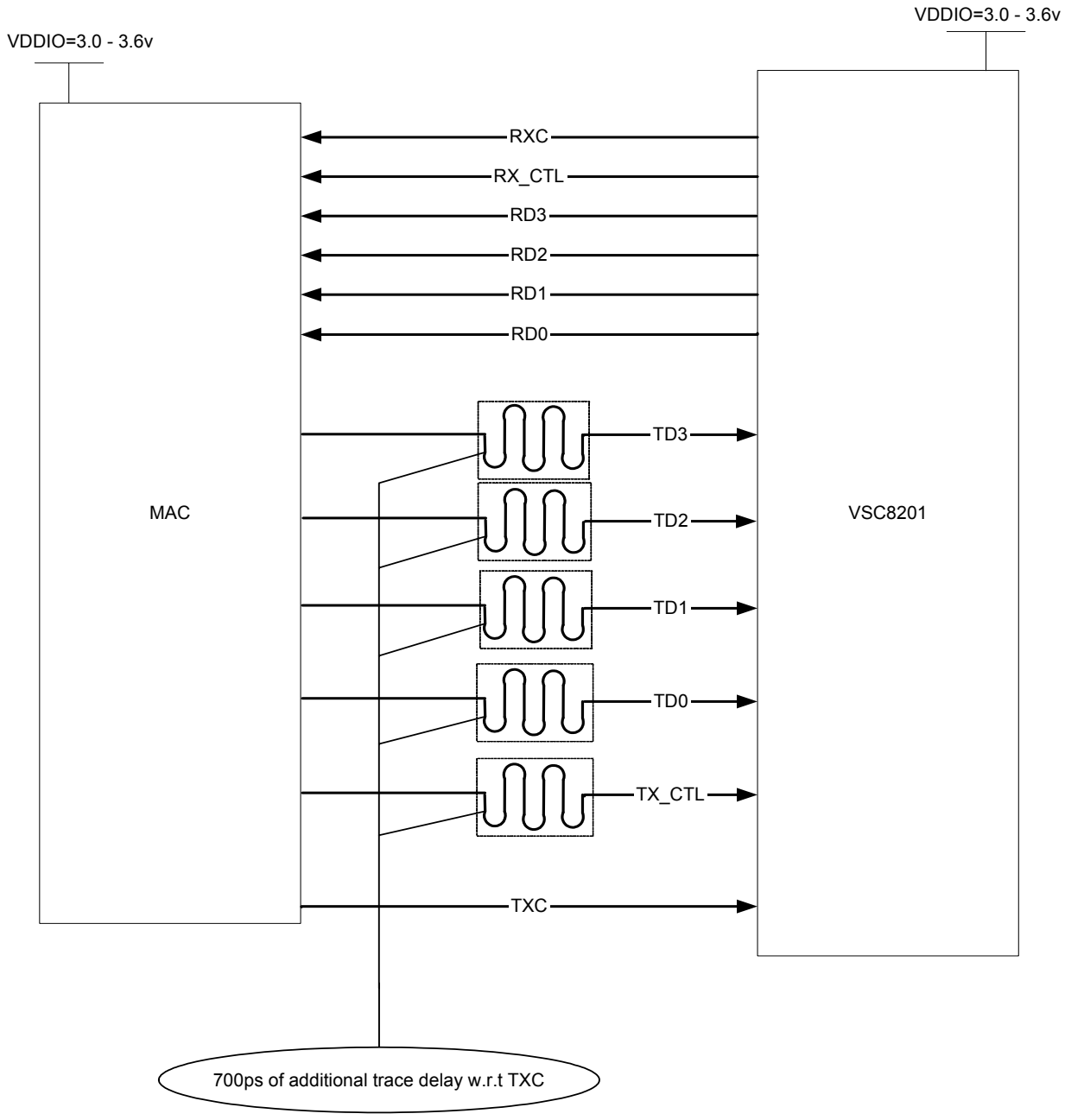
Drawbacks

- Needs extra board space for the additional trace delays on the RXC and TXC traces.

Method II - RGMII Implementation Using the Internal Clock Delay Feature

In this mode the internal clock delay feature is used i.e. MII Register bit 23.8 is set.

Board Layout



Benefits

- Does not require an external 2.5v supply, thereby reducing system cost.
- Does not require any additional delays on the TXC and RXC traces.

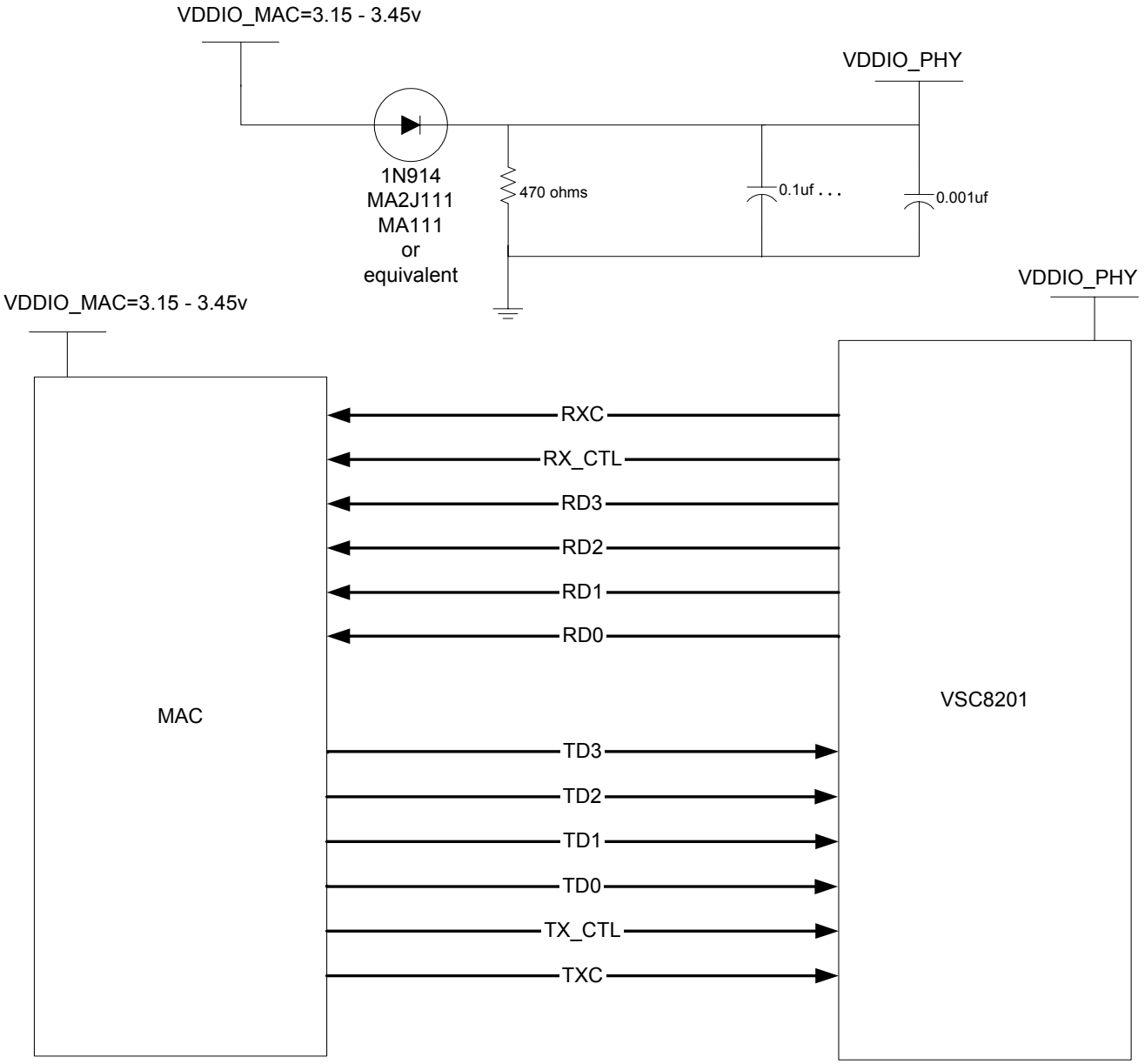
Drawbacks

- Needs extra board space for the additional trace delays needed on the TD[3:0] and the TX_CTL traces.

Method III - RGMII Implementation Using the Internal Clock Delay Feature with Locally Generated 2.5v I/O Supply

In this mode the internal clock delay feature is used i.e. MII Register Bit 23.8 is set.

Board Layout



Benefits

- Does not require an external 2.5v supply, thereby reducing system cost.
- Does not require any additional delays on the TXC and RXC traces.

Drawbacks

- Requires a diode and a resistor.
- The MAC which is at 3.3V should be capable of detecting 2.5V logic levels.

LED/ADDRESS Circuit

The following pins of the VSC8201 are input/output pins:

- ADDR(4)/ACTIVITY
- ADDR(3)/DUPLEX
- ADDR(2)/LINK1000
- ADDR(1)/LINK100
- ADDR(0)/LINK10
- REG_EN/QUALITY

In input mode these pins are sampled on the rising edge of RST# signal. After reset these are in output mode.The ADDR and REG_EN pins sampled at startup determine the polarity of the LED output signal.

The QUALITY LED is asserted when the signal quality is good.

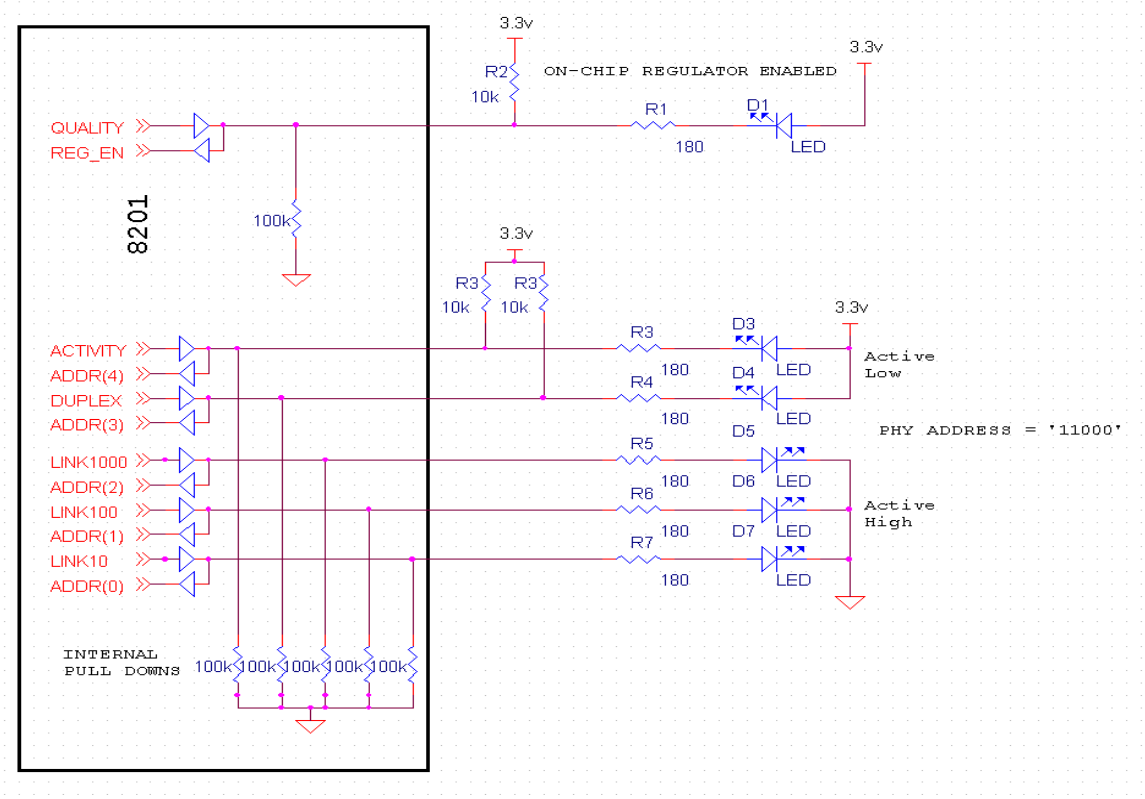


Figure 8: LED Interface Circuit

Serial Management Interface

The VSC8201 contains a standard Serial Management Interface (SMI) as defined by IEEE standards. This interface consists of the following signals:

Table 6: Serial Management Interface Pins

Signal Name	Type	Description
MDC	Input	**Management Data Clock.** A 0 to 25MHz reference input used to clock serial MDIO data into and out of the VSC8201. The expected nominal frequency is 2.5MHz, as specified by the IEEE standard. This clock is typically asynchronous with respect to the PHY's transmit or receive clock.
MDIO	Open Drain	**Management Data I/O.** MDIO configuration and status data is exchanged on this pin bidirectionally between the PHY and the Station Manager, synchronously to the rising edge of MDC. This pin normally requires a 1.5kΩ to 2kΩ external pull-up resistor at the Station Manager. The value of the pull-up resistor depends on the MDC clock frequency and the maximum capacitive load on the MDIO pin.
MDINT#	Open Drain	**Management Data Interrupt Output.** This open drain, active low output signal indicates a change in the PHY's link operating conditions for which a station manager must interrogate to determine further information. This pin should be pulled up to VDDIO at the Station Manager or controller through an external 10kΩ pull-up resistor.

It is important to note that both MDIO and MDINT# signals are configured as open drain, and thus require an external pullup resistor. Only a single pullup resistor on each signal is needed for the system, regardless of the number of devices. For MDINT# a single 10kohm system pullup resistor is sufficient.

Unlike MDINT#, the value of the pullup needed for MDIO must be chosen to match the characteristics of the system. Of critical importance is the rise time needed to charge the total capacitive load on the MDIO up to logic '1' through the pullup resistor. This constant is defined simply as:

$$\tau = R_{pu}C_{total}$$

In most cases the number of devices on the bus will be 1. But in the case where more devices are added to the bus, the rise time increases due to the increased bus capacitance. In order to lower the rise time, a smaller resistor value must be used. However, if too small of a value is used, devices will be unable to transition the bus to a logic '0'. This occurs when the current sinking capability of the pins in a logic '0' state is exceeded. For the VSC8201, the MDIO input capacitance is 5pF, and the maximum current sinking capacity is 10mA.

Typical values are given below:

- For MDC frequencies of 2.5MHz and below, a 2k pullup resistor should suffice for most applications.This assumes the input capacitance of each device is between 5-10pF and that each device can sink 1.65mA of current in the MDIO pin.
- For faster MDC frequencies (>2.5MHz), a smaller pullup is necessary. The smallest recommended pullup resistor for use with the VSC8201 is 470Ω.

RJ-45 Connectors and Magnetic Modules

RJ-45 Connector Recommendations

System designers can choose either the tab-up or tab-down connectors. LEDs can also be integrated into the connectors.

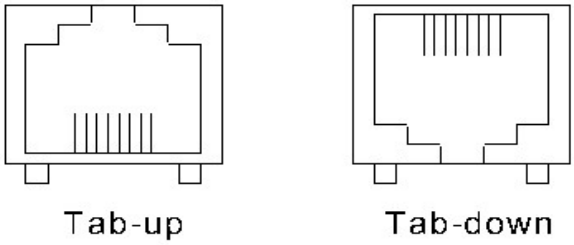


Figure 9: RJ45 Connectors

Due to the orientation, the pinouts of the tab-up and the tab-down are reversed. The VSC8201 will work equally well using either orientation. The tab-down connector is more wide-spread than the tab-up connector in the NIC card industry.

CAT-5 vs. CAT-3 Connectors

When utilizing 1000Base-T or 100Base-T, it is important that ‘CAT-5’ RJ-45 connectors be used as opposed to ‘CAT-3’. This refers to the amount of cross-talk between wire pairs within the connector.

In addition to the electrical characteristics, some manufacturers have two options for the connector pinout. These are typically labeled as ‘standard’ and ‘CAT-5’. This is not to be confused with the electrical specification for the connector. Thus, two versions of a CAT-5 RJ-45 connector are available: One with ‘standard’ pinout and one with a ‘CAT-5’ pinout:

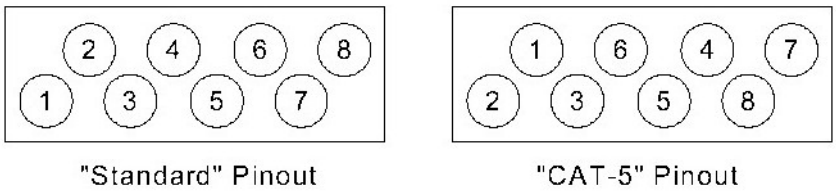


Figure 10: RJ45 Connector Pinouts

Specific RJ-45 Recommendations

Virtually any RJ-45 connector that meets the CAT-5 electrical specification will work with the VSC8201. Two such manufacturers are:

AMP (a division of Tyco International, Ltd.)
Tel: 717-564-0100

http://www.amp.com

Transpower Technologies, Inc.
Tel: 775-852-0140

http://www.trans-power.com

Table 7: Sample Part Numbers for RJ45 Connectors

Part Number	Manufacturer	Description
558341-1	AMP	Single Port, unshielded, without LEDs, tab-down, 'CAT-5' pinout.
RJ7G02	Transpower Tech., Inc.	Single Port, Through hole, Tab-up, pinout is unique to Transpower
RJ7G07	Transpower Tech., Inc.[a]	Single Port, Through hole, Tab-up, pinout is unique to Transpower

a. This module has an integrated magnetic module

Magnetic Modules

For best performance, proper magnetic modules must be used with the VSC8201. In addition, some companies integrate the magnetic modules into the RJ-45 connector.

Note on Return-Loss Compensation Circuit: Testing has indicated that some magnetic modules may not pass the IEEE specification for return loss. In these cases, an extra resistor-capacitor circuit can be added for each of the sub-channels. See "Return Loss Circuit for Pulse H5008 Transformer" on page 18. The presence of this circuit serves only to allow the system to pass IEEE return loss measurements and does not affect the performance of the PHY in any other way. The exact values required for the resistors and capacitors varies according to each manufacturer and can be found in Table 8: "Recommended Magnetic Modules."

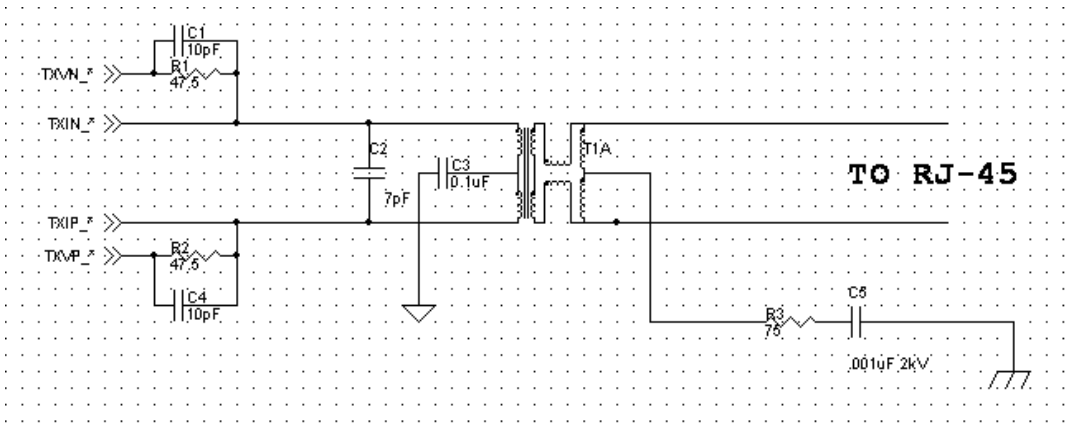


Figure 11: Return Loss Circuit for Pulse H5008 Transformer

Below is a list of recommended magnetic modules:

Delta Electronics, Inc.
Tel:

http://www.delta.com.tw/products/networking.asp

Pulse Engineering, Inc.
Tel: 858-674-8100

http://www.pulseeng.com

Halo Electronics, Inc.
Tel: 650-568-5800

http://www.haloelectronics.com

Table 8: Recommended Magnetic Modules

Part Number	Manufacturer	Description	Return Loss Compensation
LF9207A	Delta	Single-port, surface mount	
H5008	Pulse	Single-port, surface mount	C_1, C_4 = 10pF, C_2 = 6.8pF
S558-5999-P3	Bel	Single-port, surface mount	
TG1G-S002NZ	Halo	Single-port, surface mount	
GB2G04	Transpower	Single-port, surface mount	

Thermal Performance

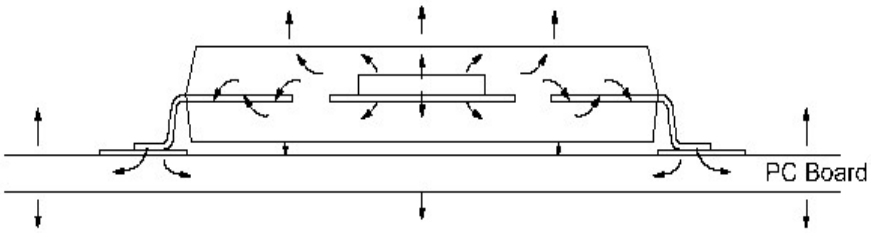


Figure 12: Heat dissipating path for IC packages

The two paths of heat dissipation shown in the above figure are as follows:

1. IC chip → Package → Atmosphere
2. IC chip → Package → lead → PC board → Atmosphere

The amount of heat dissipated by path 2. depends on various factors like pad size, wired length, layer configuration, thickness, materials etc. of the PC board but, typically, 10% to 50% of the heat is dissipated through the PC board.

Although low power consumption of the VSC8201 eliminates the need of external heatsinks or fans in most designs, it is always recommended to follow certain guidelines for adequate heat dissipation.

For proper operation of the VSC8201, a silicon junction temperature T_j equal to or below 125°C must be maintained for commercial temperature ranges. Within the constraints of the commercial temperature range, the limits for junction-to-ambient thermal resistance are as follows:[1]

$$\theta_{ja(commercial)} = \frac{T_j - T_a}{P_d} = \frac{125^oC - 70^oC}{1w} = 55^o(C/w)$$

where

θ_{ja} = Junction to ambient thermal resistance,

T_j = Junction temperature,

1. The actual θ_{ja} of the VSC8201's 128 LQFP and the 100 ball LBGA package is approx. 30°C/w to 35°C/w. This yields a

$$P_{D(max)} = (125 - 70^oC)/(35^o(C/w)) = 1.5w \quad (\text{for } T_j \le 125^oC)$$

T_a = Ambient temperature,

P_d = Power dissipation.

For the 128 pin LQFP vias which connect the nearby high frequency decoupling capacitors to the ground and power planes are sufficient for the required heat dissipation rate. See “Local High-Frequency decoupling Capacitor Layout - LQFP package” on page 2.

For proper cooling of the 100 ball LBGA, a PCB via must be placed between the thermal BGA ball pads in a checkerboard pattern (see Figure 13: ”Thermal Via Layout”, below). Each of these “thermal vias” should then be routed to the BGA ball pads near it with a wide trace or solid copper fill to increase the conductive area on the surface of the PCB. In order to dissipate heat below the BGA package, the PCB thermal vias must connect to a solid ground plane within the board. It is recommended that the ground plane have a minimum thickness of one ounce (see Figure 14: ”Thermal Ground Plane Connections”, below).

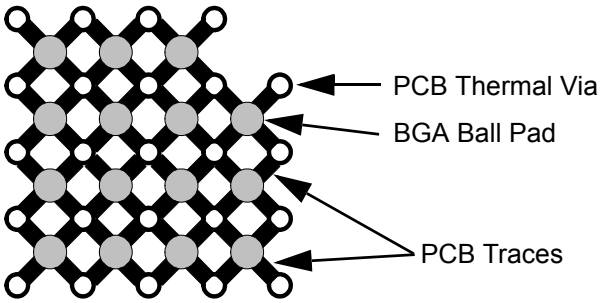


Figure 13: Thermal Via Layout

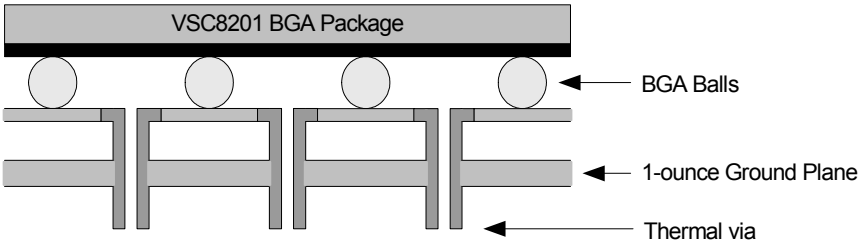


Figure 14: Thermal Ground Plane Connections

Document History & Notices

Revision Number	Date	Description
1.6.1	16 Jan 03	
1.6.2	7 Aug 03	Updated decoupling power supply, capacitor lay-out (added LBGA figure), and schematic
1.6.3	29 Sep 04	Changed CIS8201 to VSC8201 globally. Integrated the information from the CIS8201 RGMII 3.3V Appnote into this document.