# 32-Channel, 14-Bit Voltage-Output DAC

# AD5532*

## FEATURES

**High Integration: 32-Channel DAC in 12 × 12 mm² LFBGA**
**Adjustable Voltage Output Range**
**Guaranteed Monotonic**
**Readback Capability**
**DSP-/Microcontroller-Compatible Serial Interface**
**Output Impedance**
**0.5 Ω (AD5532-1, AD5532-2)**
**500 Ω (AD5532-3)**
**1 kΩ (AD5532-5)**
**Output Voltage Span**
**10 V (AD5532-1, AD5532-3, AD5532-5)**
**20 V (AD5532-2)**
**Infinite Sample-and-Hold Capability to ±0.018% Accuracy**
**Temperature Range –40°C to +85°C**

## APPLICATIONS

**Level Setting**
**Instrumentation**
**Automatic Test Equipment**
**Industrial Control Systems**
**Data Acquisition**
**Low Cost I/O**

## GENERAL DESCRIPTION

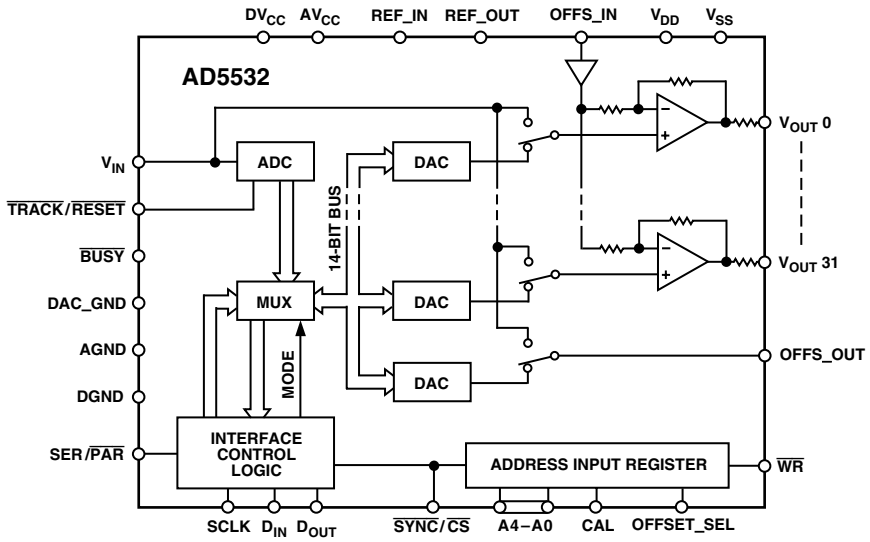
The AD5532 is a 32-channel voltage-output 14-bit DAC with an additional infinite sample-and-hold mode. The selected DAC register is written to via the 3-wire serial interface and $V_{OUT}$ for this DAC is then updated to reflect the new contents of the DAC register. DAC selection is accomplished via address bits A0–A4. The output voltage range is determined by the offset voltage at the OFFS_IN pin and the gain of the output amplifier. It is restricted to a range from $V_{SS}$ + 2 V to $V_{DD}$ – 2 V because of the headroom of the output amplifier.

The device is operated with $AV_{CC}$ = 5 V ± 5%, $DV_{CC}$ = 2.7 V to 5.25 V, $V_{SS}$ = –4.75 V to –16.5 V and $V_{DD}$ = 8 V to 16.5 V and requires a stable +3 V reference on REF_IN as well as an offset voltage on OFFS_IN.

## PRODUCT HIGHLIGHTS

1. 32-channel, 14-bit DAC in one package, guaranteed monotonic.
2. The AD5532 is available in a 74-lead LFBGA package with a body size of 12 mm × 12 mm.
3. Droopless/Infinite Sample-and-Hold Mode.

## FUNCTIONAL BLOCK DIAGRAM




*Protected by U.S. Patent No. 5,969,657; other patents pending.

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# AD5532–SPECIFICATIONS

**($V_{DD}$ = 8 V to 16.5 V, $V_{SS}$ = –4.75 V to –16.5 V; $AV_{CC}$ = 4.75 V to 5.25 V; $DV_{CC}$ = 2.7 V to 5.25 V; AGND = DGND = DAC_GND = 0 V; REF_IN = 3 V; Output Range from $V_{SS}$ + 2 V to $V_{DD}$ – 2 V. All outputs unloaded. All specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)**

| Parameter[1] | A Version[2] AD5532-1/-3/-5 | A Version[2] AD5532-2 Only | Unit | Conditions/ Comments |
|---|---|---|---|---|
| DAC DC PERFORMANCE | | | | |
| Resolution | 14 | 14 | Bits | |
| Integral Nonlinearity (INL) | ±0.39 | ±0.39 | % of FSR max | ±0.15% typ |
| Differential Nonlinearity (DNL) | ±1 | ±1 | LSB max | ±0.5% typ, Monotonic |
| Offset | 90/170/250 | 180/350/500 | mV min/typ/max | See Figure 6 |
| Gain | 3.52 | 7 | typ | |
| Full-Scale Error | ±2 | ±2 | % of FSR max | |
| VOLTAGE REFERENCE | | | | |
| REF_IN | | | | |
| Nominal Input Voltage | 3.0 | 3.0 | V | |
| Input Voltage Range[3] | 2.85/3.15 | 2.85/3.15 | V min/max | |
| Input Current | 1 | 1 | µA max | < 1 nA typ |
| REF_OUT | | | | |
| Output Voltage | 3 | 3 | V typ | |
| Output Impedance[3] | 280 | 280 | kΩ typ | |
| Reference Temperature Coefficient[3] | 60 | 60 | ppm/°C typ | |
| ANALOG OUTPUTS ($V_{OUT}$ 0–31) | | | | |
| Output Temperature Coefficient[3, 4] | 20 | 20 | ppm/°C typ | |
| DC Output Impedance[3] | | | | |
| AD5532-1 | 0.5 | 0.5 | Ω typ | |
| AD5532-3 | 500 | | Ω typ | |
| AD5532-5 | 1 | | kΩ typ | |
| Output Range | $V_{SS}$ + 2/$V_{DD}$ – 2 | $V_{SS}$ + 2 /$V_{DD}$ – 2 | V min/max | 100 µA Output Load |
| Resistive Load[3, 5] | 5 | 5 | kΩ min | |
| Capacitive Load[3, 5] | | | | |
| AD5532-1 | 500 | 500 | pF max | |
| AD5532-3 | 15 | | nF max | |
| AD5532-5 | 40 | | nF max | |
| Short-Circuit Current[3] | 10 | 10 | mA typ | |
| DC Power-Supply Rejection Ratio[3] | –70 | –70 | dB typ | $V_{DD}$ = +15 V ± 5% |
| | –70 | –70 | dB typ | $V_{SS}$ = –15 V ± 5% |
| DC Crosstalk[3] | 250 | 250 | µV max | |
| ANALOG OUTPUT (OFFS_OUT) | | | | |
| Output Temperature Coefficient[3, 4] | 20 | 20 | ppm/°C typ | |
| DC Output Impedance[3] | 1.3 | 1.3 | kΩ typ | |
| Output Range | 50 to REF_IN–12 | 50 to REF_IN–12 | mV typ | |
| Output Current | 10 | 10 | µA max | Source Current |
| Capacitive Load | 100 | 100 | pF max | |
| DIGITAL INPUTS[3] | | | | |
| Input Current | ±10 | ±10 | µA max | ±5 µA typ |
| Input Low Voltage | 0.8 | 0.8 | V max | $DV_{CC}$ = 5 V ± 5% |
| | 0.4 | 0.4 | V max | $DV_{CC}$ = 3 V ± 10% |
| Input High Voltage | 2.4 | 2.4 | V min | $DV_{CC}$ = 5 V ± 5% |
| | 2.0 | 2.0 | V min | $DV_{CC}$ = 3 V ± 10% |
| Input Hysteresis ($\overline{SCLK}$ and $\overline{CS}$ Only) | 200 | 200 | mV typ | |
| Input Capacitance | 10 | 10 | pF max | |
| DIGITAL OUTPUTS ($\overline{BUSY}$, $D_{OUT}$)[3] | | | | |
| Output Low Voltage, $DV_{CC}$ = 5 V | 0.4 | 0.4 | V max | Sinking 200 µA |
| Output High Voltage, $DV_{CC}$ = 5 V | 4.0 | 4.0 | V min | Sourcing 200 µA |
| Output Low Voltage, $DV_{CC}$ = 3 V | 0.4 | 0.4 | V max | Sinking 200 µA |
| Output High Voltage, $DV_{CC}$ = 3 V | 2.4 | 2.4 | V min | Sourcing 200 µA |
| High Impedance Leakage Current | ±1 | ±1 | µA max | $D_{OUT}$ Only |
| High Impedance Output Capacitance | 15 | 15 | pF typ | $D_{OUT}$ Only |

| Parameter[1] | A Version[2] AD5532-1/-3/-5 | A Version[2] AD5532-2 Only | Unit | Conditions/ Comments |
|---|---|---|---|---|
| POWER REQUIREMENTS | | | | |
| Power-Supply Voltages | | | | |
| $V_{DD}$ | 8/16.5 | 8/16.5 | V min/max | |
| $V_{SS}$ | –4.75/–16.5 | –4.75/–16.5 | V min/max | |
| $AV_{CC}$ | 4.75/5.25 | 4.75/5.25 | V min/max | |
| $DV_{CC}$ | 2.7/5.25 | 2.7/5.25 | V min/max | |
| Power-Supply Currents[6] | | | | |
| $I_{DD}$ | 15 | 15 | mA max | 10 mA typ. All Channels Full-Scale |
| $I_{SS}$ | 15 | 15 | mA max | 10 mA typ. All Channels Full-Scale |
| AICC | 33 | 33 | mA max | 26 mA typ |
| DICC | 1.5 | 1.5 | mA max | 1 mA typ |
| Power Dissipation[6] | 280 | 280 | mW typ | $V_{DD}$ = 10 V, $V_{SS}$ = –5 V |
| AC CHARACTERISTICS[3] | | | | |
| Output Voltage Settling Time | 22 | 30 | µs max | 500 pF, 5 kΩ Load Full-Scale Change |
| OFFS_IN Settling Time | 10 | 20 | µs max | 500 pF, 5 kΩ Load; 0 V–3 V Step |
| Digital-to-Analog Glitch Impulse | 1 | 1 | nV-s typ | 1 LSB Change Around Major Carry |
| Digital Crosstalk | 5 | 5 | nV-s typ | |
| Analog Crosstalk | 1 | 1 | nV-s typ | |
| Digital Feedthrough | 0.2 | 0.2 | nV-s typ | |
| Output Noise Spectral Density @ 1 kHz | 400 | 400 | nV/(√Hz) typ | |

NOTES
[1]See Terminology.
[2]A Version: Industrial temperature range –40°C to +85°C; typical at +25°C.
[3]Guaranteed by design and characterization, not production tested.
[4]AD780 as reference for the AD5532.
[5]Ensure that you do not exceed $T_J$ (max). See Maximum Ratings.
[6]Output unloaded.
Specifications subject to change without notice.

# SHA MODE

| Parameter[1] | A Version[2] AD5532-1/-3/-5 | A Version[2] AD5532-2 Only | Unit | Conditions/ Comments |
|---|---|---|---|---|
| ANALOG CHANNEL | | | | |
| $V_{IN}$ to $V_{OUT}$ Nonlinearity[3] | ±0.018 | ±0.018 | % max | ±0.006% typ after Offset and Gain Adjustment |
| Offset Error | ±50 | ±100 | mV max | ±10 mV typ. See Figure 7 |
| Gain | 3.46/3.52/3.6 | 6.88/7/7.12 | min/typ/max | See Figure 7 |
| ANALOG INPUT ($V_{IN}$) | | | | |
| Input Voltage Range | 0 to 3 | 0 to 3 | V | Nominal Input Range |
| Input Lower Deadband | 70 | 70 | mV max | 50 mV typ. Referred to $V_{IN}$. See Figure 7 |
| Input Upper Deadband | 40 | 40 | mV max | 12 mV typ. Referred to $V_{IN}$. See Figure 7 |
| Input Current | 1 | 1 | µA max | 100 nA typ. $V_{IN}$ Acquired on 1 Channel |
| Input Capacitance[4] | 20 | 20 | pF typ | |
| ANALOG INPUT (OFFS_IN) | | | | |
| Input Current | 1 | 1 | µA max | 100 nA typ |
| AC CHARACTERISTICS | | | | |
| Output Settling Time[4] | 3 | 3 | µs max | Output Unloaded |
| Acquisition Time | 16 | 16 | µs max | |
| AC Crosstalk[4] | 5 | 5 | nV-s typ | |

NOTES
[1]See Terminology.
[2]A version: Industrial temperature range –40°C to +85°C; typical at +25°C.
[3]Input range 100 mV to 2.96 V.
[4]Guaranteed by design and characterization, not production tested.
Specifications subject to change without notice.

# TIMING CHARACTERISTICS

**PARALLEL INTERFACE**

| Parameter[1, 2] | Limit at $T_{MIN}$, $T_{MAX}$ (A Version) | Unit | Conditions/Comments |
|---|---|---|---|
| $t_1$ | 0 | ns min | $\overline{CS}$ to $\overline{WR}$ Setup Time |
| $t_2$ | 0 | ns min | $\overline{CS}$ to $\overline{WR}$ Hold Time |
| $t_3$ | 50 | ns min | $\overline{CS}$ Pulsewidth Low |
| $t_4$ | 50 | ns min | $\overline{WR}$ Pulsewidth Low |
| $t_5$ | 20 | ns min | A4–A0, CAL, OFFS_SEL to $\overline{WR}$ Setup Time |
| $t_6$ | 0 | ns min | A4–A0, CAL, OFFS_SEL to $\overline{WR}$ Hold Time |

NOTES
[1]See Interface Timing Diagram.
[2]Guaranteed by design and characterization, not production tested.

Specifications subject to change without notice.

**SERIAL INTERFACE**

| Parameter[1, 2] | Limit at $T_{MIN}$, $T_{MAX}$ (A Version) | Unit | Conditions/Comments |
|---|---|---|---|
| $f_{CLKIN}$[3] | 14 | MHz max | SCLK Frequency |
| $t_1$ | 28 | ns min | SCLK High Pulsewidth |
| $t_2$ | 28 | ns min | SCLK Low Pulsewidth |
| $t_3$ | 10 | ns min | $\overline{SYNC}$ Falling Edge to SCLK Falling Edge Setup Time |
| $t_4$ | 50 | ns min | $\overline{SYNC}$ Low Time |
| $t_5$ | 10 | ns min | $D_{IN}$ Setup Time |
| $t_6$ | 5 | ns min | $D_{IN}$ Hold Time |
| $t_7$ | 5 | ns min | $\overline{SYNC}$ Falling Edge to SCLK Rising Edge Setup Time |
| $t_8$[4] | 20 | ns max | SCLK Rising Edge to $D_{OUT}$ Valid |
| $t_9$[4] | 60 | ns max | SCLK Falling Edge to $D_{OUT}$ High Impedance |
| $t_{10}$ | 400 | ns min | 10th SCLK Falling Edge to $\overline{SYNC}$ Falling Edge for Readback |
| $t_{11}$ | 400 | ns min | 24th SCLK Falling Edge to $\overline{SYNC}$ Falling Edge for DAC Mode Write |

NOTES
[1]See Serial Interface Timing Diagrams.
[2]Guaranteed by design and characterization, not production tested.
[3]In SHA mode the maximum SCLK frequency is 20 MHz and the minimum pulsewidth is 20 ns.
[4]These numbers are measured with the load circuit of Figure 2.

Specifications subject to change without notice.

**PARALLEL INTERFACE TIMING DIAGRAMS**

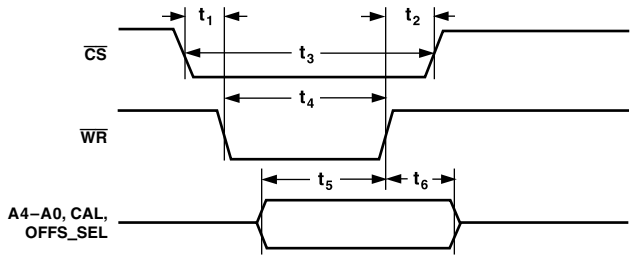



*Figure 1. Parallel Write (SHA Mode Only)*

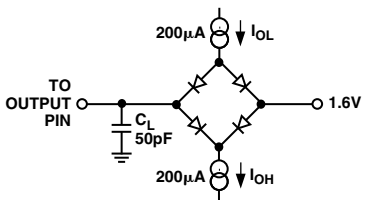



*Figure 2. Load Circuit for $D_{OUT}$ Timing Specifications*

## SERIAL INTERFACE TIMING DIAGRAMS

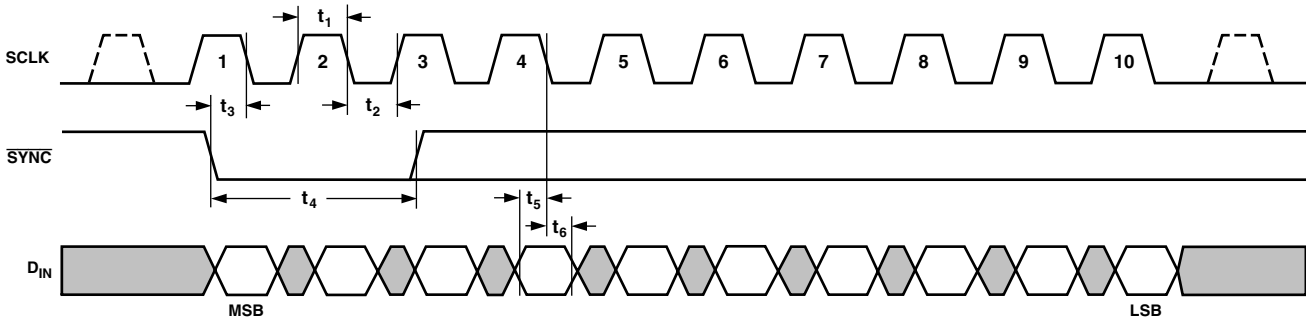



*Figure 3. 10-Bit Write (SHA Mode and Both Readback Modes)*

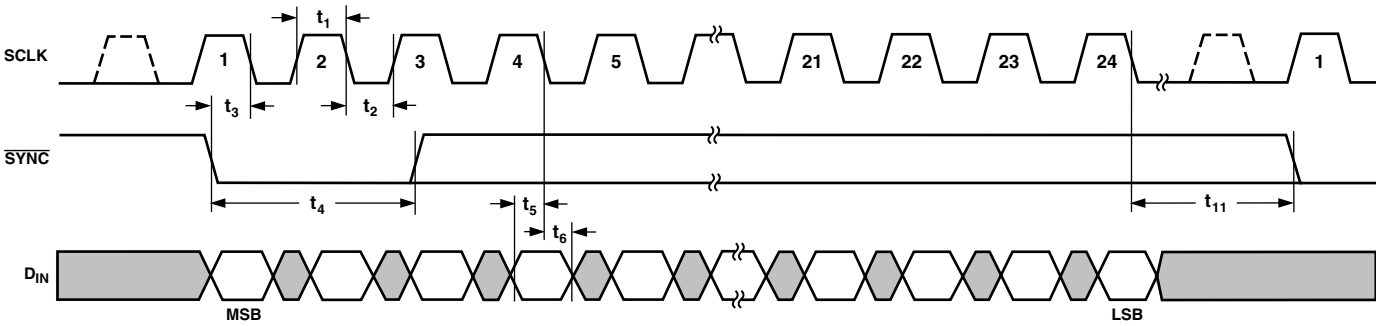



*Figure 4. 24-Bit Write (DAC Mode)*

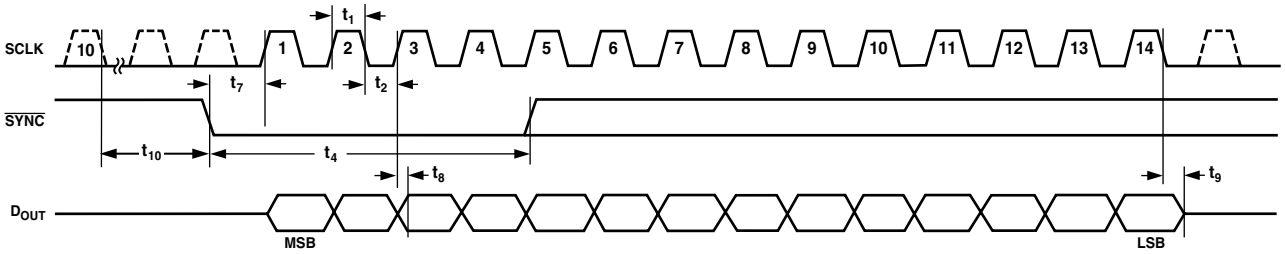



*Figure 5. 14-Bit Read (Both Readback Modes)*

**ABSOLUTE MAXIMUM RATINGS**[1, 2]

($T_A$ = 25°C unless otherwise noted)

$V_{DD}$ to AGND . . . . . –0.3 V to +17 V
$V_{SS}$ to AGND . . . . . +0.3 V to –17 V
$AV_{CC}$ to AGND, DAC_GND . . . . . –0.3 V to +7 V
$DV_{CC}$ to DGND . . . . . –0.3 V to +7 V
Digital Inputs to DGND . . . . . –0.3 V to $DV_{CC}$ + 0.3 V
Digital Outputs to DGND . . . . . –0.3 V to $DV_{CC}$ + 0.3 V
REF_IN to AGND, DAC_ GND . . . . . –0.3 V to +7 V
$V_{IN}$ to AGND, DAC_GND . . . . . –0.3 V to +7 V
$V_{OUT}$0–31 to AGND . . . . . $V_{SS}$ – 0.3 V to $V_{DD}$ + 0.3 V
$V_{OUT}$0–31 to $V_{SS}$ . . . . . –0.3 V to +24 V
OFFS_IN to AGND . . . . . $V_{SS}$ – 0.3 V to $V_{DD}$ + 0.3 V
OFFS_OUT to AGND . . . . AGND – 0.3 V to $AV_{CC}$ + 0.3 V
AGND to DGND . . . . . –0.3 V to +0.3 V

Operating Temperature Range
Industrial . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature ($T_J$ max) . . . . . 150°C
74-Lead LFBGA Package, $\theta_{JA}$ Thermal Impedance . . . 41°C/W
Reflow Soldering
Peak Temperature . . . . . 220°C
Time at Peak Temperature . . . . . 10 sec to 40 sec

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

**ORDERING GUIDE**

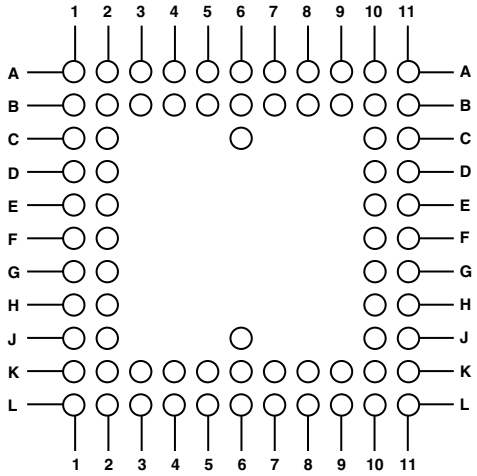
| Model | Function | Output Impedance | Output Voltage Span | Package Description | Package Option |
|---|---|---|---|---|---|
| AD5532ABC-1 | 32 DACs, 32-Channel SHA | 0.5 Ω typ | 10 V | 74-Lead LFBGA | BC-74 |
| AD5532ABC-2 | 32 DACs, 32-Channel SHA | 0.5 Ω typ | 20 V | 74-Lead LFBGA | BC-74 |
| AD5532ABC-3 | 32 DACs, 32-Channel SHA | 500 Ω typ | 10 V | 74-Lead LFBGA | BC-74 |
| AD5532ABC-5 | 32 DACs, 32-Channel SHA | 1 kΩ typ | 10 V | 74-Lead LFBGA | BC-74 |
| AD5533ABC-1* | 32-Channel SHA Only | 0.5 Ω typ | 10 V | 74-Lead LFBGA | BC-74 |
| EVAL-AD5532EB | Evaluation Board | | | | |

*Separate Data Sheet.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5532 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION




**74-Lead LFBGA Ball Configuration**

| LFBGA Number | Ball Name | LFBGA Number | Ball Name | LFBGA Number | Ball Name |
|---|---|---|---|---|---|
| A1 | N/C | C10 | AVCC1 | J10 | VO9 |
| A2 | A4 | C11 | REF_OUT | J11 | VO11 |
| A3 | A2 | D1 | VO20 | K1 | VO17 |
| A4 | A0 | D2 | DAC_GND2 | K2 | VO15 |
| A5 | $\overline{CS}$/$\overline{SYNC}$ | D10 | AVCC2 | K3 | VO27 |
| A6 | DVCC | D11 | OFFS_OUT | K4 | VSS3 |
| A7 | SCLK | E1 | VO26 | K5 | VSS1 |
| A8 | OFFSET_SEL | E2 | VO14 | K6 | VSS4 |
| A9 | $\overline{BUSY}$ | E10 | AGND1 | K7 | VDD2 |
| A10 | $\overline{TRACK}$/$\overline{RESET}$ | E11 | OFFS_IN | K8 | VO2 |
| A11 | N/C | F1 | VO25 | K9 | VO10 |
| B1 | VO16 | F2 | VO21 | K10 | VO13 |
| B2 | N/C | F10 | AGND2 | K11 | VO12 |
| B3 | A3 | F11 | VO6 | L1 | N/C |
| B4 | A1 | G1 | VO24 | L2 | VO28 |
| B5 | $\overline{WR}$ | G2 | VO8 | L3 | VO29 |
| B6 | DGND | G10 | VO5 | L4 | VO30 |
| B7 | $D_{IN}$ | G11 | VO3 | L5 | VDD3 |
| B8 | CAL | H1 | VO23 | L6 | VDD1 |
| B9 | SER/$\overline{PAR}$ | H2 | VIN | L7 | VDD4 |
| B10 | DOUT | H10 | VO4 | L8 | VO31 |
| B11 | REF_IN | H11 | VO7 | L9 | VO0 |
| C1 | VO18 | J1 | VO22 | L10 | VO1 |
| C2 | DAC_GND1 | J2 | VO19 | L11 | N/C |
| C6 | N/C | J6 | VSS2 | | |

**PIN FUNCTION DESCRIPTION**

| Pin | Function |
|---|---|
| AGND (1–2) | Analog GND Pins. |
| $AV_{CC}$ (1–2) | Analog Supply Pins. Voltage range from 4.75 V to 5.25 V. |
| $V_{DD}$ (1–4) | $V_{DD}$ Supply Pins. Voltage range from 8 V to 16.5 V. |
| $V_{SS}$ (1–4) | $V_{SS}$ Supply Pins. Voltage range from –4.75 V to –16.5 V. |
| DGND | Digital GND Pins. |
| $DV_{CC}$ | Digital Supply Pins. Voltage range from 2.7 V to 5.25 V. |
| DAC_GND(1–2) | Reference GND Supply for All the DACs. |
| REF_IN | Reference Voltage for Channels 0–31. |
| REF_OUT | Reference Output Voltage. |
| $V_{OUT}$ (0–31) | Analog Output Voltages from the 32 Channels. |
| $V_{IN}$ | Analog Input Voltage. Connect this to AGND if operating in DAC mode only. |
| A4–A1[1], A0[2] | Parallel Interface: 5-Address Pins for 32 Channels. A4 = MSB of Channel Address. A0 = LSB. |
| CAL[1] | Parallel Interface: Control input that allows all 32 channels to acquire $V_{IN}$ simultaneously. |
| $\overline{CS}/\overline{SYNC}$ | This pin is both the active low Chip Select pin for the parallel interface and the Frame Synchronization pin for the serial interface. |
| $\overline{WR}$[1] | Parallel Interface: Write pin. Active low. This is used in conjunction with the $\overline{CS}$ pin to address the device using the parallel interface. |
| OFFSET_SEL[1] | Parallel Interface: Offset Select Pin. Active high. This is used to select the offset channel. |
| SCLK[2] | Serial Clock Input for Serial Interface. This operates at clock speeds up to 14 MHz (20 MHz in SHA mode). |
| $D_{IN}$[2] | Data Input for Serial Interface. Data must be valid on the falling edge of SCLK. |
| $D_{OUT}$ | Output from the DAC Registers for readback. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK. |
| SER/$\overline{PAR}$[1] | This pin allows the user to select whether the serial or parallel interface will be used. If the pin is tied low, the parallel interface will be used. If it is tied high, the serial interface will be used. |
| OFFS_IN | Offset Input. The user can supply a voltage here to offset the output span. OFFS_OUT can also be tied to this pin if the user wants to drive this pin with the Offset Channel. |
| OFFS_OUT | Offset Output. This is the acquired/programmed offset voltage which can be tied to OFFS_IN to offset the span. |
| $\overline{BUSY}$ | This output tells the user when the input voltage is being acquired. It goes low during acquisition and returns high when the acquisition operation is complete. |
| $\overline{TRACK}/\overline{RESET}$[2] | If this input is held high, $V_{IN}$ is acquired once the channel is addressed. While it is held low, the input to the gain/offset stage is switched directly to $V_{IN}$. The addressed channel begins to acquire $V_{IN}$ on the rising edge of $\overline{TRACK}$. See $\overline{TRACK}$ Input section for further information. This input can also be used as a means of resetting the complete device to its power-on-reset conditions. This is achieved by applying a low-going pulse of between 50 ns and 150 ns to this pin. See section on $\overline{RESET}$ Function for further details. |

NOTES
[1]Internal pull-down devices on these logic inputs. Therefore, they can be left floating and will default to a logic low condition.
[2]Internal pull-up devices on these logic inputs. Therefore, they can be left floating and will default to a logic high condition.

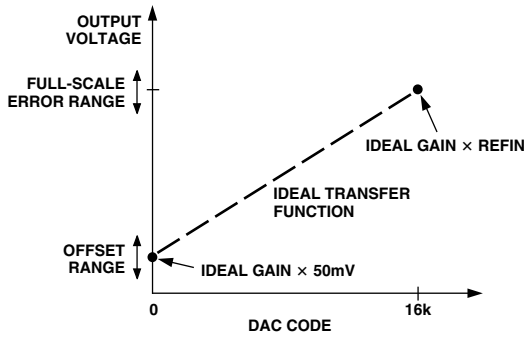



*Figure 6. DAC Transfer Function (OFFS_IN = 0)*

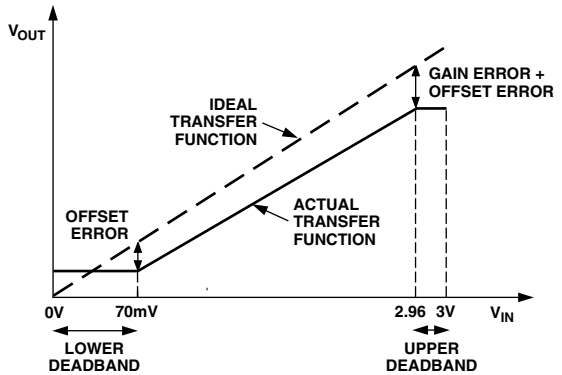



*Figure 7. SHA Transfer Function*

## TERMINOLOGY

### DAC MODE

**Integral Nonlinearity (INL)**
This is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is expressed as a percentage of full-scale span.

**Differential Nonlinearity (DNL)**
Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity.

**Offset**
Offset is a measure of the output with all zeros loaded to the DAC and OFFS_IN = 0. Since the DAC is lifted off the ground by approximately 50 mV, this output will typically be:

$$V_{OUT} = Gain \times 50\ mV$$

**Full-Scale Error**
This is a measure of the output error with all 1s loaded to the DAC. It is expressed as a percentage of full-scale range. See Figure 6. It is calculated as:

$$Full\text{-}Scale\ Error = V_{OUT(Full\text{-}Scale)} - (Ideal\ Gain \times REFIN)$$

where

*Ideal Gain* = 3.52 for AD5532-1/-3/-5
*Ideal Gain* = 7 for AD5532-2

**Output Settling Time**
This is the time taken from when the last data bit is clocked into the DAC until the output has settled to within ±0.39%.

**OFFS_IN Settling Time**
This is the time taken from a 0 V–3 V step change in input voltage on OFFS_IN until the output has settled to within ±0.39%.

**Digital-to-Analog Glitch Impulse**
This is the area of the glitch injected into the analog output when the code in the DAC register changes state. It is specified as the area of the glitch in nV-secs when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

**Digital Crosstalk**
This is the glitch impulse transferred to the output of one DAC at midscale while a full-scale code change (all 1s to all 0s and vice versa) is being written to another DAC. It is expressed in nV-secs.

**Analog Crosstalk**
This the area of the glitch transferred to the output ($V_{OUT}$) of one DAC due to a full-scale change in the output ($V_{OUT}$) of another DAC. The area of the glitch is expressed in nV-secs.

**Digital Feedthrough**
This is a measure of the impulse injected into the analog outputs from the digital control inputs when the part is not being written to, i.e., $\overline{CS}/\overline{SYNC}$ is high. It is specified in nV-secs and is measured with a worst-case change on the digital input pins, e.g., from all 0s to all 1s and vice versa.

**Output Noise Spectral Density**
This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per root Hertz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in $nV/(\sqrt{Hz})^{1/2}$.

**Output Temperature Coefficient**
This is a measure of the change in analog output with changes in temperature. It is expressed in ppm/°C.

**DC Power-Supply Rejection Ratio**
DC Power-Supply Rejection Ratio (PSRR) is a measure of the change in analog output for a change in supply voltage ($V_{DD}$ and $V_{SS}$). It is expressed in dBs. $V_{DD}$ and $V_{SS}$ are varied ±5%.

**DC Crosstalk**
This the DC change in the output level of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) and output change of all other DACs. It is expressed in µV.

### SHA MODE

**$V_{IN}$ to $V_{OUT}$ Nonlinearity**
This is a measure of the maximum deviation from a straight line passing through the endpoints of the $V_{IN}$ versus $V_{OUT}$ transfer function. It is expressed as a percentage of the full-scale span.

**Offset Error**
This is a measure of the output error when $V_{IN}$ = 70 mV. Ideally, with $V_{IN}$ = 70 mV:

$$V_{OUT} = (Gain \times 70) - ((Gain - 1) \times V_{OFFS\_IN})\ mV$$

Offset error is a measure of the difference between $V_{OUT}$ (actual) and $V_{OUT}$ (ideal). It is expressed in mV and can be positive or negative. See Figure 7.

**Gain Error**
This is a measure of the span error of the analog channel. It is the deviation in slope of the transfer function expressed in mV. See Figure 7. It is calculated as:

*Gain Error* = *Actual Full-Scale Output – Ideal Full-Scale Output – Offset Error*

where

$$Ideal\ Full\text{-}Scale\ Output = Gain \times 2.96 - ((Gain - 1) \times V_{OFFS\_IN})$$

**AC Crosstalk**
This is the area of the glitch that occurs on the output of one channel while another channel is acquiring. It is expressed in nV-secs.

**Output Settling Time**
This is the time taken from when $\overline{BUSY}$ goes high to when the output has settled to ±0.018%.

**Acquisition Time**
This is the time taken for the $V_{IN}$ input to be acquired. It is the length of time that $\overline{BUSY}$ stays low.

# AD5532–Typical Performance Characteristics

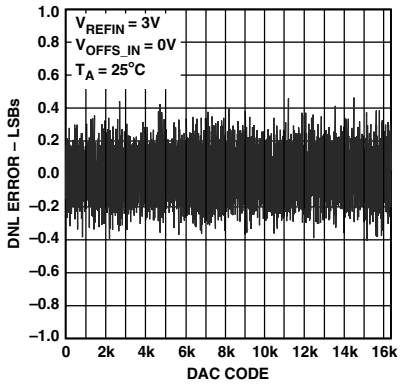



*Figure 8. Typical DNL Plot*

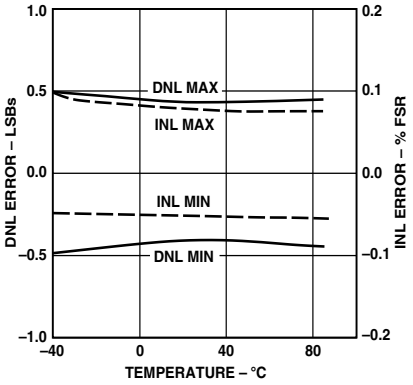



*Figure 9. INL Error and DNL Error vs. Temperature*

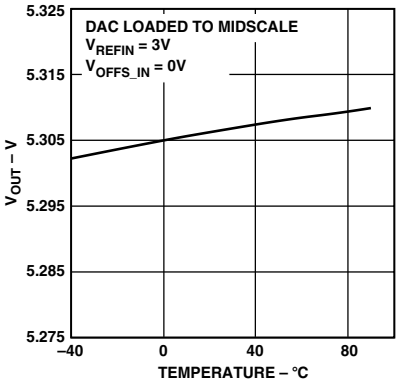



*Figure 10. $V_{OUT}$ vs. Temperature*

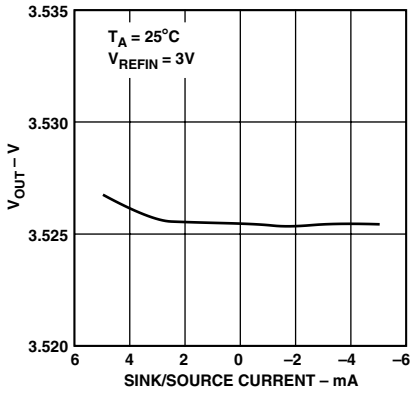



*Figure 11. $V_{OUT}$ Source and Sink Capability*

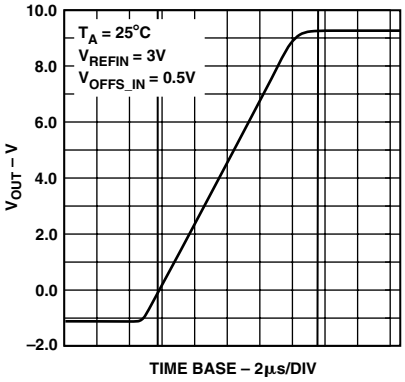



*Figure 12. Full-Scale Settling Time*

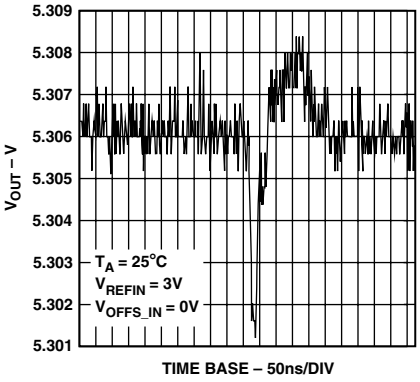



*Figure 13. Major Code Transition Glitch Impulse*

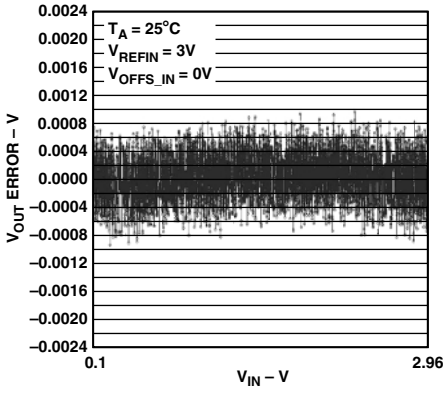



*Figure 14. $V_{IN}$ to $V_{OUT}$ Accuracy After Offset and Gain Adjustment (SHA Mode)*

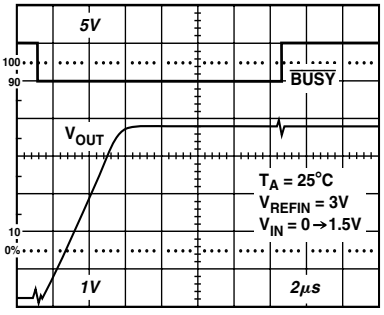



*Figure 15. Acquisition Time and Output Settling Time (SHA Mode)*

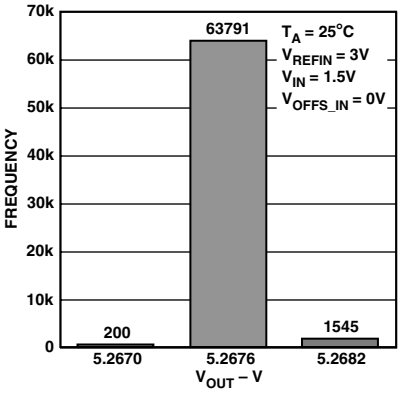



*Figure 16. SHA-Mode Repeatability (64K Acquisitions)*

## FUNCTIONAL DESCRIPTION

The AD5532 can be thought of as consisting of 32 DACs and an ADC (for SHA mode) in a single package. In DAC mode a 14-bit digital word is loaded into one of the 32 DAC registers via the serial interface. This is then converted (with gain and offset) into an analog output voltage ($V_{OUT}0$–$V_{OUT}31$).

To update a DAC's output voltage the required DAC is addressed via the serial port. When the DAC address and code have been loaded the selected DAC converts the code.

On power-on, all the DACs, including the offset channel, are loaded with zeros. The internal DAC outputs are at 50 mV typical (negative full-scale). If the OFFS_IN pin is driven by the on-board offset channel, the outputs $V_{OUT}0$ to $V_{OUT}31$ are also at 50 mV on power-on since OFFS_IN = 50 mV, $V_{OUT}$ = (Gain × $V_{DAC}$) –(Gain –1) × $V_{OFFS\_IN}$ = 50 mV.

### Output Buffer Stage—Gain and Offset

The function of the output buffer stage is to translate the 0 V–3 V output of the DAC to a wider range. This is done by gaining up the DAC output by 3.52/7 and offsetting the voltage by the voltage on OFFS_IN pin.

**AD5532-1/AD5532-3/AD5532-5:**

$$V_{OUT} = 3.52 \times V_{DAC} - 2.52 \times V_{OFFS\_IN}$$

**AD5532-2:**

$$V_{OUT} = 7 \times V_{DAC} - 6 \times V_{OFFS\_IN}$$

$V_{DAC}$ is the output of the DAC.
$V_{OFFS\_IN}$ is the voltage at the OFFS_IN pin.

The following table shows how the output range on $V_{OUT}$ relates to the offset voltage supplied by the user:

**Table I. Sample Output Voltage Ranges**

| $V_{OFFS\_IN}$ (V) | $V_{DAC}$ (V) | $V_{OUT}$ (AD5532-1/-3/-5) | $V_{OUT}$ (AD5532-2) |
|---|---|---|---|
| 0.5 | 0 to 3 | –1.26 to +9.3 | Headroom Limited |
| 1 | 0 to 3 | –2.52 to +8.04 | –6 to +15 |

$V_{OUT}$ is limited only by the headroom of the output amplifiers. $V_{OUT}$ must be within maximum ratings.

### Offset Voltage Channel

The offset voltage can be externally supplied by the user at OFFS_IN or it can be supplied by an additional offset voltage channel on the device itself. The offset can be set up in two ways. In SHA mode the required offset voltage is set up on $V_{IN}$ and acquired by the offset channel. In DAC mode the code corresponding to the offset value is loaded directly into the offset DAC. This offset channel's DAC output is directly connected to OFFS_OUT. By connecting OFFS_OUT to OFFS_IN this offset voltage can be used as the offset voltage for the 32 output amplifiers. It is important to choose the offset so that $V_{OUT}$ is within maximum ratings.

### Reset Function

The reset function on the AD5532 can be used to reset all nodes on this device to their power-on-reset condition. This is implemented by applying a low-going pulse of between 50 ns and 150 ns to the $\overline{\text{TRACK}}/\overline{\text{RESET}}$ pin on the device. If the applied pulse is less than 50 ns it is assumed to be a glitch and no operation takes place. If the applied pulse is wider than 150 ns this pin adopts its track function on the selected channel, $V_{IN}$ is switched to the output buffer and an acquisition on the channel will not occur until a rising edge of $\overline{\text{TRACK}}$.

### SHA Mode

In SHA mode the input voltage $V_{IN}$ is sampled and converted into a digital word. The noninverting input to the output buffer (gain and offset stage) is tied to $V_{IN}$ during the acquisition period to avoid spurious outputs while the DAC acquires the correct code. This is completed in 16 µs max. At this time the updated DAC output assumes control of the output voltage. The output voltage of the DAC is connected to the noninverting input of the output buffer. Since the channel output voltage is effectively the output of a DAC there is no droop associated with it. As long as power is maintained to the device the output voltage will remain constant until this channel is addressed again.

### Analog Input (SHA Mode)

The equivalent analog input circuit is shown in Figure 17. The Capacitor C1 is typically 20 pF and can be attributed to pin capacitance and 32 off-channels. When a channel is selected, an extra 7.5 pF (typ) is switched in. This Capacitor C2 is charged to the previously acquired voltage on that particular channel so it must charge/discharge to the new level. It is essential that the external source can charge/discharge this additional capacitance within 1 µs–2 µs of channel selection so that $V_{IN}$ can be acquired accurately. For this reason a low impedance source is recommended.

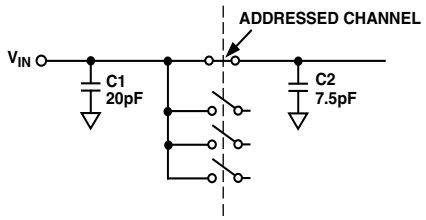



*Figure 17. Analog Input Circuit*

Large source impedances will significantly affect the performance of the ADC. This may necessitate the use of an input buffer amplifier.

### $\overline{\text{TRACK}}$ Function (SHA Mode)

Normally in SHA mode of operation, $\overline{\text{TRACK}}$ is held high and the channel begins to acquire when it is addressed. However, if $\overline{\text{TRACK}}$ is low when the channel is addressed, $V_{IN}$ is switched to the output buffer and an acquisition on the channel will not occur until a rising edge of $\overline{\text{TRACK}}$. At this stage the $\overline{\text{BUSY}}$ pin will go low until the acquisition is complete, at which point the DAC assumes control of the voltage to the output buffer and $V_{IN}$ is free to change again without affecting this output value.

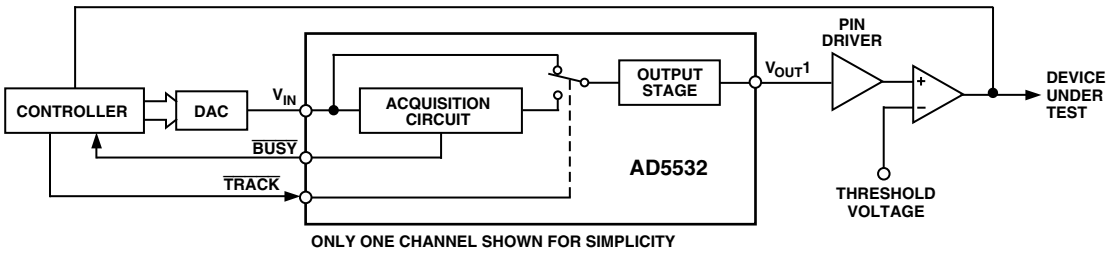



*Figure 18. Typical ATE Circuit Using $\overline{TRACK}$ Input*

This is useful in an application where the user wants to ramp up $V_{IN}$ until $V_{OUT}$ reaches a particular level (Figure 18). $V_{IN}$ does not need to be acquired continuously while it is ramping up. $\overline{TRACK}$ can be kept low and only when $V_{OUT}$ has reached its desired voltage is $\overline{TRACK}$ brought high. At this stage, the acquisition of $V_{IN}$ begins.

In the example shown, a desired voltage is required on the output of the pin driver. This voltage is represented by one input to a comparator. The microcontroller/microprocessor ramps up the input voltage on $V_{IN}$ through a DAC. $\overline{TRACK}$ is kept low while the voltage on $V_{IN}$ ramps up so that $V_{IN}$ is not continually acquired. When the desired voltage is reached on the output of the pin driver, the comparator output switches. The µC/µP then knows what code is required to be input in order to obtain the desired voltage at the DUT. The $\overline{TRACK}$ input is now brought high and the part begins to acquire $V_{IN}$. At this stage $\overline{BUSY}$ goes low until $V_{IN}$ has been acquired. The output buffer is then switched from $V_{IN}$ to the output of the DAC.

## MODES OF OPERATION

The AD5532 can be used in four different modes of operation. These modes are set by two mode bits, the first two bits in the serial word.

**Table II. Modes of Operation**

| Mode Bit 1 | Mode Bit 2 | Operating Mode |
|---|---|---|
| 0 | 0 | SHA Mode |
| 0 | 1 | DAC Mode |
| 1 | 0 | Acquire and Readback |
| 1 | 1 | Readback |

### 1. DAC Mode

In this standard mode a selected DAC register is loaded serially. This requires a 24-bit write (10 bits to address the relevant DAC plus an extra 14 bits of DAC data). MSB is written first. The user must allow 400 ns (min) between successive writes in DAC mode.

### 2. SHA Mode

In this mode a channel is addressed and that channel acquires the voltage on $V_{IN}$. This mode requires a 10-bit write (see Figure 21) to address the relevant channel ($V_{OUT}0$–$V_{OUT}31$, offset channel or all channels) MSB is written first.

### 3. Acquire and Readback Mode

This mode allows the user to acquire $V_{IN}$ and read back the data in a particular DAC register. The relevant channel is addressed (10-bit write, MSB first) and $V_{IN}$ is acquired in 16 µs (max). Following the acquisition, after the next falling edge of $\overline{SYNC}$, the data in the relevant DAC register is clocked out onto the $D_{OUT}$ line in a 14-bit serial format. The full acquisition time must elapse before the DAC register data can be clocked out.

### 4. Readback Mode

Again, this is a readback mode but no acquisition is performed. The relevant channel is addressed (10-bit write, MSB first) and on the next falling edge of $\overline{SYNC}$, the data in the relevant DAC register is clocked out onto the $D_{OUT}$ line in a 14-bit serial format. The user must allow 400 ns (min) between the last SCLK falling edge in the 10-bit write and the falling edge of $\overline{SYNC}$ in the 14-bit readback. The serial write and read words can be seen in Figure 19.

This feature allows the user to read back the DAC register code of any of the channels. In DAC mode this is useful in verification of write cycles. In SHA mode readback is useful if the system has been calibrated and the user wants to know what code in the DAC corresponds to a desired voltage on $V_{OUT}$. If the user requires this voltage again, he can input the code directly to the DAC register without going through the acquisition sequence.

## INTERFACES

### Serial Interface

The SER/$\overline{PAR}$ pin is tied high to enable the serial interface and to disable the parallel interface. The serial interface is controlled by four pins as follows:

***$\overline{SYNC}$, $D_{IN}$, SCLK***
Standard 3-wire interface pins. The $\overline{SYNC}$ pin is shared with the $\overline{CS}$ function of the parallel interface.

***$D_{OUT}$***
Data Out pin for reading back the contents of the DAC registers. The data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.

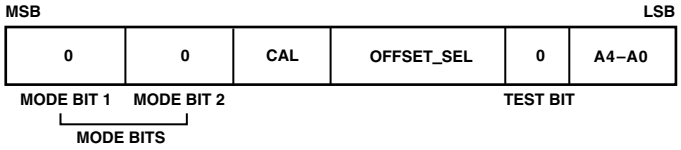
***Mode Bits***
There are four different modes of operation as described above.

***Cal Bit***
In DAC mode this is a test bit. When it is high it is used to load all zeros or all ones to the 32 DACs simultaneously. In SHA mode all 32 channels acquire $V_{IN}$ simultaneously when this bit is high. In SHA mode the acquisition time is then 45 µs (typ) and accuracy may be reduced. This bit is set low for normal operation.

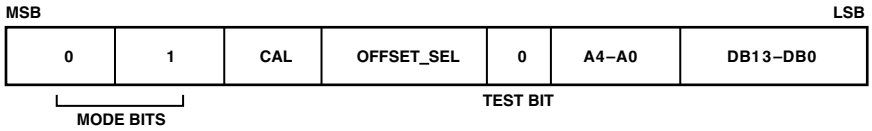
***Offset_Sel Bit***
If this is set high, the offset channel is selected and Bits A4–A0 are ignored.

***Test Bit***
This must be set low for correct operation of the part.

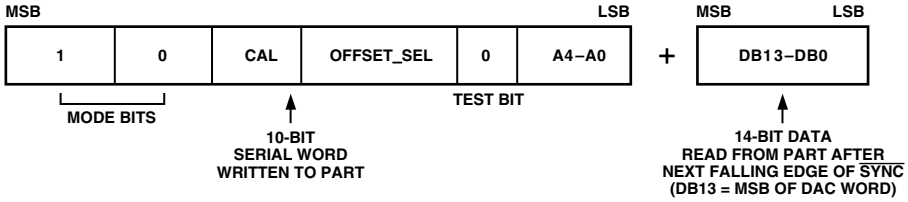
***A4–A0***
Used to address any one of the 32 channels (A4 = MSB of address, A0 = LSB).



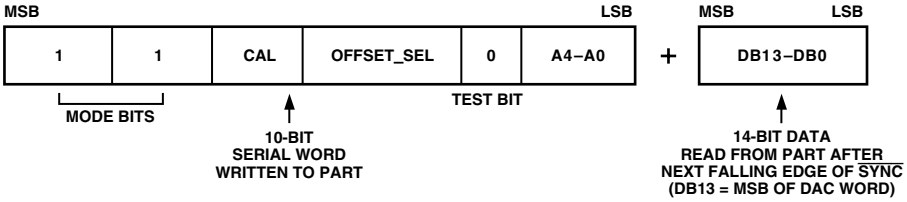

*a. 10-Bit Input Serial Write Word (SHA Mode)*




*b. 24-Bit Input Serial Write Word (DAC Mode)*




*c. Input Serial Interface (Acquire and Readback Mode)*




*d. Input Serial Interface (Readback Mode)*

*Figure 19. Serial Interface Formats*

***DB13–DB0***
These are used to write a 14-bit word into the addressed DAC register. Clearly, this is only valid when in DAC mode.

The serial interface is designed to allow easy interfacing to most microcontrollers and DSPs, e.g., PIC16C, PIC17C, QSPI, SPI, DSP56000, TMS320, and ADSP-21xx, without the need for any glue logic. When interfacing to the 8051, the SCLK must be inverted. The Microprocessor/Microcontroller Interface section explains how to interface to some popular DSPs and microcontrollers.

Figures 3, 4, and 5 show the timing diagram for a serial read and write to the AD5532. The serial interface works with both a continuous and a noncontinuous serial clock. The first falling edge of $\overline{\text{SYNC}}$ resets a counter that counts the number of serial clocks to ensure the correct number of bits are shifted in and out of the serial shift registers. Any further edges on $\overline{\text{SYNC}}$ are ignored until the correct number of bits are shifted in or out. Once the correct number of bits for the selected mode have been shifted in or out, the SCLK is ignored. In order for another serial transfer to take place the counter must be reset by the falling edge of $\overline{\text{SYNC}}$.

In readback, the first rising SCLK edge after the falling edge of $\overline{\text{SYNC}}$ causes $D_{OUT}$ to leave its high impedance state and data is clocked out onto the $D_{OUT}$ line and also on subsequent SCLK rising edges. The $D_{OUT}$ pin goes back into a high impedance state on the falling edge of the fourteenth SCLK. Data on the $D_{IN}$ line is latched in on the first SCLK falling edge after the falling edge of the $\overline{\text{SYNC}}$ signal and on subsequent SCLK falling edges. During readback $D_{IN}$ is ignored. The serial interface will not shift data in or out until it receives the falling edge of the $\overline{\text{SYNC}}$ signal.

**Parallel Interface (SHA Mode Only)**
The SER/$\overline{\text{PAR}}$ bit must be tied low to enable the parallel interface and disable the serial interface. The parallel interface is controlled by 9 pins.

***$\overline{CS}$***
Active low package select pin. This pin is shared with the $\overline{\text{SYNC}}$ function for the serial interface.

***$\overline{WR}$***
Active low write pin. The values on the address pins are latched on a rising edge of $\overline{\text{WR}}$.

***A4–A0***
Five address pins (A4 = MSB of address, A0 = LSB). These are used to address the relevant channel (out of a possible 32).

***Offset_Sel***
Offset select pin. This has the same function as the Offset_Sel bit in the serial interface. When it is high, the offset channel is addressed. The address on A4–A0 is ignored in this case.

***Cal***
When this pin is high, all 32 channels acquire $V_{IN}$ simultaneously. The acquisition time is then 45 µs (typ) and accuracy may be reduced.

## MICROPROCESSOR INTERFACING

### AD5532 to ADSP-21xx Interface

The ADSP-21xx family of DSPs are easily interfaced to the AD5532 without the need for extra logic.

A data transfer is initiated by writing a word to the TX register after the SPORT has been enabled. In a write sequence data is clocked out on each rising edge of the DSP's serial clock and clocked into the AD5532 on the falling edge of its SCLK. In readback 16 bits of data are clocked out of the AD5532 on each rising edge of SCLK and clocked into the DSP on the rising edge of SCLK. $D_{IN}$ is ignored. The valid 14 bits of data will be centered in the 16-bit RX register when using this configuration. The SPORT control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
ISCLK = 1, Internal Serial Clock
TFSR = RFSR = 1, Frame Every Word
IRFS = 0, External Framing Signal
ITFS = 1, Internal Framing Signal
SLEN = 1001, 10-Bit Data Words (SHA Mode Write)
SLEN = 0111, 3× 8-Bit Data Words (DAC Mode Write)
SLEN = 1111, 16-Bit Data Words (Readback Mode)

Figure 20 shows the connection diagram.

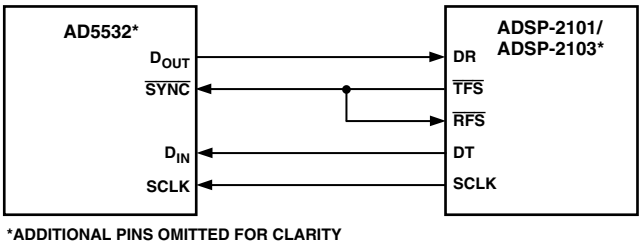



*Figure 20. AD5532 to ADSP-2101/ADSP-2103 Interface*

### AD5532 to MC68HC11

The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 0 and the Clock Phase Bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see *68HC11 User Manual*. SCK of the 68HC11 drives the SCLK of the AD5532, the MOSI output drives the serial data line ($D_{IN}$) of the AD5532 and the MISO input is driven from $D_{OUT}$. The $\overline{SYNC}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5532, the $\overline{SYNC}$ line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to transmit 10-data bits in SHA mode it is important to left-justify the data in the SPDR register. PC7 must be pulled low to start a transfer. It is taken high and pulled low again before any further read/write cycles can take place. A connection diagram is shown in Figure 21.

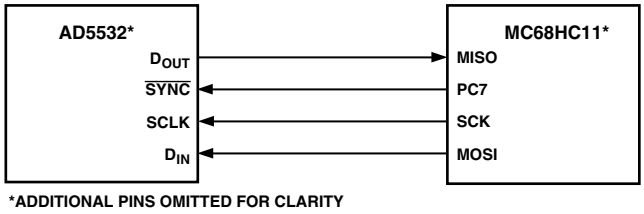



*Figure 21. AD5532 to MC68HC11 Interface*

### AD5532 to PIC16C6x/7x

The PIC16C6x/7x Synchronous Serial Port (SSP) is configured as an SPI Master with the Clock Polarity bit = 0. This is done by writing to the Synchronous Serial Port Control Register (SSPCON). See user *PIC16/17 Microcontroller User Manual*. In this example I/O port RA1 is being used to pulse $\overline{SYNC}$ and enable the serial port of the AD5532. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, two or three consecutive read/write operations are needed depending on the mode. Figure 22 shows the connection diagram.

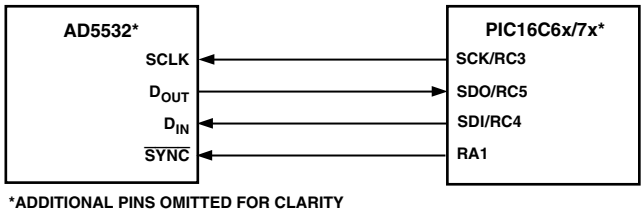



*Figure 22. AD5532 to PIC16C6x/7x Interface*

### AD5532 to 8051

The AD5532 requires a clock synchronized to the serial data. The 8051 serial interface must therefore be operated in Mode 0. In this mode serial data enters and exits through RxD and a shift clock is output on TxD. Figure 23 shows how the 8051 is connected to the AD5532. Because the AD5532 shifts data out on the rising edge of the shift clock and latches data in on the falling edge, the shift clock must be inverted. The AD5532 requires its data with the MSB first. Since the 8051 outputs the LSB first, the transmit routine must take this into account.

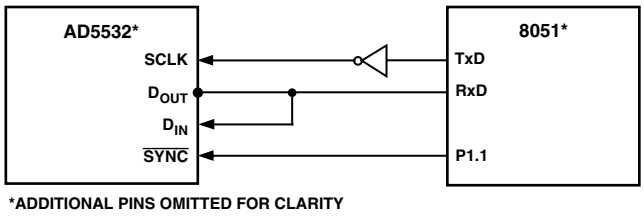



*Figure 23. AD5532 to 8051 Interface*

## APPLICATION CIRCUITS

### AD5532 in a Typical ATE System

The AD5532 is ideally suited for use in Automatic Test Equipment. Several DACs are required to control pin drivers, comparators, active loads and signal timing. Traditionally, sample-and-hold devices were used in this application.

The AD5532 has several advantages: no refreshing is required, there is no droop, pedestal error is eliminated and there is no need for extra filtering to remove glitches. Overall a higher level of integration is achieved in a smaller area (see Figure 24).

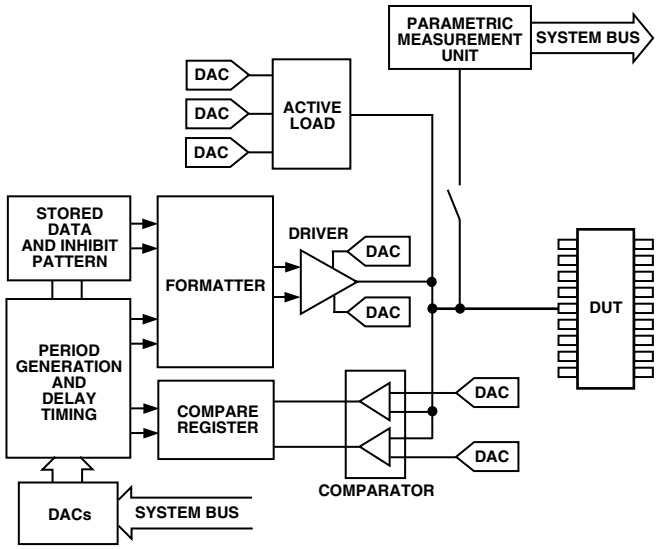



*Figure 24. AD5532 in an ATE System*

### Typical Application Circuit (SHA Mode)

The AD5532 can be used to set up voltage levels on 32 channels as shown in the circuit below. An AD780 provides the 3 V reference for the AD5532, and for the AD5541 16-bit DAC. A simple 3-wire interface is used to write to the AD5541. The DAC output is buffered by an AD820. It is essential to minimize noise on $V_{IN}$ and REFIN when laying out this circuit.

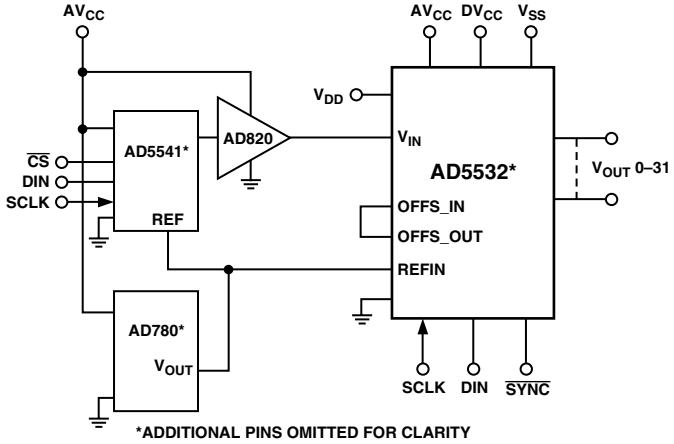



*Figure 25. Typical Application Circuit*

## POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5532 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the AD5532 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins ($V_{SS}$, $V_{DD}$, $AV_{CC}$) it is recommended to tie those pins together. The AD5532 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

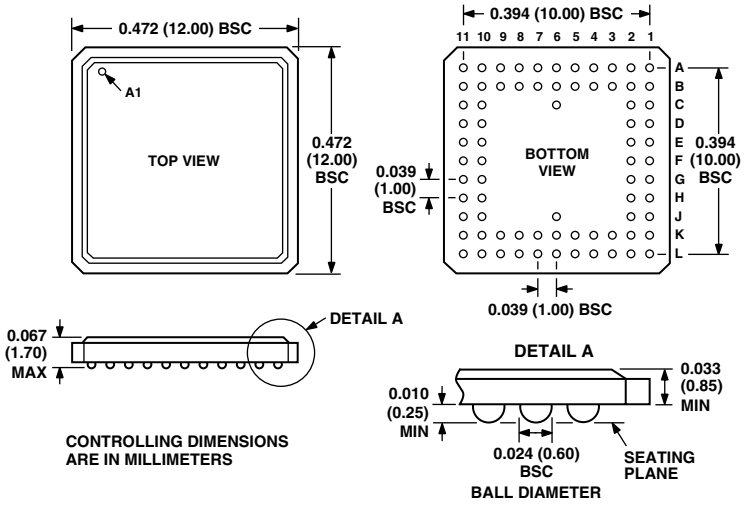
The power supply lines of the AD5532 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the $D_{IN}$ and SCLK lines will help reduce crosstalk between them (not required on a multilayer board as there will be a separate ground plane, but separating the lines will help). It is essential to minimize noise on $V_{IN}$ and REFIN lines.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 74-Lead LFBGA
### (BC-74)

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