MAXIM

Microprocessor Supervisory Circuits

MAX696/697

General Description

The MAX696/697 supervisory circuits reduce the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include μP reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MAX696/697 significantly improves system reliability and accuracy compared to that obtained with separate ICs or discrete components.

The MAX696 and MAX697 are supplied in 16 pin packages and perform six functions:

1. A Reset output during power-up, power-down and brownout conditions. The threshold for this "low line" reset is adjustable by an external voltage divider.
2. A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
3. Individual outputs for low line and watchdog fault conditions.
4. The Reset time may be left at its default value of 50 ms. or may be varied with an external capacitor or clock pulses.
5. A separate 1.3 volt threshold detector for power fail warning, low battery detection, or to monitor a power supply other than V_{CC}.

The MAX696 also has battery backup switching for CMOS RAM, CMOS microprocessor, or other low power logic.

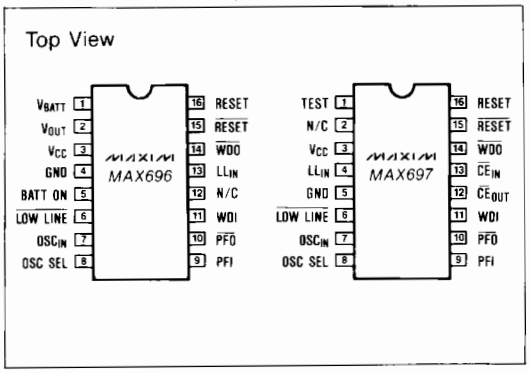
The MAX697 lacks battery backup switching, but has write protection pins ($\overline{CE}_{IN}$ and $\overline{CE}_{OUT}$) for CMOS RAM or EPROM. In addition, it consumes less than 250 microamperes.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μP Power Monitoring

Pin Configurations

Top View



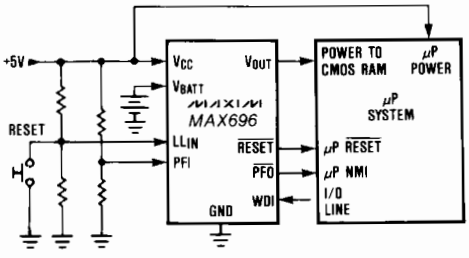
Features

- ◆ **Adjustable Low Line monitor and Power Down Reset**
- ◆ **Power OK/Reset Time Delay**
- ◆ **Watchdog Timer—100ms, 1.6 sec, or adjustable**
- ◆ **Minimum Component Count**
- ◆ **1μA Standby Current**
- ◆ **Battery Backup Power Switching (MAX696)**
- ◆ **Onboard Gating of Chip Enable Signals (MAX697)**
- ◆ **Separate Monitor for Power Fail or Low Battery Warning**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX696C/D	0°C to +70°C	Dice
MAX696CPE	0°C to +70°C	16 Lead Plastic DIP
MAX696CWE	0°C to +70°C	16 Lead Wide SO
MAX696EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX696EJE	-40°C to +85°C	16 Lead CERDIP
MAX696EWE	-40°C to +85°C	16 Lead Wide SO
MAX696MJE	-55°C to +125°C	16 Lead CERDIP
MAX697C/D	0°C to +70°C	Dice
MAX697CPE	0°C to +70°C	16 Lead Plastic DIP
MAX697CWE	0°C to +70°C	16 Lead Wide SO
MAX697EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX697EJE	-40°C to +85°C	16 Lead CERDIP
MAX697EWE	-40°C to +85°C	16 Lead Wide SO
MAX697MJE	-55°C to +125°C	16 Lead CERDIP

Typical Operating Circuit



MAX696 Typical Application

Call toll free 1-800-998-8800 for free samples or literature.

Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- V_{BATT} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{OUT} +0.5V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... short circuit protected
- All Other Outputs 20mA

Rate-of-Rise, V_{BATT}, V_{CC} 100V/μs

Operating Temperature Range
- C suffix ..... 0°C to +70°C
- E suffix ..... -40°C to +85°C
- M suffix ..... -55°C to +125°C

Power Dissipation
- 16 Pin Plastic DIP (Derate 7mW/°C above +70°C) 600mW
- 16 Pin Small Outline (Derate 7mW/°C above +70°C) 600mW
- 16 Pin CERDIP (Derate 10mW/°C above +85°C) 600mW

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (Soldering, 10 seconds) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range MAX696 V_{CC} MAX696 V_{BATT} MAX697 V_{CC}	T_A = Full	 3.0 2.0 3.0		 5.5 V_{CC} -0.3V 5.5	V
Supply Current (MAX697)	T_A = Full		160	300	μA
BATTERY BACKUP SWITCHING (MAX696)					
V_{OUT} Output Voltage	I_{OUT} = 1mA, T_A = Full I_{OUT} = 50mA, T_A = Full	V_{CC} -0.3 V_{CC} -0.5		V_{CC} -0.1 V_{CC} -0.25	V
V_{OUT} in Battery Backup Mode	I_{OUT} = 250μA, $V_{CC} < V_{BATT}$ -0.2V, T_A = Full	V_{BATT} -0.1		V_{BATT} -0.02	V
Supply Current (excludes I_{OUT})	I_{OUT} = 1mA I_{OUT} = 50mA		1.5 2.5	4 7	mA
Supply Current in Battery Backup Mode	V_{CC} = 0V, V_{BATT} = 2.8V, T_A = 25°C V_{CC} = 0V, V_{BATT} = 2.8V, T_A = Full		0.6	1 10	μA
Battery Standby Leakage Current	5.5V > V_{CC} > V_{BATT}+0.3V T_A = 25°C T_A = Full	-100 -1		+20 +0.02	nA μA
Battery Switchover Threshold V_{CC}-V_{BATT}	Power Up Power Down		70 50		mV
Battery Switchover Hysteresis			20		mV
BATT ON Output Voltage	I_{SINK} = 1.6mA			0.4	V
BATT ON Output Short Circuit Current	BATT ON = V_{OUT} = 2.4V Sink Current BATT ON = V_{OUT}, V_{CC} = 0V	 0.5	7 2.5	 25	mA μA
RESET AND WATCHDOG TIMER					
Low Line Voltage Threshold (LL_{IN})	V_{CC} = +5V, +3V, T_A = Full	1.25	1.30	1.35	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Timeout Delay	Figure 6. OSC SEL HIGH, V_{CC} = 5V	35	50	70	ms
Watchdog Timeout Period, Internal Oscillator	Long Period, V_{CC} = 5V Short Period, V_{CC} = 5V	1.0 70	1.6 100	2.25 140	sec ms
Watchdog Timeout Period, External Clock	Long Period Short Period	4032 960		4097 1025	Clock Cycles
Minimum WDI Input Pulse Width	V_{IL} = 0.4, V_{IH} = 3.5V, V_{CC} = 5V	200			ns
$\overline{RESET}$ and RESET Output Voltage (Note 3)	I_{SINK} = 400µA, V_{CC} = 2V, V_{BATT} = 0 I_{SINK} = 1.6mA, 3V < V_{CC} < 5.5V I_{SOURCE} = 1µA, V_{CC} = 5V	 3.5		0.4 0.4	V
$\overline{LOW\ LINE}$ and $\overline{WDO}$ Output Voltage	I_{SINK} = 800µA, T_A = Full I_{SOURCE} = 1µA, V_{CC} = 5V, T_A = Full	 3.5		0.4	V
Output Short Circuit Current	$\overline{RESET}$, RESET, $\overline{WDO}$, $\overline{LOW\ LINE}$	1	3	25	µA
WDI Input Threshold Logic Low Logic High (MAX696) Logic High (MAX697)	V_{CC} = 5V (Note 2)	 3.5 3.8		0.8	V
WDI Input Current	WDI = V_{OUT} WDI = 0V	 -50	20 -15	50	µA
POWER FAIL DETECTOR					
PFI Input Threshold	V_{CC} = 3V, 5V	1.2	1.3	1.4	V
PFI-LL_{IN} Threshold Difference	V_{CC} = 3V, 5V		±15	±50	mV
PFI Input Current			±0.01	±25	nA
LL_{IN} Input Current	MAX697	-25	±0.01	+25	nA
	MAX696	-500	±0.01	+25	
$\overline{PFO}$ Output Voltage	I_{SINK} = 1.6mA I_{SOURCE} = 1µA, V_{CC} = 5V	 3.5		0.4	V V
$\overline{PFO}$ Short Circuit Source Current	PFI = 0V, $\overline{PFO}$ = 0V	1	3	25	µA
CHIP ENABLE GATING (MAX697)					
$\overline{CE}$ IN Thresholds	V_{IL} V_{IH}, V_{CC} = 5V	 3.0		0.8	V
$\overline{CE}$ IN Pullup Current			3		µA
$\overline{CE}$ OUT Output Voltage	I_{SINK} = 1.6mA I_{SOURCE} = 800µA I_{SOURCE} = 1µA, V_{CC} = 0V	 V_{CC} -0.5V V_{CC} -0.05		0.4	V
$\overline{CE}$ Propagation Delay	V_{CC} = 5V		80	150	ns
OSCILLATOR					
OSC IN Input Current			±2		µA
OSC SEL Input Pullup Current			5		µA
OSC IN Frequency Range	OSC SEL = 0V	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V C_{OSC} = 47pF		4		kHz

Note 1: The input voltage limits on PFI and WDI may be exceeded providing the input current is limited to less than 10mA.
Note 2: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125 kilohms.
Note 3: T_A = Full Operating Range.

Microprocessor Supervisory Circuits

Pin Description

NAME	PIN		FUNCTION
	MAX696	MAX697	
V_{CC}	3	3	The +5V input.
V_{BATT}	1	—	Backup battery input. Connect to Ground if a backup battery is not used.
V_{OUT}	2	—	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	4	5	0V ground reference for all signals.
$\overline{RESET}$	15	15	$\overline{RESET}$ goes low whenever LL_{IN} falls below 1.3 volts or V_{CC} falls below the V_{BATT} input voltage. $\overline{RESET}$ remains low for 50ms after LL_{IN} goes above 1.3 volts. $\overline{RESET}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table 1.
WDI	11	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	9	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.3V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.
$\overline{PFO}$	10	10	$\overline{PFO}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
$\overline{CE}$ IN	—	13	The input to the $\overline{CE}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{CE}$ OUT	—	12	$\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and LL_{IN} is above 1.3V. See Figure 5.
BATT ON	5	—	BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 7mA and can directly drive the base of an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}.
$\overline{LOW\ LINE}$	6	6	$\overline{LOW\ LINE}$ goes low when LL_{IN} falls below 1.3 volts. It returns high as soon as LL_{IN} rises above 1.3 volts. See Figure 5, Reset Timing.
RESET	16	16	RESET is an active high output. It is the inverse $\overline{RESET}$.
OSC SEL	8	8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3μA internal pullup. See Table 1.
OSC IN	7	7	OSC IN sets the Reset delay timing and Watchdog timeout period when OSC SEL floats or is driven low. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 7. When OSC SEL is high, OSC IN selects between fast and slow Watchdog timeout periods.
$\overline{WDO}$	14	14	The Watchdog Output, $\overline{WDO}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.
NC	12	2	NO CONNECT. Leave this pin open.
LL_{IN}	13	4	LOW LINE INPUT. LL_{IN} is the CMOS input to a comparator whose other input is a precision 1.3 volt reference. The output is $\overline{LOW\ LINE}$ and is also connected to the reset pulse generator. See Figure 2.
TEST	—	1	Used during Maxim manufacture only. Always ground this pin.

Typical Applications

MAX696

A typical connection for the MAX696 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 50mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 7mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 200Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1μA maximum when V_{CC} is between 0V and V_{BATT} -700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a $\overline{RESET}$ output to hold the microprocessor's $\overline{RESET}$ line low when LL_{IN} is below 1.3V. An internal monostable holds $\overline{RESET}$ low for 50ms after LL_{IN} rises above 1.3V. This prevents repeated toggling of $\overline{RESET}$ even if the V_{CC} power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, $\overline{RESET}$ must be held low until the microprocessor clock oscillator has started. The power-up $\overline{RESET}$ pulse lasts 50ms to allow for this oscillator start-up time. An inverted, active high, RESET output is also supplied.

Power Fail Detector

The MAX696 issues a non-maskable interrupt (NMI) to the microprocessor when a power failure occurs. The power line is monitored via two external resistors connected to the Power Fail Input (PFI). When the voltage at PFI falls below 1.3V, the Power Fail Output ($\overline{PFO}$) drives the processor's NMI input low. An earlier power fail warning can be generated if the unregulated DC input of the regulator is available for monitoring.

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI is not toggled, the MAX696 will issue a 50ms $\overline{RESET}$ pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new $\overline{RESET}$ pulse is issued every 1.6 seconds until WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{WDO}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{WDO}$ goes low it remains low until a transition occurs at WDI while $\overline{RESET}$ is high. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 7.

MAX697

The MAX697 is nearly identical to the MAX696. The MAX697 lacks the battery backup feature, so it does not have the V_{BATT}, V_{OUT}, or BATT ON pins. This allows the MAX697 to consume less than 250 microamperes, and it allows the inclusion of RAM write protection pins. See Figure 2.

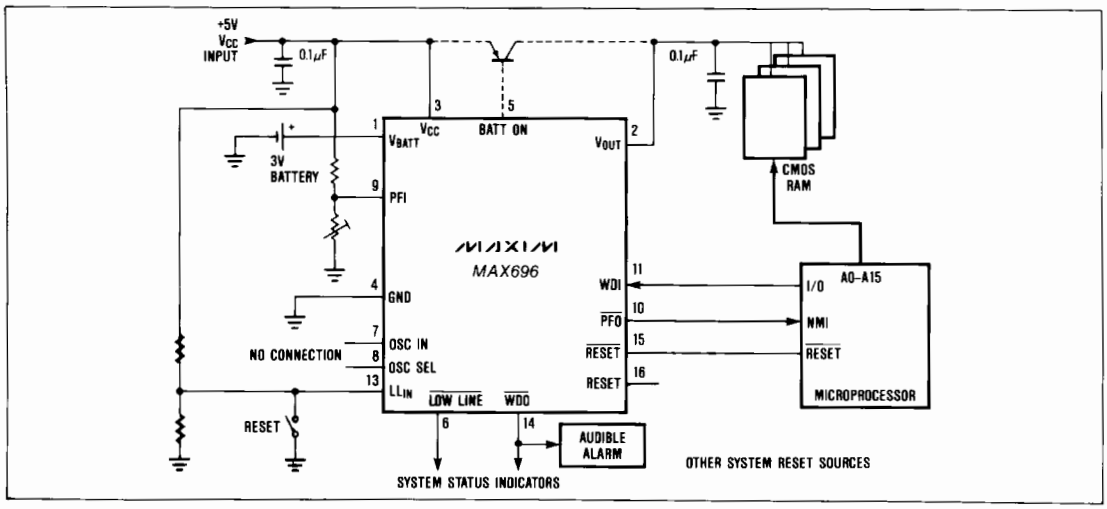
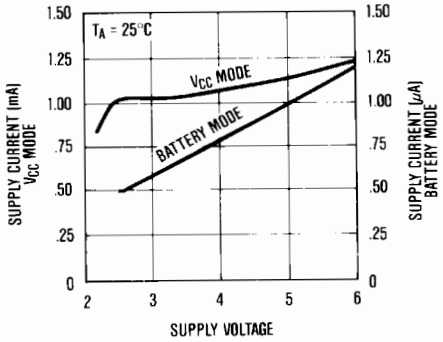


Figure 1. MAX696 Typical Application

MAX696
SUPPLY CURRENT AS A FUNCTION
OF SUPPLY VOLTAGE



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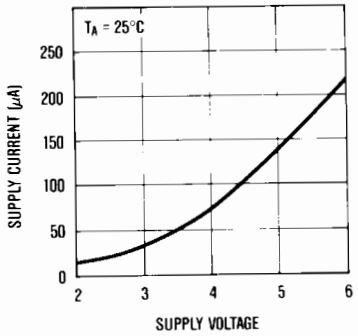
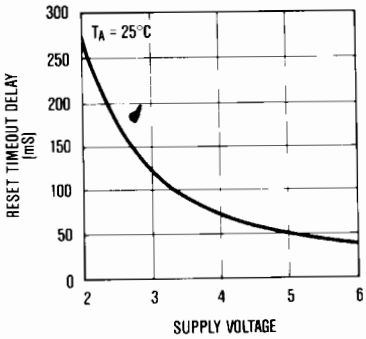


RESET TIMEOUT DELAY AS A
FUNCTION OF SUPPLY VOLTAGE



Detailed Description

Battery-Switchover and V_{OUT} (MAX696)

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and when V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (See Figure 3). The switchover comparator has 20mV of hysteresis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 50mA output current capability. Use an external PNP pass transistor in parallel with the internal transistor if the output current requirement at V_{OUT} exceeds 50mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output can directly drive the base of the external transistor.

It should be noted that the MAX696 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns. A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 200Ω MOSFET connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT} the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} -700mV) the typical supply current is only 600nA typical, 1µA maximum.

The MAX696 operates with battery voltages from 2.0V to 4.25V. The battery voltage should not be within 0.5V of V_{CC} or switchover may occur. High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup. The capacitor charging voltage should include a diode to limit the fully charged voltage to approximately 0.5V less than V_{CC}. The charging resistor for rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists if the resistor is connected to V_{CC}.

A small leakage current of typically 10nA (20nA max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged, and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf-life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum current (20nA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the state of the inputs and output in the low power battery backup mode.

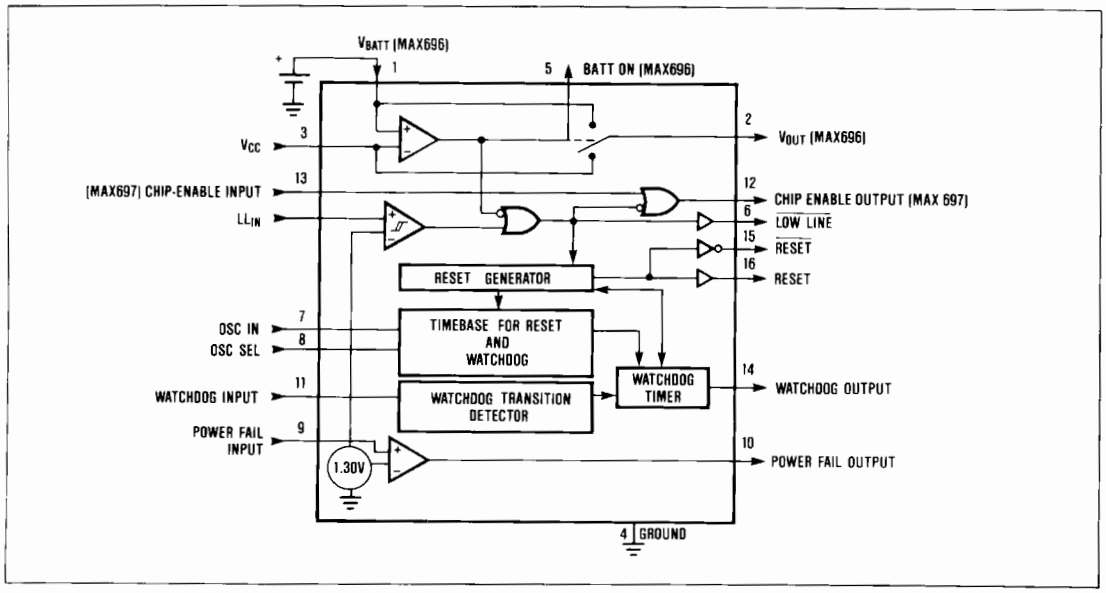


Figure 2. MAX696/697 Block Diagram

Microprocessor Supervisory Circuits

Reset Output

$\overline{RESET}$ is an active low output which goes low whenever LL_{IN} falls below 1.3 volts. It will remain low until LL_{IN} rises above 1.312 volts for 50 milliseconds. (See Figures 4 and 5.)

The guaranteed minimum and maximum low line thresholds of the MAX696/697 are 1.2 and 1.4 volts. The LL_{IN} comparator has approximately 12mV of hysteresis.

The response time of the reset voltage comparator is about 100 microseconds. LL_{IN} should be bypassed to ensure that glitches do not activate RESET output.

$\overline{RESET}$ also goes low if the Watchdog Timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{RESET}$ has an internal 3μA pullup, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pullup resistor.

$\overline{CE}$ Gating and RAM Write Protection

The MAX697 uses two pins to control the Chip Enable or Write inputs of CMOS RAMs. When LL_{IN} is > 1.3V, $\overline{CE}$ OUT is a buffered replica of $\overline{CE}$ IN, with a 50ns propagation delay. If LL_{IN} input falls below 1.3V (1.2 min., 1.4 max.) an internal gate forces $\overline{CE}$ OUT high, independent of $\overline{CE}$ IN. The $\overline{CE}$ output is also forced high when V_{CC} is less than V_{BATT}. (See Figure 4.)

$\overline{CE}$ OUT typically drives the $\overline{CE}$, $\overline{CS}$ or $\overline{Write}$ input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{CE}$ OUT to drive the $\overline{Store}$ or $\overline{Write}$ inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{CE}$ OUT is too long, connect $\overline{CE}$ IN to GND and use the resulting $\overline{CE}$ OUT to control a high speed external logic gate. A second alternative is to AND the $\overline{LOW\ LINE}$ output with the $\overline{CE}$ or $\overline{WR}$ signal. An external logic gate and the $\overline{RESET}$ output of the MAX696/697 can also be used for CMOS RAM write protection.

1.25V Comparator and Power Fail Warning

The Power Fail Input (PFI) is compared to an internal 1.3V reference. The Power Fail Output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.3V. Typically PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's V_{CC} regulator or the regulated output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3V several milliseconds before the LL_{IN} falls below 1.3V. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before LL_{IN} falls below 1.3V and the $\overline{RESET}$ output goes low.

The Power Fail Detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the Power Fail Detector comparator is turned off and $\overline{PFO}$ is forced low when V_{CC} is lower than the V_{BATT} input voltage.

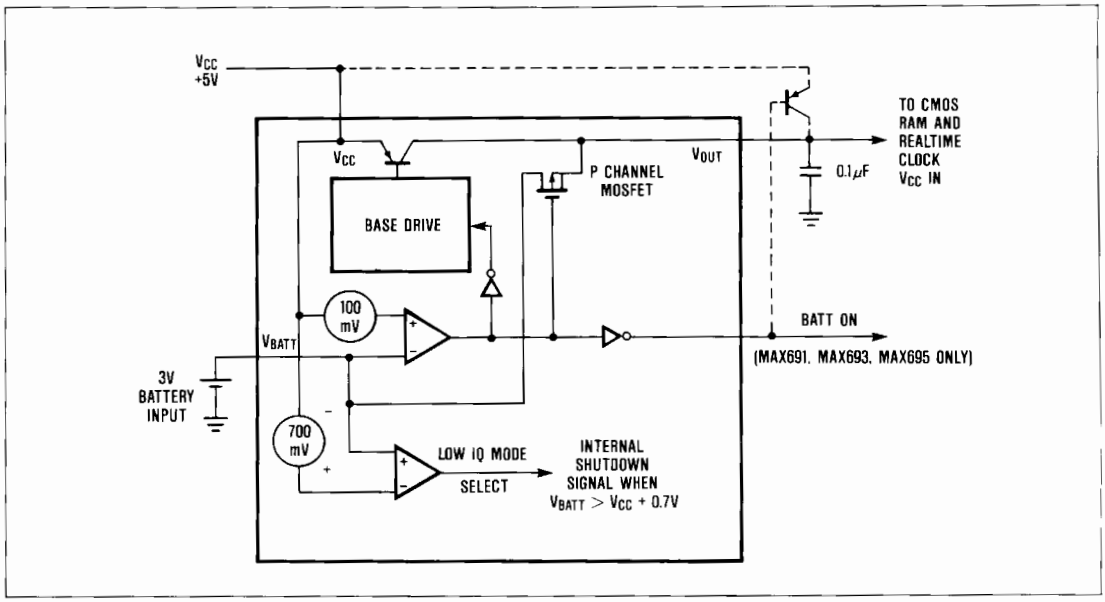


Figure 3. MAX696 Battery-Switchover Block Diagram

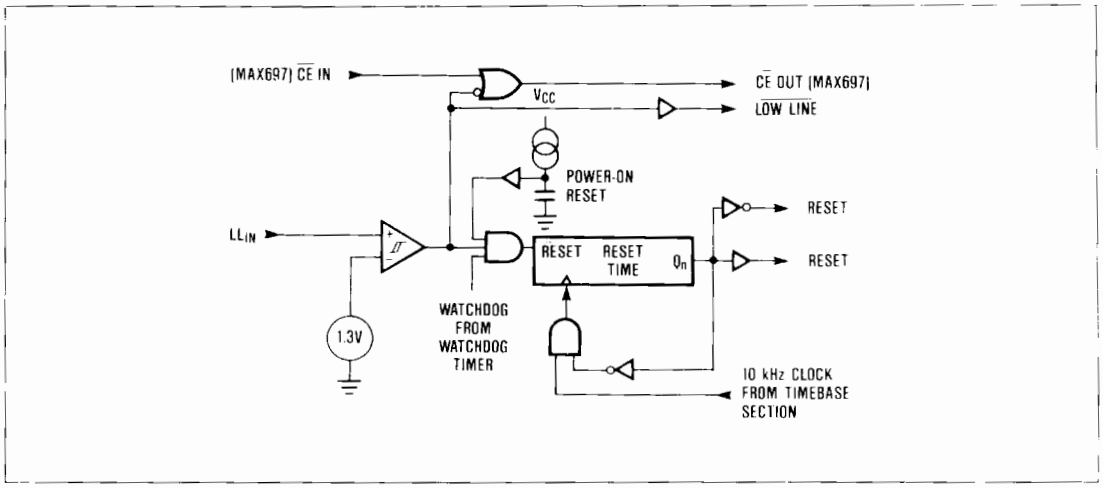


Figure 4. Reset Block Diagram

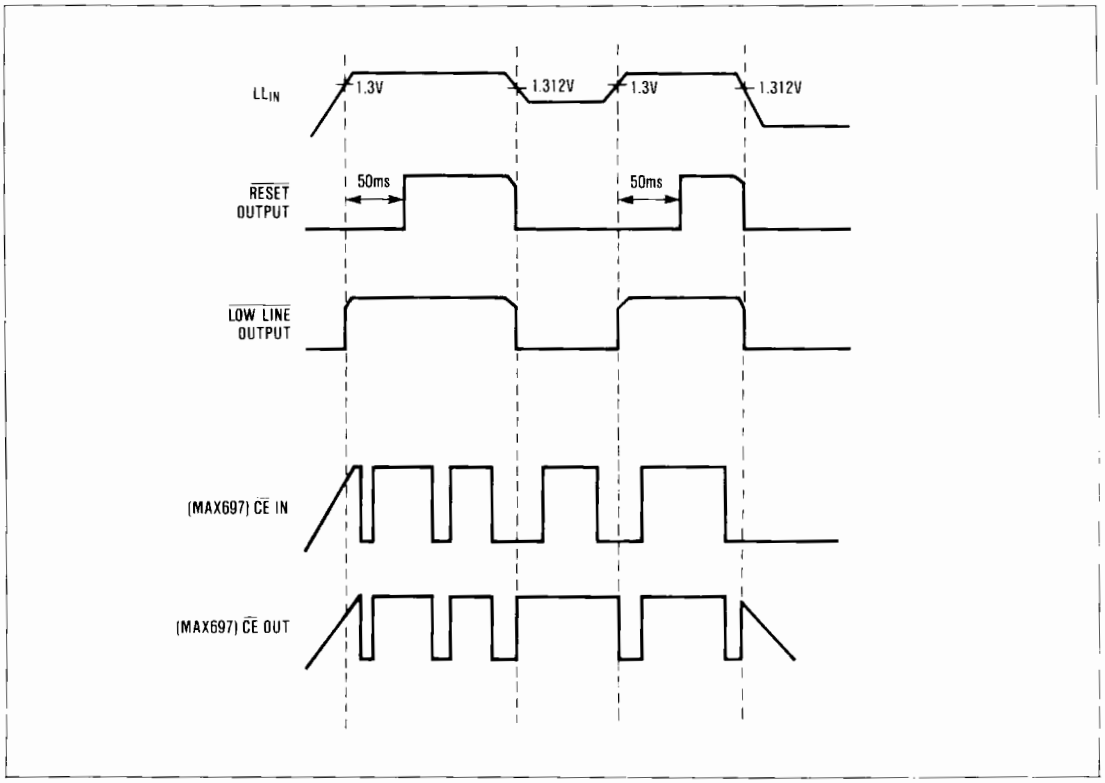


Figure 5. MAX697 Reset Timing

Microprocessor Supervisory Circuits

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50 milliseconds $\overline{\text{RESET}}$ pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MAX696/697 has a longer timeout period after a reset is issued. The normal timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone high. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by LL_{IN} falling below 1.3V. If WDI remains either high or low, reset pulses will be issued every 1.6 seconds. The watchdog monitor can be deactivated by floating the Watchdog Input (WDI).

The Watchdog Output $\overline{\text{WDO}}$ goes low if the watchdog timer "times out," and it remains low until set high by the next transition on the watchdog input. $\overline{\text{WDO}}$ is also set high when LL_{IN} goes below 1.3V.

The watchdog timeout period defaults to 1.6 seconds and the reset pulse width defaults to 50ms. The MAX696 and MAX697 allow these times to be adjusted per Table 1.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100ms watchdog timeout periods. In either case, immediately after a reset the timeout period is 1.6 seconds. This gives the microprocessor time to reinitialize the system. WD transmissions while $\overline{\text{RESET}}$ is low are ignored. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70ms.

Application Hints

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is non-inverting, hysteresis can be added by connecting a resistor between the PFO output and the PFI input as shown in Figure 7. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 8). The drawback to this circuit is that a software fault may erroneously 3-state the buffer, thereby preventing the MAX690 from detecting that the microprocessor is no longer working. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 9. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01μF capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100ms or the 1.6 sec period is chosen, depending on which diode in Figure 9 is used.

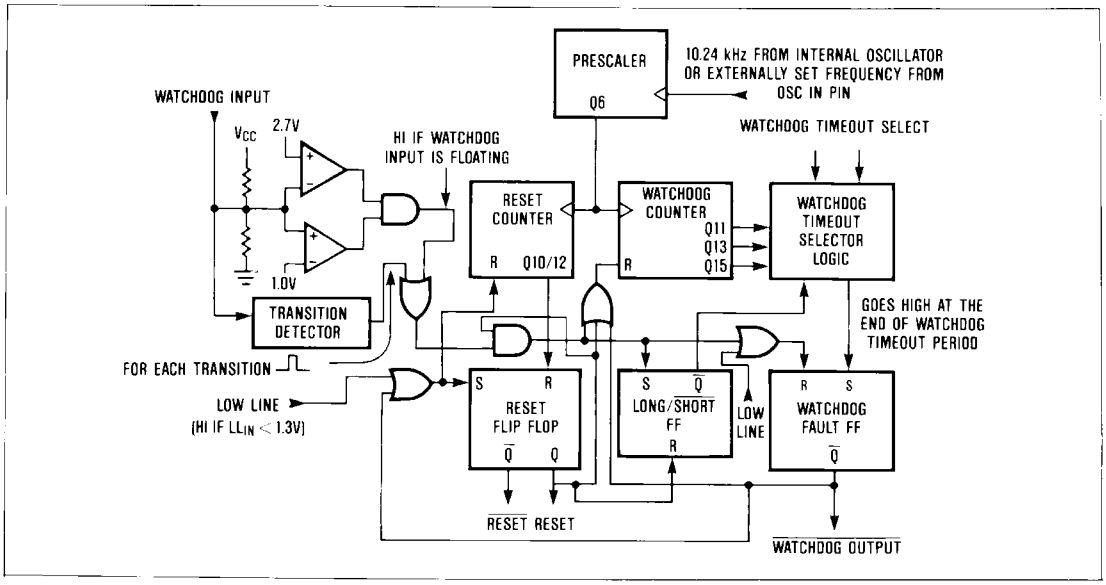


Figure 6. Watchdog Timer Block Diagram

Table 1. MAX696 and MAX697 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL (Note 3)	OSC IN	WATCHDOG TIMEOUT PERIOD NORMAL	WATCHDOG TIMEOUT PERIOD IMMEDIATELY AFTER RESET	RESET TIMEOUT PERIOD
Low	External Clock Input	1024 clks	4096 clks	512 clks
Low	External Capacitor	$\frac{400ms}{47pf} \times C$	$\frac{1.6\ sec}{47pf} \times C$	$\frac{200ms}{47pf} \times C$
High/Floating	Low	100ms	1.6 sec	50ms
High/Floating	Floating	1.6 sec	1.6 sec	50ms

Note 1: When the MAX696/697 OSC SEL pin is low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is $F_{OSC}(Hz) = \frac{184,000}{C_{OSC}(pF)}$

Note 2: See Electrical Characteristics Table for minumum and maximum timing values.

Note 3: "HIGH" for the OSC SEL pin should be connected to V_{OUT}, not V_{CC} (on MAX696).

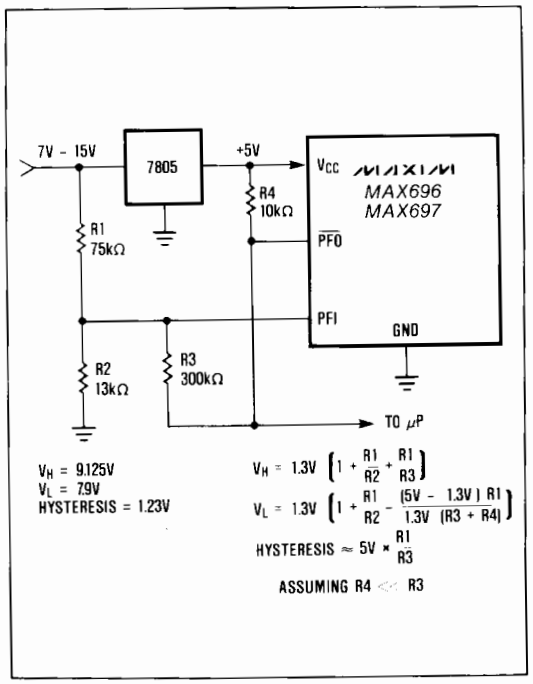


Figure 7. Adding Hysteresis to the Power Fail Voltage Comparator

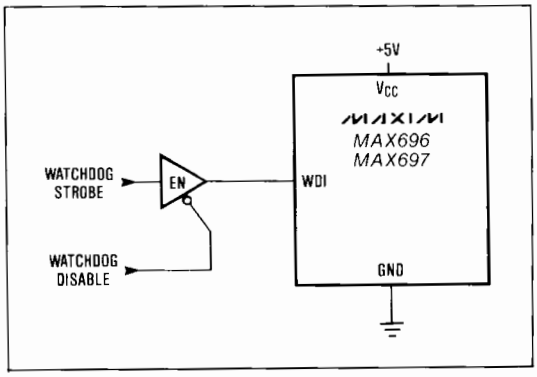


Figure 8. Disabling the Watchdog Under Program Control

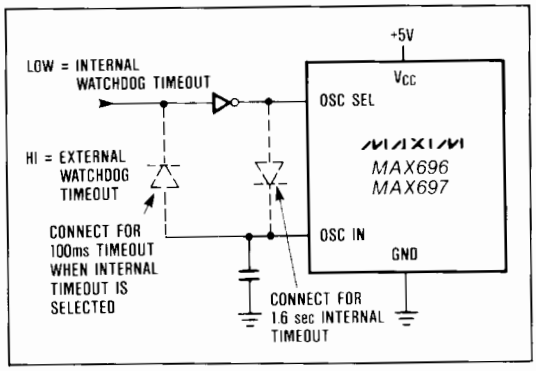


Figure 9. Selecting Internal or External Watchdog Timeout

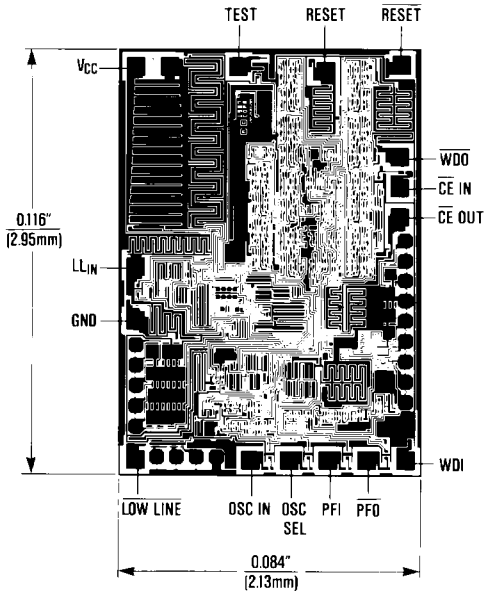
Microprocessor Supervisory Circuits

Table 2. Input and Output Status in Battery Backup Mode

V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET. (MAX696 only)
$\overline{RESET}$	Logic low
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low
BATT ON	Logic high (MAX696 only)
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high
PFI	The Power Fail Comparator is turned off and the Power Fail Input voltage has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low
$\overline{CE}$ IN	$\overline{CE}$ IN is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current. (MAX697 only)
$\overline{CE}$ OUT	Logic high (MAX697 only)
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12μA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} + 100mV and V_{BATT} - 700mV. The supply current is 1μA maximum when V_{CC} is less than V_{BATT} - 700mV.

Chip Topography

MAX697



MAX696