19-3439; Rev 0; 10/04

EVALUATION KIT AVAILABLE

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

General Description

The MAX6872/MAX6873 EEPROM-configurable, multivoltage supply sequencers/supervisors monitor several voltage detector inputs and four general-purpose logic inputs. The MAX6872/MAX6873 feature programmable outputs for highly configurable power-supply sequencing applications. The MAX6872 features six voltage detector inputs and eight programmable outputs, while the MAX6873 features four voltage detector inputs and five programmable outputs. Manual reset and margin disable inputs offer additional flexibility.

All voltage detectors offer two configurable thresholds for undervoltage/overvoltage or dual undervoltage detection. One high voltage input (IN1) provides detector threshold voltages from +2.5V to +13.2V in 50mV increments, or from +1.25V to +7.625V in 25mV increments. A bipolar input (IN2) provides detector threshold voltages from ±2.5V to ±15.25V in 50mV increments, or from ±1.25V to ±7.625V in 25mV increments. Positive inputs (IN3–IN6) provide detector threshold voltages from +1V to +5.5V in 20mV increments, or from +0.5V to +3.05V in 10mV increments.

Programmable output stages control power-supply sequencing or system resets/interrupts. Programmable output options include: active-high, active-low, open-drain, weak pullup, push-pull, and charge pump. Programmable timing delay blocks configure each output to wait between 25µs and 1600ms before deasserting. A fault register logs the condition that caused each output to assert (undervoltage, overvoltage, manual reset, etc.).

An SMBus™-/I²C-compatible, serial data interface programs and communicates with the configuration EEPROM, the configuration registers, the internal 4kb user EEPROM, and the fault registers of the MAX6872/MAX6873.

The MAX6872/MAX6873 are available in a 7mm x 7mm x 0.8mm 32-pin thin QFN package and operate over the extended -40°C to +85°C temperature range.

Applications

Telecommunications/Central Office Systems
Networking Systems
Servers/Workstations
Base Stations
Storage Equipment
Multimicroprocessor/Voltage Systems

Pin Configurations, Typical Operating Circuit, and Selector Guide appear at end of data sheet.

Features

- **Six (MAX6872) or Four (MAX6873) Configurable Input Voltage Detectors**
  - **One High Voltage Input (+1.25V to +7.625V or +2.5V to +13.2V Thresholds)**
  - **One Bipolar Voltage Input (±1.25V to ±7.625V or ±2.5V to ±15.25V Thresholds)**
  - **Four (MAX6872) or Two (MAX6873) Positive Voltage Inputs (+0.5V to +3.05V or +1V to +5.5V Thresholds)**
- **Four General-Purpose Logic Inputs**
- **Two Configurable Watchdog Timers**
- **Eight (MAX6872) or Five (MAX6873) Programmable Outputs**
  - **Active-High, Active-Low, Open-Drain, Weak Pullup, Push-Pull, Charge-Pump**
  - **Timing Delays from 25µs to 1600ms**
- **Margining Disable and Manual Reset Controls**
- **4kb Internal User EEPROM**
  - **Endurance: 100,000 Erase/Write Cycles**
  - **Data Retention: 10 Years**
- **I²C/SMBus-Compatible Serial Configuration/Communication Interface**
- **±1% Threshold Accuracy**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6872ETJ	-40°C to +85°C	32 Thin QFN	T3277-2
MAX6873ETJ	-40°C to +85°C	32 Thin QFN	T3277-2

SMBus is a trademark of Intel Corp.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
IN3–IN6, ABP, SDA, SCL, A0, A1,
GPI1–GPI4, $\overline{MR}$, $\overline{MARGIN}$, PO5–PO8
(MAX6872), PO3–PO5 (MAX6873).....-0.3V to +6V
IN1, PO1–PO4 (MAX6872), PO1–PO2 (MAX6873)...-0.3V to +14V
IN2.....-20V to +20V
DBP .....-0.3V to +3V
Input/Output Current (all pins).....±20mA

Continuous Power Dissipation (T_A = +70°C)
32-Pin 7mm x 7mm Thin QFN
(derate 33.3mW/°C above +70°C).....2667mW
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1} = +6.5V to +13.2V, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 3)	V_{IN1}	Voltage on IN1 to ensure the device is fully operational, IN3–IN6 = GND		4.0		13.2	V
	V_{IN3} to V_{IN6}	Voltage on any one of IN3–IN6 to ensure the device is fully operational, IN1 = GND		2.7		5.5	
IN1 Supply Voltage (Note 3)	V_{IN1P}	Minimum voltage on IN1 to guarantee that the device is powered through IN1				6.5	V
Undervoltage Lockout	V_{UVLO}	Minimum voltage on one of IN3–IN6 to guarantee the device is EEPROM configured.				2.5	V
Supply Current	I_{CC}	V_{IN1} = +13.2V, IN2–IN6 = GND, no load			1.2	1.5	mA
		Writing to configuration registers or EEPROM, no load			1.3	2	mA
Threshold Range	V_{TH}	V_{IN1} (50mV increments)		2.5		13.2	V
		V_{IN1} (25mV increments)		1.250		7.625	
		V_{IN2} (50mV increments)		±2.50		±15.25	
		V_{IN2} (25mV increments)		±1.250		±7.625	
		V_{IN3}–V_{IN6} (20mV increments)		1.0		5.5	
		V_{IN3}–V_{IN6} (10mV increments)		0.50		3.05	
Threshold Accuracy		IN1–IN6 positive, $V_{IN\_}$ falling	T_A = +25°C	-1.0		+1.0	%
			T_A = -40°C to +85°C	-1.5		+1.5	
		-15.25V ≤ V_{IN2} ≤ -5V, V_{IN2} falling	T_A = +25°C	-1.5		+1.5	
			T_A = -40°C to +85°C	-2		+2	
		-5V ≤ V_{IN2} ≤ 0, V_{IN2} falling	T_A = +25°C	-75		+75	mV
			T_A = -40°C to +85°C	-100		+100	
Threshold Hysteresis	$V_{TH-HYST}$				0.3		% V_{TH}
Reset Threshold Temperature Coefficient	ΔV_{TH}/°C				10		ppm/°C
Threshold-Voltage Differential Nonlinearity	V_{TH} DNL			-1		+1	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = +6.5V to +13.2V, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN1 Input Leakage Current	I_{LIN1}	For V_{IN1} < the highest of V_{IN3}–V_{IN6}			100	140	µA
IN2 Input Impedance	R_{IN2}			160	230	320	kΩ
IN3–IN6 Input Impedance	R_{IN3} to R_{IN6}	V_{IN1} > 6.5V		70	100	145	kΩ
Power-Up Delay	t_{PU}	$V_{ABP} \geq V_{UVLO}$				3.5	ms
IN_ to PO_ Delay	t_{DPO}	$V_{IN\_}$ falling or rising, 100mV overdrive			25		µs
PO_ Timeout Period	t_{RP}	Register contents (Table 23)	000		25		µs
			001	1.406	1.5625	1.719	ms
			010	5.625	6.25	6.875	
			011	22.5	25	27.5	
			100	45	50	55	
			101	180	200	220	
			110	360	400	440	
			111	1440	1600	1760	
PO1–PO4 (MAX6872), PO1–PO2 (MAX6873) Output Low (Note 3)	V_{OL}	$V_{ABP} \geq$ +2.5V, I_{SINK} = 500µA				0.3	V
		$V_{ABP} \geq$ +4.0V, I_{SINK} = 2mA				0.4	
PO5–PO8 (MAX6872), PO3–PO5 (MAX6873) Output Low (Note 3)	V_{OL}	$V_{ABP} \geq$ +2.5V, I_{SINK} = 1mA				0.3	V
		$V_{ABP} \geq$ +4.0V, I_{SINK} = 4mA				0.4	
PO1–PO8 Output Initial Pulldown Current	I_{PD}	$V_{ABP} \leq V_{UVLO}$, $V_{PO\_}$ = 0.8V			10	40	µA
PO1–PO8 Output Open-Drain Leakage Current	I_{LKG}	Output high impedance		-1		+1	µA
PO1–PO8 Output Pullup Resistance, Weak Pullup Selected	R_{PU}	$V_{PO\_}$ = 2V		6.6	10	15	kΩ
PO1–PO4 (MAX6872), PO1–PO2 (MAX6873) Turn-On Time, Charge Pump Selected (Note 4)	t_{ON}	$C_{PO\_}$ = 1500pF, V_{ABP} = +3.3V, $V_{PO\_}$ = +7.8V		0.5	1.5	3.0	ms
PO1–PO4 (MAX6872), PO1–PO2 (MAX6873) Turn-Off Time, Charge Pump Selected	t_{OFF}	$C_{PO\_}$ = 1500pF, V_{ABP} = +3.3V, $V_{PO\_}$ = +0.5V			30		µs
PO1–PO4 (MAX6872), PO1–PO2 (MAX6873) Output High, Charge Pump Selected (Notes 3, 4)	V_{OHCP}	With respect to V_{ABP}, $I_{PO\_}$ < 100nA			5.5		V
		With respect to V_{ABP}, $I_{PO\_}$ < 1µA		4.0	5.0	6.0	
PO5–PO8 (MAX6872), PO3–PO5 (MAX6873) Output High, Push-Pull Selected (Note 3)	V_{OH}	Any one of V_{IN3}–V_{IN6} ≥ +2.7V, I_{SOURCE} = 10mA, output pulled up to the same IN_		1.5			V
		Any one of V_{IN3}–V_{IN6} ≥ +2.7V, I_{SOURCE} = 1mA, output pulled up to the same IN_		0.8 x $V_{IN\_}$			
		Any one of V_{IN3}–V_{IN6} ≥ +4.5V, I_{SOURCE} = 2mA, output pulled up to the same IN_		0.8 x $V_{IN\_}$			

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = +6.5V to +13.2V, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{MR}$, $\overline{MARGIN}$, GPI_ Input Voltage	V_{IL}					0.8	V
	V_{IH}			1.4			
$\overline{MR}$ Input Pulse Width	t_{MR}			1			µs
$\overline{MR}$ Glitch Rejection					100		ns
$\overline{MR}$ to PO_ Delay	t_{DMR}				2		µs
$\overline{MR}$ to V_{DBP} Pullup Current	I_{MR}	$V_{\overline{MR}}$ = +1.4V		5	10	15	µA
$\overline{MARGIN}$ to V_{DBP} Pullup Current	I_{MARGIN}	$V_{\overline{MARGIN}}$ = +1.4V		5	10	15	µA
GPI_ to PO_ Delay	$t_{DGPI\_}$				200		ns
GPI_ Pulldown Current	$I_{GPI\_}$	$V_{GPI\_}$ = +0.8V		5	10	15	µA
Watchdog Input Pulse Width	t_{WDI}	GPI_ configured as a watchdog input		50			ns
Watchdog Timeout Period	t_{WD}	Register contents (Table 26)	000	5.625	6.25	6.875	ms
			001	22.5	25	27.5	
			010	90	100	110	
			011	360	400	440	
			100	1.44	1.6	1.76	s
			101	5.76	6.4	7.04	
			110	23.04	25.6	28.16	
			111	92.16	102.4	112.64	
SERIAL INTERFACE LOGIC (SDA, SCL, A0, A1)							
Logic Input Low Voltage	V_{IL}					0.8	V
Logic Input High Voltage	V_{IH}			2.0			V
Input Leakage Current	I_{LKG}			-1		+1	µA
Output Voltage Low	V_{OL}	I_{SINK} = 3mA				0.4	V
Input/Output Capacitance	$C_{I/O}$				10		pF

TIMING CHARACTERISTICS

(IN1 = GND, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 2)						
Serial Clock Frequency	f_{SCL}				400	kHz
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Bus-Free Time	t_{BUF}		1.3			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Data-In Setup Time	$t_{SU:DAT}$		100			ns
Data-In Hold Time	$t_{HD:DAT}$		0		900	ns
Receive SCL/SDA Minimum Rise Time	t_R	(Note 5)		20 + 0.1 x C_{BUS}		ns
Receive SCL/SDA Maximum Rise Time	t_R	(Note 5)		300		ns
Receive SCL/SDA Minimum Fall Time	t_F	(Note 5)		20 + 0.1 x C_{BUS}		ns
Receive SCL/SDA Maximum Fall Time	t_F	(Note 5)		300		ns
Transmit SDA Fall Time	t_F	C_{BUS} = 400pF	20 + 0.1 x C_{BUS}		300	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 6)		50		ns
EEPROM Byte Write Cycle Time	t_{WR}	(Note 7)			11	ms

Note 1: Specifications guaranteed for the stated global conditions. The device also meets the parameters specified when 0 < V_{IN1} < +6.5V, and at least one of V_{IN3} through V_{IN6} is between +2.7V and +5.5V, while the remaining V_{IN3} through V_{IN6} are between 0 and +5.5V.

Note 2: Device may be supplied from any one of IN_, except IN2.

Note 3: The internal supply voltage, measured at ABP, equals the maximum of IN3–IN6 if V_{IN1} = 0, or equals +5.4V if V_{IN1} > +6.5V. For +4V < V_{IN1} < +6.5V and V_{IN3} through V_{IN6} > +2.7V, the input that powers the device cannot be determined.

Note 4: 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.

Note 5: C_{BUS} = total capacitance of one bus line in pF. Rise and fall times are measured between 0.1 x V_{BUS} and 0.9 x V_{BUS}.

Note 6: Input filters on SDA, SCL, A0, and A1 suppress noise spikes < 50ns.

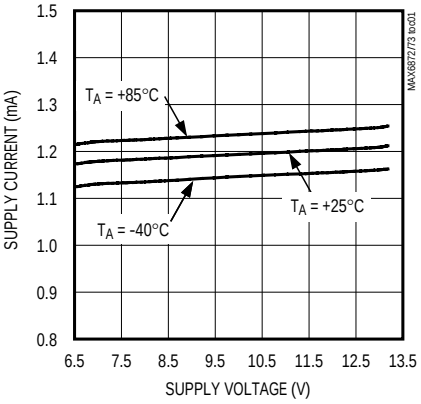
Note 7: An additional cycle is required when writing to configuration memory for the first time.

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

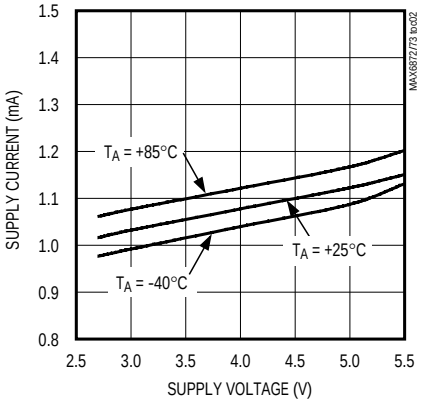
Typical Operating Characteristics

(V_{IN1} = +6.5V to +13.2V, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = +25°C, unless otherwise noted.)

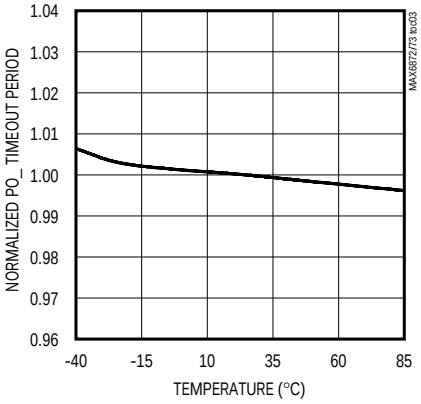
SUPPLY CURRENT vs. SUPPLY VOLTAGE (IN1)



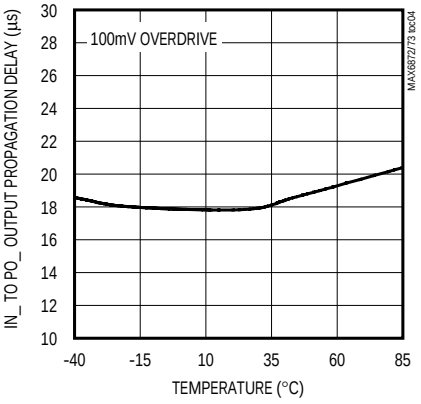
SUPPLY CURRENT vs. SUPPLY VOLTAGE (IN3–IN6)



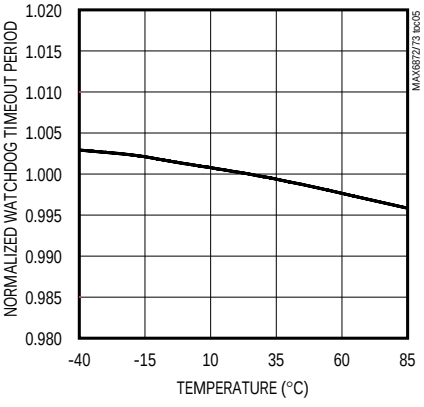
NORMALIZED PO_ TIMEOUT PERIOD vs. TEMPERATURE



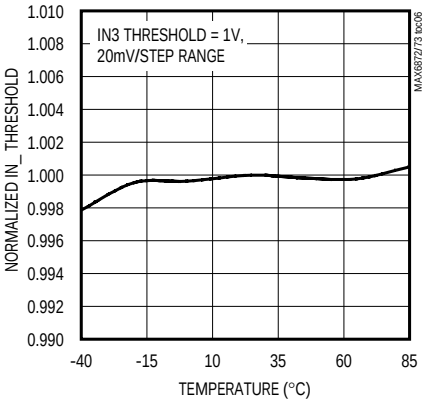
IN_ TO PO_ PROPAGATION DELAY vs. TEMPERATURE



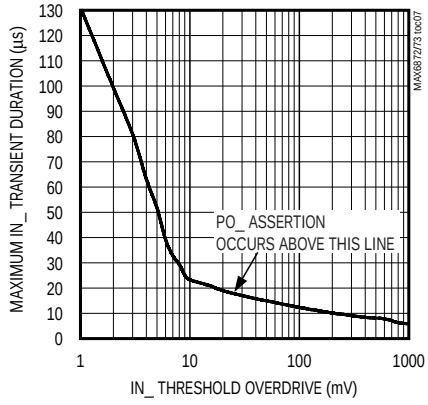
NORMALIZED WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



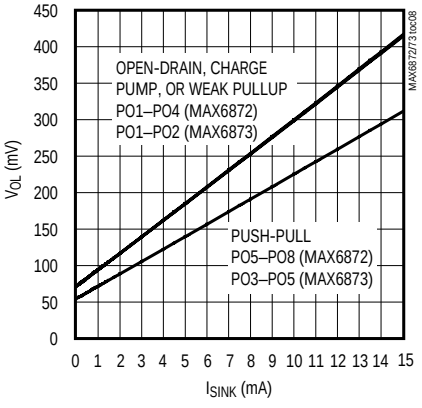
NORMALIZED IN_ THRESHOLD vs. TEMPERATURE



MAXIMUM IN_ TRANSIENT DURATION vs. IN_ THRESHOLD OVERDRIVE



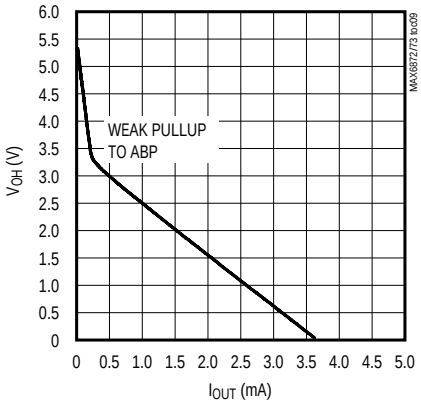
OUTPUT VOLTAGE LOW vs. SINK CURRENT



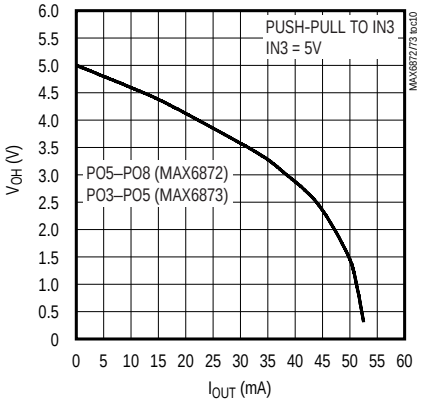
Typical Operating Characteristics (continued)

(V_{IN1} = +6.5V to +13.2V, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = +25°C, unless otherwise noted.)

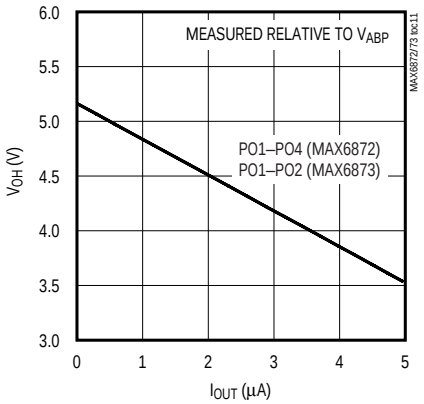
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT (WEAK PULLUP OUTPUT)



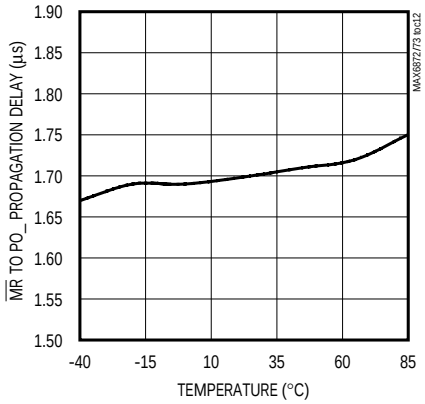
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT (PUSH-PULL OUTPUT)



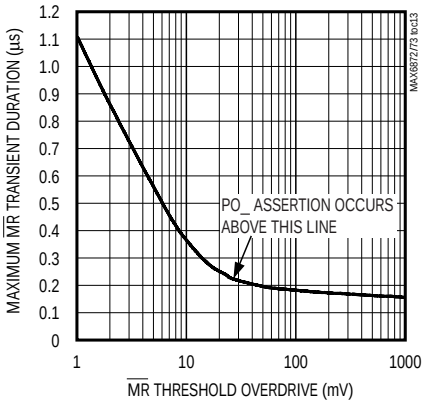
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT (CHARGE-PUMP OUTPUT)



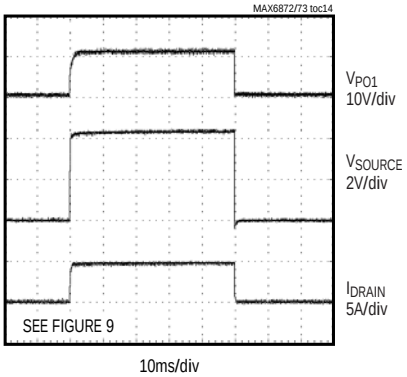
$\overline{MR}$ TO PO_ PROPAGATION DELAY vs. TEMPERATURE



MAXIMUM $\overline{MR}$ TRANSIENT DURATION vs. $\overline{MR}$ THRESHOLD OVERDRIVE



FET (IRF7811W) TURN-ON WITH CHARGE PUMP



Pin Description

PIN		NAME	FUNCTION
MAX6872	MAX6873		
1	3	PO2	Programmable Output 2. Configurable, active-high, active-low, open-drain, weak pullup, or charge-pump output. PO2 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO2 assumes its programmed conditional output state when ABP exceeds UVLO.
2	5	PO3	Programmable Output 3. Configurable, active-high, active-low, open-drain, weak pullup (MAX6872), push-pull (MAX6873), or charge-pump (MAX6872) output. PO3 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO3 assumes its programmed conditional output state when ABP exceeds UVLO.
3	6	PO4	Programmable Output 4. Configurable, active-high, active-low, open-drain, weak pullup (MAX6872), push-pull (MAX6873), or charge-pump (MAX6872) output. PO4 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO4 assumes its programmed conditional output state when ABP exceeds UVLO.
4	4	GND	Ground
5	7	PO5	Programmable Output 5. Configurable, active-high, active-low, open-drain, weak pullup, or push-pull output. PO5 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO5 assumes its programmed conditional output state when ABP exceeds UVLO.
6	—	PO6	Programmable Output 6. Configurable, active-high, active-low, open-drain, weak pullup, or push-pull output. PO6 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO6 assumes its programmed conditional output state when ABP exceeds UVLO.
7	—	PO7	Programmable Output 7. Configurable, active-high, active-low, open-drain, weak pullup, or push-pull output. PO7 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO7 assumes its programmed conditional output state when ABP exceeds UVLO.
8	—	PO8	Programmable Output 8. Configurable, active-high, active-low, open-drain, weak pullup, or push-pull output. PO8 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO8 assumes its programmed conditional output state when ABP exceeds UVLO.
9, 10, 23, 24	1, 8, 9, 10, 23–26, 32	N.C.	No Connection. Not internally connected.
11	11	$\overline{MARGIN}$	Margin Input. Configure $\overline{MARGIN}$ to either assert PO_ into a programmed state or to hold PO_ in its existing state when driving $\overline{MARGIN}$ low (see Table 7). Leave $\overline{MARGIN}$ unconnected or connect to DBP if unused. $\overline{MARGIN}$ overrides $\overline{MR}$ if both assert at the same time. $\overline{MARGIN}$ is internally pulled up to DBP through a 10µA current source.
12	12	$\overline{MR}$	Manual Reset Input. Configure $\overline{MR}$ to either assert PO_ into a programmed state or to have no effect on PO_ when driving $\overline{MR}$ low (see Table 6). Leave $\overline{MR}$ unconnected or connect to DBP if unused. $\overline{MR}$ is internally pulled up to DBP through a 10µA current source.
13	13	SDA	Serial Data Input/Output (Open-Drain). SDA requires an external pullup resistor.
14	14	SCL	Serial Clock Input. SCL requires an external pullup resistor.
15	15	A0	Address Input 0. Address inputs allow up to four MAX6872/MAX6873 connections on one common bus. Connect A0 to GND or to the serial interface power supply.
16	16	A1	Address Input 1. Address inputs allow up to four MAX6872/MAX6873 connections on one common bus. Connect A1 to GND or to the serial interface power supply.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX6872	MAX6873		
17	17	GPI4	General-Purpose Logic Input 4. An internal 10µA current source pulls GPI4 to GND. Configure GPI4 to control watchdog timer functions or the programmable outputs.
18	18	GPI3	General-Purpose Logic Input 3. An internal 10µA current source pulls GPI3 to GND. Configure GPI3 to control watchdog timer functions or the programmable outputs.
19	19	GPI2	General-Purpose Logic Input 2. An internal 10µA current source pulls GPI2 to GND. Configure GPI2 to control watchdog timer functions or the programmable outputs.
20	20	GPI1	General-Purpose Logic Input 1. An internal 10µA current source pulls GPI1 to GND. Configure GPI1 to control watchdog timer functions or the programmable outputs.
21	21	ABP	Internal Power-Supply Output. Bypass ABP to GND with a 1µF ceramic capacitor. ABP powers the internal circuitry of the MAX6872/MAX6873. ABP supplies the input voltage to the internal charge pumps when the programmable outputs are configured as charge-pump outputs. Do not use ABP to supply power to external circuitry.
22	22	DBP	Internal Digital Power-Supply Output. Bypass DBP to GND with a 1µF ceramic capacitor. DBP supplies power to the EEPROM memory and the internal logic circuitry. Do not use DBP to supply power to external circuitry.
25	—	IN6	Voltage Input 6. Configure IN6 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN6 to GND with a 0.1µF capacitor installed as close to the device as possible.
26	—	IN5	Voltage Input 5. Configure IN5 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN5 to GND with a 0.1µF capacitor installed as close to the device as possible.
27	27	IN4	Voltage Input 4. Configure IN4 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN4 to GND with a 0.1µF capacitor installed as close to the device as possible.
28	28	IN3	Voltage Input 3. Configure IN3 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN3 to GND with a 0.1µF capacitor installed as close to the device as possible.
29	29	IN2	Bipolar Voltage Input 2. Configure IN2 to detect negative voltage thresholds from -2.5V to -15.25V in 50mV increments or -1.25V to -7.625V in 25mV increments. Alternatively, configure IN2 to detect positive voltage thresholds from 2.5V to 15.25V in 50mV increments or 1.25V to 7.625V in 25mV increments. For improved noise immunity, bypass IN2 to GND with a 0.1µF capacitor installed as close to the device as possible.
30	30	IN1	High-Voltage Input 1. Configure IN1 to detect voltage thresholds from 2.5V to 13.2V in 50mV increments or 1.25V to 7.625V in 25mV increments. For improved noise immunity, bypass IN1 to GND with a 0.1µF capacitor installed as close to the device as possible.
31	31	I.C.	Internal Connection. Leave unconnected.
32	2	PO1	Programmable Output 1. Configurable active-high, active-low, open-drain, weak pullup, or charge-pump output. PO1 pulls low with a weak 10µA internal current sink for $1V < V_{ABP} < V_{UVLO}$. PO1 assumes its programmed conditional output state when ABP exceeds UVLO.
—	—	EP	Exposed Paddle. Exposed paddle is internally connected to GND.

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Detailed Description

The MAX6872/MAX6873 EEPROM-configurable, multivoltage supply sequencers/supervisors monitor several voltage-detector inputs and four general-purpose logic inputs, and feature programmable outputs for highly configurable, power-supply sequencing applications. The MAX6872 features six voltage-detector inputs and eight programmable outputs, while the MAX6873 features four voltage-detector inputs and five programmable outputs. Manual reset and margin disable inputs simplify board-level testing during the manufacturing process. The MAX6872/MAX6873 feature an accurate internal 1.25V reference.

All voltage detectors provide two configurable thresholds for undervoltage/overvoltage or dual undervoltage detection. One high-voltage input (IN1) provides detector threshold voltages from +1.25V to +7.625V in 25mV increments or +2.5V to +13.2V in 50mV increments. A bipolar input (IN2) provides detector threshold voltages from ±1.25V to ±7.625V in 25mV increments, or ±2.5V to ±15.25V in 50mV increments. Positive inputs (IN3–IN6) provide detector threshold voltages from +0.5V to +3.05V in 10mV increments, or +1.0V to +5.5V in 20mV increments.

The host controller communicates with the MAX6872/MAX6873s' internal 4kb user EEPROM, configuration EEPROM, configuration registers, and fault registers through an SMBus/I^{2}C-compatible serial interface (see Figure 1).

Programmable output options include active-high, active-low, open-drain, weak pullup, push-pull, and charge pump. Select the charge-pump output feature to drive n-channel FETs for power-supply sequencing (see the *Applications Information* section). The outputs swing between 0 and (V_{ABP} + 5V) when configured for charge-pump operation.

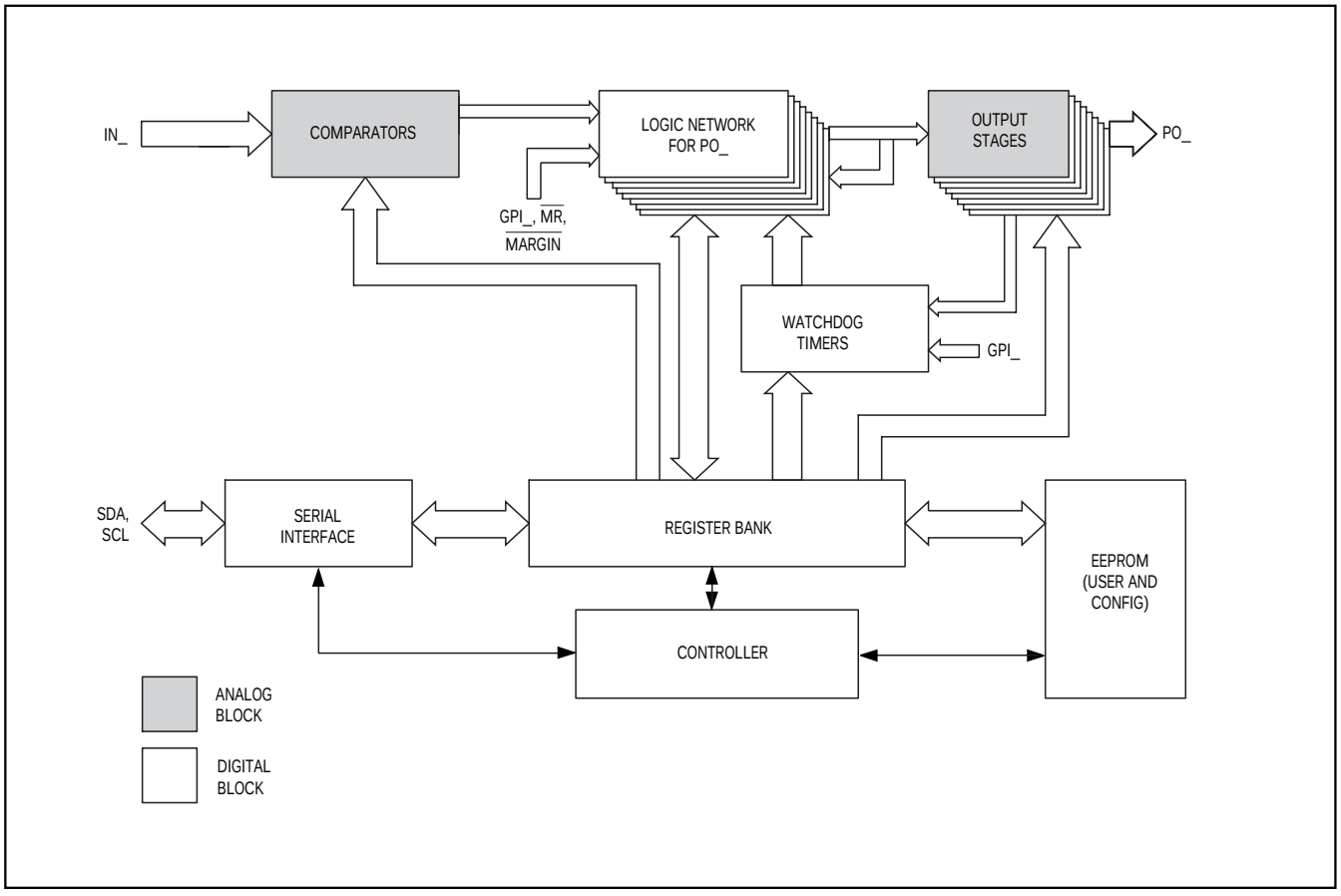
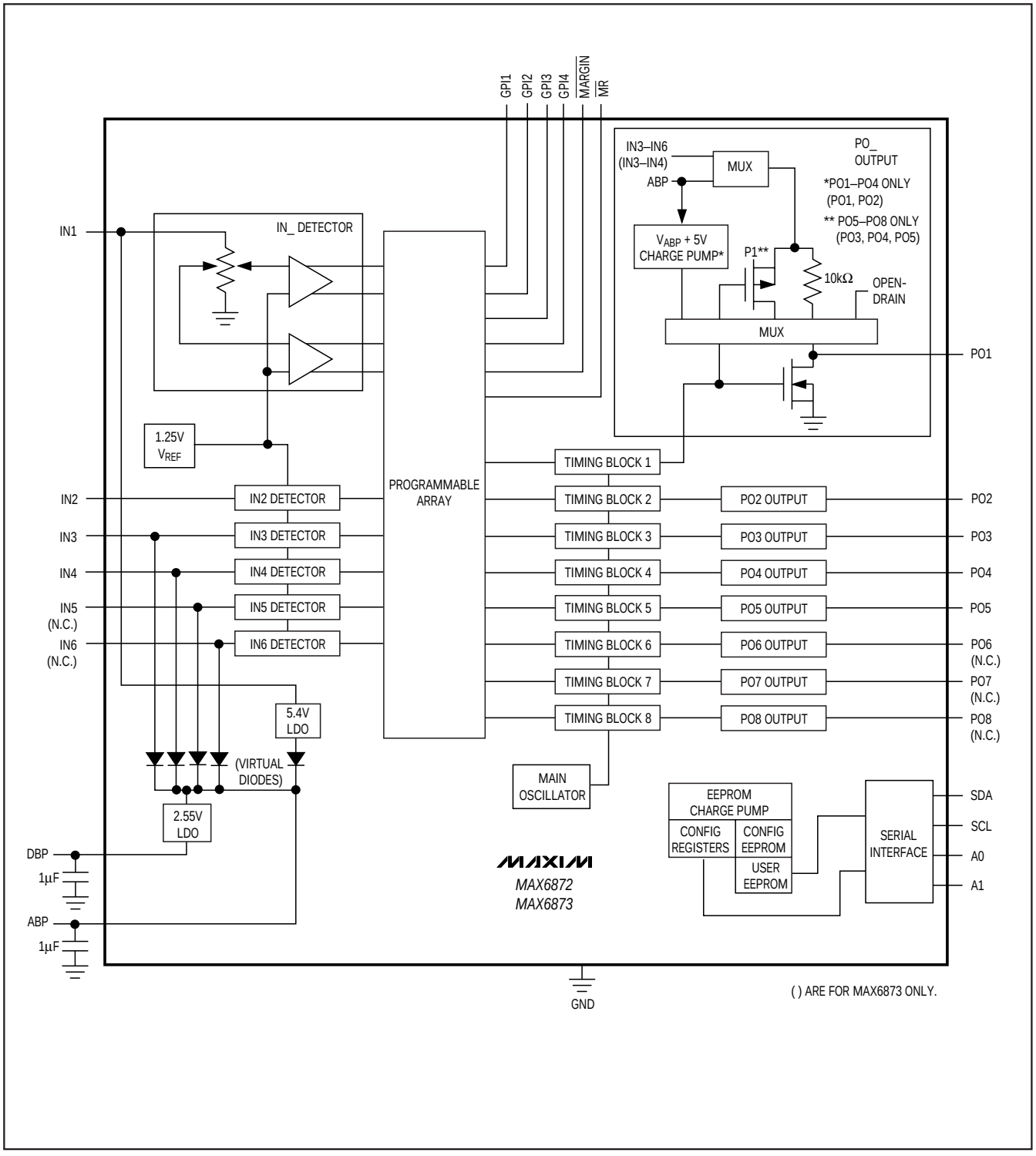


Figure 1. Top-Level Block Diagram

Functional Diagram



EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Program each output to assert on any voltage-detector input, general-purpose logic input, watchdog timer, manual reset, or other output stages. Programmable timing-delay blocks configure each output to wait between 25µs and 1600ms before deasserting. A fault register logs the conditions that caused each output to assert (undervoltage, overvoltage, manual reset, etc.).

The MAX6872/MAX6873 feature two watchdog timers, adding flexibility. Program each watchdog timer to assert one or more programmable outputs. Program each watchdog timer to clear on a combination of one GPI_ input and one programmable output, one of the GPI_ inputs only, or one of the programmable outputs only. The initial and normal watchdog timeout periods are independently programmable from 6.25ms to 102.4s.

A virtual diode-ORing scheme selects the input that powers the MAX6872/MAX6873. The MAX6872/MAX6873 derive power from IN1 if V_{IN1} > +6.5V or from the highest voltage on IN3–IN6 if V_{IN1} < +2.7V. The power source cannot be determined if +4V < V_{IN1} < +6.5V and one of V_{IN3} through V_{IN6} > +2.7V. The programmable outputs maintain the correct programmed logic state for V_{ABP} > V_{UVLO}. One of IN3 through IN6 must be greater than +2.7V or IN1 must be greater than +4V for device operation.

Powering the MAX6872/MAX6873

The MAX6872/MAX6873 derive power from the positive voltage-detector inputs: IN1 or IN3–IN6. A virtual diode-ORing scheme selects the positive input that supplies power to the device (see the *Functional Diagram*). IN1 must be at least +4V or one of IN3–IN6 (MAX6872)/ IN3–IN4 (MAX6873) must be at least +2.7V to ensure device operation. An internal LDO regulates IN1 down to +5.4V.

The highest input voltage on IN3–IN6 (MAX6872)/ IN3–IN4 (MAX6873) supplies power to the device, unless $V_{IN1} \geq$ +6.5V, in which case IN1 supplies power to the device. For +4V < V_{IN1} < +6.5V and one of V_{IN3} through V_{IN6} > +2.7V, the input power source cannot be determined due to the dropout voltage of the LDO. Internal hysteresis ensures that the supply input that initially powered the device continues to power the device when multiple input voltages are within 50mV of each other.

ABP powers the analog circuitry; bypass ABP to GND with a 1µF ceramic capacitor installed as close to the device as possible. The internal supply voltage, measured at ABP, equals the maximum of IN3–IN6 (MAX6872)/IN3–IN4 (MAX6873) if V_{IN1} = 0, or equals +5.4V when V_{IN1} > +6.5V. Do not use ABP to provide power to external circuitry.

The MAX6872/MAX6873 also generate a digital supply voltage (DBP) for the internal logic circuitry and the EEPROM; bypass DBP to GND with a 1µF ceramic capacitor installed as close to the device as possible. The nominal DBP output voltage is +2.55V. Do not use DBP to provide power to external circuitry.

Inputs

The MAX6872/MAX6873 contain multiple logic and voltage-detector inputs. Each voltage-detector input is simultaneously monitored for primary and secondary thresholds. The primary threshold must be an undervoltage threshold. The secondary threshold may be an undervoltage or overvoltage threshold. Table 1 summarizes these various inputs.

Set the primary and secondary threshold voltages for each voltage-detector input with registers 00h–0Bh. Each primary threshold voltage must be an undervoltage threshold. Configure each secondary threshold voltage as an undervoltage or overvoltage threshold (see register 0Ch). Set the threshold range for each voltage detector with register 0Dh.

High-Voltage Input (IN1)

IN1 offers threshold voltages of +2.5V to +13.2V in 50mV increments, or +1.25V to +7.625V in 25mV increments. Use the following equations to set the threshold voltages for IN1:

$$x = \frac{V_{TH} - 2.5V}{0.05V} \text{ for } +2.5V \text{ to } +13.2V \text{ range}$$

$$x = \frac{V_{TH} - 1.25V}{0.025V} \text{ for } +1.25V \text{ to } +7.625V \text{ range}$$

where V_{TH} is the desired threshold voltage and x is the decimal code for the desired threshold (Table 2). For the +2.5V to +13.2V range, x must equal 214 or less, otherwise the threshold exceeds the maximum operating voltage of IN1.

Bipolar-Voltage Input (IN2)

IN2 offers negative thresholds from -2.5V to -15.25V in 50mV increments, or from -1.25V to -7.625V in 25mV increments. Alternatively, IN2 offers positive thresholds from +2.5V to +15.25V in 50mV increments, or +1.25V to +7.625V in 25mV increments. Use the following equations to set the threshold voltages for IN2:

$$x = \frac{-(V_{TH} - 2.5V)}{0.05V} \text{ for } -2.5V \text{ to } -15.25V \text{ range}$$

Table 1. Programmable Features

FEATURE	DESCRIPTION
High-Voltage Input (IN1)	• Primary undervoltage threshold • Secondary overvoltage or undervoltage threshold • +2.5V to +13.2V threshold in 50mV increments • +1.25V to +7.625V threshold in 25mV increments
Bipolar-Voltage Input (IN2)	• Primary undervoltage threshold • Secondary overvoltage or undervoltage threshold • ±2.5V to ±15.25V threshold in 50mV increments • ±1.25V to ±7.625V threshold in 25mV increments
Positive-Voltage Input IN3–IN6 (MAX6872), IN3–IN4 (MAX6873)	• Primary undervoltage threshold • Secondary overvoltage or undervoltage threshold • +1V to +5.5V threshold in 20mV increments • +0.5V to +3.05V threshold in 10mV increments
Programmable Outputs PO1–PO4 (MAX6872), PO1–PO2 (MAX6873)	• Active high or active low • Open-drain, weak pullup, or charge-pump output • Weak pullup to IN3–IN6 (IN3 or IN4 for MAX6873) or ABP • Dependent on $\overline{MR}$, $\overline{MARGIN}$, IN_, GPI1–GPI4 , WD1 and WD2, and/or PO_ • Programmable timeout periods of 25µs, 1.5625ms, 6.25ms, 25ms, 50ms, 200ms, 400ms, or 1.6s
Programmable Outputs PO5–PO8 (MAX6872), PO3–PO5 (MAX6873)	• Active high or active low • Open-drain, weak pullup, or push-pull output • Weak pullup to IN3–IN6 (IN3 or IN4 for MAX6873) or ABP • Push-pull to IN3–IN6 (IN3 or IN4 for MAX6873) • Dependent on $\overline{MR}$, $\overline{MARGIN}$, IN_, GPI1–GPI4 , WD1 and WD2, and/or PO_ • Programmable timeout periods of 25µs, 1.5625ms, 6.25ms, 25ms, 50ms, 200ms, 400ms, or 1.6s
General-Purpose Logic Inputs (GPI1–GPI4)	• Active high or active low logic levels • Configure GPI_ as inputs to watchdog timers or programmable output stages
Watchdog Timers	• Clear dependent on any combination of one GPI_ input and one programmable output, a GPI_ input only, or a programmable output only • Initial watchdog timeout period of 6.25ms, 25ms, 100ms, 400ms, 1.6s, 6.4s, 25.6s, or 102.4s • Normal watchdog timeout period of 6.25ms, 25ms, 100ms, 400ms, 1.6s, 6.4s, 25.6s, or 102.4s • Watchdog enable/disable • Initial watchdog timeout period enable/disable
Manual Reset Input ($\overline{MR}$)	• Forces PO_ into the active output state when $\overline{MR}$ = GND • PO_ deassert after $\overline{MR}$ releases high and the PO_ timeout period expires • PO_ cannot be a function of $\overline{MR}$ only
Margining Input ($\overline{MARGIN}$)	• Holds PO_ in existing state or asserts PO_ to a programmed output state, independent of changes in monitored inputs or watchdog timers, when $\overline{MARGIN}$ = GND • Overrides $\overline{MR}$ when both assert at the same time
Write Disable	• Locks user EEPROM based on PO_
Configuration Lock	• Locks configuration EEPROM

Table 2. IN1 Threshold Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
00h	8000h	[7:0]	IN1 primary undervoltage detector threshold (V1A) (see equations in the *High-Voltage Input (IN1)* section).
06h	8006h	[7:0]	IN1 secondary undervoltage/overvoltage detector threshold (V1B) (see equations in the *High-Voltage Input (IN1)* section).
0Ch	800Ch	[0]	IN1 secondary overvoltage/undervoltage selection: 0 = overvoltage threshold. 1 = undervoltage threshold.
0Dh	800Dh	[0]	IN1 range selection: 0 = 2.5V to 13.2V range in 50mV increments. 1 = 1.25V to 7.625V range in 25mV increments.

Table 3. IN2 Threshold Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
01h	8001h	[7:0]	IN2 primary undervoltage detector threshold (V2A) (see equations in the *Bipolar-Voltage Input (IN2)* section).
07h	8007h	[7:0]	IN2 secondary undervoltage/overvoltage detector threshold (V2B) (see equations in the *Bipolar-Voltage Input (IN2)* section).
0Ch	800Ch	[1]	IN2 secondary overvoltage/undervoltage selection: 0 = overvoltage threshold. 1 = undervoltage threshold.
0Dh	800Dh	[7:6]	IN2 range selection: 00 = -2.5V to -15.25V range in 50mV increments. 01 = -1.25V to -7.625V range in 25mV increments. 10 = +2.5V to +15.25V range in 50mV increments. 11 = +1.25V to +7.625V range in 25mV increments.

$$x = \frac{-(V_{TH} - 1.25V)}{0.025V} \text{ for } -1.25V \text{ to } -7.625V \text{ range}$$

$$x = \frac{V_{TH} - 2.5V}{0.05V} \text{ for } +2.5V \text{ to } +15.25V \text{ range}$$

$$x = \frac{V_{TH} - 1.25V}{0.025V} \text{ for } +1.25V \text{ to } +7.625V \text{ range}$$

where V_{TH} is the desired threshold voltage and x is the decimal code for the desired threshold (Table 3).

IN3–IN6

IN3–IN6 offer positive voltage detectors monitor voltages from +1V to +5.5V in 20mV increments, or +0.5V to +3.05V in 10mV increments. Use the following equations to set the threshold voltages for IN_:

$$x = \frac{V_{TH} - 1V}{0.02V} \text{ for } +1V \text{ to } +5.5V \text{ range}$$

$$x = \frac{V_{TH} - 0.5V}{0.01V} \text{ for } +0.5V \text{ to } +3.05V \text{ range}$$

where V_{TH} is the desired threshold voltage and x is the decimal code for the desired threshold (Table 4). For the +1V to +5.5V range, x must equal 225 or less, oth-

Table 4. IN3–IN6 Threshold Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
02h	8002h	[7:0]	IN3 primary undervoltage detector threshold (V3A) (see equations in the *IN3–IN6* section).
03h	8003h	[7:0]	IN4 primary undervoltage detector threshold (V4A) (see equations in the *IN3–IN6* section).
04h	8004h	[7:0]	IN5 (MAX6872 only) primary undervoltage detector threshold (V5A) (see equations in the *IN3–IN6* section).
05h	8005h	[7:0]	IN6 (MAX6872 only) primary undervoltage detector threshold (V6A) (see equations in the *IN3–IN6* section).
08h	8008h	[7:0]	IN3 secondary undervoltage/overvoltage detector threshold (V3B) (see equations in the *IN3–IN6* section).
09h	8009h	[7:0]	IN4 secondary undervoltage/overvoltage detector threshold (V4B) (see equations in the *IN3–IN6* section).
0Ah	800Ah	[7:0]	IN5 (MAX6872 only) secondary undervoltage/overvoltage detector threshold (V5B) (see equations in the *IN3–IN6* section).
0Bh	800Bh	[7:0]	IN6 (MAX6872 only) secondary undervoltage/overvoltage detector threshold (V6B) (see equations in the *IN3–IN6* section).
0Ch	800Ch	[2]	IN3 secondary overvoltage/undervoltage selection. 0 = overvoltage threshold. 1 = undervoltage threshold.
		[3]	IN4 secondary overvoltage/undervoltage selection. 0 = overvoltage threshold. 1 = undervoltage threshold.
		[4]	IN5 (MAX6872 only) secondary overvoltage/undervoltage selection. 0 = overvoltage threshold. 1 = undervoltage threshold.
		[5]	IN6 (MAX6872 only) secondary overvoltage/undervoltage selection. 0 = overvoltage threshold. 1 = undervoltage threshold.
		[7:6]	Not used.
0Dh	800Dh	[1]	IN3 range selection. 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments.
		[2]	IN4 range selection. 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments.
		[3]	IN5 (MAX6872 only) range selection. 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments.
		[4]	IN6 (MAX6872 only) range selection. 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments.
		[5]	Not used.

erwise the threshold exceeds the maximum operating voltage of IN3–IN6.

GPI1–GPI4

The GPI1–GPI4 programmable logic inputs control power-supply sequencing (programmable outputs), reset/interrupt signaling, and watchdog functions (see the *Configuring the Watchdog Timers (Registers 3Ch–3Fh)* section). Configure GPI1–GPI4 for active-low or active-high logic (Table 5). GPI1–GPI4 internally pull down to GND through a 10µA current sink.

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

$\overline{MR}$

The manual reset ($\overline{MR}$) input initiates a reset condition. Register 40h determines the programmable outputs that assert while $\overline{MR}$ is low (Table 6). All affected programmable outputs remain asserted (see the *Programmable Outputs* section) for their PO_ timeout periods after $\overline{MR}$ releases high. An internal 10µA current source pulls $\overline{MR}$ to DBP. Leave $\overline{MR}$ unconnected or connect to DBP if unused. A programmable output cannot depend solely on $\overline{MR}$.

$\overline{MARGIN}$

$\overline{MARGIN}$ allows system-level testing while power supplies exceed the normal ranges. Registers 41h and 42h determine whether the programmable outputs assert to a predetermined state or hold the last state as $\overline{MARGIN}$ is driven low (Table 7). Drive $\overline{MARGIN}$ low to set the programmable outputs in a known state while system-level testing occurs. Leave $\overline{MARGIN}$ unconnected or connect to DBP if unused. An internal 10µA current source pulls $\overline{MARGIN}$ to DBP. The state of each programmable output does not change while $\overline{MARGIN}$ = GND. $\overline{MARGIN}$ overrides $\overline{MR}$ if both assert at the same time.

Programmable Outputs

The MAX6872 features eight programmable outputs, while the MAX6873 features five programmable outputs. Selectable output-stage configurations include: active low or active high, open drain, weak pullup, push-pull, or charge pump. During power-up, the programmable outputs pull to GND with an internal 10µA current sink for 1V < V_{ABP} < V_{UVLO}. The programmable outputs remain in their active states until their respective PO_ timeout periods expire, and all of the programmed conditions are met for each output. Any output programmed to depend on no condition always remains in its active state (Table 20). An active-high configured output is considered asserted

Table 5. GPI1–GPI4 Active Logic States

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
3Bh	803Bh	[0]	GPI1. 0 = active low. 1 = active high.
		[1]	GPI2. 0 = active low. 1 = active high.
		[2]	GPI3. 0 = active low. 1 = active high.
		[3]	GPI4. 0 = active low. 1 = active high.

Table 6. Programmable Output Behavior and $\overline{MR}$

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
40h	8040h	[0]	PO1 (MAX6872 only). 0 = PO1 independent of $\overline{MR}$. 1 = PO1 asserts when $\overline{MR}$ = low.
		[1]	PO2 (MAX6872 only). 0 = PO2 independent of $\overline{MR}$. 1 = PO2 asserts when $\overline{MR}$ = low.
		[2]	PO3 (MAX6872)/PO1 (MAX6873). 0 = PO3/PO1 independent of $\overline{MR}$. 1 = PO3/PO1 asserts when $\overline{MR}$ = low.
		[3]	PO4 (MAX6872)/PO2 (MAX6873). 0 = PO4/PO2 independent of $\overline{MR}$. 1 = PO4/PO2 asserts when $\overline{MR}$ = low.
		[4]	PO5 (MAX6872)/PO3 (MAX6873). 0 = PO5/PO3 independent of $\overline{MR}$. 1 = PO5/PO3 asserts when $\overline{MR}$ = low.
		[5]	PO6 (MAX6872)/PO4 (MAX6873). 0 = PO6/PO4 independent of $\overline{MR}$. 1 = PO6/PO4 asserts when $\overline{MR}$ = low.
		[6]	PO7 (MAX6872)/PO5 (MAX6873). 0 = PO7/PO5 independent of $\overline{MR}$. 1 = PO7/PO5 asserts when $\overline{MR}$ = low.
		[7]	PO8 (MAX6872 only). 0 = PO8 independent of $\overline{MR}$. 1 = PO8 asserts when $\overline{MR}$ = low.

when that output is logic-high. No output can depend solely on $\overline{MR}$.

The positive voltage monitors generate fault signals (logical 0) to the MAX6872/MAX6873s' logic array when an input voltage is below the programmed undervoltage threshold, or when that voltage is above the overvoltage threshold. The negative voltage monitor (IN2) generates a fault signal to the logic array when the input voltage is less negative than the undervoltage threshold, or when that voltage is more negative than the overvoltage threshold.

Registers 0Eh through 3Ah and 40h configure each of the programmable outputs. Programmable timing blocks set the PO_ timeout period from 25µs to 1600ms

Table 7. Programmable Output Behavior and $\overline{MARGIN}$

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	AFFECTED OUTPUT	DESCRIPTION
41h	8041h	[0]	PO1 (MAX6872 only)	0 = output held in existing state. 1 = output asserts high or low (see 42h[0]).
		[1]	PO2 (MAX6872 only)	0 = output held in existing state. 1 = output asserts high or low (see 42h[1]).
		[2]	PO3 (MAX6872) PO1 (MAX6873)	0 = output held in existing state. 1 = output asserts high or low (see 42h[2]).
		[3]	PO4 (MAX6872) PO2 (MAX6873)	0 = output held in existing state. 1 = output asserts high or low (see 42h[3]).
		[4]	PO5 (MAX6872) PO3 (MAX6873)	0 = output held in existing state. 1 = output asserts high or low (see 42h[4]).
		[5]	PO6 (MAX6872) PO4 (MAX6873)	0 = output held in existing state. 1 = output asserts high or low (see 42h[5]).
		[6]	PO7 (MAX6872) PO5 (MAX6873)	0 = output held in existing state. 1 = output asserts high or low (see 42h[6]).
		[7]	PO8 (MAX6872 only)	0 = output held in existing state. 1 = output asserts high or low (see 42h[7]).
42h	8042h	[0]	PO1 (MAX6872 only)	0 = output asserts low if 41h[0] = 1. 1 = output asserts high if 41h[0] = 1.
		[1]	PO2 (MAX6872 only)	0 = output asserts low if 41h[1] = 1. 1 = output asserts high if 41h[1] = 1.
		[2]	PO3 (MAX6872) PO1 (MAX6873)	0 = output asserts low if 41h[2] = 1. 1 = output asserts high if 41h[2] = 1.
		[3]	PO4 (MAX6872) PO2 (MAX6873)	0 = output asserts low if 41h[3] = 1. 1 = output asserts high if 41h[3] = 1.
		[4]	PO5 (MAX6872) PO3 (MAX6873)	0 = output asserts low if 41h[4] = 1. 1 = output asserts high if 41h[4] = 1.
		[5]	PO6 (MAX6872) PO4 (MAX6873)	0 = output asserts low if 41h[5] = 1. 1 = output asserts high if 41h[5] = 1.
		[6]	PO7 (MAX6872) PO5 (MAX6873)	0 = output asserts low if 41h[6] = 1. 1 = output asserts high if 41h[6] = 1.
		[7]	PO8 (MAX6872 only)	0 = output asserts low if 41h[7] = 1. 1 = output asserts high if 41h[7] = 1.

Table 8. PO1 (MAX6872 Only) Output Dependency

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
0Eh	800Eh	[0]	1 = PO1 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO1 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO1 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO1 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO1 assertion depends on IN5 primary undervoltage threshold (Table 4).
		[5]	1 = PO1 assertion depends on IN6 primary undervoltage threshold (Table 4).
		[6]	1 = PO1 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO1 assertion depends on watchdog 2 (Tables 25 and 26).
0Fh	800Fh	[0]	1 = PO1 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO1 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO1 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO1 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO1 assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4).
		[5]	1 = PO1 assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4).
		[6]	1 = PO1 assertion depends on GPI1 (Table 5).
		[7]	1 = PO1 assertion depends on GPI2 (Table 5).
10h	8010h	[0]	1 = PO1 assertion depends on GPI3 (Table 5).
		[1]	1 = PO1 assertion depends on GPI4 (Table 5).
		[2]	1 = PO1 assertion depends on PO2 (Table 9).
		[3]	1 = PO1 assertion depends on PO3 (Tables 10 and 11).
		[4]	1 = PO1 assertion depends on PO4 (Tables 12 and 13).
		[5]	1 = PO1 assertion depends on PO5 (Tables 14 and 15).
		[6]	1 = PO1 assertion depends on PO6 (Tables 16 and 17).
		[7]	1 = PO1 assertion depends on PO7 (Table 18).
11h	8011h	[0]	1 = PO1 assertion depends on PO8 (Table 19).
40h	8040h	[0]	1 = PO1 asserts when $\overline{MR}$ = low (Table 6).

for each programmable output. See register 3Ah (Table 20) to set the active state (active-high or active-low) for each programmable output and registers 11h, 15h, 1Ch, 23h, 2Ah, 31h, 35h, and 39h to select the output stage types (Tables 21 and 22), and PO_ timeout periods (Table 23) for each output.

Control selected programmable outputs with a sum of products (Tables 8–19). Each product allows a different set of conditions to assert each output. Outputs PO3 (MAX6872)/PO1 (MAX6873) and PO6 (MAX6872)/PO4 (MAX6873) allow two sets of different conditions to assert each output. Outputs PO1 and PO2 (MAX6872 only), PO7 (MAX6872)/PO5 (MAX6873), and PO8 (MAX6872 only) allow only one set of conditions to assert each output.

For example, Product 1 of the PO3 (MAX6872—Table 10) programmable output may depend on the IN1 primary undervoltage threshold, and the states of GPI1, PO1, and PO2. Write a one to R16h[0], R17h[6], and R18h[3:2] to configure Product 1 as indicated. IN1 must be above the primary undervoltage threshold (Table 2), GPI1 must be inactive (Table 5), and PO1 (Tables 8 and 20) and PO2 (Tables 10 and 21) must be in their deasserted states for Product 1 to be a logical 1. Product 1 is equivalent to the logic statement: V1A • GPI1 • PO1 • PO2.

Product 2 of PO3 (MAX6872, Table 11) may depend on an entirely different set of conditions, or the same conditions, depending on the system requirements. For example, Product 2 may depend on the IN1 undervolt-

Table 9. PO2 (MAX6872 Only) Output Dependency

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
12h	8012h	[0]	1 = PO2 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO2 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO2 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO2 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO2 assertion depends on IN5 primary undervoltage threshold (Table 4).
		[5]	1 = PO2 assertion depends on IN6 primary undervoltage threshold (Table 4).
		[6]	1 = PO2 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO2 assertion depends on watchdog 2 (Tables 25 and 26).
13h	8013h	[0]	1 = PO2 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO2 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO2 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO2 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO2 assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4).
		[5]	1 = PO2 assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4).
		[6]	1 = PO2 assertion depends on GPI1 (Table 5).
		[7]	1 = PO2 assertion depends on GPI2 (Table 5).
14h	8014h	[0]	1 = PO2 assertion depends on GPI3 (Table 5).
		[1]	1 = PO2 assertion depends on GPI4 (Table 5).
		[2]	1 = PO2 assertion depends on PO1 (Table 8).
		[3]	1 = PO2 assertion depends on PO3 (Tables 10 and 11).
		[4]	1 = PO2 assertion depends on PO4 (Tables 12 and 13).
		[5]	1 = PO2 assertion depends on PO5 (Tables 14 and 15).
		[6]	1 = PO2 assertion depends on PO6 (Tables 16 and 17).
		[7]	1 = PO2 assertion depends on PO7 (Table 18).
15h	8015h	[0]	1 = PO2 assertion depends on PO8 (Table 19).
40h	8040h	[1]	1 = PO2 asserts when $\overline{MR}$ = low (Table 6).

age threshold, and the states of GPI2 and WD1. Write ones to R19h[6, 0] and R1Ah[7] to configure Product 2 as indicated. IN1 must be above the primary undervoltage threshold (Table 2), GPI2 must be inactive (Table 5), and the WD1 timer must not have expired (Tables 25 and 26) for Product 2 to be a logical 1. Product 2 is equivalent to the logic statement: V1A • GPI2 • WD1. PO3 deasserts if either Product 1 or Product 2 is a logical 1. The logical statement: Product 1 + Product 2 determines the state of PO3.

Table 8 only applies to PO1 of the MAX6872. Write a 0 to a bit to make the PO1 output independent of the respective signal (IN1–IN6 primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs).

Table 9 only applies to PO2 of the MAX6872. Write a 0 to a bit to make the PO2 output independent of the respective signal (IN1–IN6 primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs).

Table 10. PO3 (MAX6872)/PO1 (MAX6873) Output Dependency (Product 1)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
16h	8016h	[0]	1 = PO3/PO1 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO3/PO1 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO3/PO1 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO3/PO1 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO3 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO3 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO3/PO1 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO3/PO1 assertion depends on watchdog 2 (Tables 25 and 26).
17h	8017h	[0]	1 = PO3/PO1 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO3/PO1 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO3/PO1 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO3/PO1 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO3 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO3 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO3/PO1 assertion depends on GPI1 (Table 5).
		[7]	1 = PO3/PO1 assertion depends on GPI2 (Table 5).
18h	8018h	[0]	1 = PO3/PO1 assertion depends on GPI3 (Table 5).
		[1]	1 = PO3/PO1 assertion depends on GPI4 (Table 5).
		[2]	1 = PO3 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO3 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO3/PO1 assertion depends on PO4 (MAX6872)/PO2 (MAX6873) (Tables 12 and 13).
		[5]	1 = PO3/PO1 assertion depends on PO5 (MAX6872)/PO3 (MAX6873) (Tables 14 and 15).
		[6]	1 = PO3/PO1 assertion depends on PO6 (MAX6872)/PO4 (MAX6873) (Tables 16 and 17).
		[7]	1 = PO3/PO1 assertion depends on PO7 (MAX6872)/PO5 (MAX6873) (Table 18).
1Ch	801Ch	[0]	1 = PO3 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[2]	1 = PO3/PO1 asserts when $\overline{MR}$ = low (Table 6).

Table 10 only applies to PO3 of the MAX6872 and PO1 of the MAX6873. Write a 0 to a bit to make the PO3/PO1 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs). See Table 11 for Product 2. PO3 (MAX6872)/PO1 (MAX6873) deasserts when Product 1 or Product 2 = 1.

Table 11. PO3 (MAX6872)/PO1 (MAX6873) Output Dependency (Product 2)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
19h	8019h	[0]	1 = PO3/PO1 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO3/PO1 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO3/PO1 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO3/PO1 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO3 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO3 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO3/PO1 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO3/PO1 assertion depends on watchdog 2 (Tables 25 and 26).
1Ah	801Ah	[0]	1 = PO3/PO1 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO3/PO1 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO3/PO1 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO3/PO1 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO3 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO3 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO3/PO1 assertion depends on GPI1 (Table 5).
		[7]	1 = PO3/PO1 assertion depends on GPI2 (Table 5).
1Bh	801Bh	[0]	1 = PO3/PO1 assertion depends on GPI3 (Table 5).
		[1]	1 = PO3/PO1 assertion depends on GPI4 (Table 5).
		[2]	1 = PO3 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO3 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO3/PO1 assertion depends on PO4 (MAX6872)/PO2 (MAX6873) (Tables 12 and 13).
		[5]	1 = PO3/PO1 assertion depends on PO5 (MAX6872)/PO3 (MAX6873) (Tables 14 and 15).
		[6]	1 = PO3/PO1 assertion depends on PO6 (MAX6872)/PO4 (MAX6873) (Tables 16 and 17).
		[7]	1 = PO3/PO1 assertion depends on PO7 (MAX6872)/PO5 (MAX6873) (Table 18).
1Ch	801Ch	[1]	1 = PO3 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[2]	1 = PO3/PO1 asserts when $\overline{MR}$ = low (Table 6).

Table 11 only applies to PO3 of the MAX6872 and PO1 of the MAX6873. Write a 0 to a bit to make the PO3/PO1 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs). See Table 10 for Product 1. PO3 (MAX6872)/PO1 (MAX6873) deasserts when Product 1 or Product 2 = 1.

Table 12. PO4 (MAX6872)/PO2 (MAX6873) Output Dependency (Product 1)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
1Dh	801Dh	[0]	1 = PO4/PO2 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO4/PO2 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO4/PO2 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO4/PO2 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO4 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO4 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO4/PO2 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO4/PO2 assertion depends on watchdog 2 (Tables 25 and 26).
1Eh	801Eh	[0]	1 = PO4/PO2 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO4/PO2 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO4/PO2 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO4/PO2 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO4 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO4 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO4/PO2 assertion depends on GPI1 (Table 5).
		[7]	1 = PO4/PO2 assertion depends on GPI2 (Table 5).
1Fh	801Fh	[0]	1 = PO4/PO2 assertion depends on GPI3 (Table 5).
		[1]	1 = PO4/PO2 assertion depends on GPI4 (Table 5).
		[2]	1 = PO4 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO4 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO4/PO2 assertion depends on PO3 (MAX6872)/PO1 (MAX6873) (Tables 10 and 11).
		[5]	1 = PO4/PO2 assertion depends on PO5 (MAX6872)/PO3 (MAX6873) (Tables 14 and 15).
		[6]	1 = PO4/PO2 assertion depends on PO6 (MAX6872)/PO4 (MAX6873) (Tables 16 and 17).
		[7]	1 = PO4/PO2 assertion depends on PO7 (MAX6872)/PO5 (MAX6873) (Table 18).
23h	8023h	[0]	1 = PO4 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[3]	1 = PO4/PO2 asserts when $\overline{MR}$ = low (Table 6).

Table 12 only applies to PO4 of the MAX6872 and PO2 of the MAX6873. Write a 0 to a bit to make the PO4/PO2 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs). See Table 13 for Product 2. PO4 (MAX6872)/PO2 (MAX6873) deasserts when Product 1 or Product 2 = 1.

Table 13. PO4 (MAX6872)/PO2 (MAX6873) Output Dependency (Product 2)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
20h	8020h	[0]	1 = PO4/PO2 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO4/PO2 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO4/PO2 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO4/PO2 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO4 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO4 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO4/PO2 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO4/PO2 assertion depends on watchdog 2 (Tables 25 and 26).
21h	8021h	[0]	1 = PO4/PO2 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO4/PO2 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO4/PO2 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO4/PO2 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO4 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO4 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO4/PO2 assertion depends on GPI1 (Table 5).
		[7]	1 = PO4/PO2 assertion depends on GPI2 (Table 5).
22h	8022h	[0]	1 = PO4/PO2 assertion depends on GPI3 (Table 5).
		[1]	1 = PO4/PO2 assertion depends on GPI4 (Table 5).
		[2]	1 = PO4 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO4 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO4/PO2 assertion depends on PO3 (MAX6872)/PO1 (MAX6873) (Tables 10 and 11).
		[5]	1 = PO4/PO2 assertion depends on PO5 (MAX6872)/PO3 (MAX6873) (Tables 14 and 15).
		[6]	1 = PO4/PO2 assertion depends on PO6 (MAX6872)/PO4 (MAX6873) (Tables 16 and 17).
		[7]	1 = PO4/PO2 assertion depends on PO7 (MAX6872)/PO5 (MAX6873) (Table 18).
23h	8023h	[1]	1 = PO4 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[3]	1 = PO4/PO2 asserts when $\overline{MR}$ = low (Table 6).

Table 13 only applies to PO4 of the MAX6872 and PO2 of the MAX6873. Write a 0 to a bit to make the PO4/PO2 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1 to GPI4, $\overline{MR}$, or other programmable outputs). See Table 12 for Product 1. PO4 (MAX6872)/PO2 (MAX6873) deasserts when Product 1 or Product 2 = 1.

Table 14. PO5 (MAX6872)/PO3 (MAX6873) Output Dependency (Product 1)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
24h	8024h	[0]	1 = PO5/PO3 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO5/PO3 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO5/PO3 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO5/PO3 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO5 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO5 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO5/PO3 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO5/PO3 assertion depends on watchdog 2 (Tables 25 and 26).
25h	8025h	[0]	1 = PO5/PO3 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO5/PO3 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO5/PO3 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO5/PO3 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO5 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO5 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO5/PO3 assertion depends on GPI1 (Table 5).
		[7]	1 = PO5/PO3 assertion depends on GPI2 (Table 5).
26h	8026h	[0]	1 = PO5/PO3 assertion depends on GPI3 (Table 5).
		[1]	1 = PO5/PO3 assertion depends on GPI4 (Table 5).
		[2]	1 = PO5 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO5 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO5/PO3 assertion depends on PO3 (MAX6872)/PO1 (MAX6873) (Tables 10 and 11).
		[5]	1 = PO5/PO3 assertion depends on PO4 (MAX6872)/PO2 (MAX6873) (Tables 12 and 13).
		[6]	1 = PO5/PO3 assertion depends on PO6 (MAX6872)/PO4 (MAX6873) (Tables 16 and 17).
		[7]	1 = PO5/PO3 assertion depends on PO7 (MAX6872)/PO5 (MAX6873) (Table 18).
2Ah	802Ah	[0]	1 = PO5 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[4]	1 = PO5/PO3 asserts when $\overline{MR}$ = low (Table 6).

Table 14 only applies to PO5 of the MAX6872 and PO3 of the MAX6873. Write a 0 to a bit to make the PO5/PO3 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs). See Table 15 for Product 2. PO5 (MAX6872)/PO3 (MAX6873) deasserts when Product 1 or Product 2 = 1.

Table 15. PO5 (MAX6872)/PO3 (MAX6873) Output Dependency (Product 2)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
27h	8027h	[0]	1 = PO5/PO3 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO5/PO3 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO5/PO3 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO5/PO3 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO5 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO5 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO5/PO3 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO5/PO3 assertion depends on watchdog 2 (Tables 25 and 26).
28h	8028h	[0]	1 = PO5/PO3 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO5/PO3 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO5/PO3 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO5/PO3 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO5 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO5 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO5/PO3 assertion depends on GPI1 (Table 5).
		[7]	1 = PO5/PO3 assertion depends on GPI2 (Table 5).
29h	8029h	[0]	1 = PO5/PO3 assertion depends on GPI3 (Table 5).
		[1]	1 = PO5/PO3 assertion depends on GPI4 (Table 5).
		[2]	1 = PO5 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO5 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO5/PO3 assertion depends on PO3 (MAX6872)/PO1 (MAX6873) (Tables 10 and 11).
		[5]	1 = PO5/PO3 assertion depends on PO4 (MAX6872)/PO2 (MAX6873) (Tables 12 and 13).
		[6]	1 = PO5/PO3 assertion depends on PO6 (MAX6872)/PO4 (MAX6873) (Tables 16 and 17).
		[7]	1 = PO5/PO3 assertion depends on PO7 (MAX6872)/PO5 (MAX6873) (Table 18).
3Bh	803Bh	[4]	1 = PO5 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[4]	1 = PO5/PO3 asserts when $\overline{MR}$ = low (Table 6).

Table 15 only applies to PO5 of the MAX6872 and PO3 of the MAX6873. Write a 0 to a bit to make the PO5/PO3 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs). See Table 14 for Product 1. PO5 (MAX6872)/PO3 (MAX6873) deasserts when Product 1 or Product 2 = 1.

Table 16. PO6 (MAX6872)/PO4 (MAX6873) Output Dependency (Product 1)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
2Bh	802Bh	[0]	1 = PO6/PO4 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO6/PO4 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO6/PO4 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO6/PO4 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO6 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO6 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO6/PO4 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO6/PO4 assertion depends on watchdog 2 (Tables 25 and 26).
2Ch	802Ch	[0]	1 = PO6/PO4 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO6/PO4 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO6/PO4 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO6/PO4 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO6 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO6 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO6/PO4 assertion depends on GPI1 (Table 5).
		[7]	1 = PO6/PO4 assertion depends on GPI2 (Table 5).
2Dh	802Dh	[0]	1 = PO6/PO4 assertion depends on GPI3 (Table 5).
		[1]	1 = PO6/PO4 assertion depends on GPI4 (Table 5).
		[2]	1 = PO6 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO6 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO6/PO4 assertion depends on PO3 (MAX6872)/PO1 (MAX6873) (Tables 10 and 11).
		[5]	1 = PO6/PO4 assertion depends on PO4 (MAX6872)/PO2 (MAX6873) (Tables 12 and 13).
		[6]	1 = PO6/PO4 assertion depends on PO5 (MAX6872)/PO3 (MAX6873) (Tables 14 and 15).
		[7]	1 = PO6/PO4 assertion depends on PO7 (MAX6872)/PO5 (MAX6873) (Table 18).
31h	8031h	[0]	1 = PO6 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[5]	1 = PO6/PO4 asserts when $\overline{MR}$ = low (Table 6).

Table 16 only applies to PO6 of the MAX6872 and PO4 of the MAX6873. Write a 0 to a bit to make the PO6/PO4 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs). See Table 17 for Product 2. PO6 (MAX6872)/PO4 (MAX6873) deasserts when Product 1 or Product 2 = 1.

Table 17. PO6 (MAX6872)/PO4 (MAX6873) Output Dependency (Product 2)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
2Eh	802Eh	[0]	1 = PO6/PO4 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO6/PO4 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO6/PO4 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO6/PO4 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO6 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO6 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO6/PO4 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO6/PO4 assertion depends on watchdog 2 (Tables 25 and 26).
2Fh	802Fh	[0]	1 = PO6/PO4 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO6/PO4 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO6/PO4 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO6/PO4 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO6 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO6 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO6/PO4 assertion depends on GPI1 (Table 5).
		[7]	1 = PO6/PO4 assertion depends on GPI2 (Table 5).
30h	8030h	[0]	1 = PO6/PO4 assertion depends on GPI3 (Table 5).
		[1]	1 = PO6/PO4 assertion depends on GPI4 (Table 5).
		[2]	1 = PO6 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO6 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO6/PO4 assertion depends on PO3 (MAX6872)/PO1 (MAX6873) (Tables 10 and 11).
		[5]	1 = PO6/PO4 assertion depends on PO4 (MAX6872)/PO2 (MAX6873) (Tables 12 and 13).
		[6]	1 = PO6/PO4 assertion depends on PO5 (MAX6872)/PO3 (MAX6873) (Tables 14 and 15).
		[7]	1 = PO6/PO4 assertion depends on PO7 (MAX6872)/PO5 (MAX6873) (Table 18).
3Bh	803Bh	[5]	1 = PO6 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[5]	1 = PO6/PO4 asserts when $\overline{MR}$ = low (Table 6).

Table 17 only applies to PO6 of the MAX6872 and PO4 of the MAX6873. Write a 0 to a bit to make the PO6/PO4 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs). See Table 16 for Product 1. PO6 (MAX6872)/PO4 (MAX6873) deasserts when Product 1 or Product 2 = 1.

Table 18. PO7 (MAX6872)/PO5 (MAX6873) Output Dependency

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
32h	8032h	[0]	1 = PO7/PO5 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO7/PO5 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO7/PO5 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO7/PO5 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO7 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO7 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO7/PO5 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO7/PO5 assertion depends on watchdog 2 (Tables 25 and 26).
33h	8033h	[0]	1 = PO7/PO5 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO7/PO5 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO7/PO5 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO7/PO5 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO7 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO7 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO7/PO5 assertion depends on GPI1 (Table 5).
		[7]	1 = PO7/PO5 assertion depends on GPI2 (Table 5).
34h	8034h	[0]	1 = PO7/PO5 assertion depends on GPI3 (Table 5).
		[1]	1 = PO7/PO5 assertion depends on GPI4 (Table 5).
		[2]	1 = PO7 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO7 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO7/PO5 assertion depends on PO3 (MAX6872)/PO1 (MAX6873) (Tables 10 and 11).
		[5]	1 = PO7/PO5 assertion depends on PO4 (MAX6872)/PO2 (MAX6873) (Tables 12 and 13).
		[6]	1 = PO7/PO5 assertion depends on PO5 (MAX6872)/PO3 (MAX6873) (Tables 14 and 15).
		[7]	1 = PO7/PO5 assertion depends on PO6 (MAX6872)/PO4 (MAX6873) (Tables 16 and 17).
35h	8035h	[0]	1 = PO7 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[6]	1 = PO7 asserts when $\overline{MR}$ = low (Table 6).

Table 18 only applies to PO7 of the MAX6872 and PO5 of the MAX6873. Write a 0 to a bit to make the PO7/PO5 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs).

Table 19. PO8 (MAX6872 only) Output Dependency

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
36h	8036h	[0]	1 = PO8 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO8 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO8 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO8 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO8 assertion depends on IN5 primary undervoltage threshold (Table 4).
		[5]	1 = PO8 assertion depends on IN6 primary undervoltage threshold (Table 4).
		[6]	1 = PO8 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO8 assertion depends on watchdog 2 (Tables 25 and 26).
37h	8037h	[0]	1 = PO8 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO8 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO8 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO8 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO8 assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4).
		[5]	1 = PO8 assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4).
		[6]	1 = PO8 assertion depends on GPI1 (Table 5).
		[7]	1 = PO8 assertion depends on GPI2 (Table 5).
38h	8038h	[0]	1 = PO8 assertion depends on GPI3 (Table 5).
		[1]	1 = PO8 assertion depends on GPI4 (Table 5).
		[2]	1 = PO8 assertion depends on PO1 (Table 8).
		[3]	1 = PO8 assertion depends on PO2 (Table 9).
		[4]	1 = PO8 assertion depends on PO3 (Tables 10 and 11).
		[5]	1 = PO8 assertion depends on PO4 (Tables 12 and 13).
		[6]	1 = PO8 assertion depends on PO5 (Tables 14 and 15).
		[7]	1 = PO8 assertion depends on PO6 (Tables 16 and 17).
39h	8039h	[0]	1 = PO8 assertion depends on PO7 (Table 18).
40h	8040h	[7]	1 = PO8 asserts when $\overline{MR}$ = low (Table 6).

Table 19 only applies to PO8 of the MAX6872. Write a 0 to a bit to make the PO8 output independent of the respective signal (IN1–IN6 primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, $\overline{MR}$, or other programmable outputs).

Output Stage Configurations

Independently program each programmable output as active high or active low (Table 20). Additionally, program each programmable output as weak pullup, push-pull, open-drain, or charge pump (Tables 21 and 22). Every programmable output can be configured as open-drain or weak pullup; however, only PO1–PO4 (MAX6872) or PO1–PO2 (MAX6873) can be configured as charge-pump outputs, and only PO5–PO8 (MAX6872) or PO3–PO5 (MAX6873) can be configured as push-pull outputs. Finally, set the PO_ timeout period for each programmable output (Table 23).

An internal 10kΩ resistor provides the pullup resistance for outputs configured as weak pullup stages. Program each weak pullup output stage to refer to ABP or one of the IN3–IN6 inputs. The programmable outputs source up to 10mA and sink up to 4mA when configured as push-pull stages. Program each push-pull output stage to reference to one of IN3–IN6. PO1–PO4 (MAX6872)/ PO1–PO2 (MAX6873) pull to V_{ABP} + 5V when configured as charge-pump outputs.

Table 20. Programmable Output Active States

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
3Ah	803Ah	[0]	PO1 (MAX6872 only). 0 = active low, 1 = active high.
		[1]	PO2 (MAX6872 only). 0 = active low, 1 = active high.
		[2]	PO3 (MAX6872)/PO1 (MAX6873). 0 = active low, 1 = active high.
		[3]	PO4 (MAX6872)/PO2 (MAX6873). 0 = active low, 1 = active high.
		[4]	PO5 (MAX6872)/PO3 (MAX6873). 0 = active low, 1 = active high.
		[5]	PO6 (MAX6872)/PO4 (MAX6873). 0 = active low, 1 = active high.
		[6]	PO7 (MAX6872)/PO5 (MAX6873). 0 = active low, 1 = active high.
		[7]	PO8 (MAX6872 only). 0 = active low, 1 = active high.

Table 21. Programmable Output Stage Options (MAX6872)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	AFFECTED OUTPUT	DESCRIPTION
11h	8011h	[6:4]	PO1	000 = open drain, 001 = weak pullup to IN3, 010 = weak pullup to IN4, 011 = weak pullup to IN5, 100 = weak pullup to IN6, 101 = weak pullup to ABP, 110 = charge-pump output, 111 = not used.
15h	8015h	[6:4]	PO2	
1Ch	801Ch	[7:5]	PO3	
23h	8023h	[7:5]	PO4	
2Ah	802Ah	[7:4]	PO5	0000 = open drain, 0001 = weak pullup to IN3, 0010 = weak pullup to IN4, 0011 = weak pullup to IN5, 0100 = weak pullup to IN6, 0101 = weak pullup to ABP, 0110 = push-pull to IN3, 0111 = push-pull to IN4, 1000 = push-pull to IN5, 1001 = push-pull to IN6, 1010–1111 = not used.
31h	8031h	[7:4]	PO6	
35h	8035h	[7:4]	PO7	
39h	8039h	[7:4]	PO8	

Table 22. Programmable Output Stage Options (MAX6873)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	AFFECTED OUTPUT	DESCRIPTION
1Ch	801Ch	[7:5]	PO1	000 = open drain, 001 = weak pullup to IN3, 010 = weak pullup to IN4, 011–100 = not used, 101 = weak pullup to ABP, 110 = charge-pump output, 111 = not used.
23h	8023h	[7:5]	PO2	
2Ah	802Ah	[7:4]	PO3	0000 = open drain, 0001 = weak pullup to IN3, 0010 = weak pullup to IN4, 0011–0100 = not used, 0101 = weak pullup to ABP, 0110 = push-pull to IN3, 0111 = push-pull to IN4, 1000–1111 = not used.
31h	8031h	[7:4]	PO4	
35h	8035h	[7:4]	PO5	

Table 23. PO_ Timeout Periods

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	AFFECTED OUTPUTS		DESCRIPTION
			MAX6872	MAX6873	
11h	8011h	[3:1]	PO1	—	000 = 25µs 001 = 1.5625ms 010 = 6.25ms 011 = 25ms 100 = 50ms 101 = 200ms 110 = 400ms 111 = 1600ms
15h	8015h	[3:1]	PO2	—	
1Ch	801Ch	[4:2]	PO3	PO1	
23h	8023h	[4:2]	PO4	PO2	
2Ah	802Ah	[3:1]	PO5	PO3	
31h	8031h	[3:1]	PO6	PO4	
35h	8035h	[3:1]	PO7	PO5	
39h	8039h	[3:1]	PO8	—	

Charge-Pump Output Configuration

Configure the programmable outputs of the MAX6872/MAX6873 as charge-pump outputs to drive n-channel FETs for power-supply sequencing applications. Only PO1–PO4 (MAX6872) or PO1 and PO2 (MAX6873) can be configured as charge-pump output stages. The charge-pump output high voltage is typically V_{ABP} +5.5V when unloaded.

Push-Pull Output Configuration

The MAX6872/MAX6873s' programmable outputs sink 4mA and source 10mA when configured as push-pull outputs. Only PO5–PO8 (MAX6872) or PO3–PO5 (MAX6873) can be configured as push-pull output stages. The push-pull output stages refer to any of IN3–IN6 (MAX6872)/IN3–IN4 (MAX6873) as configured in Tables 21 and 22. Use the push-pull output configuration to drive loads with fast rise/fall times, or those with low impedance.

Weak Pullup Output Configuration

The MAX6872/MAX6873s' programmable outputs sink 4mA when configured as weak pullups. The weak pullup of 10kΩ refers to any of IN3–IN6 (MAX6872)/IN3–IN4 (MAX6873) or ABP as configured in Tables 21 and 22. All programmable outputs of the MAX6872/MAX6873 may be configured as weak pullups.

Open-Drain Output Configuration

Connect an external pullup resistor from the programmable output to an external voltage when configured as an open-drain output. PO1–PO4 (PO1 and PO2 for the MAX6873) may be pulled up to +13.2V. PO5–PO8 (PO3–PO5 for the MAX6873) may be pulled up to a voltage less than or equal to ABP. Choose the pullup resistor depending on the number of devices connected to the open-drain output and the allowable current consumption. The open-drain output configuration allows wire-ORed connections, and provides flexibility in setting the pullup current.

Configuring the MAX6872/MAX6873

The MAX6872/MAX6873 factory-default configuration sets all EEPROM registers to 00h except register 3Ah, which is set to FFh. This configuration sets all of the programmable outputs as active high, open drain (putting all outputs into high-impedance states until the device is reconfigured by the user). Each device requires configuration before full power is applied to the system. To configure the MAX6872/MAX6873, first apply an input voltage to IN1 or one of IN3–IN6 (MAX6872)/IN3–IN4 (MAX6873) (see the *Powering the MAX6872/MAX6873* section). V_{IN1} > +4V or one of V_{IN3}–V_{IN6} > +2.7V, to ensure device operation. Next, transmit data through the serial interface. Use the block write protocol to quickly configure the device. Write to the configuration registers first to ensure the device is configured properly. After completing the setup procedure, use the read word protocol to verify the data from the configuration registers. Lastly, use the write word protocol to write this data to the EEPROM registers. After completing EEPROM register configuration, apply full power to the system to begin normal operation. The non-volatile EEPROM stores the latest configuration upon removal of power. Write zeros to all EEPROM registers to clear the memory.

Software Reboot

A software reboot allows the user to restore the EEPROM configuration to the volatile registers without cycling the power supplies. Use the send byte command with data byte 88h to initiate a software reboot. The 3.5ms (max) power-up delay also applies after a software reboot.

SMBus/I²C-Compatible Serial Interface

The MAX6872/MAX6873 feature an I²C/SMBus-compatible serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL allow bidirectional communication between the MAX6872/MAX6873 and the master device at clock rates up to 400kHz. Figure 2 shows the interface timing diagram. The MAX6872/MAX6873 are transmit/receive slave-only devices, relying upon a master device to generate a clock signal. The master device (typically a microcontroller) initiates data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX6872/MAX6873 by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (SR) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse.

SCL is a logic input, while SDA is a logic input/open-drain output. SCL and SDA both require external pullup resistors to generate the logic-high voltage. Use 4.7kΩ for most applications.

Bit Transfer

Each clock pulse transfers one data bit. The data on SDA must remain stable while SCL is high (Figure 3), otherwise the MAX6872/MAX6873 register a START or STOP condition (Figure 4) from the master. SDA and SCL idle high when the bus is not busy.

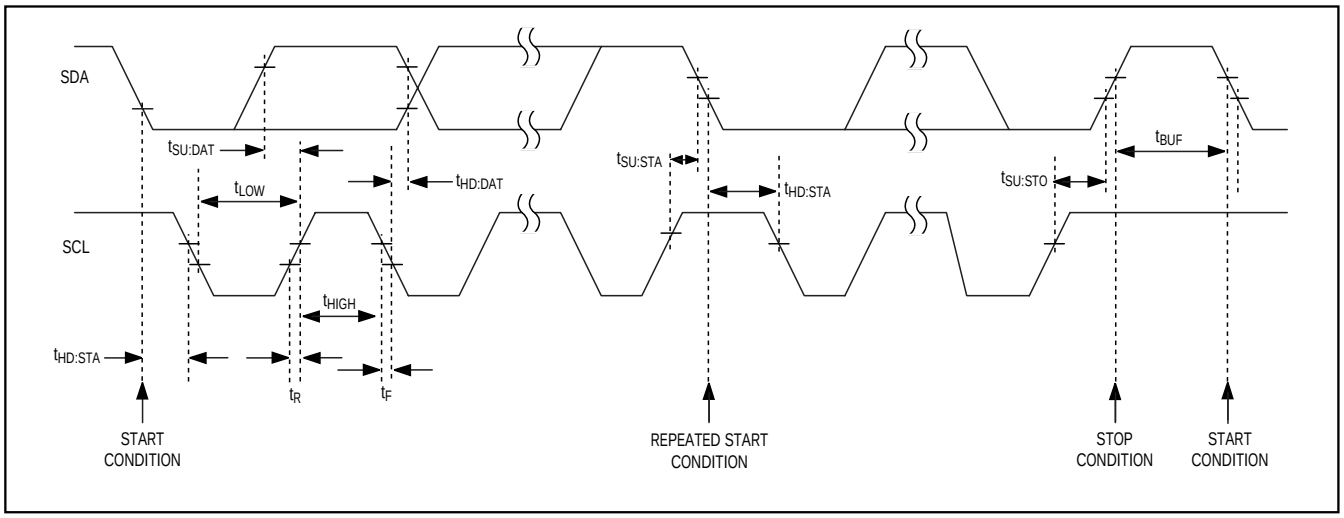


Figure 2. Serial-Interface Timing Details

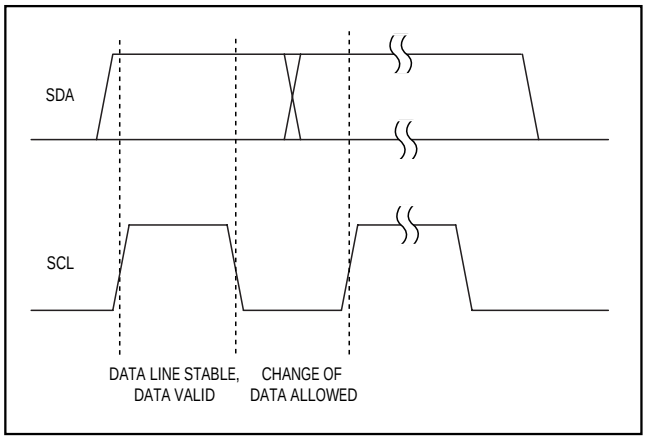


Figure 3. Bit Transfer

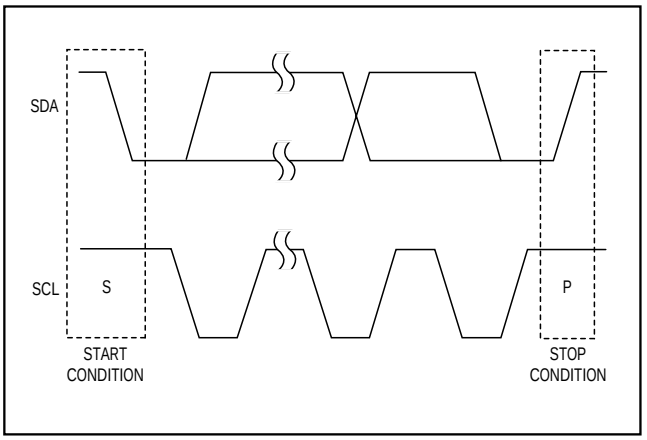


Figure 4. Start and Stop Conditions

Start and Stop Conditions

Both SCL and SDA idle high when the bus is not busy. A master device signals the beginning of a transmission with a START (S) condition (Figure 4) by transitioning SDA from high to low while SCL is high. The master device issues a STOP (P) condition (Figure 4) by transitioning SDA from low to high while SCL is high. A STOP condition frees the bus for another transmission. The bus remains active if a REPEATED START condition is generated, such as in the block read protocol (see Figure 7).

Early STOP Conditions

The MAX6872/MAX6873 recognize a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition. This condition is not a legal I^2C format. At least one clock pulse must separate any START and STOP conditions.

Repeated START Conditions

A REPEATED START (SR) condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation (see Figure 7). SR may also be used when the bus master is writing to several I^2C devices and does not want to relinquish control of the bus. The MAX6872/MAX6873 serial interface supports continuous write operations with or without an SR condition separating them. Continuous read operations require SR conditions because of the change in direction of data flow.

Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. The receiving device always generates an ACK. The MAX6872/MAX6873 generate an ACK when receiving an address or data by pulling SDA low during the 9th clock period (Figure 5). When transmitting data, such as when the master device reads data back from the MAX6872/MAX6873, the MAX6872/MAX6873 wait for the master device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if the receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time. The MAX6872/MAX6873 generate a NACK after the slave address during a software reboot, while writing to the EEPROM, or when receiving an illegal memory address.

Slave Address

The MAX6872/MAX6873 slave address conforms to the following table:

SA7 (MSB)	SA6	SA5	SA4	SA3	SA2	SA1	SA0 (LSB)
1	0	1	0	A1	A0	X	R/$\overline{W}$

X = Don't care.

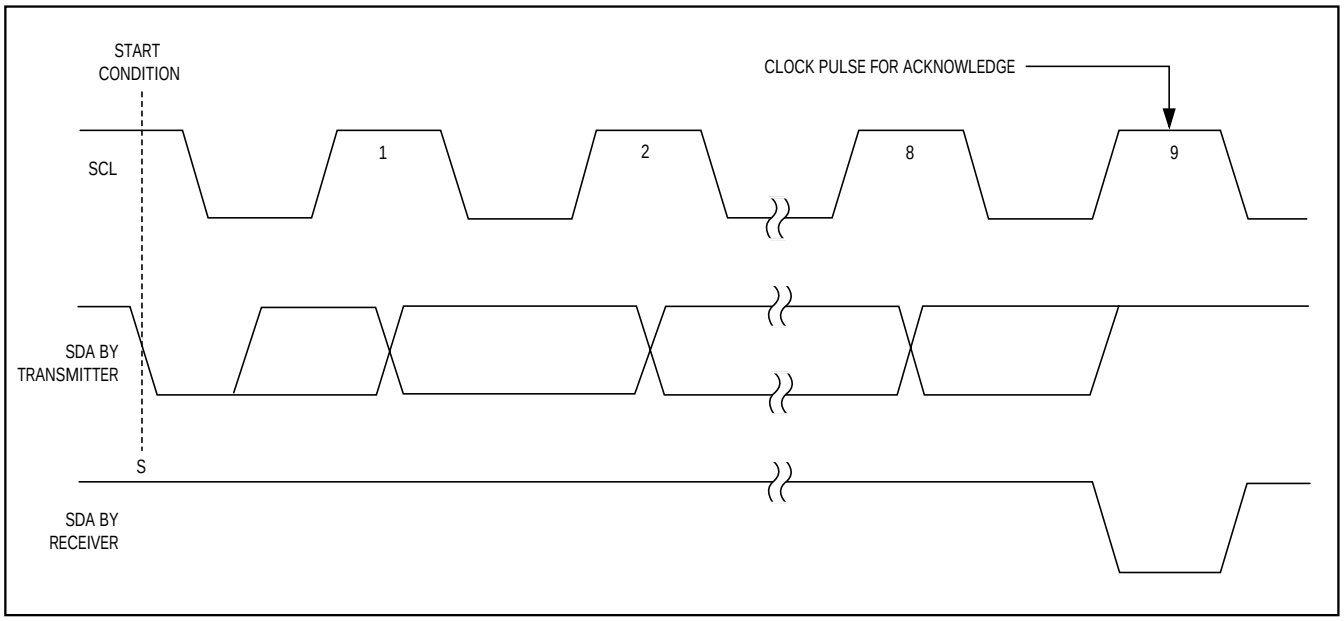


Figure 5. Acknowledge

SA7 through SA4 represent the standard interface address (1010) for devices with EEPROM. SA3 and SA2 correspond to the A1 and A0 address inputs of the MAX6872/MAX6873 (hard-wired as logic-low or logic-high). SA0 is a read/write flag bit (0 = write, 1 = read).

The A0 and A1 address inputs allow up to four MAX6872/MAX6873 devices to connect to one bus. Connect A0 and A1 to GND or to the serial interface power supply (see Figure 6).

Send Byte

The send byte protocol allows the master device to send one byte of data to the slave device (see Figure 7). The send byte presets a register pointer address for a subsequent read or write. The slave sends a NACK instead of an ACK if the master tries to send an address that is not allowed. If the master sends 80h, 81h, or 82h, the data is ACK. This could be start of the write byte/word protocol, and the slave expects at least one further data byte. If the master sends a stop condition, the internal address pointer does not change. If the master sends 84h, this signifies that the block read protocol is expected, and a repeated start condition should follow. The device reboots if the master sends 88h. The send byte procedure follows:

1) The master sends a start condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit data byte.
5) The addressed slave asserts an ACK on SDA.
6) The master sends a stop condition.

Write Byte/Word

The write byte/word protocol allows the master device to write a single byte in the register bank, preset an EEPROM (configuration or user) address for a subsequent read, or to write a single byte to the configuration or user EEPROM (see Figure 7). The write byte/word procedure follows:

1) The master sends a start condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit command code.
5) The addressed slave asserts an ACK on SDA.
6) The master sends an 8-bit data byte.
7) The addressed slave asserts an ACK on SDA.
8) The master sends a stop condition or sends another 8-bit data byte.
9) The addressed slave asserts an ACK on SDA.
10) The master sends a stop condition.

To write a single byte to the register bank, only the 8-bit command code and a single 8-bit data byte are sent. The command code must be in the range of 00h to 45h. The data byte is written to the register bank if the command code is valid. The slave generates a NACK at step 5 if the command code is invalid.

To preset an EEPROM (configuration or user) address for a subsequent read, the 8-bit command code and a single 8-bit data byte are sent. The command code must be 80h if the write is to be directed into the configuration EEPROM, or 81h or 82h, if the write is to be

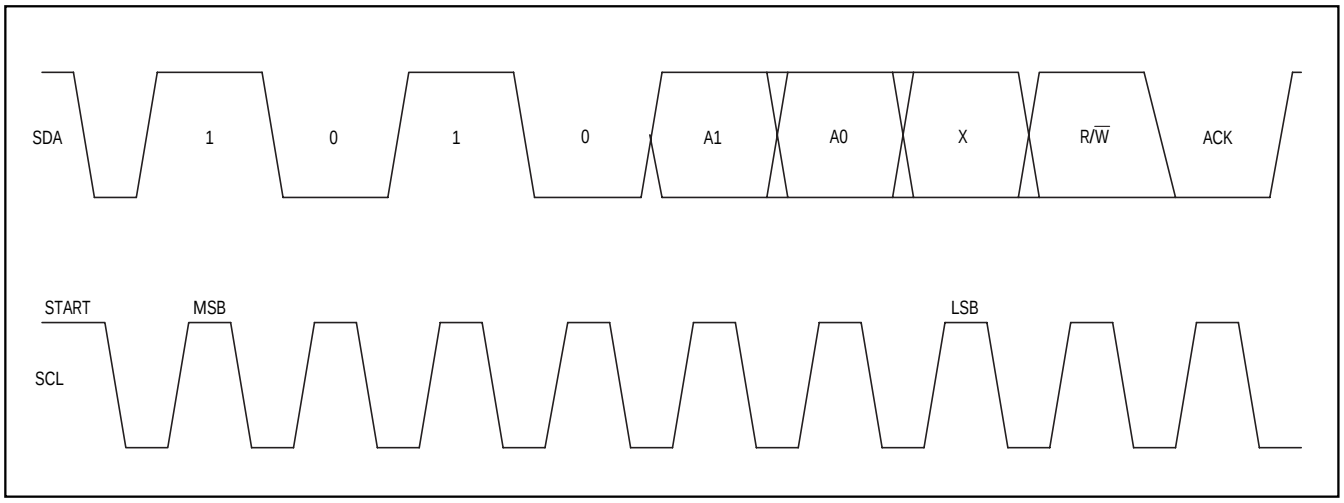


Figure 6. Slave Address

SEND BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	DATA	ACK	P
	7 bits	0		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Data Byte–presets the internal address pointer.

WRITE WORD FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	DATA	ACK	DATA	ACK	P
	7 bits	0		8 bits		8 bits		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Command Byte–MSB of the EEPROM register being written.

Data Byte–first byte is the LSB of the EEPROM address. Second byte is the actual data.

RECEIVE BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	DATA	$\overline{ACK}$	P
	7 bits	1		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Data Byte–reads data from the register commanded by the last read byte or write byte transmission. Also dependent on a send byte.

WRITE BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	DATA	ACK	P
	7 bits	0		8 bits		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Command Byte–selects register being written.

Data Byte–data goes into the register set by the command byte if the command is below 50h. If the command is 80h, 81h, or 82h, the data byte presets the LSB of an EEPROM address.

BLOCK WRITE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	BYTE COUNT= N	ACK	DATA BYTE 1	ACK	DATA BYTE ...	ACK	DATA BYTE N	ACK	P
	7 bits	0		83h		8 bits		8 bits		8 bits		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Command Byte–prepares device for block operation.

Data Byte–data goes into the register set by the command byte.

BLOCK READ FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	SR	ADDRESS	$\overline{WR}$	ACK	BYTE COUNT= 16	ACK	DATA BYTE 1	ACK	DATA BYTE ...	ACK	DATA BYTE N	ACK	P
	7 bits	0		84h			7 bits	1		10h		8 bits		8 bits		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Command Byte–prepares device for block operation.

Slave Address–equivalent to chip-select line of a 3-wire interface.

Data Byte–data goes into the register set by the command byte.

S = Start condition.
P = Stop condition.

Shaded = Slave transmission.
SR = Repeated start condition.

Figure 7. SMBus/I²C Protocols

directed into the user EEPROM. If the command code is 80h, the data byte must be in the range of 00h to 45h. If the command code is 81h or 82h, the data byte can be 00h to FFh. A NACK is generated in step 7 if none of the above conditions are true.

To write a single byte of data to the user or configuration EEPROM, the 8-bit command code and a single 8-bit data byte are sent. The following 8-bit data byte is written to the addressed EEPROM location.

Block Write

The block write protocol allows the master device to write a block of data (1 to 16 bytes) to the EEPROM or to the register bank (see Figure 7). The destination address must already be set by the send byte or write byte protocol and the command code must be 83h. If the number of bytes to be written causes the address pointer to exceed 45h for the configuration register or configuration EEPROM, the address pointer stays at 45h, overwriting this memory address with the remaining bytes of data. The last data byte sent is stored at register address 45h. If the number of bytes to be written exceeds the address pointer FFh for the user EEPROM, the address pointer loops back to 00h, and continues writing bytes until all data is written. The block write procedure follows:

1) The master sends a start condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends the 8-bit command code for block write (83h).
5) The addressed slave asserts an ACK on SDA.
6) The master sends the 8-bit byte count (1 to 16 bytes) N.
7) The addressed slave asserts an ACK on SDA.
8) The master sends 8 bits of data.
9) The addressed slave asserts an ACK on SDA.
10) Repeat steps 8 and 9 one time.
11) The master generates a stop condition.

Receive Byte

The receive byte protocol allows the master device to read the register content of the MAX6872/MAX6873 (see Figure 7). The EEPROM or register address must be preset with a send byte or write word protocol first. Once the read is complete, the internal pointer increases by one. Repeating the receive byte protocol reads the contents of the next address. The receive byte procedure follows:

1) The master sends a start condition.
2) The master sends the 7-bit slave address and a read bit (high).
3) The addressed slave asserts an ACK on SDA.
4) The slave sends 8 data bits.
5) The master asserts a NACK on SDA.
6) The master generates a stop condition.

Block Read

The block read protocol allows the master device to read a block of 16 bytes from the EEPROM or register bank (see Figure 7). Read fewer than 16 bytes of data by issuing an early STOP condition from the master, or by generating a NACK with the master. The send byte or write byte protocol predetermines the destination address with a command code of 84h. The block read procedure follows:

1) The master sends a start condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends 8 bits of the block read command (84h).
5) The slave asserts an ACK on SDA, unless busy.
6) The master generates a repeated start condition.
7) The master sends the 7-bit slave address and a read bit (high).
8) The slave asserts an ACK on SDA.
9) The slave sends the 8-bit byte count (16).
10) The master asserts an ACK on SDA.
11) The slave sends 8 bits of data.
12) The master asserts an ACK on SDA.
13) Repeat steps 8 and 9 fifteen times.
14) The master generates a stop condition.

Address Pointers

Use the send byte protocol to set the register address pointers before read and write operations. For the configuration registers, valid address pointers range from 00h to 45h. Register addresses outside of this range result in a NACK being issued from the MAX6872/MAX6873. When using the block write protocol, the address pointer automatically increments after each data byte, except when the address pointer is already at 45h. If the address pointer is already 45h, and more data bytes are being sent, these subsequent bytes overwrite address 45h repeatedly, leaving only the last data byte sent stored at this register address.

For the configuration EEPROM, valid address pointers range from 8000h to 8045h. Registers 8046h to 804Fh are reserved and should not be overwritten. Register addresses from 8050h to 80FFh return a NACK from the MAX6872/MAX6873. When using the block write protocol, the address pointer automatically increments after each data byte, except when the address pointer is already at 8045h. If the address pointer is already 8045h, and more data bytes are being sent, these subsequent bytes overwrite address 8045h repeatedly, leaving only the last data byte sent stored at this register address.

For the user EEPROM, valid address pointers range from 8100h to 81FFh and 8200h to 82FFh. Block write and block read protocols allow the address pointer to reset (to 8100h or 8200h) when attempting to write or read beyond 81FFh or 82FFh.

Configuration EEPROM

The configuration EEPROM addresses range from 8000h to 8045h. Write data to the configuration EEPROM to automatically set up the MAX6872/MAX6873 upon power-up. Data transfers from the configuration EEPROM to the configuration registers when ABP exceeds UVLO during power-up or after a software reboot. After ABP exceeds UVLO, an internal 1MHz clock starts after a 5µs delay, and data transfer begins. Data transfer disables access to the configuration registers and EEPROM. The data transfer from EEPROM to configuration registers takes 3.5ms (max). Read configuration EEPROM data at any time after power-up or software reboot. Write commands to the configuration EEPROM are allowed at any time after power-up or software reboot, unless the configuration lock bit is set (see Table 28). The maximum cycle time to write a single byte is 11ms (max).

User EEPROM

The 512 byte user EEPROM addresses range from 8100h to 82FFh (see Figure 8). Store software-revision data, board-revision data, and other data in these registers. The maximum cycle time to write a single byte is 11ms (max).

Configuration Register Bank and EEPROM

The configuration registers can be directly modified by the serial interface without modifying the EEPROM after the power-up procedure terminates and the configuration EEPROM data has been loaded into the configuration register bank. Use the write byte or block write protocols to write directly to the configuration registers. Changes to the configuration registers take effect immediately and are lost upon power removal.

At device power-up, the register bank loads configuration data from the EEPROM. Configuration data may be directly altered in the register bank during application development, allowing maximum flexibility. Transfer the new configuration data, byte by byte, to the configuration EEPROM with the write byte protocol. The next device power-up or software reboot automatically loads the new configuration.

Configuring the Watchdog Timers (Registers 3Ch–3Fh)

A watchdog timer monitors microprocessor (µP) software execution for a stalled condition and resets the µP if it stalls. The output of a watchdog timer (one of the

Table 24. Register Map

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/ WRITE	DESCRIPTION
00h	8000h	R/W	IN1 primary undervoltage detector threshold (Table 2)
01h	8001h	R/W	IN2 primary undervoltage detector threshold (Table 3)
02h	8002h	R/W	IN3 primary undervoltage detector threshold (Table 4)
03h	8003h	R/W	IN4 primary undervoltage detector threshold (Table 4)
04h	8004h	R/W	IN5 primary undervoltage detector threshold (MAX6872 only) (Table 4)
05h	8005h	R/W	IN6 primary undervoltage detector threshold (MAX6872 only) (Table 4)
06h	8006h	R/W	IN1 secondary undervoltage/overvoltage detector threshold (Table 2).
07h	8007h	R/W	IN2 secondary undervoltage/overvoltage detector threshold (Table 3)
08h	8008h	R/W	IN3 secondary undervoltage/overvoltage detector threshold (Table 4)
09h	8009h	R/W	IN4 secondary undervoltage/overvoltage detector threshold (Table 4)
0Ah	800Ah	R/W	IN5 secondary undervoltage/overvoltage detector threshold (MAX6872 only) (Table 4)

Table 24. Register Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/ WRITE	DESCRIPTION
0Bh	800Bh	R/W	IN6 secondary undervoltage/overvoltage detector threshold (MAX6872 only) (Table 4)
0Ch	800Ch	R/W	Secondary undervoltage/overvoltage selection (Tables 2, 4)
0Dh	800Dh	R/W	Threshold range selection (Tables 2, 3, 4)
0Eh	800Eh	R/W	PO1 (MAX6872 only) input selection (Table 8)
0Fh	800Fh	R/W	PO1 (MAX6872 only) input selection (Table 8)
10h	8010h	R/W	PO1 (MAX6872 only) input selection (Table 8)
11h	8011h	R/W	PO1 (MAX6872 only) input selection, PO_ timeout period, and output type selection (Tables 8, 21, and 23)
12h	8012h	R/W	PO2 (MAX6872 only) input selection (Table 9)
13h	8013h	R/W	PO2 (MAX6872 only) input selection (Table 9)
14h	8014h	R/W	PO2 (MAX6872 only) input selection (Table 9)
15h	8015h	R/W	PO2 (MAX6872 only) input selection, PO_ timeout period, and output type selection (Tables 9, 21, and 23)
16h	8016h	R/W	PO3 (MAX6872)/PO1 (MAX6873) input selection—Product 1 (Table 10)
17h	8017h	R/W	PO3 (MAX6872)/PO1 (MAX6873) input selection—Product 1 (Table 10)
18h	8018h	R/W	PO3 (MAX6872)/PO1 (MAX6873) input selection—Product 1 (Table 10)
19h	8019h	R/W	PO3 (MAX6872)/PO1 (MAX6873) input selection—Product 2 (Table 11)
1Ah	801Ah	R/W	PO3 (MAX6872)/PO1 (MAX6873) input selection—Product 2 (Table 11)
1Bh	801Bh	R/W	PO3 (MAX6872)/PO1 (MAX6873) input selection—Product 2 (Table 11)
1Ch	801Ch	R/W	PO3 (MAX6872)/PO1 (MAX6873) input selection—Products 1 and 2, PO_ timeout period, and output type selection (Tables 10, 11, 21, 22, and 23)
1Dh	801Dh	R/W	PO4 (MAX6872)/PO2 (MAX6873) input selection—Product 1 (Table 12)
1Eh	801Eh	R/W	PO4 (MAX6872)/PO2 (MAX6873) input selection—Product 1 (Table 12)
1Fh	801Fh	R/W	PO4 (MAX6872)/PO2 (MAX6873) input selection—Product 1 (Table 12)
20h	8020h	R/W	PO4 (MAX6872)/PO2 (MAX6873) input selection—Product 2 (Table 13)
21h	8021h	R/W	PO4 (MAX6872)/PO2 (MAX6873) input selection—Product 2 (Table 13)
22h	8022h	R/W	PO4 (MAX6872)/PO2 (MAX6873) input selection—Product 2 (Table 13)
23h	8023h	R/W	PO4 (MAX6872)/PO2 (MAX6873) input selection—Products 1 and 2, PO_ timeout period, and output type selection (Tables 12, 13, 21, 22, and 23)
24h	8024h	R/W	PO5 (MAX6872)/PO3 (MAX6873) input selection—Product 1 (Table 14)
25h	8025h	R/W	PO5 (MAX6872)/PO3 (MAX6873) input selection—Product 1 (Table 14)
26h	8026h	R/W	PO5 (MAX6872)/PO3 (MAX6873) input selection—Product 1 (Table 14)
27h	8027h	R/W	PO5 (MAX6872)/PO3 (MAX6873) input selection—Product 2 (Table 15)
28h	8028h	R/W	PO5 (MAX6872)/PO3 (MAX6873) input selection—Product 2 (Table 15)
29h	8029h	R/W	PO5 (MAX6872)/PO3 (MAX6873) input selection—Product 2 (Table 15)
2Ah	802Ah	R/W	PO5 (MAX6872)/PO3 (MAX6873) input selection—Products 1 and 2, PO_ timeout period, and output type selection (Tables 14, 21, 22, and 23)
2Bh	802Bh	R/W	PO6 (MAX6872)/PO4 (MAX6873) input selection—Product 1 (Table 16)
2Ch	802Ch	R/W	PO6 (MAX6872)/PO4 (MAX6873) input selection—Product 1 (Table 16)

Table 24. Register Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/ WRITE	DESCRIPTION
2Dh	802Dh	R/W	PO6 (MAX6872)/PO4 (MAX6873) input selection—Product 1 (Table 16)
2Eh	802Eh	R/W	PO6 (MAX6872)/PO4 (MAX6873) input selection—Product 2 (Table 17)
2Fh	802Fh	R/W	PO6 (MAX6872)/PO4 (MAX6873) input selection—Product 2 (Table 17)
30h	8030h	R/W	PO6 (MAX6872)/PO4 (MAX6873) input selection—Product 2 (Table 17)
31h	8031h	R/W	PO6 (MAX6872)/PO4 (MAX6873) input selection—Products 1 and 2, PO_ timeout period, and output type selection (Tables 16, 21, 22, and 23)
32h	8032h	R/W	PO7 (MAX6872)/PO5 (MAX6873) input selection (Table 18)
33h	8033h	R/W	PO7 (MAX6872)/PO5 (MAX6873) input selection (Table 18)
34h	8034h	R/W	PO7 (MAX6872)/PO5 (MAX6873) input selection (Table 18)
35h	8035h	R/W	PO7 (MAX6872)/PO5 (MAX6873) input selection, PO_ timeout period, and output type selection (Tables 18, 21, 22, and 23)
36h	8036h	R/W	PO8 (MAX6872 only) input selection (Table 19)
37h	8037h	R/W	PO8 (MAX6872 only) input selection (Table 19)
38h	8038h	R/W	PO8 (MAX6872 only) input selection (Table 19)
39h	8039h	R/W	PO8 (MAX6872 only) input selection, PO_ timeout period, and output type selection (Tables 19, 21, 22, and 23)
3Ah	803Ah	R/W	Programmable output polarity (active high/active low) (Table 20)
3Bh	803Bh	R/W	GPI_ input polarity, PO5, PO6 (Tables 5, 15, and 17)
3Ch	803Ch	R/W	WD1 input selection and timeout enable (Table 25)
3Dh	803Dh	R/W	WD1 initial and normal timeout duration (Table 26)
3Eh	803Eh	R/W	WD2 input selection and timeout enable (Table 25)
3Fh	803Fh	R/W	WD2 initial and normal timeout duration (Table 26)
40h	8040h	R/W	$\overline{MR}$ input and programmable output behavior (Table 6)
41h	8041h	R/W	$\overline{MARGIN}$ and programmable output behavior (Table 7)
42h	8042h	R/W	Programmable output state with $\overline{MARGIN}$ assertion (Table 7)
43h	8043h	R/W	User EEPROM write disable (Table 29)
44h	8044h	R/W	Set to 0
45h	8045h	R/W	Configuration lock (Table 28)
46h	8046h	—	Reserved. Should not be overwritten.
47h	8047h	—	Reserved. Should not be overwritten.
48h	8048h	—	Reserved. Should not be overwritten.
49h	8049h	—	Reserved. Should not be overwritten.
4Ah	804Ah	—	Reserved. Should not be overwritten.
4Bh	804Bh	—	Reserved. Should not be overwritten.
4Ch	804Ch	—	Reserved. Should not be overwritten.
4Dh	804Dh	—	Reserved. Should not be overwritten.
4Eh	804Eh	—	Reserved. Should not be overwritten.
4Fh	804Fh	—	Reserved. Should not be overwritten.

Table 24. Register Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/ WRITE	DESCRIPTION
50h	—	R	Reserved. Should not be overwritten.
51h	—	R	Reserved. Should not be overwritten.
52h	—	R	Reserved. Should not be overwritten.
53h	—	R	Reserved. Should not be overwritten.
54h	—	R	Reserved. Should not be overwritten.
55h	—	R	Reserved. Should not be overwritten.
56h	—	R	Reserved. Should not be overwritten.
57h	—	R	Reserved. Should not be overwritten.
58h	—	R	Reserved. Should not be overwritten.
59h	—	R	Reserved. Should not be overwritten.
5Ah	—	R	Reserved. Should not be overwritten.
5Bh	—	R	Reserved. Should not be overwritten.
5Ch	—	R	Reserved. Should not be overwritten.
5Dh	—	R	Reserved. Should not be overwritten.
5Eh	—	R	Reserved. Should not be overwritten.
5Fh	—	R	Reserved. Should not be overwritten.
60h	—	R	Fault flags for IN1–IN6 (primary thresholds) (Table 27)
61h	—	R	Fault flags for IN1–IN6 (secondary thresholds) (Table 27)
62h	—	R	Fault flags for WD_, GPI_, and $\overline{MR}$ (Table 27)

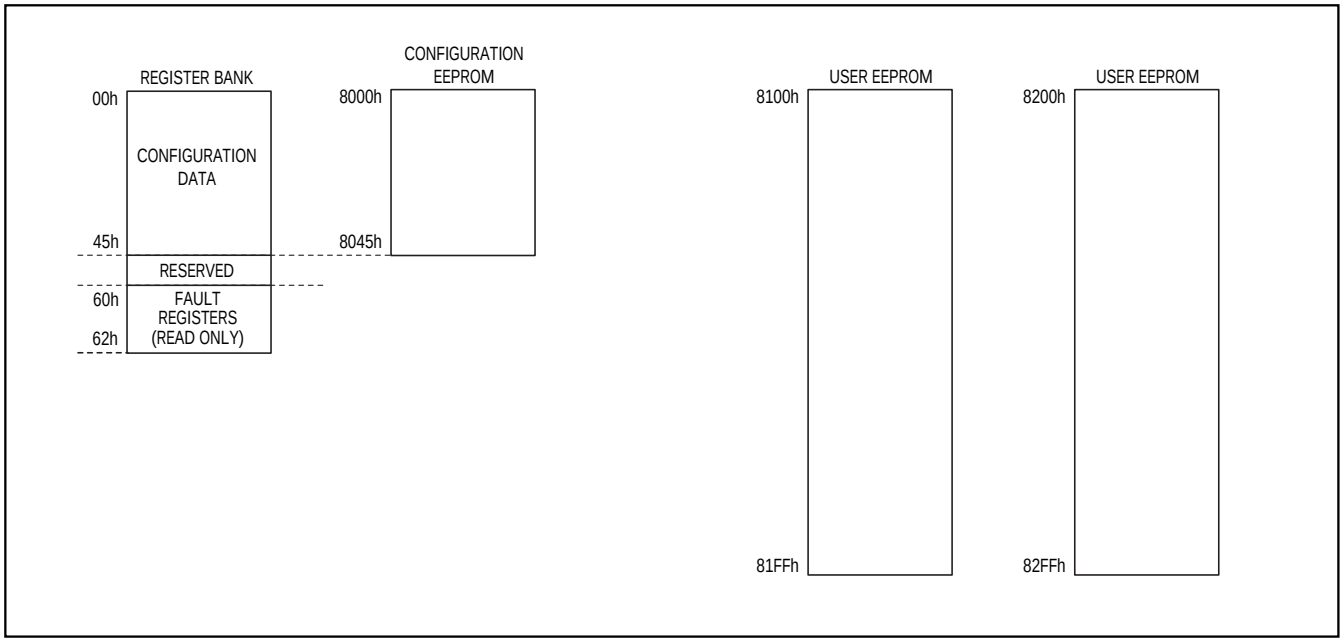


Figure 8. Memory Map

programmable outputs) connects to the reset input or a nonmaskable interrupt of the µP.

Registers 3Ch–3Fh configure the watchdog functionality of the MAX6872/MAX6873. Program each watchdog timer to assert one or more programmable outputs (see Tables 8–19). Program each watchdog timer to reset on one of the GPI_ inputs, one of the programmable outputs, or a combination of one GPI_ input and one programmable output.

Each watchdog timer features independent initial and normal watchdog timeout periods. The initial watchdog timeout period applies immediately after power-up, after a reset event takes place, or after enabling the watchdog timer. The initial watchdog timeout period allows the µP to perform its initialization process. If no pulse occurs during the initial watchdog timeout period, the µP is taking too long to initialize, indicating a potential problem.

The normal watchdog timeout period applies in every other cycle after the initial watchdog timeout period occurs. The normal watchdog timeout period monitors a pulsed output of the µP that indicates when normal processor behavior occurs. If no pulse occurs during the normal watchdog timeout period, this indicates that the processor has stopped operating or is stuck in an infinite execution loop.

Disable or enable each initial timeout period through registers 3Ch and 3Eh. Registers 3Dh and 3Fh program the initial and normal watchdog timeout periods, and enable or disable each watchdog timer. See Tables 25 and 26 for a summary of the watchdog behavior.

Fault Detector

Registers 60h–62h store all fault conditions, including undervoltage, overvoltage, GPI_, and watchdog timer faults (see Table 27). Fault registers are read-only and lose contents upon power removal. The first read command from the fault registers after power-up gives invalid data. Any $\overline{MR}$ assertion writes to the fault register. Reading the fault register clears all fault flags. Both GPI_ and WD_ bits assert if any of the GPI_ inputs are configured as watchdog inputs (WD_) and a watchdog fault occurs.

Table 25. Watchdog Inputs (Addresses 3Ch (Watchdog 1), 3Eh (Watchdog 2))

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
3Ch (watchdog 1) 3Eh (watchdog 2)	803Ch (watchdog 1) 803Eh (watchdog 2)	[1:0]	Watchdog Input Selection: 00 = GPI1 01 = GPI2 10 = GPI3 11 = GPI4
		[4:2]	Watchdog Internal Input Selection: 000 = PO1 (MAX6872), not used (MAX6873) 001 = PO2 (MAX6872), not used (MAX6873) 010 = PO3 (MAX6872), PO1 (MAX6873) 011 = PO4 (MAX6872), PO2 (MAX6873) 100 = PO5 (MAX6872), PO3 (MAX6873) 101 = PO6 (MAX6872), PO4 (MAX6873) 110 = PO7 (MAX6872), PO5 (MAX6873) 111 = PO8 (MAX6872), not used (MAX6873)
		[6:5]	Watchdog Dependency on Inputs: 00 = 11 = Watchdog clear depends on both GPI_ from 3Ch[1:0] (watchdog 1) or 3Eh[1:0] (watchdog 2) and PO_ from 3Ch[4:2] (watchdog 1) or 3Eh[4:2] (watchdog 2). 01 = watchdog clear depends only on PO_ from 3Ch[4:2] (watchdog 1) or 3Eh[4:2] (watchdog 2). 10 = watchdog clear depends only on GPI_ from 3Ch[1:0] (watchdog 1) or 3Eh[1:0] (watchdog 2).
		[7]	Initial Watchdog Timeout Period Enable: 0 = Disables initial watchdog timeout period (normal watchdog timeout period not affected). 1 = Enables initial watchdog timeout period.

Table 26. Watchdog Timeout Period Selection (Addresses 3Dh (Watchdog 1), 3Fh (Watchdog 2))

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
3Dh (watchdog 1) 3Fh (watchdog 2)	803Dh (watchdog 1) 803Fh (watchdog 2)	[2:0]	Normal Watchdog Timeout Period: 000 = 6.25ms 001 = 25ms 010 = 100ms 011 = 400ms 100 = 1.6s 101 = 6.4s 110 = 25.6s 111 = 102.4s
		[5:3]	Initial Watchdog Timeout Period (Immediately following power-up, reset event, or enabling watchdog): 000 = 6.25ms 001 = 25ms 010 = 100ms 011 = 400ms 100 = 1.6s 101 = 6.4s 110 = 25.6s 111 = 102.4s
		[6]	Watchdog Enable: 0 = Disables watchdog timer 1 = Enables watchdog timer
		[7]	Not Used

Configuration Lock

Lock the configuration register bank and configuration EEPROM contents after initial programming by setting the lock bit high (see Table 28). Locking the configuration prevents write operations to all registers except the configuration lock register. Clear the lock bit to reconfigure the device.

Write Disable

A unique write disable feature protects the MAX6872/MAX6873 from inadvertent user EEPROM writes. As input voltages that power the serial interface, a µP, or any other writing devices fall, unintentional data may be written onto the data bus. The user EEPROM write disable function (see Table 29) ensures that unintentional data does not corrupt the MAX6872/MAX6873 EEPROM data.

Applications Information

Configuration Download at Power-Up

The configuration of the MAX6872/MAX6873 (undervoltage/overvoltage thresholds, PO_ timeout periods, watchdog behavior, programmable output conditions and configurations, etc.) depends on the contents of the EEPROM. The EEPROM comprises buffered latches that store the configuration. The local volatile memory latches lose their contents at power-down. Therefore, at power-up, the device configuration must be restored by downloading the contents of the EEPROM (non-volatile memory) to the local latches. This download occurs in a number of steps:

1) Programmable outputs go high impedance with no power applied to the device.
2) When ABP exceeds +1V, all programmable outputs are weakly pulled to GND through a 10µA current sink.
3) When ABP exceeds UVLO, the configuration EEPROM starts to download its contents to the volatile configuration registers. The programmable outputs assume their programmed conditional output state when download is complete.
4) Any attempt to communicate with the device prior to this download completion results in a NACK being issued from the MAX6872/MAX6873.

Table 27. Fault Registers (60h–62h)

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
60h	[0]	1 = IN1 falls below primary undervoltage threshold.
	[1]	1 = IN2 falls below primary undervoltage threshold.
	[2]	1 = IN3 falls below primary undervoltage threshold.
	[3]	1 = IN4 falls below primary undervoltage threshold.
	[4]	1 = IN5 (MAX6872 only) falls below primary undervoltage threshold.
	[5]	1 = IN6 (MAX6872 only) falls below primary undervoltage threshold.
	[7:6]	Not used.
61h	[0]	1 = IN1 falls below secondary undervoltage threshold or rises above secondary overvoltage threshold, depending on the settings in register 0Ch (see Tables 2, 3, and 4).
	[1]	1 = IN2 falls below secondary undervoltage threshold or rises above secondary overvoltage threshold, depending on the settings in register 0Ch (see Tables 2, 3, and 4).
	[2]	1 = IN3 falls below secondary undervoltage threshold or rises above secondary overvoltage threshold, depending on the settings in register 0Ch (see Tables 2, 3, and 4).
	[3]	1 = IN4 falls below secondary undervoltage threshold or rises above secondary overvoltage threshold, depending on the settings in register 0Ch (see Tables 2, 3, and 4).
	[4]	1 = IN5 (MAX6872 only) falls below secondary undervoltage threshold or rises above secondary overvoltage threshold, depending on the settings in register 0Ch (see Tables 2, 3, and 4).
	[5]	1 = IN6 (MAX6872 only) falls below secondary undervoltage threshold or rises above secondary overvoltage threshold, depending on the settings in register 0Ch (see Tables 2, 3, and 4).
	[7:6]	Not used.
62h	[0]	1 = WD1 asserted.
	[1]	1 = WD2 asserted.
	[2]	1 = GPI1 asserted.
	[3]	1 = GPI2 asserted.
	[4]	1 = GPI3 asserted.
	[5]	1 = GPI4 asserted.
	[6]	1 = $\overline{MR}$ asserted.
	[7]	Not used.

Forcing Programmable Outputs High During Power-Up

A weak 10µA pulldown holds all programmable outputs low during power-up until ABP exceeds the undervoltage lockout (UVLO) threshold. Applications requiring a guaranteed high programmable output for ABP down to GND require external pullup resistors to maintain the logic state until ABP exceeds UVLO. Use 20kΩ resistors for most applications.

Driving High-Side MOSFET Switches with the MAX6872/MAX6873

High-side MOSFET switches are commonly used in power-supply sequencing applications. First, configure the programmable output of the MAX6872/MAX6873 as an active-low charge-pump output and set the conditions to assert this output. Connect the programmable output to the gate of an n-channel MOSFET. As the conditions to deassert this output are met, the output deasserts high (V_{ABP} +5V), turning on the FET, thus allowing the voltage on the drain to pass through to the downstream device (see Figure 9).

Table 28. Configuration Lock Register

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
45h	8045h	[0]	0 = configuration unlocked. 1 = configuration locked.
		[7:1]	Not used.

Table 29. Write Disable Register

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
43h	8043h	[0]	0 = write not disabled if PO1 asserts (MAX6872). 1 = write disabled if PO1 asserts (MAX6872). Set to 0 (MAX6873).
		[1]	0 = write not disabled if PO2 asserts (MAX6872). 1 = write disabled if PO2 asserts (MAX6872). Set to 0 (MAX6873).
		[2]	0 = write not disabled if PO3 (MAX6872)/PO1 (MAX6873) asserts. 1 = write disabled if PO3 (MAX6872)/PO1 (MAX6873) asserts.
		[3]	0 = write not disabled if PO4 (MAX6872)/PO2 (MAX6873) asserts. 1 = write disabled if PO4 (MAX6872)/PO2 (MAX6873) asserts.
		[4]	0 = write not disabled if PO5 (MAX6872)/PO3 (MAX6873) asserts. 1 = write disabled if PO5 (MAX6872)/PO3 (MAX6873) asserts.
		[5]	0 = write not disabled if PO6 (MAX6872)/PO4 (MAX6873) asserts. 1 = write disabled if PO6 (MAX6872)/PO4 (MAX6873) asserts.
		[6]	0 = write not disabled if PO7 (MAX6872)/PO5 (MAX6873) asserts. 1 = write disabled if PO7 (MAX6872)/PO5 (MAX6873) asserts.
		[7]	0 = write not disabled if PO8 asserts (MAX6872). 1 = write disabled if PO8 asserts (MAX6872). Set to 0 (MAX6873).

Uses for General-Purpose Inputs (GPI1–GPI4)

Watchdog Timer

Program GPI_ as an input to one of the watchdog timers in the MAX6872/MAX6873. The GPI_ input must toggle within the watchdog timeout period, otherwise any programmable output dependent on the watchdog timer asserts.

Additional Manual Reset Functions

The PO7 (MAX6872)/PO5 (MAX6873) programmable outputs allow a single set (product 1 only) of conditions to assert the output. Program the set of conditions to depend on one of the GPI_ inputs. Any output that depends on GPI_ asserts when GPI_ is held in its active state, effectively acting as a manual reset input.

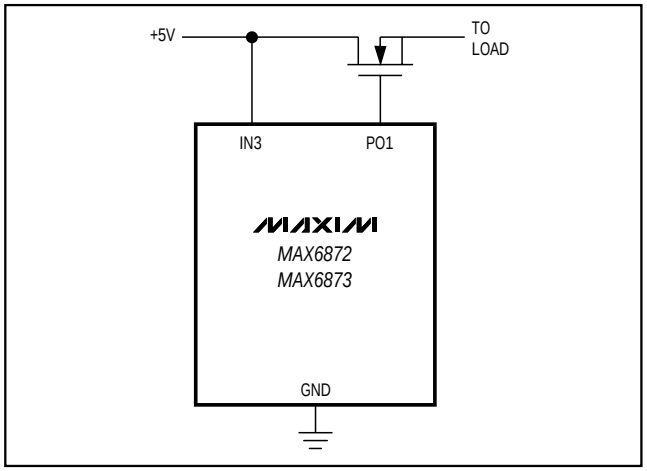
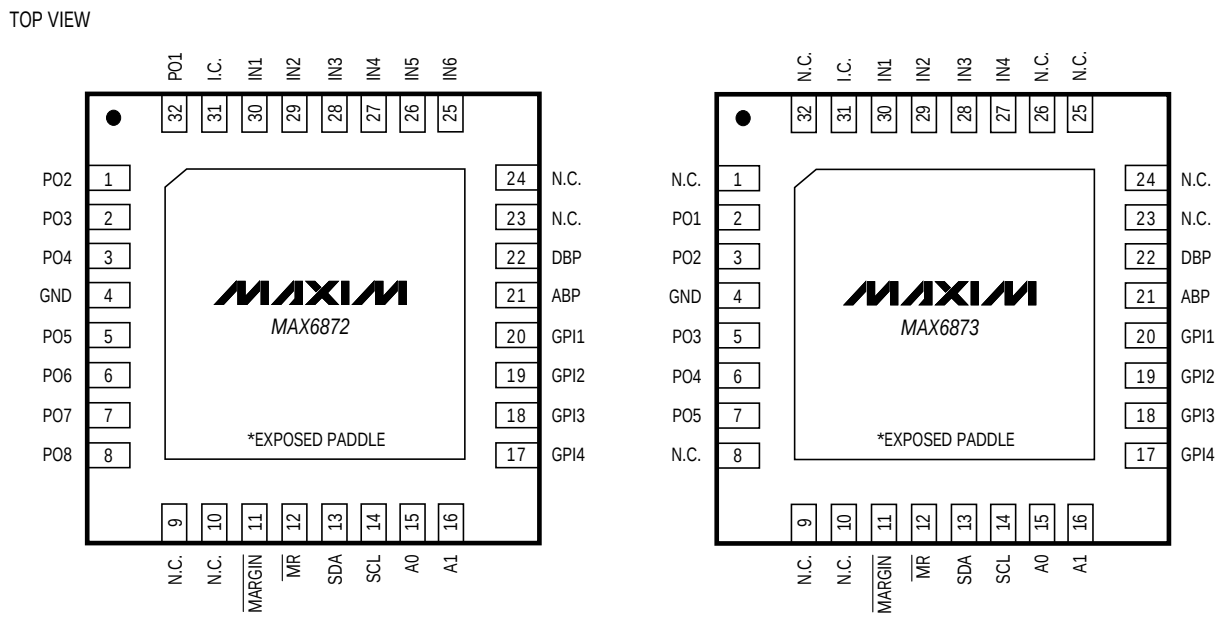


Figure 9. Driving High-Side n-Channel MOSFET Switches

Pin Configurations



Selector Guide

PART	VOLTAGE-DETECTOR INPUTS	GENERAL-PURPOSE INPUTS	PROGRAMMABLE OUTPUTS
MAX6872ETJ	6	4	8
MAX6873ETJ	4	4	5

Other Fault Signals from µC

Connect a general-purpose output from a µC to one of the GPI_ inputs to allow interrupts to assert any output of the MAX6872/MAX6873. Configure one of the programmable outputs to assert on whichever GPI_ input connects to the general-purpose output of the µC.

Layout and Bypassing

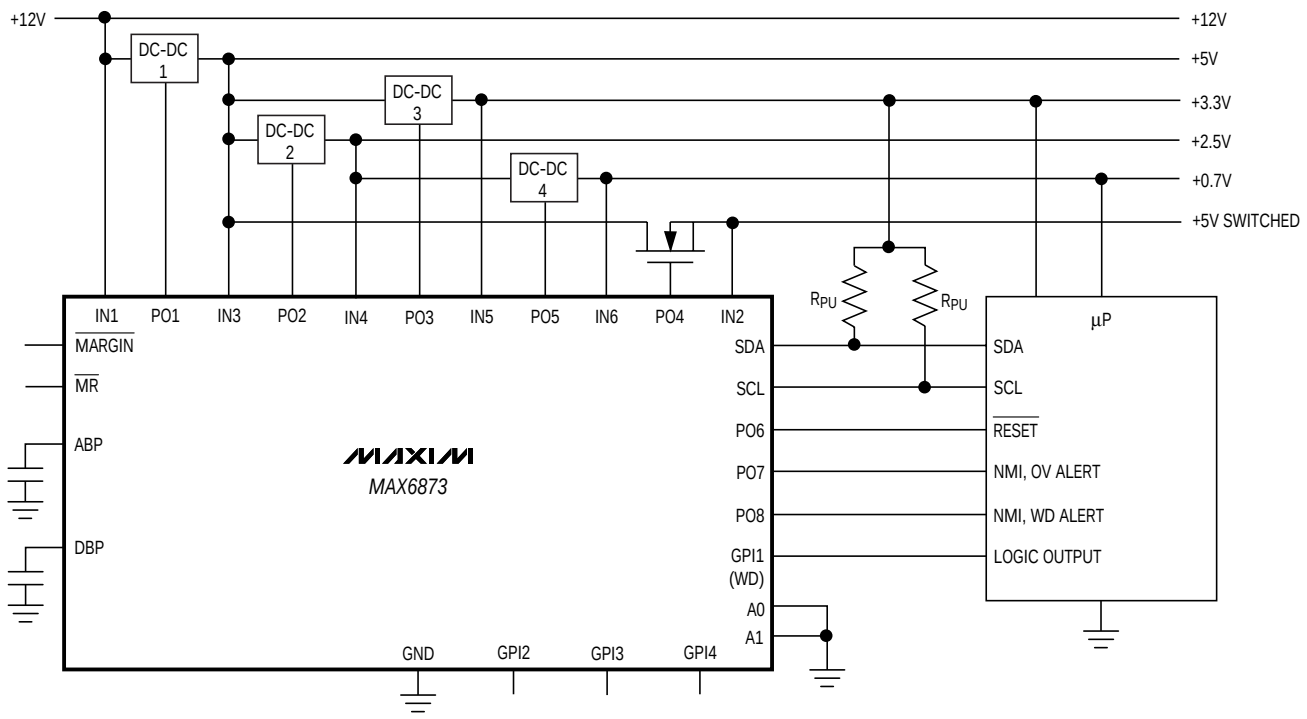
For better noise immunity, bypass each of the voltage detector inputs to GND with 0.1µF capacitors installed as close to the device as possible. Bypass ABP and DBP to GND with 1µF capacitors installed as close to the device as possible. ABP and DBP are internally generated voltages and should not be used to supply power to external circuitry.

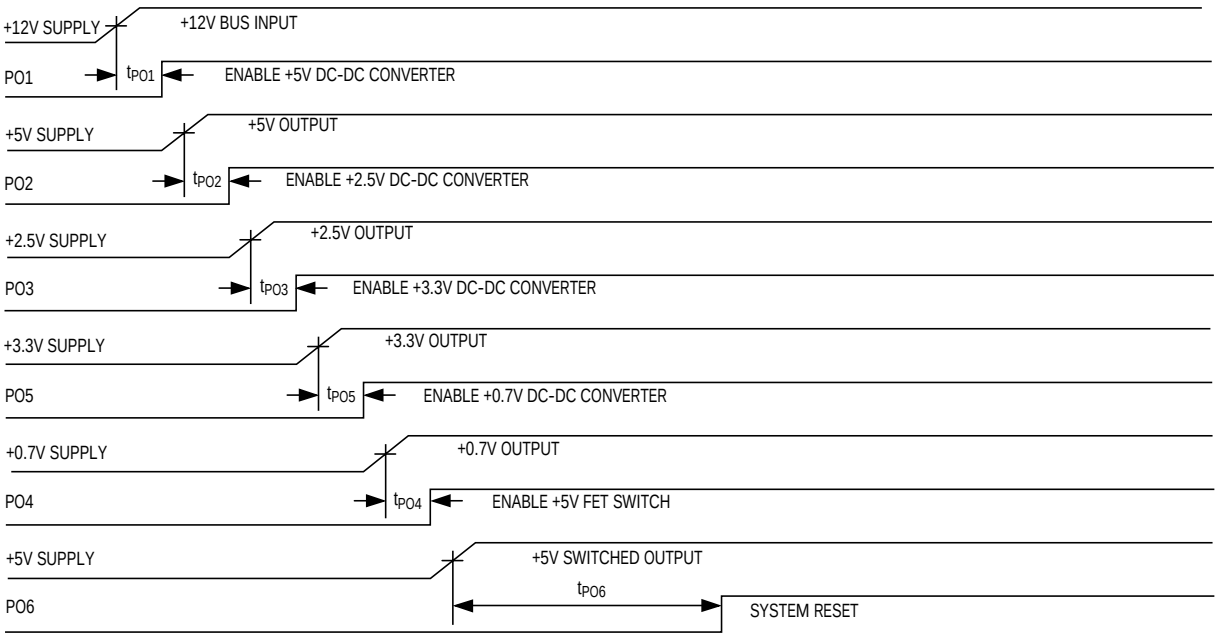
Configuration Latency Period

A delay of less than 5µs occurs between writing to the configuration registers and the time when these changes actually take place, except when changing one of the voltage-detector thresholds. Changing a voltage-detector threshold typically takes 150µs. When changing EEPROM contents, a software reboot or cycling of power is required for these changes to transfer to volatile memory.

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Typical Operating Circuit

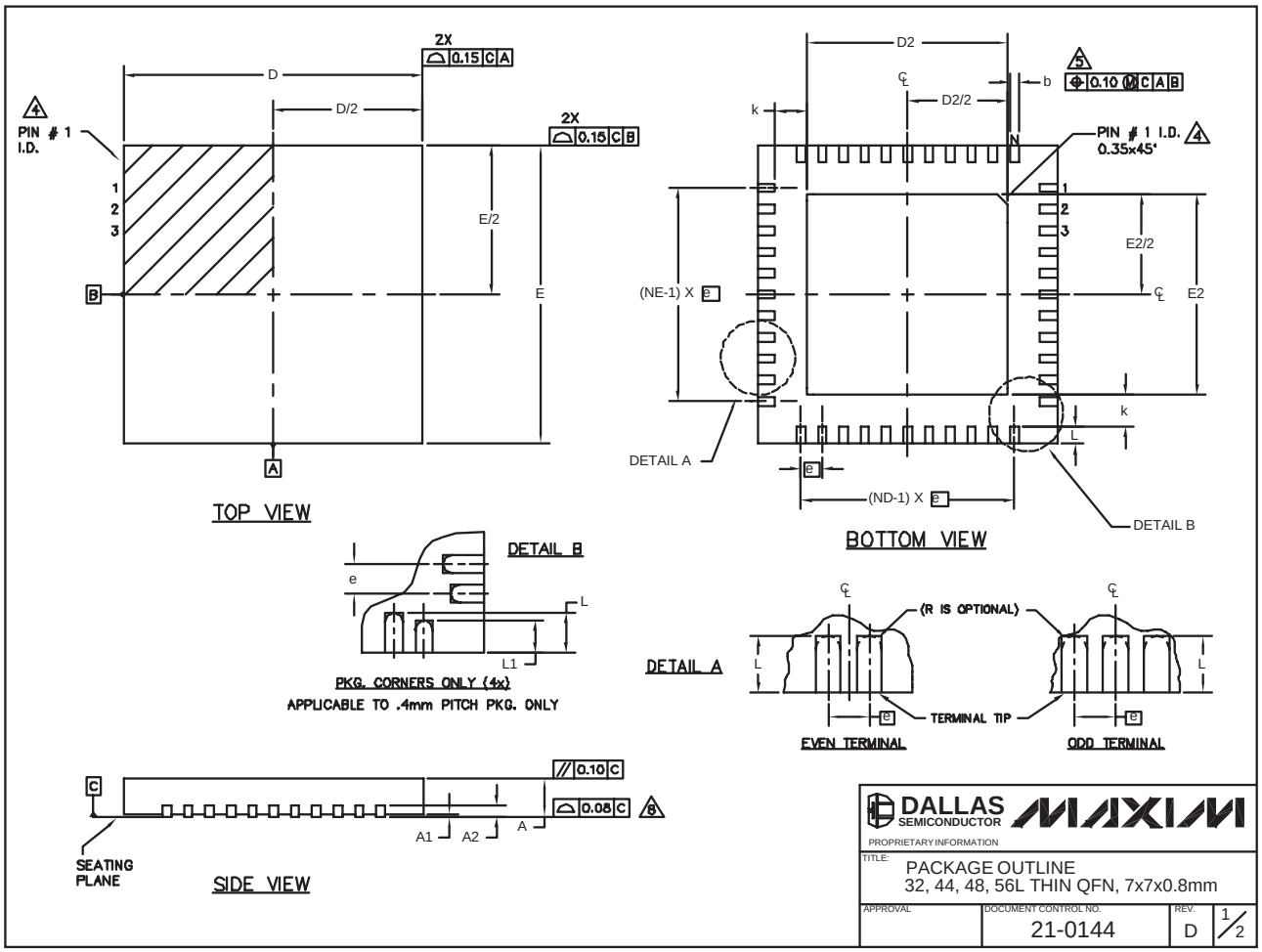




Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN.EPS



Chip Information

PROCESS: BiCMOS

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.40	0.50	0.60
L1	–	–	–	–	–	–	–	–	–	–	–	–	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS									
PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C	DOWN BONDS ALLOWED
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T3277-1	–	4.55	4.70	4.85	4.55	4.70	4.85	–	NO
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–	YES
T4477-1	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	NO
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–	NO
T4877-2	–	5.45	5.60	5.63	5.45	5.60	5.63	–	NO
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T4877-4	–	5.45	5.60	5.63	5.45	5.60	5.63	–	YES
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–	NO
T4877-6	–	5.45	5.60	5.63	5.45	5.60	5.63	–	NO
T5677-1	–	5.20	5.30	5.40	5.20	5.30	5.40	–	YES

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T3277-1; T4877-1/-2/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	D	2/2