HI-7153

NOT RECOMMENDED FOR NEW DESIGNS
See HI5810
or contact our Technicl Support Center at
1-888-INTERSIL or www.intersil.com/tsc

8-Channel, 10-Bit High Speed Sampling A/D Converter

December 1997

Features

- 5μs Conversion Time
- 8 Channel Input Multiplexer
- 200,000 Channels/Second Throughput Rate
- Over 9 Effective Bits at 20kHz
- No Offset or Gain Adjustments Necessary
- Analog and Reference Inputs Fully Buffered
- On-Chip Track and Hold Amplifier
- μP Compatible Interface
- 2's Complement Data Output
- 150mW Power Consumption
- Only a Single 2.5V Reference Required for a ±2.5V Input Range
- Out-of-Range Flag
- /883 Version Available

Applications

- μP Controlled Data Acquisition Systems
- DSP
  - Avionics
  - Sonar
- Process Control
  - Automotive Transducer Sensing
  - Industrial
- Robotics
- Digital Communications

Description

The HI-7153 is an 8 channel high speed 10 bit A/D converter which uses a Two Step Flash algorithm to achieve through-put rates of 200kHz. The converter features an 8 channel CMOS analog multiplexer with random channel addressing. A unique switched capacitor technique allows a new input voltage to be sampled while a conversion is taking place.

Internal high speed CMOS buffers at both the analog and reference inputs simplifies interface requirements.

A Track and Hold amplifier is included on the chip, consisting of two high speed amplifiers and an internal hold capacitor, reducing external circuitry.

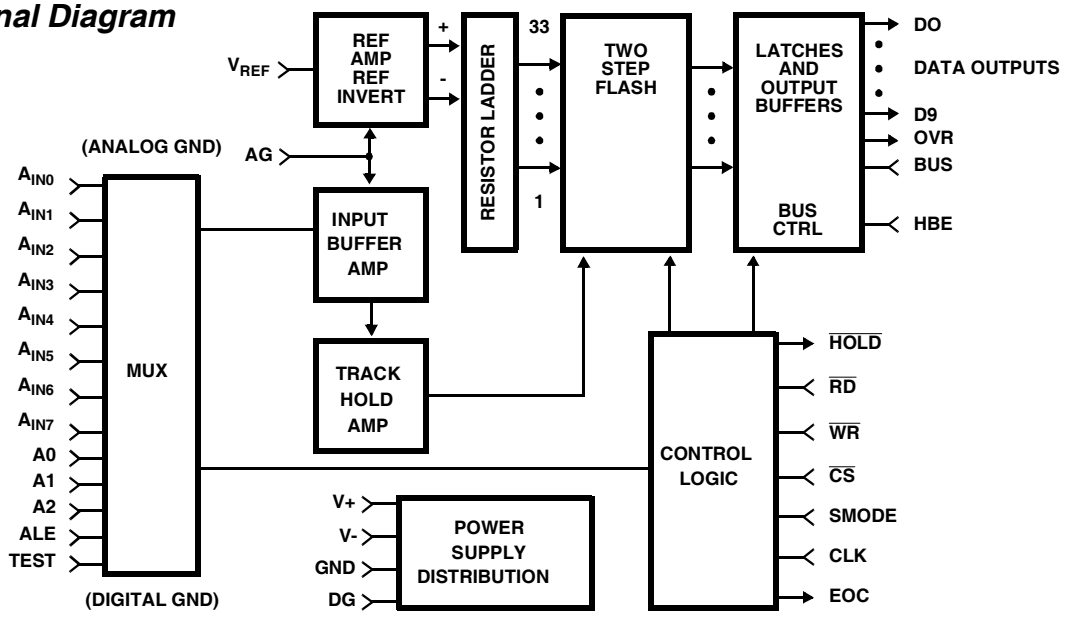
Microprocessor bus interfacing is simplified by the use of standard Chip Select, Read, and Write control signals. The digital three-state outputs are byte organized for bus interface to 8 or 16 bit systems. An Out-of-Range pin, together with the MSB bit, can be used to indicate an under or over-range condition.

The HI-7153 operates with ±5V supplies. Only a single +2.5V reference is required to provide a bipolar input range from -2.5V to +2.5V.

Ordering Information

PART NUMBER	LINEARITY (MAX ILE)	TEMPERATURE RANGE	PACKAGE
HI3-7153J-5	±1.0 LSB	0°C to +70°C	40 Lead Plastic DIP
HI3-7153A-9	±1.0 LSB	-40°C to +85°C	40 Lead Plastic DIP

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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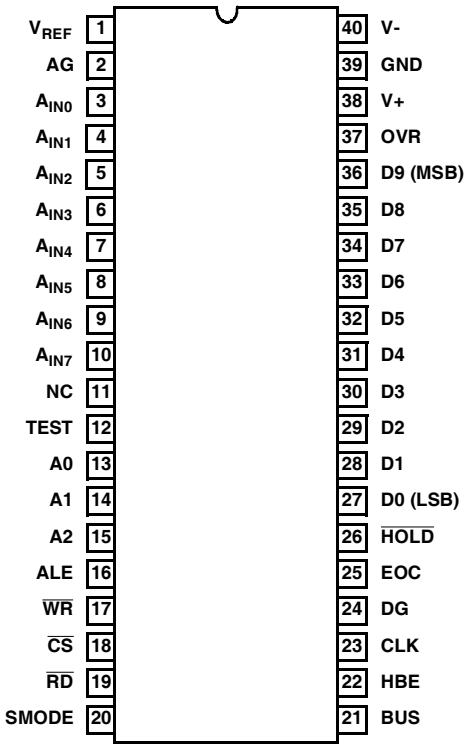
Pinouts

HI-7153
(CDIP, PDIP)
TOP VIEW



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Absolute Maximum Ratings

Supply Voltage
V+ to GND (DG/AG/GND) . . . . . -0.3V < V+ < +5.7V
V- to GND (DG/AG/GND) . . . . . -5.7V < V- < +0.3V
Analog InputPins (Note 1)
(A_{IN0} - A_{IN7}, V_{REF}) . . . . . V- -0.3V < V_{INA} < V+ +0.3V
Digital I/O Pins (Note 1) . . . . . DG -0.3V < $V_{I/O}$ < V+ +0.3V
(D0 - D9, OVR, CLK, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, ALE, SMODE, $\overline{HOLD}$, EOC, HBE, BUS, A0 - A2, TEST)
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s). . . . . +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic . . . . . 50°C/W
Operating Temperature Range
HI3-7153X-5 . . . . . 0°C to +70°C
HI3-7153X-9 . . . . . -40°C to +85°C
HI1-7153X-2 . . . . . -55°C to +125°C
Power Dissipation (Note 2) 500mW
Derate above +70°C at 10mW/°C

NOTES:

1. Input voltages may exceed the supply voltage, on input or channel at a time, provided the input current is limited to ±10mA
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq 25$ns, 50% Duty Cycle. All Typical Values have been Characterized but are Not Tested.

(NOTE 4) PARAMETER	SYMBOL	TEMPERATURE	(NOTE 3) J, A, S GRADE MIN	TYP	MAX	UNITS
ACCURACY						
Resolution (Note 5)	RES	T_A = +25°C	10	-	-	Bits
		$T_{MIN} \leq T_A \leq T_{MAX}$	10	-	-	Bits
Integral Linearity Error	ILE	T_A = +25°C	-	±0.5	±1.0	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.75	±1.0	LSB
Differential Linearity Error	DLE	T_A = +25°C	-	±0.5	±1.0	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.75	±1.0	LSB
Bipolar Offset Error	V_{OS}	T_A = +25°C	-	±1.0	±2.5	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±1.5	±3.0	LSB
Unadjusted Gain Error	FSE	T_A = +25°C	-	±1.0	±2.5	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±1.5	±3.0	LSB
Channel to Channel Mismatch		T_A = +25°C	-	±0.002	-	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.002	-	LSB

NOTES:

1. Input voltages may exceed the supply voltage, one input or channel at a time, provided the input current is limited to 10mA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. See Ordering Information Table.
4. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V).
5. Parameter Not tested. Parameter guaranteed by design, simulation, or characterization.
6. T_{MIN} and T_{MAX} limits guaranteed by +25°C test.

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Electrical Specifications

T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq$ 25ns, 50% Duty Cycle. All Typical Values have been Characterized but are Not Tested.

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C TYP	UNITS
DYNAMIC CHARACTERISTICS				
Signal to Noise Ratio	SNR	f_{IN} = 4.932kHz, ±2.5V	59	dB
		f_{IN} = 14.697kHz, ±2.5V	59	dB
		f_{IN} = 24.462kHz, ±2.5V	58	dB
		f_{IN} = 43.994kHz, ±2.5V	56	dB
Signal to Noise + Distortion	SINAD	f_{IN} = 4.932kHz, ±2.5V	59	dB
		f_{IN} = 14.697kHz, ±2.5V	58	dB
		f_{IN} = 24.462kHz, ±2.5V	55	dB
		f_{IN} = 43.994kHz, ±2.5V	48	dB
Total Harmonic Distortion	THD	f_{IN} = 4.932kHz, ±2.5V	-66	dBc
		f_{IN} = 14.697kHz, ±2.5V	-61	dBc
		f_{IN} = 24.462kHz, ±2.5V	-56	dBc
		f_{IN} = 43.994kHz, ±2.5V	-48	dBc
Spurious-Free Dynamic Range	SFDR	f_{IN} = 4.932kHz, ±2.5V	-76	dB
		f_{IN} = 14.697kHz, ±2.5V	-77	dB
		f_{IN} = 24.462kHz, ±2.5V	-77	dB
		f_{IN} = 43.994kHz, ±2.5V	-74	dB

NOTE:

1. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V)

DC Electrical Specifications

T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq$ 25ns, 50% Duty Cycle, Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested.

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
ANALOG MULTIPLEXER INPUT												
Input Range	VIR		$-V_{REF}$	-	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	V
Input Resistance	R_{IN}		-	10	-	-	-	-	-	-	-	MΩ
Input Leakage Current	IBI	A_{IN} = 0V	-	0.01	100	-	100	-	100	-	100	nA
On Channel Input Capacitance	$CA_{IN(ON)}$	A_{IN} = 0V, Note 2	-	10	30	-	30	-	30	-	30	pF
Off Channel Input Capacitance	$CA_{IN(OFF)}$	A_{IN} = 0V, Note 2	-	8	20	-	20	-	20	-	20	pF
MUX On-Resistance	$R_{DS(ON)}$	A_{IN} = ±2.5V, I_{IN} =100µA	-	1.1	2.5	-	2.5	-	2.5	-	2.5	KΩ
Greatest Change in $R_{DS(ON)}$ Between Any Two Channels	$\Delta R_{DS(ON)}$	-2.5V ≤ A_{IN} ≤ +2.5V	-	2.5	-	-	-	-	-	-	-	%

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DC Electrical Specifications T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, t_R = t_F ≤ 25ns, 50% Duty Cycle, Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested. **(Con-**

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Off-Channel Isolation	OIRR	F_{IN} =100kHz, Note 4	-	-96	-	-	-	-	-	-	-	dB
Channel to Channel Isolation	CCRR	F_{IN} =100kHz, Note 4	-	-83	-	-	-	-	-	-	-	dB
REFERENCE INPUT												
Reference Input Range	VRR	Note 3	2.2	-	2.6	2.2	2.6	2.2	2.6	2.2	2.6	V
Reference Input Bias Current	IBR	V_{REF} = +2.50V	-	0.01	100	-	100	-	100	-	100	nA
Reference Input Capacitance	CV_R	Note 2	-	8	20	-	-	-	-	-	-	pF
LOGIC INPUTS												
Input High Voltage	V_{IH}		2.4	-	-	2.4	-	2.4	-	2.4	-	V
Input Low Voltage	V_{IL}		-	-	0.8	-	0.8	-	0.8	-	0.8	V
Logic Input Current	I_{IL}	V_{IN} = 0V, +5V	-	0.05	1	-	1	-	1	-	1	µA
Input Capacitance	C_{IN}	Note 2	-	7	17	-	-	-	-	-	-	pF
LOGIC OUTPUTS												
Output High Voltage	V_{OH}	I_{OH} = -200µA	2.4	-	-	2.4	-	2.4	-	2.4	-	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6mA	-	-	0.4	-	0.4	-	0.4	-	0.4	V
Output Leakage Current	I_{OL}	$\overline{RD}$ = +5V, V_{OUT} = +5V	-	0.04	1	-	10	-	10	-	10	µA
		$\overline{RD}$ = +5V, V_{OUT} = 0V	-1	-0.01	-	-10	-	-10	-	-10	-	µA
Output Capacitance	C_{OUT}	High-Z State, Note 2	-	7	15	-	-	-	-	-	-	pF
POWER SUPPLY VOLTAGE RANGE												
	V+	Functional Operation Only, Note 3	4.5	5.0	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
	V-		-4.5	-5.0	-5.5	-4.5	-5.5	-4.5	-5.5	-4.5	-5.5	V
POWER SUPPLY REJECTION												
V+, V- Gain Error	ΔFSE	V+ = 5V, V- = -4.75V, -5.25V	-	0.1	0.5	-	0.6	-	0.6	-	0.8	LSB
		V- = -5V, V+ = 4.75V, 5.25V	-	0.1	0.5	-	0.6	-	0.6	-	0.8	LSB
V+, V- Offset Error	ΔVOS	V+ = 5V, V- = -4.75V, -5.25V	-	0.15	0.5	-	0.6	-	0.6	-	0.8	LSB
		V- = -5V, V+ = 4.75V, 5.25V	-	0.15	0.5	-	0.6	-	0.6	-	0.8	LSB

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DC Electrical Specifications T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, t_R = t_F ≤ 25ns, 50% Duty Cycle, Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested. **(Con-**

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
SUPPLY CURRENTS												
V+ Supply Current	I+	V+ = 5V, V- = -5V, V_{IN} = 0V, Digital Outputs Are Unloaded	-	20	30	-	30	-	30	-	30	mA
V- Supply Current	I-		-	-10	-15	-	-15	-	-15	-	-15	mA
GND Current	IGND		-	-8	-	-	-	-	-	-	-	mA
DG Current	IDG		-	-2	-	-	-	-	-	-	-	mA
AG Current	IAG		-	0.02	-	-	-	-	-	-	-	µA

NOTES:

1. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V)
2. Parameter Not tested. Parameter guaranteed by design, simulation, or characterization
3. Functionality is guaranteed by negative GAIN ERROR test.
4. Channel Isolation is tested with an input signal of ±2.5Vp-p, 100kHz and the measured pin is loaded with 100Ω to GND

DC Electrical Specifications T_A = +25°C, V+ = 5V ±10%, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz, t_R = t_F ≤ 25ns, 50% Duty Cycle, C_L = 100pF (Including Stray for D0-D9, OVR, $\overline{HOLD}$), Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested.

(NOTE 4) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
TIMING CHARACTERISTICS												
Continuous Conversion Time	t_{SPS}	Note 2	-	-	5	-	5	-	5	-	5	µs
		Note 9	60	-	-	60	-	60	-	60	-	µs
		Notes 2, 8	-	-	$3t_{CLK}$	-	$3t_{CLK}$	-	$3t_{CLK}$	-	$3t_{CLK}$	µs
Conversion Time, First Conversion	t_{CONV}	Notes 1, 9	-	-	$4t_{CLK}$ + 0.63	-	$4t_{CLK}$ + 0.75	-	$4t_{CLK}$ + 0.75	-	$4t_{CLK}$ + 0.8	µs
Continuous Throughput	t_{CYC}	Note 2	-	-	$t_{CLK}/3$	-	$t_{CLK}/3$	-	$t_{CLK}/3$	-	$t_{CLK}/3$	CPS
Clock Period	t_{CLK}		-	$1/f_{CLK}$	-	-	-	-	-	-	-	-
Clock Input Duty Cycle	D	Note 9	45	50	55	45	55	45	55	45	55	%
ALE Pulse Width	t_{ALEW}	Note 9	30	15	-	40	-	40	-	50	-	ns
Address Setup Time	t_{AS}	Note 9	40	15	-	80	-	80	-	80	-	ns
Address Hold Time	t_{AH}		0	-16	-	0	-	0	-	0	-	ns
$\overline{WR}$ Pulse Width	t_{WRL}	Notes 1, 3, 9	100	20	$t_{CLK}/2$	100	$t_{CLK}/2$	100	$t_{CLK}/2$	100	$t_{CLK}/2$	ns
$\overline{WR}$ to EOC Low	t_{WREOC}	Notes 1, 9	-	80	130	-	160	-	160	-	160	ns
$\overline{WR}$ to $\overline{HOLD}$ Delay	t_{HOLD}	Notes 1, 9	-	80	150	-	170	-	170	-	170	ns
Clock to $\overline{HOLD}$ Rise Delay	t_{CKHR}	Note 9	150	265	450	140	500	120	500	120	500	ns
Clock to $\overline{HOLD}$ Fall Delay	t_{CKHF}	Notes 2, 9	50	95	200	40	225	40	225	40	225	ns

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DC Electrical Specifications

T_A = +25°C, V+ = 5V ±10%, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq$ 25ns, 50% Duty Cycle, C_L = 100pF (Including Stray for D0-D9, OVR, $\overline{HOLD}$), Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested. **(Continued)**

(NOTE 4) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Clock to EOC High	t_{CKEOC}	Notes 1, 9	-	460	630	-	750	-	750	-	800	ns
$\overline{HOLD}$ to DATA Change	t_{DATA}	Notes 2, 9	100	200	350	90	400	90	400	90	400	ns
$\overline{CS}$ to DATA	t_{CD}	Note 9	-	40	70	-	85	-	85	-	85	ns
HBE to DATA	t_{AD}	Note 9	-	30	50	-	70	-	70	-	70	ns
$\overline{RD}$ LOW to Active	t_{RD}	Notes 6, 9	-	70	100	-	125	-	125	-	125	ns
$\overline{RD}$ HIGH to Inactive	t_{RX}	Notes 7, 9	-	30	60	-	70	-	70	-	70	ns
Output Rise Time	t_R	Notes 5, 9	-	20	40	-	60	-	60	-	60	ns
Output Fall Time	t_F	Notes 5, 9	-	15	30	-	50	-	50	-	50	ns

NOTES:

1. Slow memory mode timing
2. Fast memory or DMA mode of operation, except the first conversion which is equal to t_{CONV}
3. Maximum specification to prevent multiple triggering with $\overline{WR}$
4. All input drive signals are specified with $t_R = t_F \leq$ 10ns and shall swing from 0.4V to 2.4V for all timing specifications. A signal is considered to change state as it crosses a 1.4V threshold (except t_{RD} and t_{RX})
5. t_R and t_F load is C_L = 100pF (including stray capacitance) to DG and is measured from the 10% - 90% point
6. t_{RD} is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. High-Z to V_{OH} is measured with R_L = 2.5KΩ and C_L = 100pF (including stray) to DG. High-Z to V_{OL} is measured with R_L = 2.5KΩ to V+ and C_L = 100pF (including stray) to DG
7. t_{RX} is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. V_{OH} to High-Z is measured with R_L = 2.5KΩ and C_L = 10pF (including stray) to DG. V_{OL} to High-Z is measured with R_L = 2.5KΩ to V+ and C_L = 10pF (including stray) to DG
8. For clock frequencies other than 600kHz
9. Parameter Not Tested. Parameter guaranteed by design, simulation, or characterization

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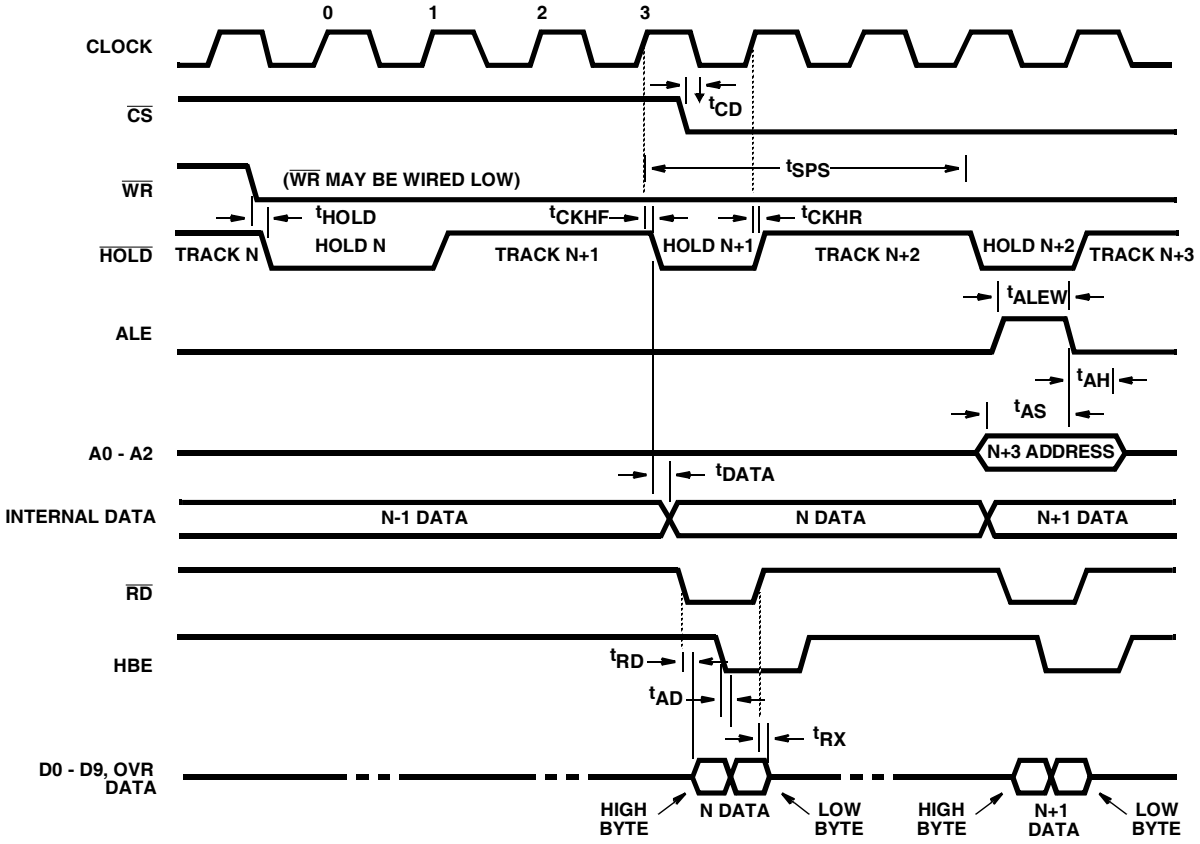
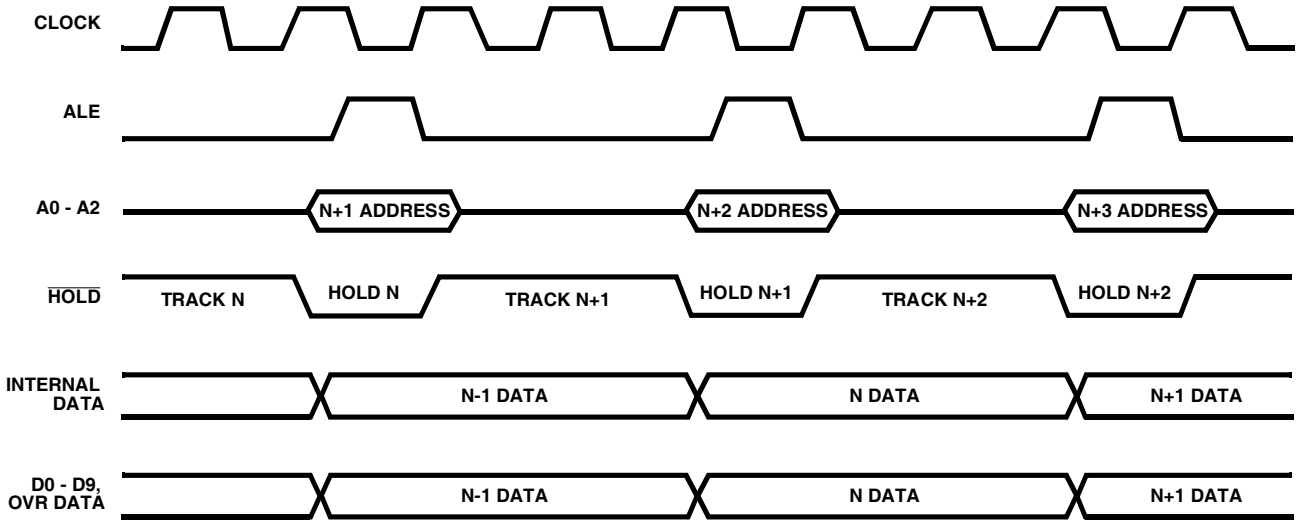
Timing Diagrams

FAST MEMORY MODE (8 BIT DATA BUS)



CONDITIONS: SMODE = DG. Bus = DG
NOTE: With SMODE = DG, the internal logic diables the output latches from being updated during a read. The EOC output is LOW continuously.

DMA MODE (16 BIT DATA BUS)



CONDITIONS: SMODE = V+, CS = WR = RD = DG, Bus = V+, HBE = DG or V+
NOTE: EOC output is low continuously

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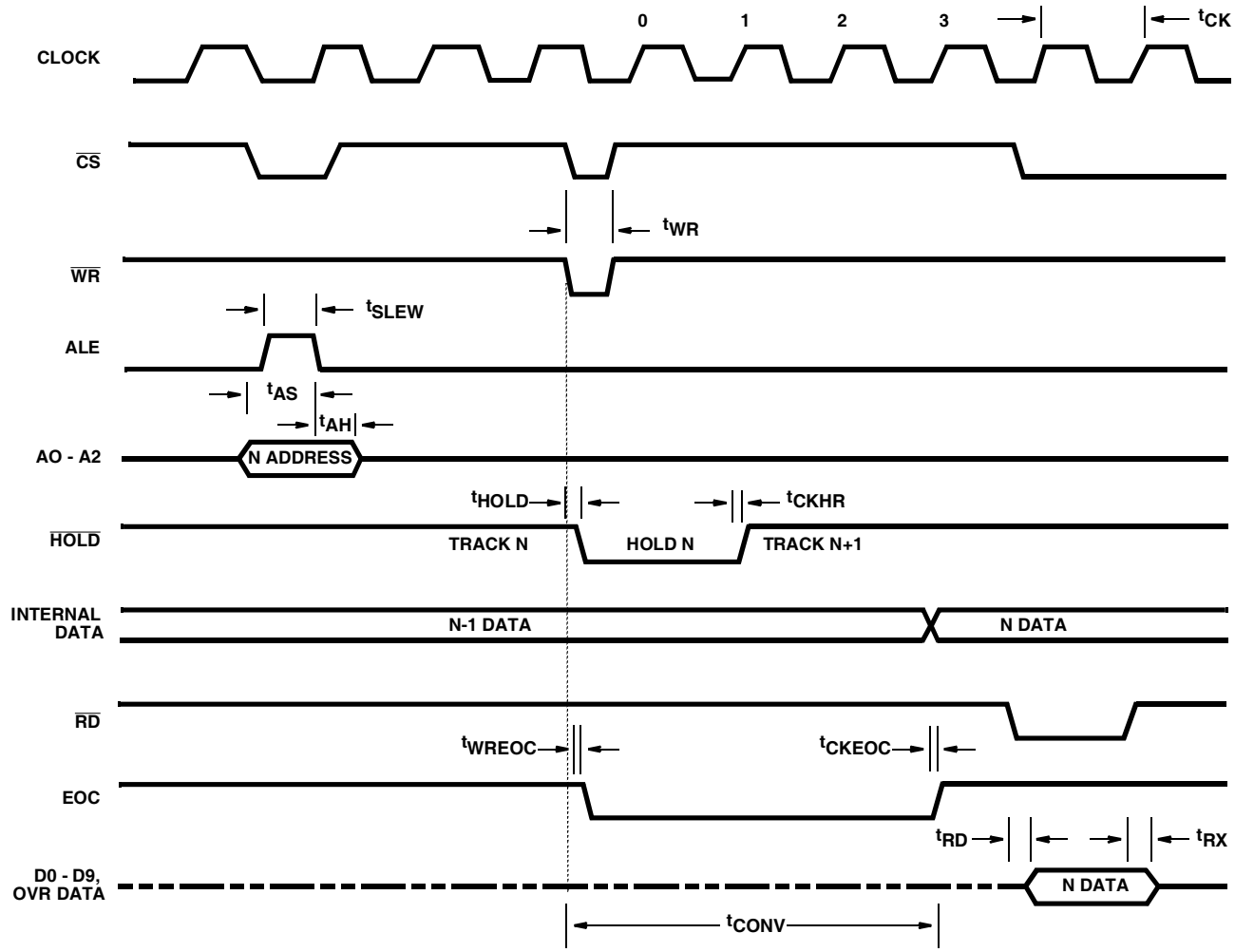
Timing Diagrams (Continued)

SLOW MEMORY MODE (16 BIT DATA BUS)



CONDITIONS: SMODE = V+, Bus = V+, HBE = DG or V+

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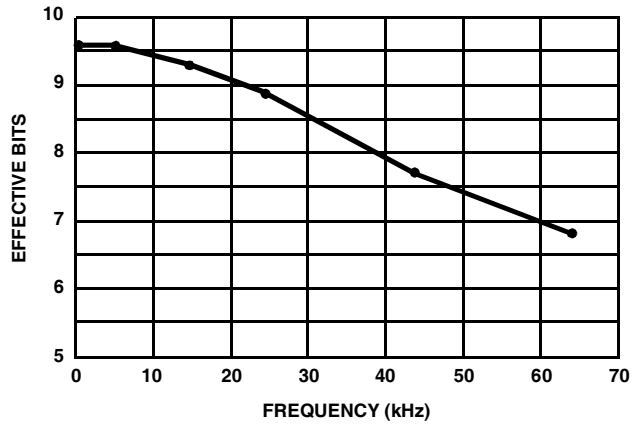
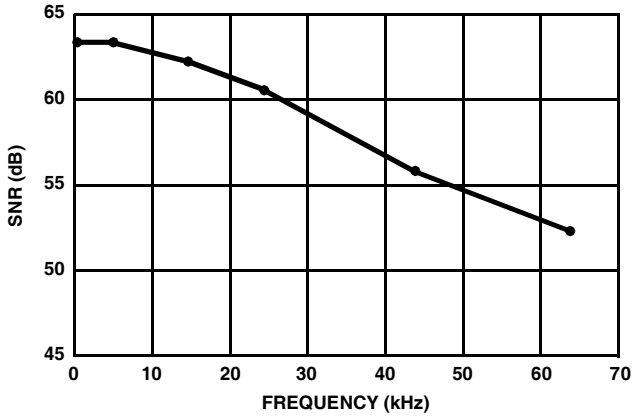
Typical Dynamic Performance Characteristics

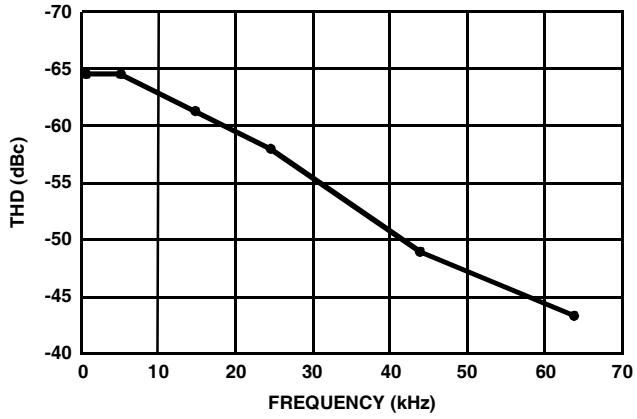
EFFECTIVE NUMBER OF BITS



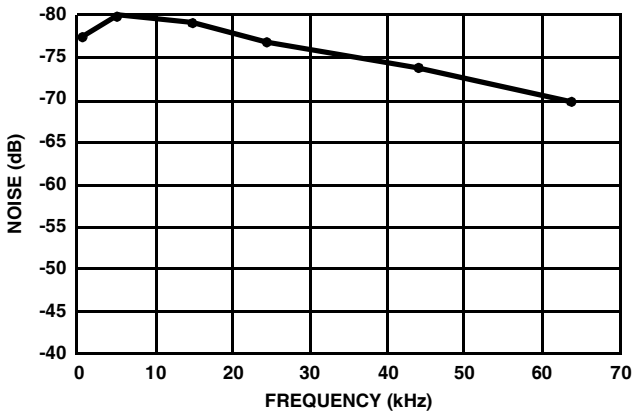
SIGNAL-TO-NOISE RATIO



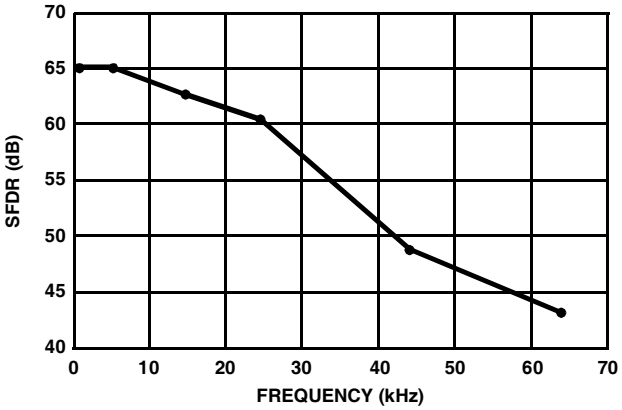
TOTAL HARMONIC DISTORTION



PEAK NOISE



SPURIOUS-FREE DYNAMIC RANGE



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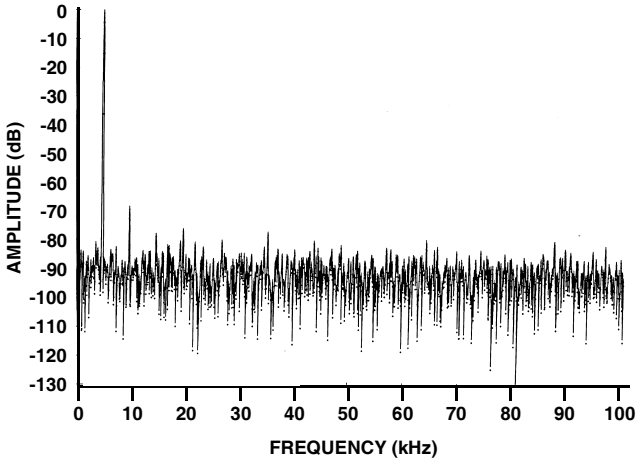
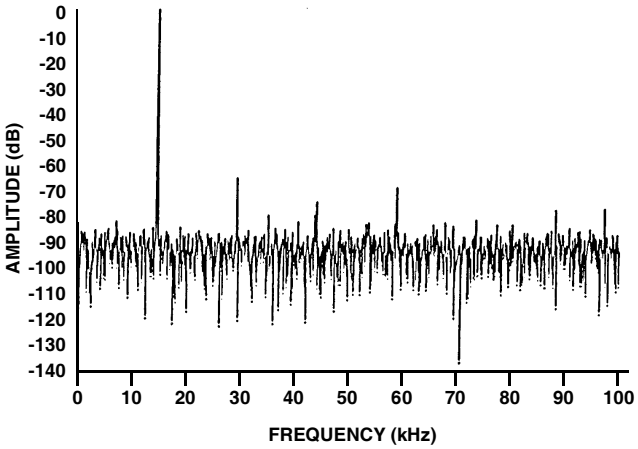
Typical Dynamic Performance Characteristics (Continued)

FFT SPECTRUMS



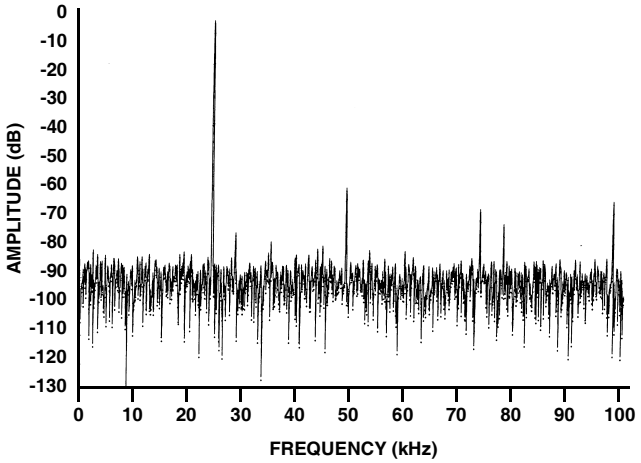
NOTES:

INPUT FREQUENCY: 4931Hz
SAMPLING RATE: 200kHz
SNR: 59.40dB
THD: -67.26dB
PEAK NOISE: -75.98dB
SPURIOUS FREE DYNAMIC RANGE: -68.36dB
3RD HARMONIC: -77.19dB



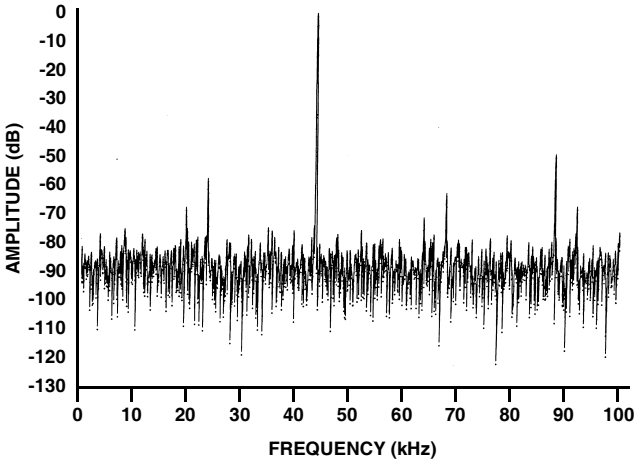
NOTES:

INPUT FREQUENCY: 14697Hz
SAMPLING RATE: 200kHz
SNR: 58.98dB
THD: -61.44dB
PEAK NOISE: -77.29dB
SPURIOUS FREE DYNAMIC RANGE: -63.42dB
3RD HARMONIC: -72.44dB



NOTES:

INPUT FREQUENCY: 24462Hz
SAMPLING RATE: 200kHz
SNR: 58.36dB
THD: -55.59dB
PEAK NOISE: -76.65dB
SPURIOUS FREE DYNAMIC RANGE: -57.72dB
3RD HARMONIC: -64.53dB



NOTES:

INPUT FREQUENCY: 4399Hz
SAMPLING RATE: 200kHz
SNR: 56.26dB
THD: -48.19dB
PEAK NOISE: -74.34dB
SPURIOUS FREE DYNAMIC RANGE: -48.66dB
3RD HARMONIC: -62.87dB

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Pin Description

DIP PIN	SYMBOL	DESCRIPTION
1	V_{REF}	Reference voltage input (+2.50V)
2	AG	Analog ground reference (0V)
3	A_{IN0}	Analog input channel 0
4	A_{IN1}	Analog input channel 1
5	A_{IN2}	Analog input channel 2
6	A_{IN3}	Analog input channel 3
7	A_{IN4}	Analog input channel 4
8	A_{IN5}	Analog input channel 5
9	A_{IN6}	Analog input channel 6
10	A_{IN7}	Analog input channel 7
11	NC	No connect or tie to V+ only
12	TEST	Test pin. Connect to DG for normal operation
13	A0	Mux address input. (LSB) Active high.
14	A1	Mux address input. (LSB) Active high.
15	A2	Mux address input. (MSB) Active high.
16	ALE	Mux address enable. When high, the latch is transparent. Address data is latched on the falling edge.
17	$\overline{WR}$	Write input. With $\overline{CS}$ low, starts conversion when pulsed low; continuous conversions when kept low.
18	$\overline{CS}$	Chip select input. Active low.
19	$\overline{RD}$	Read input. With $\overline{CS}$ low, enables output buffers when pulsed low; outputs updated at the end of conversion.
20	SMODE	Slow memory mode input. Active high.

DIP PIN	SYMBOL	DESCRIPTION
21	BUS	Bus select input. High = all outputs enabled together D0-D9, OVR Low = Outputs enabled by HBE
22	HBE	Byte select (HBE/LBE) input for 8 bit bus. High = High byte select, D8 - D9, OVR Low = Low byte select, D0 - D7
23	CLK	Clock input. TTL compatible.
24	DG	Digital ground (0V)
25	EOC	End-of-conversion status. Pulses high at the end-of-conversion.
26	$\overline{HOLD}$	Start of conversion status. Pulses low at the start-of-conversion.
27	D0	Bit 0 (LSB)
28	D1	Bit 1
29	D2	Bit 2 Output
30	D3	Bit 3 Data
31	D4	Bit 4 Bits
32	D5	Bit 5
33	D6	Bit 6
34	D7	Bit 7
35	D8	Bit 8
36	D9	Bit 9 (MSB)
37	OVR	Out of Range flag. Valid at end of conversion when output exceeds full scale.
38	V+	Positive supply voltage input (+5.0V)
39	GND	Ground return for comparators (0V)
40	V-	Negative supply voltage input (-5.0V)

Detailed Description

The HI-7153 is an 8 channel high speed 10 bit A/D converter which achieves throughput rates of 200kHz by use of a Two Step Flash algorithm. A pipelined operation has been achieved through the use of switched capacitor techniques which allows the device to sample a new input voltage while a conversion is taking place. The 8 channel multiplexer can be randomly addressed. The HI-7153 requires a single reference input of +2.5V, which is internally inverted to -2.5V, thereby allowing an input range of -2.5V to +2.5V. The ten bits are two's complement coded. The analog and reference inputs are internally buffered by high speed CMOS buffers, which greatly simplifies the external analog drive requirements for the device.

Analog to Digital

Section The HI-7153 uses a conversion technique which is generally called a ''Two Step Flash'' algorithm. This algorithm enables very fast conversion rates without the penalty of high power dissipation or high cost. A detailed functional diagram is presented in Figure 1.

The reference input to the HI-7153 is buffered by a high speed CMOS amplifier which is used to drive one end of the resistor string. Another high speed amplifier configured in the inverting unity gain mode inverts the reference voltage with respect to analog ground and forces it onto the other end of the resistor string. Both reference amplifiers are offset trimmed during manufacturing in order to increase the accuracy of the HI-7153 and to simplify its usage.

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The input voltage is first converted into a 5 bit result (plus Out of Range information) by the flash converter. This flash converter consists of an array of 33 auto-zeroed comparators which perform a comparison between the input voltage and subdivisions of the reference voltage. These subdivisions of the reference voltage are formed by forcing the reference voltage and its negative on the two ends of a string of 32 resistors.

The 5 bit result of the first flash conversion is latched into the upper five bits of double buffered latches. It is also converted back into an analog signal by choosing the ladder voltage which is closest to but less than the input voltage. The selected voltage (VTAP) is then subtracted from the input voltage. The residual is then amplified by a factor of 32 and referenced to the negative reference voltage (VSCA = 32(VIN - VTAP) + V_{REF-}). This subtraction and amplification operation is performed by a Switched Capacitor amplifier (SCA). The output of the SCA amplifier is between the positive and negative reference voltages and can therefore be digitized by the original 5 bit flash converter (second flash conversion).

The 5 bit result of the second flash conversion is latched into the lower five bits of double buffered latches. At the end of a conversion, 10 bits of data plus an Out of Range bit are latched into the second level of latches and can then be put on the digital output pins.

The conversion takes place in three clock cycles and is illustrated in Figure 2. When the conversion begins, the track and hold goes into its hold mode for 1 clock cycle. During the first half clock cycle the comparator array is in its auto-zero mode and it samples the input voltage. During the second half clock cycle, the comparators make a comparison between the input voltage and the ladder voltages. At the beginning of the third half clock cycle, the first most significant 5 bit result becomes available. During the first clock cycle, the SCA was sampling the input voltage. After the first flash result becomes available and a ladder tap voltage has been selected the SCA amplifies the residue between the input and ladder tap voltages. During the next three half clock cycles, while the SCA output is settling to its required accuracy, the comparators go into their auto-zero mode and sample this voltage. During the sixth half clock cycle, the comparators perform another comparison whose 5 bit result becomes available on the next clock edge.

Reference Input

The reference input to the HI-7153 is buffered by a high speed CMOS amplifier. The reference input range is 2.2V to 2.6V. The reference input voltage should be applied following the application of V+ and V- supplies.

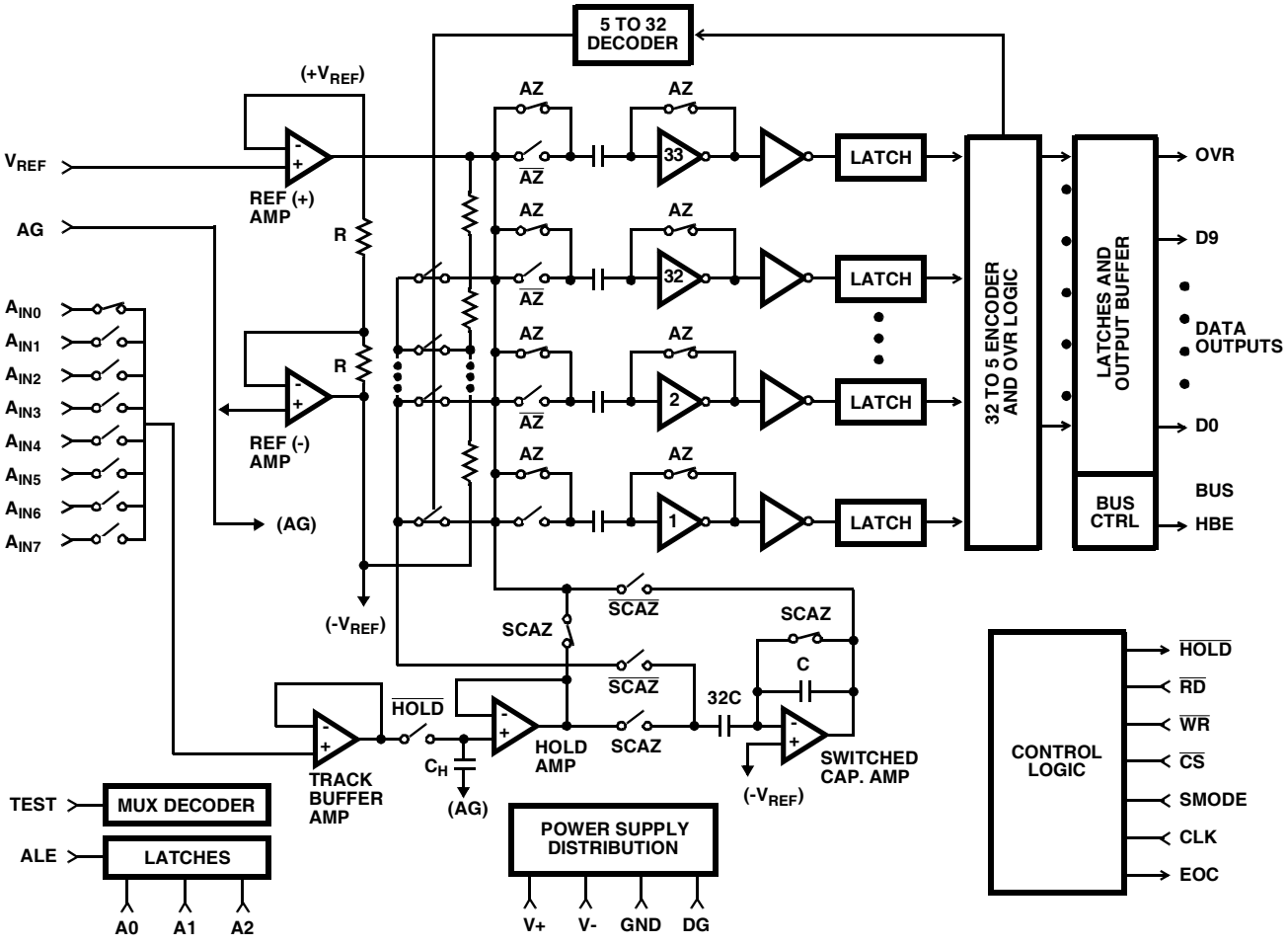

FIGURE 1. DETAILED BLOCK DIAGRAM

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Analog Multiplexer

The multiplexer channel assignments are shown in Table 1 and can be randomly addressed. Address inputs A0 - A2 are binary coded and are TTL/CMOS compatible. During power up the circuit is initialized and multiplexer channel A_{IN0} is selected. The multiplexer address is transparent when ALE is high and $\overline{CS}$ is low. The address data is latched on the falling edge of the ALE signal. The multiplexer channel acquisition timing (Timing Diagrams, Slow Memory Mode) occurs approximately 500ns after the rising edge of $\overline{HOLD}$. The multiplexer features a typical break-before-make switch action of 44ns.

Track And Hold

A Track and Hold amplifier has been fully integrated on the front end of the A/D converter. Because of the sampling nature of this A/D converter, the input is required to stay constant only during the first clock cycle. Therefore, the Track and Hold (T/H) amplifier "holds" the input voltage only during the first clock cycle and it acquires the input voltage for the next conversion during the remaining two clock cycles. The high input impedance of the T/H input amplifier simplifies analog interfacing. Input signals up to $\pm V_{REF}$ can be directly connected to the A/D without buffering. The T/H amplifier typically settles to within $^1/_4$ LSB in 1.5µs. The A/D output code table is presented in Table 2.

The timing signals for the Track and Hold amplifier are generated internally, and are also provided externally ($\overline{HOLD}$) for synchronization purposes.

All of the internal amplifiers are offset trimmed during manufacturing to give improved accuracy and to minimize the number of external components. If necessary, offset error can be adjusted by using digital post correction.

TABLE 1. MULTIPLEXER CHANNEL SELECTION

ADDRESS AND CONTROL INPUTS					ANALOG CHANNEL SELECTED
A2	A1	A0	$\overline{CS}$	ALE	
0	0	0	0	1	A_{IN0}
0	0	1	0	1	A_{IN1}
0	1	0	0	1	A_{IN2}
0	1	1	0	1	A_{IN3}
1	0	0	0	1	A_{IN4}
1	0	1	0	1	A_{IN5}
1	1	0	0	1	A_{IN6}
1	1	1	0	1	A_{IN7}

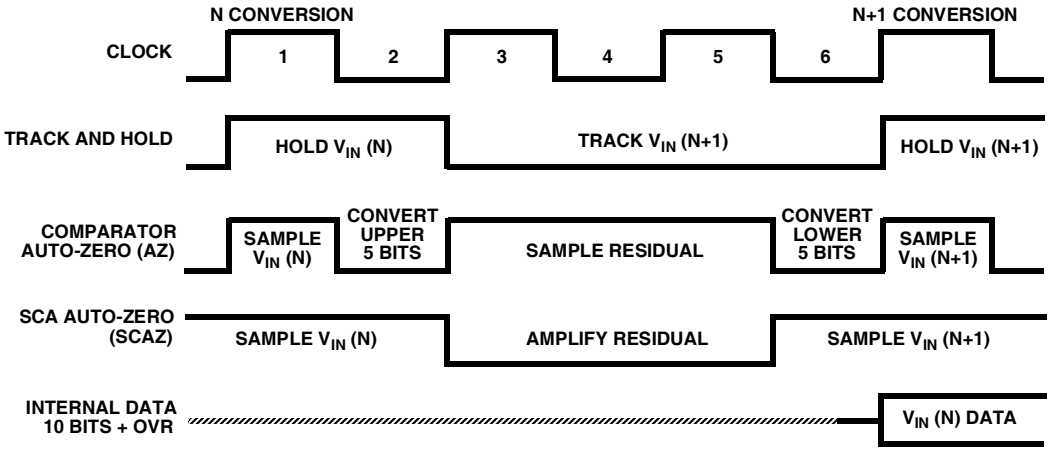

FIGURE 2. INTERNAL ADC TIMING DIAGRAM

TABLE 2. A/D OUTPUT CODE TABLE

ANALOG INPUT*		OUTPUT DATA (2'S COMPLEMENT)										
LSB = $2(V_{REF})/1024$	V_{REF} = 2.500V	OVR	MSB 9	8	7	6	5	4	3	2	1	LSB 0
$\geq +V_{REF}$	2.500 to V+ (+OVR)	1	0	0	0	0	0	0	0	0	0	0
$+V_{REF}$ - 1LSB	2.49512 (+Full Scale)	0	0	1	1	1	1	1	1	1	1	1
+1LSB	0.00488	0	0	0	0	0	0	0	0	0	0	1
0	0.000	0	0	0	0	0	0	0	0	0	0	0
-1LSB	-0.00488	0	1	1	1	1	1	1	1	1	1	1
$-V_{REF}$	-2.500 (-Full Scale)	0	1	0	0	0	0	0	0	0	0	0
$\leq -V_{REF}$ - 1LSB	2.50488 to V- (-OVR)	1	1	0	0	0	0	0	0	0	0	0

* The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

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Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance for one channel of the A/D system. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured rms signal to rms sum of noise at a specified input and sampling frequency. The noise is the rms sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76)dB. For an ideal 10 bit converter the SNR is 62dB. Differential and integral linearity errors will degrade SNR.

$$SNR = 10\log\frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured rms signal to rms sum of noise plus harmonic power and is expressed by the following.

$$SINAD = 10\log\frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd thru 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data;

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

$$THD = 10\log\frac{\text{Total Harmonic Power (2nd - 6th harmonics)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. It is usually determined by the largest harmonic. However, if the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10\log\frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

Clock

The clock input is TTL compatible. The converter will function with clock inputs between 10kHz and 800kHz.

Microprocessor Interface

The HI-7153 can be interfaced to microprocessors through the use of standard Write, Read, Chip Select, and HBE control pins. The digital outputs are two's complement coded, three-state gated, and byte organized for bus interface with 8 and 16 bit systems. The digital outputs (D0 - D9, OVR) may be accessed under control of BUS, byte enable input HBE, chip select, and read inputs for a simple parallel bus interface. The microprocessor can read the current data in the output latches in typically 60ns/byte (t_{RD}). An over-range pin (OVR) together with the MSB (D9) pin set to either a logic 0 or 1 will indicate a positive or negative over-range condition respectively. All digital output buffers are capable of driving one TTL load. The multiplexer can be interfaced to either multiplexed or separate address and data bus systems.

The HI-7153 can be interfaced to a microprocessor using one of three modes: slow memory, fast memory, or DMA mode.

Slow Memory Mode

In slow memory mode, the conversion will be initiated by the microprocessor by selecting the chip ($\overline{CS}$) and pulsing $\overline{WR}$ low. This mode is selected by hardwiring the SMODE pin to V+. Note that the converter will change to the DMA interface mode if the $\overline{WR}$ to $\overline{RD}$ active timing is less than 100ns. The end-of-conversion (EOC) output signals an interrupt for the microprocessor to jump to a read subroutine at the end of conversion. When the 8 bit bus operation is selected, high and low byte data may be accessed in either order. An I/O truth table is presented in Table 3 for the slow memory mode of operation.

Fast Memory Mode

The fast memory mode of operation is selected by tying the SMODE and $\overline{WR}$ pins to DG. In this mode, the chip performs continuous conversions and only $\overline{CS}$ and $\overline{RD}$ are required to read the data. Whenever the SMODE pin is low, $\overline{WR}$ is independent of $\overline{CS}$ in starting a conversion cycle. During the first conversion cycle, $\overline{HOLD}$ follows $\overline{WR}$ going low. $\overline{HOLD}$ will be one clock period wide for subsequent conversion cycles.

Data can be read a byte at a time or all 11 bits at once. When the 8 bit bus operation is selected, high and low byte data may be accessed in either order. EOC is continuously low in this mode of operation. The conversion data can be read after $\overline{HOLD}$ has gone low. An I/O truth table is presented in Table 4 for the fast memory mode of operation.

DMA Mode

This is a hardwired mode where the HI-7153 continuously converts. The user implements hardware to store the results in memory, bypassing the microprocessor. This mode is recognized by the chip when SMODE is connected to V+ and $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ are connected to DG. When 8 bit bus operation is selected, high and low byte data may be accessed in either order. EOC is continuously low in this mode. The conversion data can be read approximately 300ns after $\overline{HOLD}$ has gone low. An I/O truth table is

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TABLE 3. SLOW MEMORY MODE I/O TRUTH TABLE (SMODE = V+)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	ALE	FUNCTION
0	0	X	X	X	X	Initiates a conversion.
0	X	X	X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	X	X	X	Disables all chip commands.
0	X	0	1	X	X	Enables D0 - D9 and OVR.
0	X	0	0	0	X	Low byte enable: D0 - D7
0	X	0	0	1	X	High byte enable: D8 - D9, OVR
X	X	1	X	X	X	Disables all outputs (high impedance).

X = Don't Care

TABLE 4. FAST MEMORY MODE I/O TRUTH TABLE (SMODE = DG)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	ALE	FUNCTION
0	0	X	X	X	X	Continuous conversion, $\overline{WR}$ may be tied to DG.
0	X	X	X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	X	X	X	Disables all chip commands.
0	X	0	1	X	X	Enables D0 - D9 and OVR.
0	X	0	0	0	X	Low byte enable: D0 - D7
0	X	0	0	1	X	High byte enable: D8 - D9, OVR
X	X	1	X	X	X	Disables all outputs (high impedance).

X = Don't Care

TABLE 5. DMA MODE I/O TRUTH TABLE (SMODE = V+, $\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = DG)

BUS	HBE	ALE	FUNCTION
X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	Enables D0 - D9 and OVR.
0	0	X	Low byte enable: D0 - D7
0	1	X	High byte enable: D8 - D9, OVR

X = Don't Care

presented in Table 5 for the DMA mode of operation.

Optimizing System Performance

The HI-7153 has three ground pins (AG, DG, GND) for improved system accuracy. Proper grounding and bypassing is illustrated in Figure 3. The AG pin is a ground pin and is used internally as a reference ground. The reference input and analog input should be referenced to the analog ground (AG) pin. The digital inputs and outputs should be referenced to the digital ground (DG) pin. The GND pin is a return point for the supply current of the comparator array. The comparator array is designed such that this current is approximately constant at all times and does not vary with input voltage. By virtue of the switched capacitor nature of the comparators, it is necessary to hold GND firmly at zero volts at all times. Therefore, the system ground star connection should be located as close to this pin as possible.

As in any analog system, good supply bypassing is necessary in order to achieve optimum system performance. The power supplies should be bypassed with at least a 20µF tantalum and a 0.1µF ceramic capacitor to GND. The reference input should be bypassed with a 0.1µF ceramic capacitor to AG. The capacitor leads should be as short as possible.

The pins on the HI-7153 are arranged such that the analog pins are well isolated from the digital pins. In spite of this arrangement, there is always some pin-to-pin coupling. Therefore the analog inputs to the device should not be driven from very high output impedance sources. PC board layout should screen the analog and reference inputs with guard rings on both sides of the PC board, connected to AG.

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Applications

Figure 4 illustrates an application where the HI-7153 is used to form a multi-channel data acquisition system. Either slow memory or fast memory modes of operation can be selected. Fast memory mode should be selected for maximum throughput. The output data is configured for 16 bit bus operation in these applications. By tying BUS to DG and connecting the HBE input to the system address decoder, the output data can be configured for 8 bit bus systems.

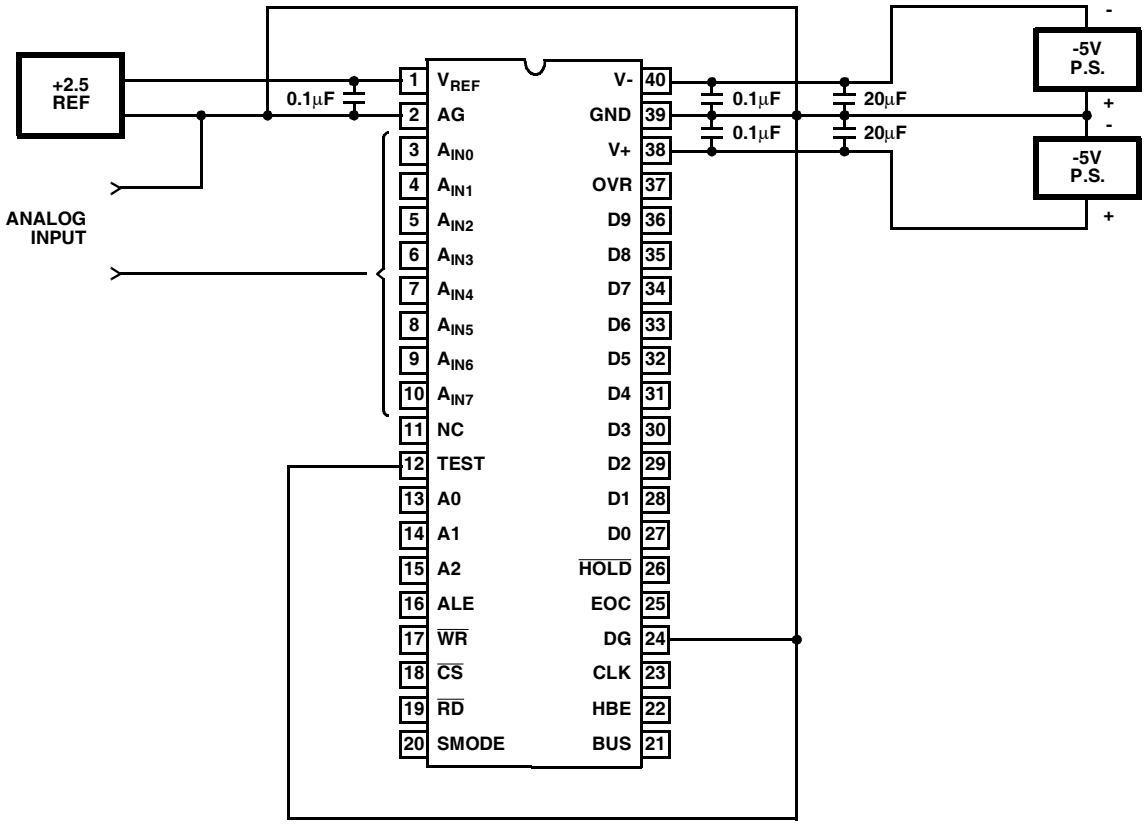

FIGURE 3. GROUND AND POWER SUPPLY DECOUPLING

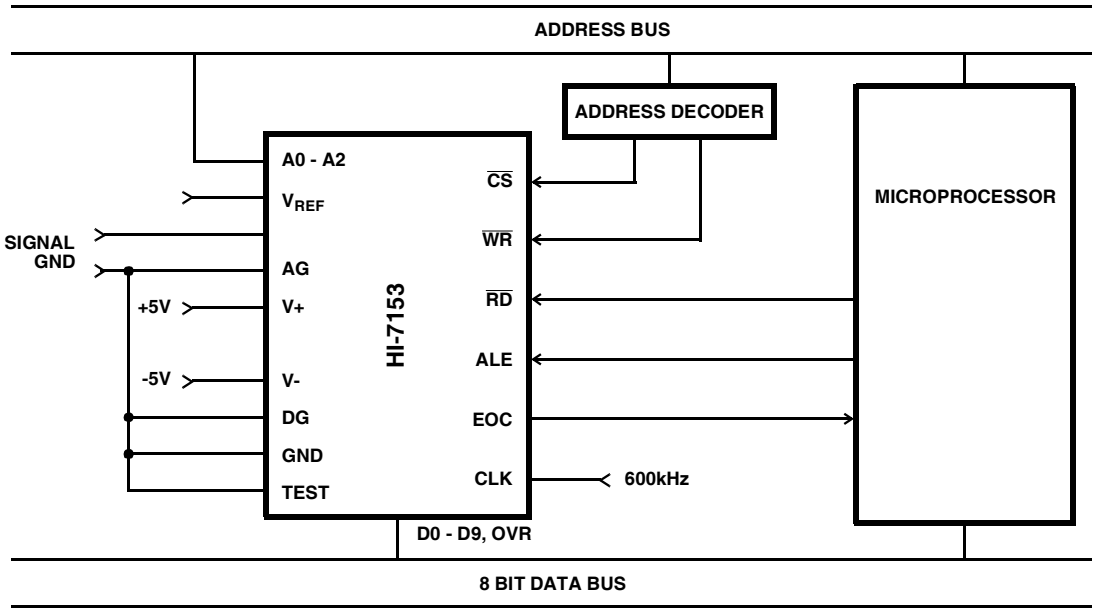

FIGURE 4. MULTI-CHANNEL DATA ACQUISITION SYSTEM

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