19-0541; Rev 1; 10/06

Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

General Description

The MAX6782–MAX6790 are low-power, 1% accurate, dual-/triple-/quad-level battery monitors offered in small TDFN and TQFN packages. These devices are ideal for monitoring single lithium-ion (Li+) cells, or multicell alkaline/NiCd/NiMH power sources. These devices feature fixed and adjustable hysteresis options to eliminate output chattering associated with battery-voltage monitors.

The MAX6782/MAX6783 offer four battery monitors in a single package with factory-set (0.5%, 5%, 10%) or adjustable hysteresis. The MAX6784/MAX6785 provide three battery monitors with factory-set (0.5%, 5%, 10%) or adjustable hysteresis. The MAX6786/MAX6787/MAX6788 offer two battery monitors with external inputs for setting the rising and falling thresholds, allowing external hysteresis control. The MAX6789/MAX6790 feature quad-level overvoltage detectors with complementary outputs.

The MAX6782–MAX6790 are offered with either open-drain or push-pull outputs. The MAX6782/MAX6784/MAX6786/MAX6789 are available with push-pull outputs while the MAX6783/MAX6785/MAX6787/MAX6790 are available with open-drain outputs. The MAX6788 is available with one open-drain output and one push-pull output (see the *Selector Guide*). This family of devices is offered in space-saving TDFN and TQFN packages and is fully specified over the -40°C to +85°C extended temperature range.

Applications

Battery-Powered Systems (Single-Cell Li+ or Multicell NiMH, NiCd, Alkaline)

Cell Phones/Cordless Phones

Pagers

Portable Medical Devices

PDAs

Electronic Toys

MP3 Players

Features

- **1% Accurate Threshold Specified Over Full Temperature Range**
- **Dual-/Triple-/Quad, Low-Battery Output Options**
- **Low 5.7µA Battery Current**
- **Open-Drain or Push-Pull Outputs**
- **Fixed or Adjustable Hysteresis**
- **Low Input Bias Current**
- **Guaranteed Valid Low-Battery-Output Logic State Down to V_{BATT} = 1.05V**
- **Reverse-Battery Protection**
- **Immune to Short Battery Transients**
- **Fully Specified from -40°C to +85°C**
- **Small TDFN and TQFN Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6782TE_+	-40°C to +85°C	16 TQFN-EP*	T1633-4
MAX6783TE_+	-40°C to +85°C	16 TQFN-EP*	T1633-4
MAX6784TC_+	-40°C to +85°C	12 TQFN-EP*	T1233-1
MAX6785TC_+	-40°C to +85°C	12 TQFN-EP*	T1233-1

Ordering Information continued at end of data sheet.

+Denotes lead-free package.

**EP = Exposed paddle.*

The MAX6782/MAX6783/MAX6784/MAX6785 are available with factory-trimmed hysteresis. Specify trim by replacing "_" with "A" for 0.5%, "B" for 5%, or "C" for 10% hysteresis.

Pin Configuration and Typical Operating Circuit appear at end of data sheet.

Selector Guide

PART	MONITOR LEVEL	$\overline{LBO}$ OUTPUT	OV	$\overline{OV}$	OUTPUT TYPE	HYSTERESIS
MAX6782TE_+	4	Quad	—	—	Push-Pull	Fixed/Adj
MAX6783TE_+	4	Quad	—	—	Open Drain	Fixed/Adj
MAX6784TC_+	3	Triple	—	—	Push-Pull	Fixed/Adj
MAX6785TC_+	3	Triple	—	—	Open Drain	Fixed/Adj
MAX6786TA+	2	Dual	—	—	Push-Pull	Adj
MAX6787TA+	2	Dual	—	—	Open Drain	Adj
MAX6788TA+	2	Dual	—	—	Push-Pull/Open Drain	Adj
MAX6789TB+	4	—	Single	Single	Push-Pull	—
MAX6790TB+	4	—	Single	Single	Open Drain	—

Note: *All devices are available in tape and reel in 2.5k increments. For tape and reel orders, add a "T" after the "+" to complete the part number.*

Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
BATT .....-0.3V to +6V
IN1–IN4, LBH1, LBL1, LBH2, LBL2 .....-0.3V to Min ((V_{BATT} + 0.3V) and +6V)
HADJ1–HADJ4, REF .....-0.3V to Min ((V_{BATT} + 0.3V) and +6V)
$\overline{LBO1}$–$\overline{LBO4}$ (push-pull) ..-0.3V to Min ((V_{BATT} + 0.3V) and +6V)
$\overline{LBO1}$–$\overline{LBO4}$ (open drain).....-0.3V to +6V
Input Current (all pins) 20mA
Output Current (all pins) 20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 23.8mW/°C above +70°C) 1905mW
10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
12-Pin Thin QFN (derate 16.7mW/°C above +70°C) ..1333mW
16-Pin Thin QFN (derate 20.8mW/°C above +70°C) ..1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BATT} = 1.6V to 5.5V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 2)	V_{BATT}	T_A = 0°C to +70°C	1.05		5.5	V
		T_A = -40°C to +85°C	1.2		5.5	
Supply Current	I_Q	V_{BATT} = 3.7V, no load		6.3	10	µA
		V_{BATT} = 1.8V, no load		5.7		µA
Startup Time (Note 3)		V_{BATT} rising from 0 to 1.6V			5	ms
MAX6782/MAX6783/MAX6784/MAX6785						
IN_ Falling Threshold (Note 4)	V_{INF}	0.5% hysteresis (A version)	0.5994	0.6055	0.6115	V
		5% hysteresis (B version)	0.5723	0.5781	0.5839	
		10% hysteresis (C version)	0.5422	0.5477	0.5531	
IN_ Rising Threshold (Note 4)	V_{INR}		0.6024	0.6085	0.6146	V
IN_, HADJ_ Input Leakage Current		$V_{IN\_}$, $V_{HADJ\_}$ ≥ 0.3V			5	nA
Reference Output	V_{REF}		0.6024	0.6085	0.6146	V
Reference Load Regulation		I_{REF} = 0 to 1mA		0.3		mV/mA
Reference Temperature Coefficient	TEMPCO			15		ppm/°C
Reference Short-Circuit Current				20		mA
Hysteresis Adjustment Range			0.4		V_{REF}	V
Hysteresis Adjustment Logic Low	V_{HALL}				0.07	V
Hysteresis Adjustment Logic High	V_{HALH}		0.17			V
MAX6786/MAX6787/MAX6788						
LBL_, LBH_ Threshold	V_{TH}		0.6024	0.6085	0.6146	V
LBL_, LBH_ Input Leakage Current		V_{LBL}, $V_{LBH\_}$ ≥ 0.3V			5	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 1.6V to 5.5V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAX6782–MAX6788						
$\overline{LBO\_}$ Propagation Delay	t_{PD}	±100mV overdrive		30		µs
$\overline{LBO\_}$ Output Low Voltage (Push-Pull or Open Drain)	V_{OL}	V_{BATT} ≥ 1.2V, I_{SINK} = 100µA			0.3	V
		V_{BATT} ≥ 2.7V, I_{SINK} = 1.2mA			0.3	V
		V_{BATT} ≥ 4.5V, I_{SINK} = 3.2mA			0.4	V
$\overline{LBO\_}$ Output High Voltage (Push-Pull) (Note 5)	V_{OH}	V_{BATT} ≥ 1.6V, I_{SOURCE} = 10µA	0.8 x V_{BATT}			V
		V_{BATT} ≥ 2.7V, I_{SOURCE} = 500µA	0.8 x V_{BATT}			V
		V_{BATT} ≥ 4.5V, I_{SOURCE} = 800µA	0.8 x V_{BATT}			V
$\overline{LBO\_}$ Output Leakage Current (Open Drain)		Output not asserted, $V_{\overline{LBO\_}}$ = 0 or 5V			500	nA
MAX6789/MAX6790						
IN_ Rising Threshold	V_{TH+}		0.6024	0.6085	0.6146	V
IN_ Hysteresis				31		mV
IN_ Input Leakage Current		$V_{IN\_}$ ≥ 0.3V			5	nA
$\overline{OV}$, OV Delay Time	t_{PD}	±100mV overdrive		30		µs
$\overline{OV}$ Output Low Voltage (Push-Pull or Open Drain)	V_{OL}	V_{BATT} ≥ 1.6V, I_{SINK} = 100µA, output asserted			0.3	V
		V_{BATT} ≥ 2.7V, I_{SINK} = 1.2mA, output asserted			0.3	
		V_{BATT} ≥ 4.5V, I_{SINK} = 3.2mA, output asserted			0.4	
$\overline{OV}$ Output High Voltage (Push-Pull) (Note 5)	V_{OH}	V_{BATT} ≥ 1.2V, I_{SOURCE} = 10µA, output not asserted	0.8 x V_{BATT}			V
		V_{BATT} ≥ 2.7V, I_{SOURCE} = 500µA, output not asserted	0.8 x V_{BATT}			
		V_{BATT} ≥ 4.5V, I_{SINK} = 800µA, output not asserted	0.8 x V_{BATT}			
$\overline{OV}$ Output Leakage Current (Open Drain)		Output not asserted, V_{OV}, $V_{\overline{OV}}$ = 0 or 5V			500	nA
OV Output Low Voltage (Push-Pull or Open Drain)	V_{OL}	V_{BATT} ≥ 1.2V, I_{SINK} = 100µA, output not asserted			0.3	V
		V_{BATT} ≥ 2.7V, I_{SINK} = 1.2mA, output not asserted			0.3	
		V_{BATT} ≥ 4.5V, I_{SINK} = 3.2mA, output not asserted			0.4	

Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 1.6V to 5.5V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OV Output High Voltage (Push-Pull) (Note 5)	V_{OH}	V_{BATT} ≥ 1.6V, I_{SOURCE} = 10µA, output asserted	0.8 x V_{BATT}			V
		V_{BATT} ≥ 2.7V, I_{SOURCE} = 500µA, output asserted	0.8 x V_{BATT}			
		V_{BATT} ≥ 4.5V, I_{SOURCE} = 800µA, output asserted	0.8 x V_{BATT}			
OV Output Leakage Current (Open Drain)		Output asserted, V_{OV} = 0 or 5V			500	nA
$\overline{CLEAR}$ Input Low Voltage	V_{IL}				0.3 x V_{BATT}	V
$\overline{CLEAR}$ Input High Voltage	V_{IH}		0.7 x V_{BATT}			V
$\overline{CLEAR}$ Pullup Resistance			25		80	kΩ
$\overline{CLEAR}$ Minimum Pulse Width			1			µs
$\overline{CLEAR}$ Delay Time	t_{CLD}			300		ns

Note 1: Devices are tested at T_A = +25°C and guaranteed by design for T_A = T_{MIN} to T_{MAX} as specified.

Note 2: Operating voltage range ensures low battery output is in the correct state. Minimum battery voltage for electrical specification is 1.6V.

Note 3: Reference and threshold accuracy is only guaranteed after the startup time. Startup time is guaranteed by design.

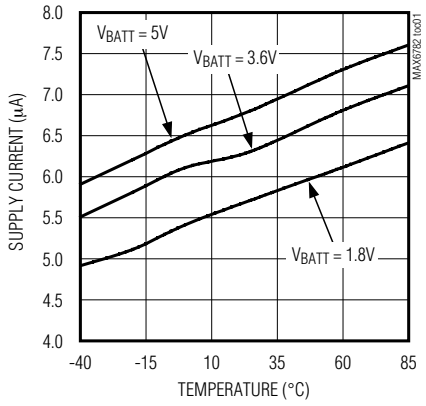
Note 4: The rising threshold is guaranteed to be higher than the falling threshold.

Note 5: The source current is the total source current from all outputs.

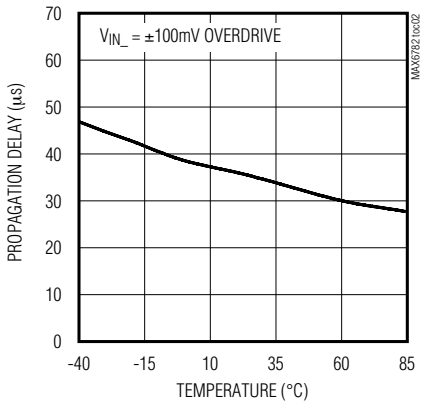
Typical Operating Characteristics

(V_{BATT} = 3.6V, T_A = +25°C, unless otherwise noted.)

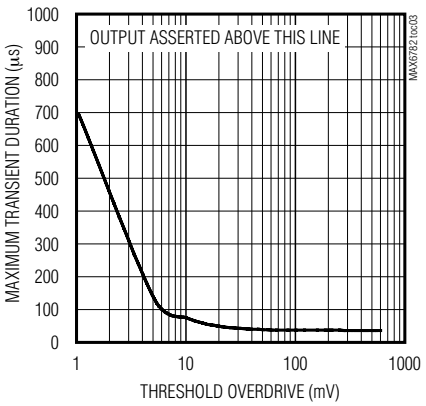
SUPPLY CURRENT vs. TEMPERATURE



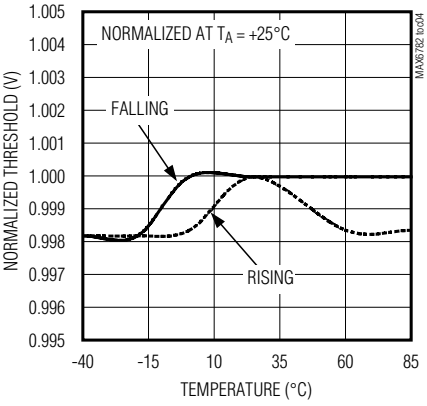
PROPAGATION DELAY vs. TEMPERATURE



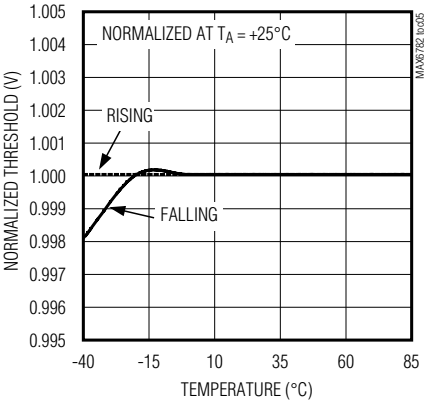
MAXIMUM TRANSIENT DURATION vs. THRESHOLD OVERDRIVE



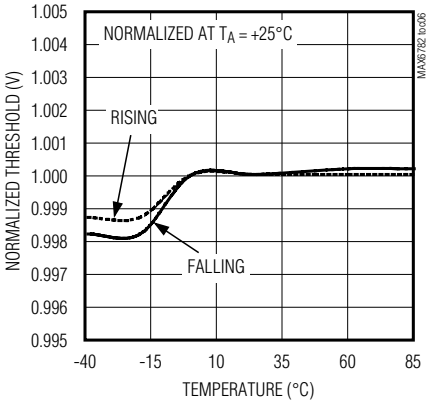
NORMALIZED THRESHOLD VOLTAGES vs. TEMPERATURE (MAX6782TEA)



NORMALIZED THRESHOLD VOLTAGES vs. TEMPERATURE (MAX6782TEB)



NORMALIZED THRESHOLD VOLTAGES vs. TEMPERATURE (MAX6782TEC)

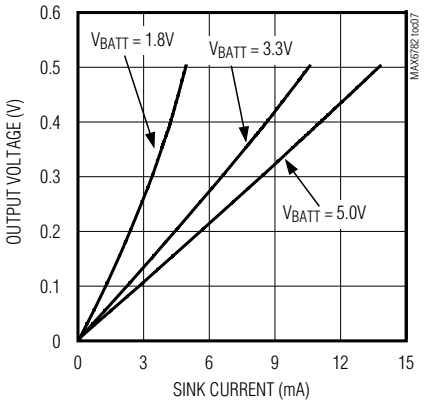


Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

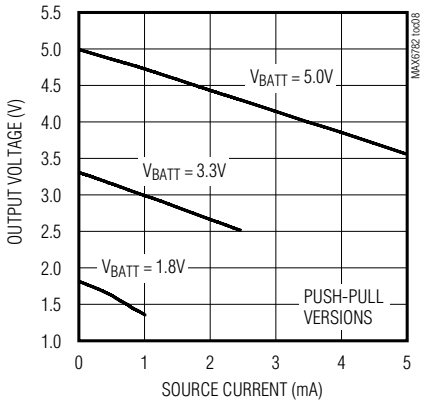
Typical Operating Characteristics (continued)

(V_{BATT} = 3.6V, T_A = +25°C, unless otherwise noted.)

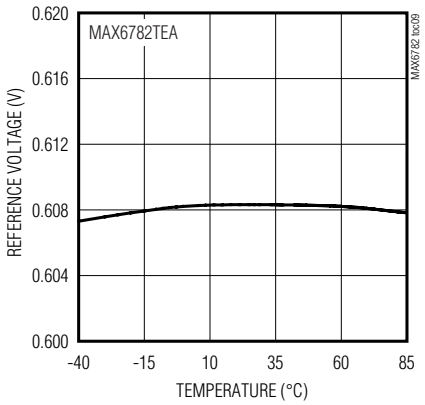
$\overline{LBO}$ OUTPUT VOLTAGE LOW vs. SINK CURRENT



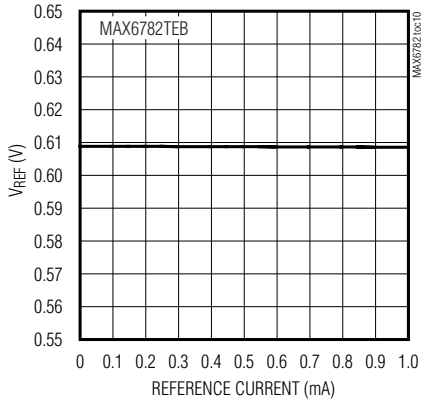
$\overline{LBO}$ OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT



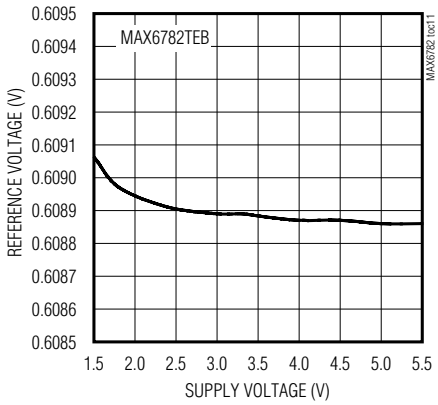
REFERENCE VOLTAGE vs. TEMPERATURE



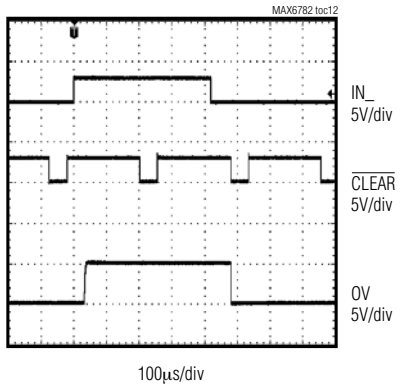
REFERENCE VOLTAGE vs. REFERENCE CURRENT



REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



$\overline{CLEAR}$ LATCH CIRCUIT



Pin Description

MAX6782/MAX6783/MAX6784/MAX6785

PIN		NAME	FUNCTION
MAX6782/ MAX6783	MAX6784/ MAX6785		
1	1	IN2	Battery Monitor Input 2. Connect to an external resistive divider to set the trip threshold for monitor 2.
2	2	IN3	Battery Monitor Input 3. Connect to an external resistive divider to set the trip threshold for monitor 3.
3	—	IN4	Battery Monitor Input 4. Connect to an external resistive divider to set the trip threshold for monitor 4.
4	3	REF	Reference Output. REF can source up to 1mA. REF does not require an external bypass capacitor for stability. Keep the capacitance from REF to GND below 50pF.
5	4	HADJ1	Hysteresis Adjustment Input 1. Connect HADJ1 to GND to select an internal preset hysteresis option. Connect a resistive divider from REF to HADJ1 and to GND to externally adjust the hysteresis for IN1 from its internal preset hysteresis (see Figure 6).
6	5	HADJ2	Hysteresis Adjustment Input 2. Connect HADJ2 to GND to select an internal preset hysteresis option. Connect a resistive divider from REF to HADJ2 and to GND to externally adjust the hysteresis for IN2 from its internal preset hysteresis (see Figure 6).
7	6	HADJ3	Hysteresis Adjustment Input 3. Connect HADJ3 to GND to select an internal preset hysteresis option. Connect a resistive divider from REF to HADJ3 and to GND to externally adjust the hysteresis for IN3 from its internal preset hysteresis (see Figure 6).
8	—	HADJ4	Hysteresis Adjustment Input 4. Connect HADJ4 to GND to select an internal preset hysteresis option. Connect a resistive divider from REF to HADJ4 and to GND to externally adjust the hysteresis for IN4 from its internal preset hysteresis (see Figure 6).
9	—	$\overline{LBO4}$	Active-Low, Low-Battery Output 4. $\overline{LBO4}$ asserts when V_{IN4} falls below the falling threshold voltage. $\overline{LBO4}$ deasserts when V_{IN4} exceeds the rising threshold voltage.
10	7	$\overline{LBO3}$	Active-Low, Low-Battery Output 3. $\overline{LBO3}$ asserts when V_{IN3} falls below the falling threshold voltage. $\overline{LBO3}$ deasserts when V_{IN3} exceeds the rising threshold voltage.
11	8	$\overline{LBO2}$	Active-Low, Low-Battery Output 2. $\overline{LBO2}$ asserts when V_{IN2} falls below the falling threshold voltage. $\overline{LBO2}$ deasserts when V_{IN2} exceeds the rising threshold voltage.
12	9	$\overline{LBO1}$	Active-Low, Low-Battery Output 1. $\overline{LBO1}$ asserts when V_{IN1} falls below the falling threshold voltage. $\overline{LBO1}$ deasserts when V_{IN1} exceeds the rising threshold voltage.
13	10	BATT	Battery Input. Power supply to the device. For better noise immunity, bypass BATT to GND with a 0.1µF capacitor as close to the device as possible.
14	11	GND	Ground
15	—	N.C.	No Connection. Not internally connected.
16	12	IN1	Battery Monitor Input 1. Connect to an external resistive divider to set the trip threshold for monitor 1.

Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

Pin Description (continued)

MAX6786/MAX6787/MAX6788

PIN	NAME	FUNCTION
1	LBL1	Falling Trip Level Input 1. Connect to an external resistive divider to set the falling trip level.
2	LBH1	Rising Trip Level Input 1. Connect to an external resistive divider to set the rising trip level.
3	LBL2	Falling Trip Level Input 2. Connect to an external resistive divider to set the falling trip level.
4	LBH2	Rising Trip Level Input 2. Connect to an external resistive divider to set the rising trip level.
5	GND	Ground
6	$\overline{LBO2}$	Active-Low, Low-Battery Output 2. $\overline{LBO2}$ asserts when V_{LBL2} falls below the falling threshold voltage. $\overline{LBO2}$ deasserts when V_{LBH2} exceeds the rising threshold voltage.
7	$\overline{LBO1}$	Active-Low, Low-Battery Output 1. $\overline{LBO1}$ asserts when V_{LBL1} falls below the falling threshold voltage. $\overline{LBO1}$ deasserts when V_{LBH1} exceeds the rising threshold voltage.
8	BATT	Battery Input. Power supply to the device. For better noise immunity, bypass BATT to GND with a 0.1µF capacitor as close to the device as possible.

MAX6789/MAX6790

PIN	NAME	FUNCTION
1	IN1	Overvoltage Monitor Input 1
2	IN2	Overvoltage Monitor Input 2
3	IN3	Overvoltage Monitor Input 3
4	IN4	Overvoltage Monitor Input 4
5	GND	Ground
6	$\overline{CLEAR}$	Active-Low Clear Input. $\overline{OV}$ and OV do not latch when an overvoltage fault is detected if $\overline{CLEAR}$ is held low. $\overline{CLEAR}$ has an internal pullup resistor to BATT.
7	N.C.	No Connection. Not internally connected.
8	$\overline{OV}$	Active-Low Overvoltage Output. When any of the inputs ($V_{IN\_}$) exceeds its respective rising threshold voltage, $\overline{OV}$ asserts and stays asserted until $\overline{CLEAR}$ is pulled low or the power to the device is cycled. $\overline{OV}$ does not latch when an overvoltage fault is detected if $\overline{CLEAR}$ is held low.
9	OV	Active-High Overvoltage Output. Inverse of $\overline{OV}$.
10	BATT	Battery Input. Power supply to the device. For better noise immunity, bypass BATT to GND with a 0.1µF capacitor as close to the device as possible.

Detailed Description

The MAX6782–MAX6788 are designed to monitor two to four battery levels (1% accuracy) and assert an active-low output indicator when the monitored voltage level falls below the user-set threshold. Each battery level is associated with an independent open-drain or push-pull output. Each of these independent outputs can be used to provide low battery warnings at different voltage levels. Each of these monitored levels offers fixed or adjustable hysteresis in order to prevent the output from chattering as the battery recovers from the lighter loads. The MAX6782–MAX6785 also feature reference outputs that can source up to 1mA.

The MAX6789/MAX6790 monitor four overvoltage conditions and assert the complementary overvoltage outputs when any voltage at the inputs exceeds its respective threshold. The MAX6789/MAX6790 allow each trip threshold to be set with external resistors. These devices also feature a latch and a clear function.

Figures 1, 2, and 3 show the simplified block diagrams for the MAX6782–MAX6790. See the *Selector Guide*.

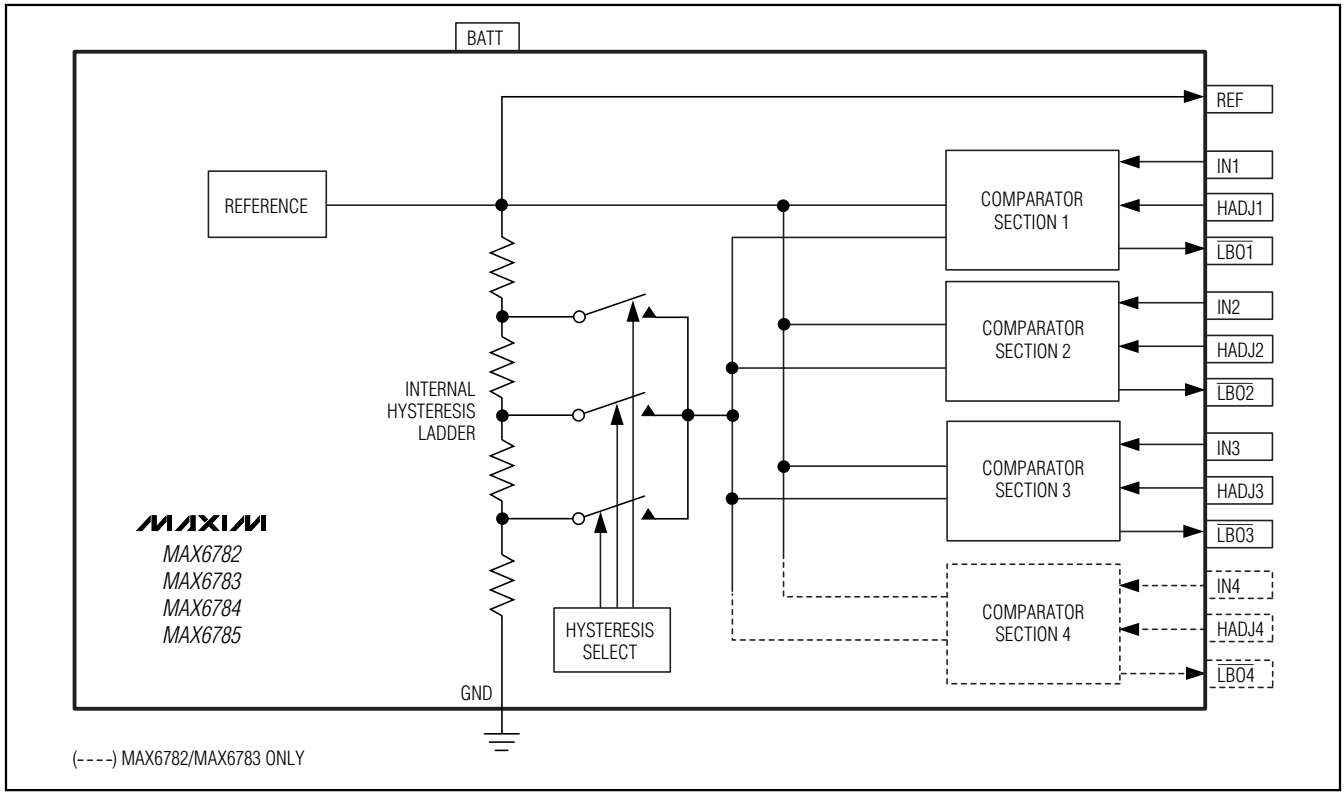


Figure 1. MAX6782–MAX6785 Block Diagram

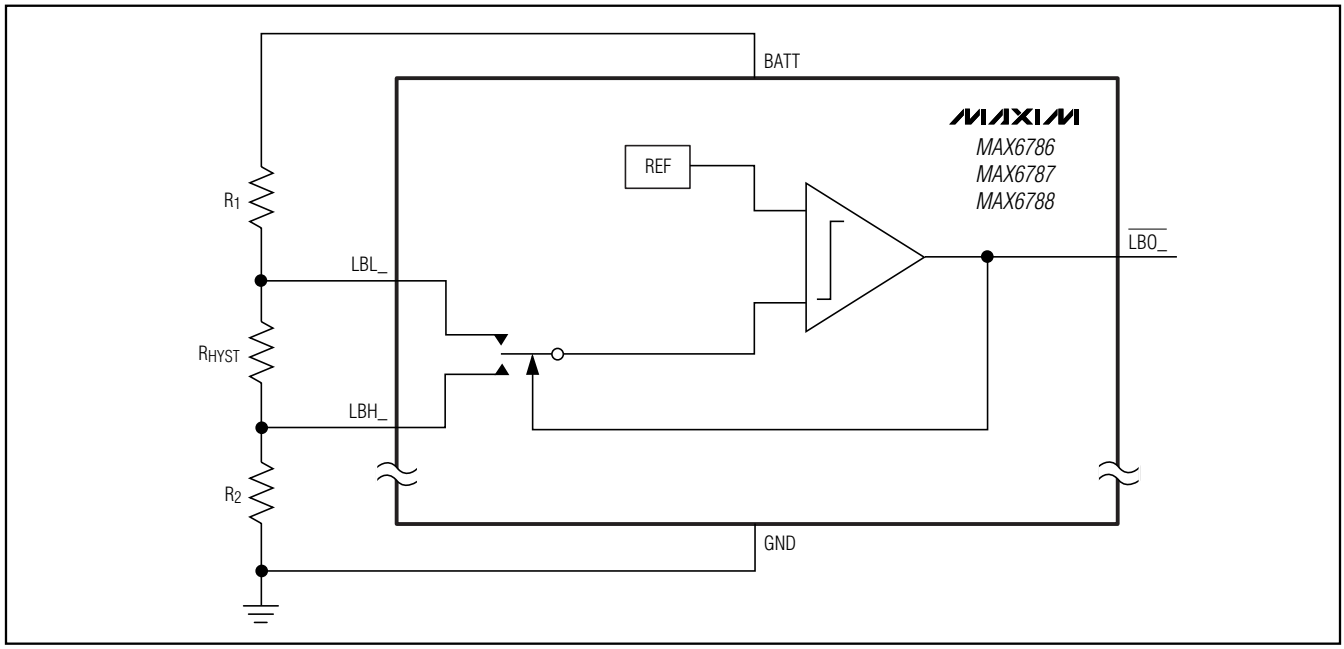


Figure 2. MAX6786/MAX6787/MAX6788 Block Diagram

Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

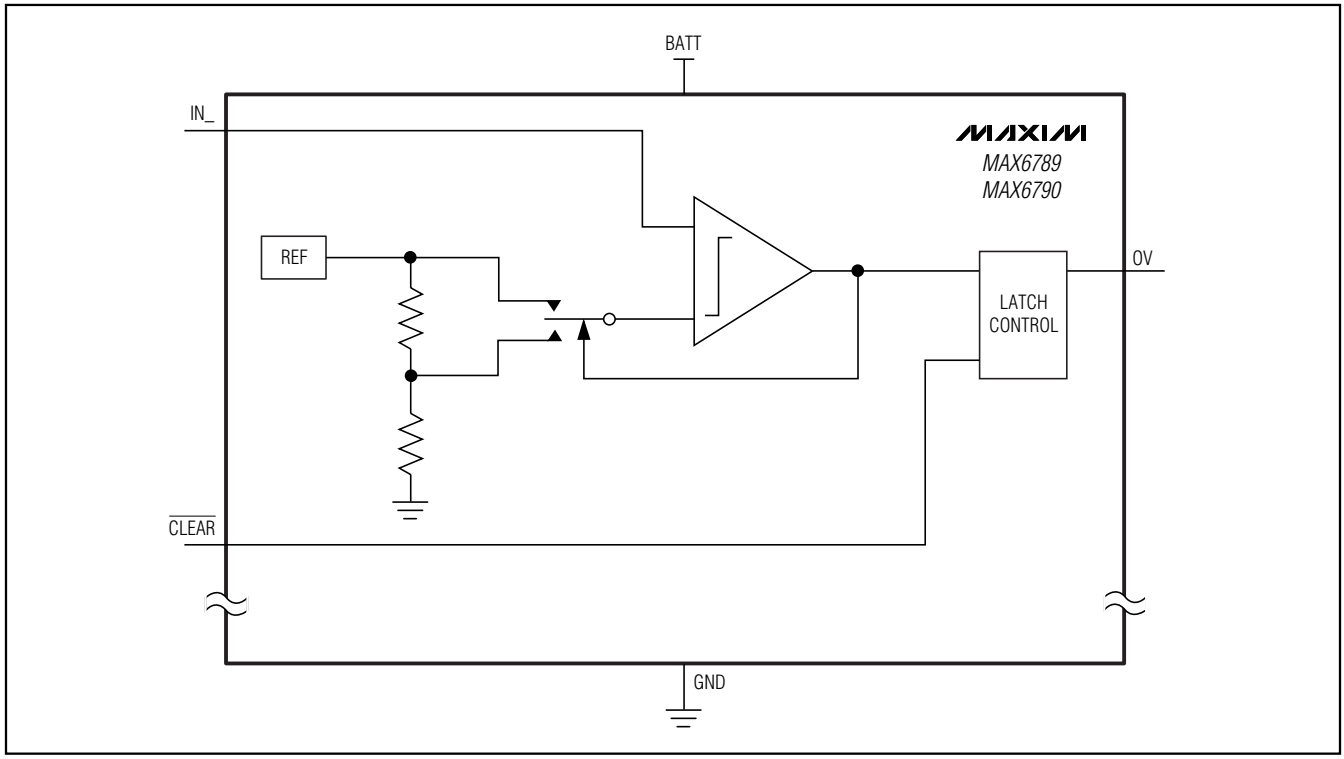


Figure 3. MAX6789/MAX6790 Block Diagram

Low-Battery/Overvoltage Output

All devices are offered with either push-pull or open-drain outputs (see the *Selector Guide*). The MAX6788 has one push-pull output and one open-drain output, configured as shown in Table 1.

Table 1. MAX6788 Outputs

DEVICE	$\overline{\text{LBO1}}$	$\overline{\text{LBO2}}$
MAX6788	Push-Pull	Open Drain

All open-drain outputs require an external pullup resistor. The open-drain pullup resistor may be connected to an external voltage up to +6V, regardless of the voltage at BATT.

Hysteresis

Input hysteresis defines two thresholds, separated by the hysteresis voltage, configured so the output asserts when the input falls below the falling threshold, and deasserts only when the input rises above the rising threshold. Figures 4 and 5 show this graphically. Hysteresis removes, or greatly reduces, the possibility of the output changing state in response to noise or battery-terminal voltage recovery after load removal.

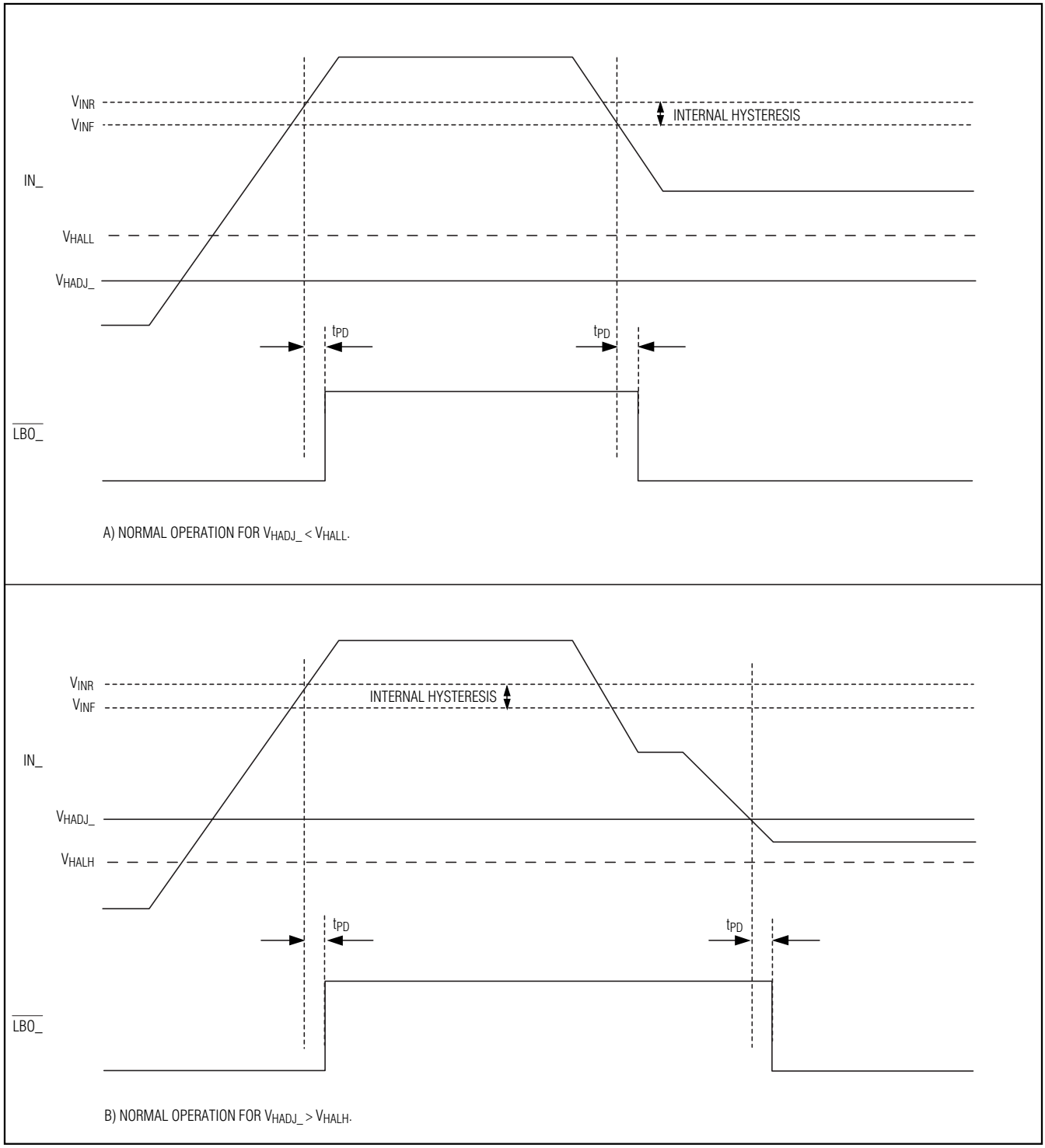


Figure 4. MAX6782–MAX6785 Timing

Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

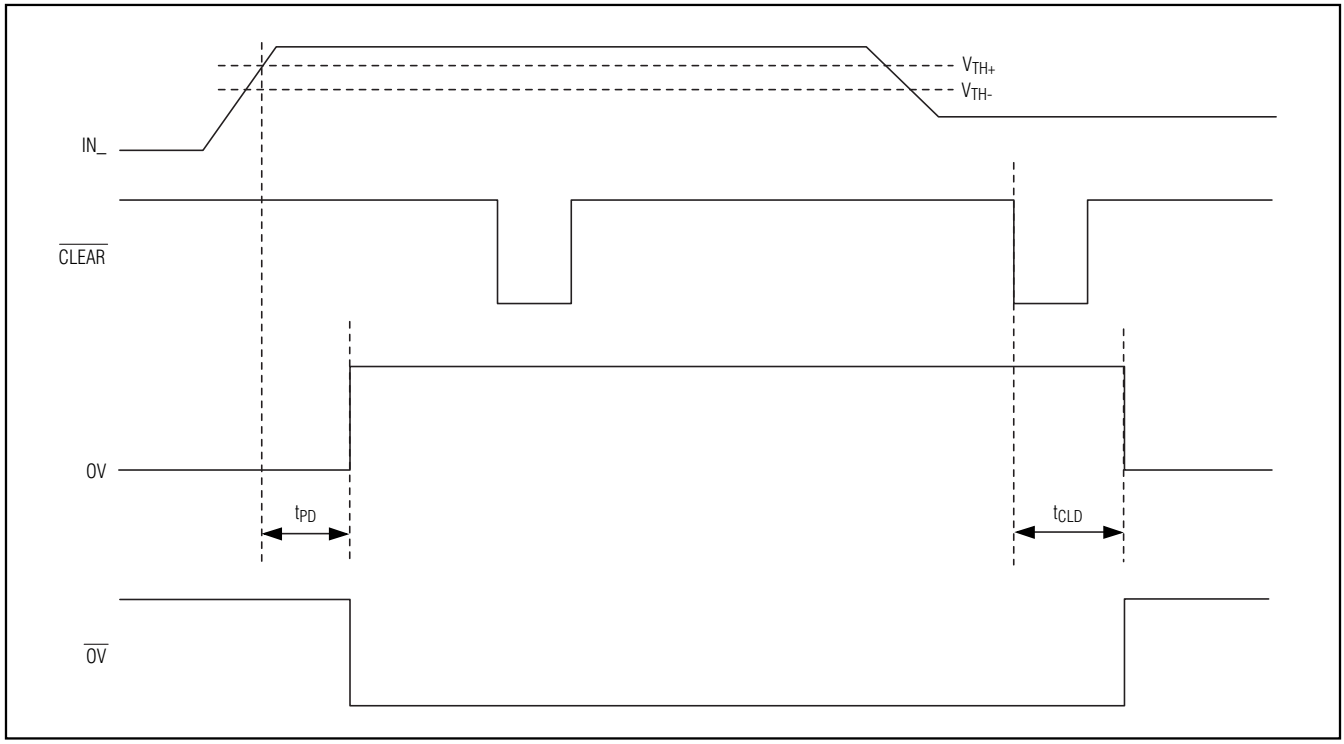


Figure 5. MAX6789/MAX6790 Timing

MAX6782–MAX6785 Hysteresis

Factory-Set Hysteresis

The MAX6782–MAX6785 have factory-set hysteresis for ease of use and reduced external parts count. For these devices the absolute hysteresis voltage is a percentage of the internally generated reference. The amount depends on the device option. "A" devices have 0.5% hysteresis, "B" devices have 5% hysteresis, and "C" devices have 10% hysteresis. Table 2 presents the threshold voltages for devices with factory-set hysteresis. For factory-set hysteresis, connect HADJ_ to GND.

Table 2. Typical Falling and Rising Thresholds for MAX6782–MAX6785 (HADJ_ = GND)

DEVICE OPTION	PERCENT HYSTERESIS (%)	FALLING THRESHOLD (V_{INF}) (V)	RISING THRESHOLD (V_{INR}) (V)
A	0.5	0.6055	0.6085
B	5	0.5781	0.6085
C	10	0.5477	0.6085

Externally Adjusted Hysteresis

The MAX6782–MAX6785 can also be configured for externally adjustable hysteresis. Connect a resistive divider from REF to HADJ_ and to GND (Figure 6) to set the hysteresis voltage. The hysteresis adjustment range is from 0.4V to V_{REF}, and the voltage at HADJ_ ($V_{HADJ\_}$) must be set higher than Hysteresis Adjustment Logic High (V_{HALH}) (Figure 4b). Note that if $V_{HADJ\_}$ is lower than Hysteresis Adjustment Logic Low (V_{HALL}), these devices switch back to the internal factory-set hysteresis (Figure 4a).

MAX6786/MAX6787/MAX6788 Adjustable Hysteresis

The MAX6786/MAX6787/MAX6788 offer external hysteresis control through the resistive divider that monitors battery voltage. Figure 2 shows the connections for external hysteresis. See *Calculating an External Hysteresis Resistive Divider* (MAX6786/MAX6787/MAX6788) section for more information.

Reference Output

The reference output can provide up to 1mA of output current. The output is not buffered. Excessive loading affects the accuracy of the thresholds. An external capacitor is not required for stability and is stable for capacitive loads up to 50pF. In applications where the load or the supply can experience step changes, a capacitor reduces the amount of overshoot (undershoot) and improves the circuit's transient response. Place the capacitor as close to the device as possible for best performance.

Applications Information

Resistor-Value Selection

Choosing the proper external resistors is a balance between accuracy and power use. The input to the voltage monitor, while high impedance, draws a small current, and that current travels through the resistive divider, introducing error. If extremely high resistor values are used, this current introduces significant error. With extremely low resistor values, the error becomes negligible, but the resistive divider draws more power from the battery than necessary, and shortens battery life. See Figure 6 and calculate the optimum value for R1 using:

$$R_1 = \frac{e_A \times V_{BATT}}{I_L}$$

where e_A is the fraction of the maximum acceptable absolute resistive divider error attributable to the input leakage current (use 0.01 for 1%), V_{BATT} is the battery voltage at which LBO should activate, and I_L is the worst-case IN_ leakage current, from the *Electrical Characteristics*. For example, for 0.5% error, a 2.8V battery minimum, and 5nA leakage, R_1 = 2.80MΩ. Calculate R_2 using:

$$R_2 = \frac{V_{INF} \times R_1}{V_{BATT} - V_{INF}}$$

where V_{INF} is the falling threshold voltage from Table 2. Continuing the above example, and selecting V_{INF} = 0.5477V (10% hysteresis device), R_2 = 681kΩ. There are other sources of error for the battery threshold, including resistor and input monitor tolerances.

Calculating an External Hysteresis Resistive Divider (MAX6782–MAX6785)

To set the hysteresis, place a resistive divider from REF to HADJ_ as shown in Figure 6. The resistive divider sets voltage on HADJ_, which controls the falling threshold (V_{INF}) on the associated IN_ (the rising threshold (V_{INR}) is fixed). See Table 2. Calculate R_3 using:

$$R_3 = \frac{e_A \times V_{REF}}{I_L}$$

where e_A is the fraction of the maximum acceptable absolute resistive divider error attributable to the input leakage current (use 0.01 for 1%), V_{REF} is the reference output voltage, and I_L is the worst-case HADJ_ leakage current. Calculate R_4 using:

$$R_4 = \frac{V_{INF} \times R_3}{V_{REF} - V_{INF}}$$

where V_{INF} is the desired falling voltage threshold. To calculate the percent hysteresis, use:

$$\text{Hysteresis } (\%) = 100 \times \frac{V_{INR} - V_{INF}}{V_{INR}}$$

where V_{INR} is the rising voltage.

Calculating an External Hysteresis Resistive Divider (MAX6786/MAX6787/MAX6788)

Setting the hysteresis externally requires calculating three resistor values, as indicated in Figure 2. First calculate R_1 using:

$$R_1 = \frac{e_A \times V_{BATT}}{I_L}$$

and R_{20} using:

$$R_{20} = \frac{V_{TH} \times R_1}{V_{BATT} - V_{TH}} \text{ (as in the above example)}$$

where $R_{20} = R_2 + R_{HYST}$ determine the total resistive-divider current, I_{TOTAL}, at the trip voltage using:

$$I_{TOTAL} = \frac{V_{BATT}}{R_1 + R_{20}}$$

Then, determine R_{HYST} using:

$$R_{HYST} = \frac{V_{HYST}}{I_{TOTAL}}$$

where V_{HYST} is the required hysteresis voltage.

Finally, determine R_2 using:

$$R_2 = R_{20} - R_{HYST}$$

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Monitoring a Battery Voltage Higher than the Allowable V_{BATT}

For monitoring higher voltages, supply a voltage to BATT, which is within the specified supply range, and power the input resistive divider from the high voltage to be monitored. Do not exceed the Absolute Maximum Ratings.

Maintaining Reference Accuracy

Since the ground connection of the MAX6782–MAX6790 has a small series resistance, any current flowing into an output flows to ground and causes a small voltage to develop from the internal ground to GND. This has the effect of slightly increasing the reference voltage. To minimize the effect on the reference voltage, keep the total output sink current below 3mA.

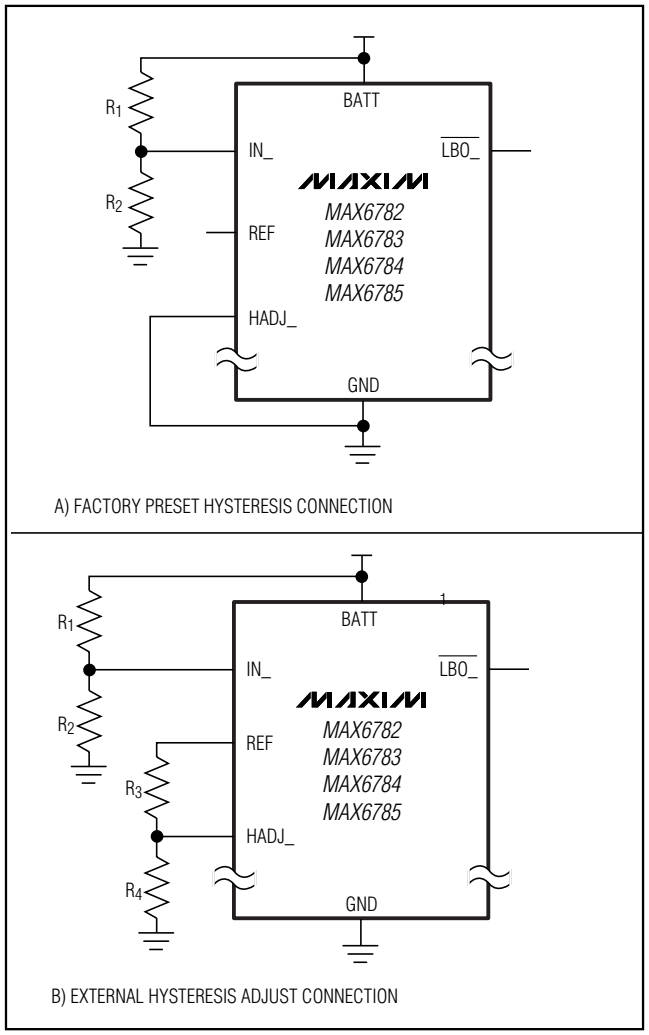


Figure 6. Internal Preset or Externally Adjusted Hysteresis Connection

Adding External Capacitance to Reduce Noise and Transients

If monitoring voltages in a noisy environment, add a bypass capacitor of 0.1µF from BATT to GND as close as possible to the device. For systems with large transients, additional capacitance may be required.

Reverse-Battery Protection

To prevent damage to the device during a reverse-battery condition, connect the MAX6782–MAX6785 in the configuration shown in Figure 6a or 6b. For the internal reverse-battery protection to function correctly on the MAX6782–MAX6790, several conditions must be satisfied:

- The connections to IN_/LBL_/LBH_ must be made to the center node of a resistive divider going from BATT to GND. The Thevenin equivalent impedance of the resistive divider must not fall below 1kΩ in order to limit the current.
- HADJ_ (MAX6782–MAX6785 only) must either be connected to GND or to the center node of a resistive divider going from REF to GND.
- The outputs may only be connected to devices powered by the same battery as the MAX6782–MAX6790.

Note that the MAX6782–MAX6790 will not protect other devices in the circuit.

Additional Application Circuit

Figure 7 shows the MAX6786/MAX6787/MAX6788 in a typical two-battery-level monitoring circuit.

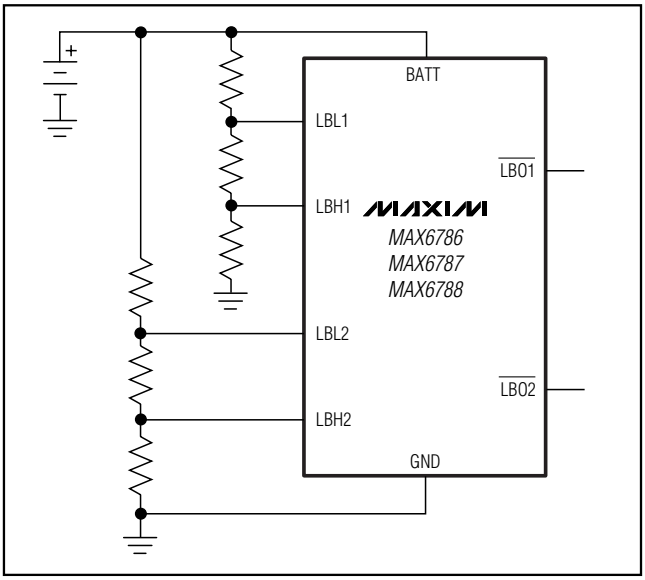
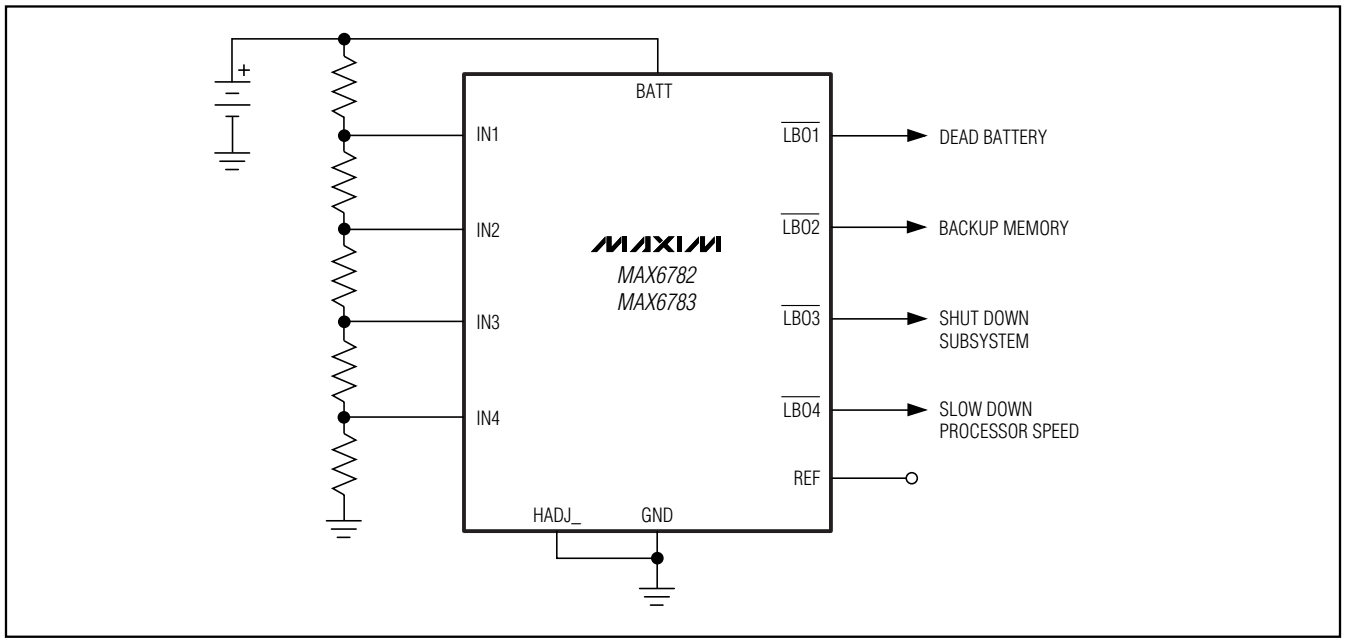


Figure 7. Two-Battery-Level Monitor Configuration

Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

Typical Operating Circuit



Top Marks

PART	TOP MARK
MAX6782TEA+	+AEG
MAX6782TEB+	+AEH
MAX6782TEC+	+AEI
MAX6783TEA+	+AEJ
MAX6783TEB+	+AEK
MAX6783TEC+	+AEL
MAX6784TCA+	+AAV
MAX6784TCB+	+AAW
MAX6784TCC+	+AAX
MAX6785TCA+	+AAY
MAX6785TCB+	+AAZ
MAX6785TCC+	+ABA
MAX6786TA+	+APU
MAX6787TA+	+APV
MAX6788TA+	+APW
MAX6789TB+	+AQI
MAX6790TB+	+AQJ

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6786TA+T	-40°C to +85°C	8 TDFN-EP*	T833-3
MAX6787TA+T	-40°C to +85°C	8 TDFN-EP*	T833-3
MAX6788TA+T	-40°C to +85°C	8 TDFN-EP*	T833-3
MAX6789TB+T	-40°C to +85°C	10 TDFN-EP*	T1033-1
MAX6790TB+T	-40°C to +85°C	10 TDFN-EP*	T1033-1

+Denotes lead-free package.

**EP = Exposed paddle.*

The MAX6782/MAX6783/MAX6784/MAX6785 are available with factory-trimmed hysteresis. Specify trim by replacing "_" with "A" for 0.5%, "B" for 5%, or "C" for 10% hysteresis.

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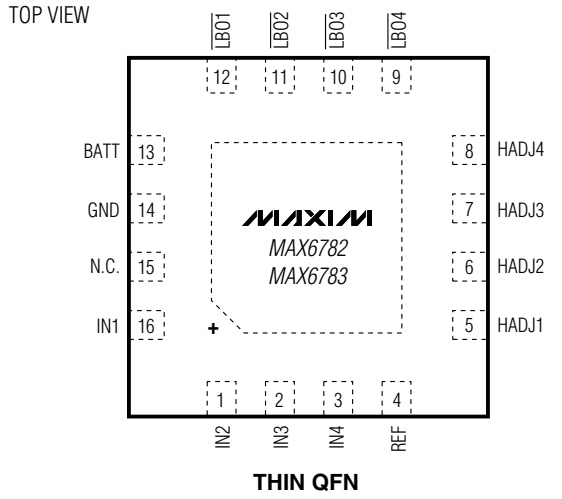
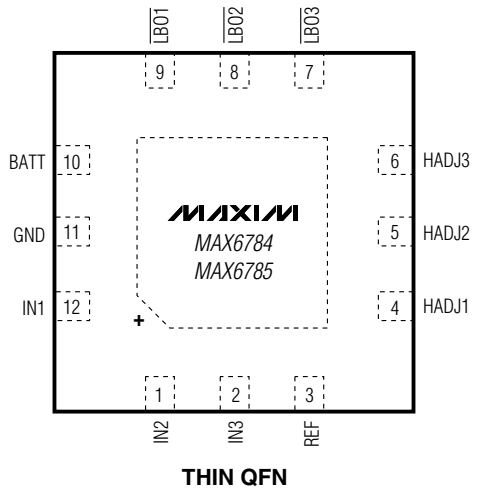
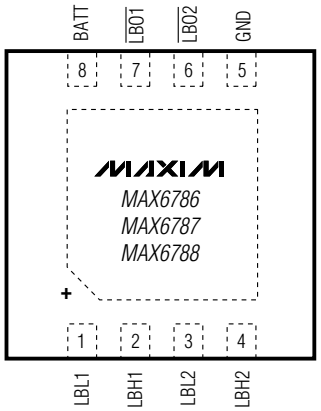
Pin Configurations



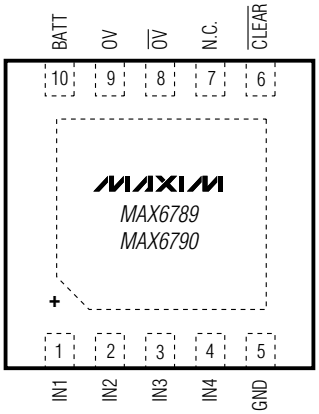
THIN QFN



THIN QFN



TDFN



TDFN

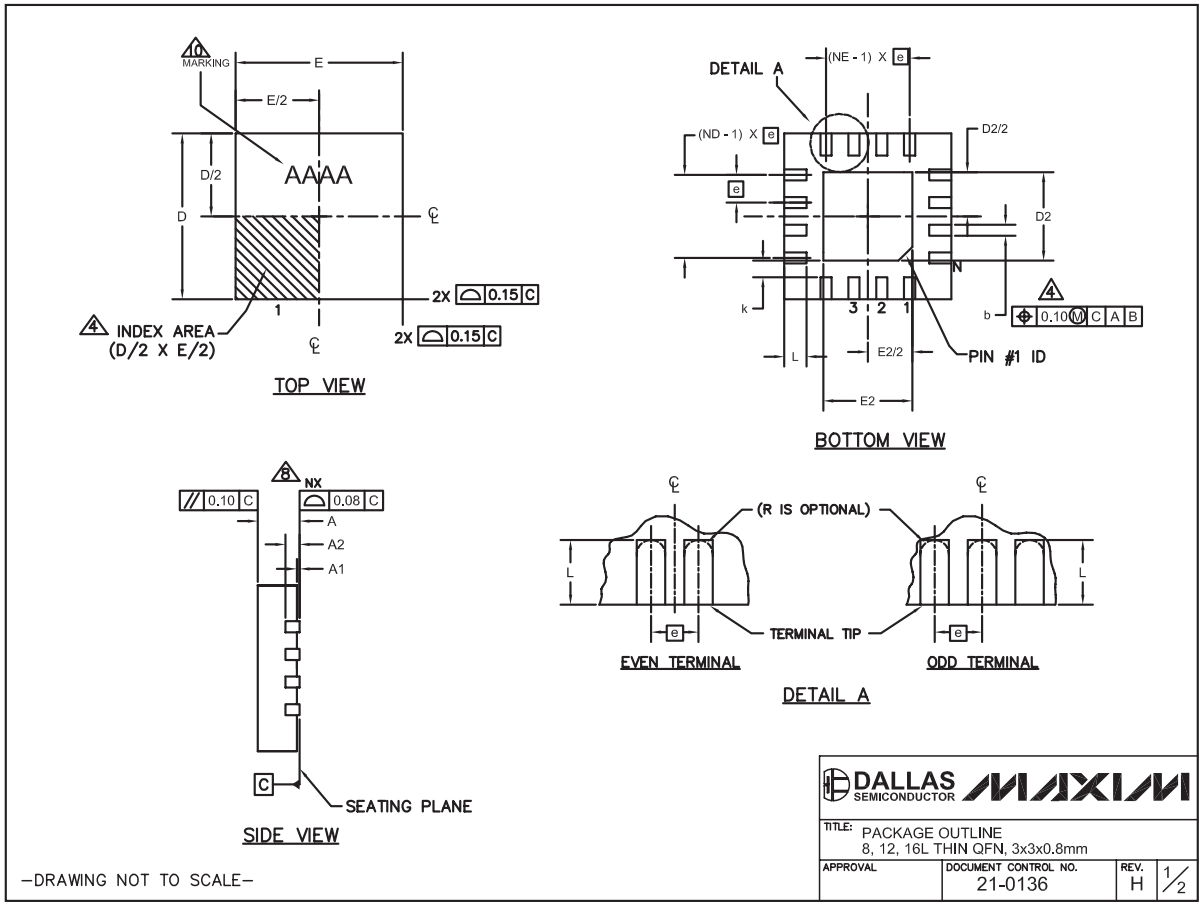
Chip Information

PROCESS: BiCMOS

Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

–DRAWING NOT TO SCALE–

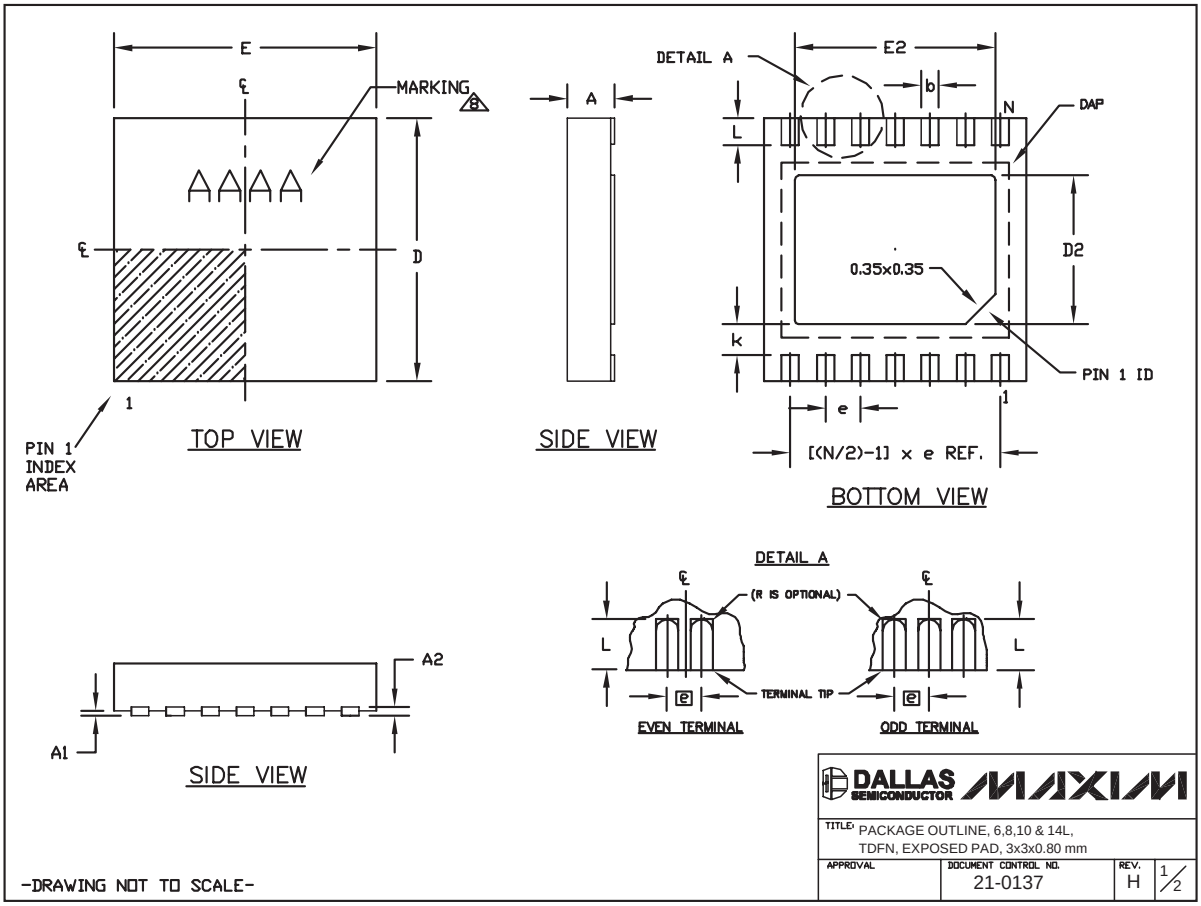
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 8, 12, 16L THIN QFN, 3x3x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	H	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Low-Power, 1% Accurate, Dual-/Triple-/Quad-Level Battery Monitors in Small TDFN and TQFN Packages

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	H	2/2

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