

PCM1700U  
PCM1700P

## Dual 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

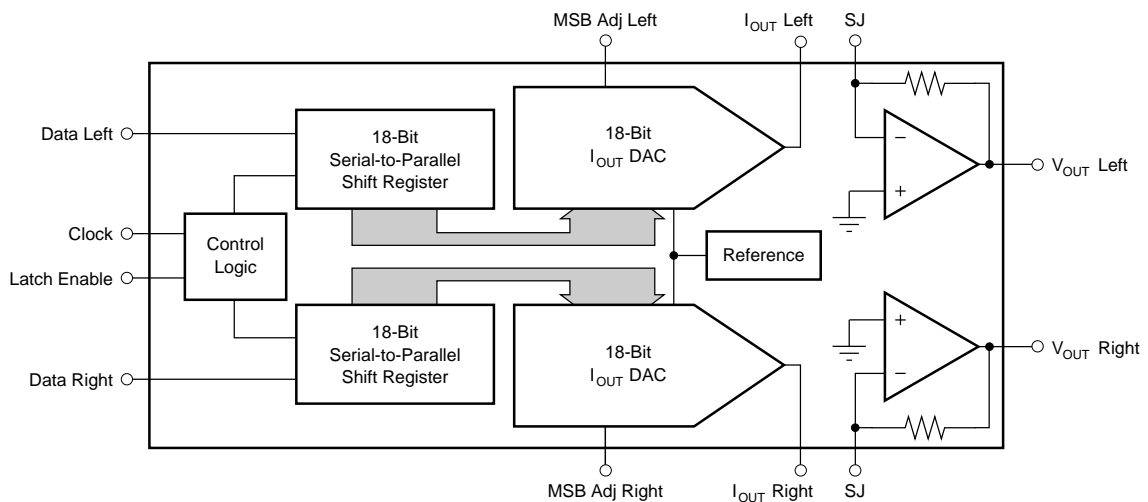
### FEATURES

- DUAL 18-BIT LOW-POWER MONOLITHIC AUDIO D/A CONVERTER
- VERY LOW MAX THD+N:  $-92\text{dB}$  Without External Adjust
- CO-PHASE, LOW-GLITCH  $\pm 3\text{V}$  OR  $\pm 670\mu\text{A}$  AUDIO OUTPUTS
- CAPABLE OF 16X PER CHANNEL OVERSAMPLING RATE
- COMPLETE WITH INTERNAL REFERENCE
- SERIAL INPUT FORMAT 100% COMPATIBLE WITH INDUSTRY STD PCM56P
- RUNS ON  $\pm 5\text{V}$  SUPPLIES AND DISSIPATES 300mW MAX
- COMPACT 28-PIN PLASTIC DIP OR SOIC

### DESCRIPTION

The PCM1700 is a low cost, high-performance, dual 18-bit digital-to-analog converter. The PCM1700 features low glitch, co-phase current and voltage outputs and only requires  $\pm 5\text{V}$  supplies. The PCM1700 comes complete with an internal reference and optional MSB adjustability for even greater THD performance. Total power dissipation is less than 400mW max. Low maximum Total Harmonic Distortion + Noise ( $-92\text{dB}$  max; PCM1700P-K) is 100% tested. The very fast PCM1700 is also capable of 16X oversampling rates on both channels simultaneously, providing freedom in output filter selection.

The PCM1700 comes in space-saving 28-pin plastic DIP and SOIC packages. PCM1700 accepts a serial data input format that is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.



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# SPECIFICATIONS

## ELECTRICAL

At 25°C, and  $\pm V_{CC} = \pm 5.00V$  unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

PARAMETER	CONDITIONS	PCM1700U/J-U-K, PCM1700P/P-J/P-K			UNITS
		MIN	TYP	MAX	
RESOLUTION		18			Bits
DYNAMIC RANGE			+108		dB
<b>INPUT</b>					
<b>DIGITAL INPUT</b> Logic Family Logic Level: $V_{IH}$ $V_{IL}$ $I_{IH}$ $I_{IL}$ Data Format Input Clock Frequency	$V_{IH} = +2.7V$ $V_{IL} = +0.4V$	+2 0	TTL Compatible  Serial BTC <sup>(1)</sup> 20	$+V_{DD}$ +0.8 +1 -50	V V $\mu A$ $\mu A$ MHz
<b>DYNAMIC CHARACTERISTICS</b>					
<b>TOTAL HARMONIC DISTORTION + N<sup>(6)</sup></b> PCM1700_: f = 991kHz (0dB) f = 991kHz (-20dB) f <sub>IN</sub> = 991kHz (-60dB) PCM1700_-J: f = 991kHz (0dB) f = 991kHz (-20dB) f = 991kHz (-60dB) PCM1700_-K: f = 991kHz (0dB) f = 991kHz (-20dB) f = 991kHz (-60dB)	f <sub>S</sub> = 352.8kHz <sup>(4)</sup> f <sub>S</sub> = 352.8kHz f <sub>S</sub> = 352.8kHz f <sub>S</sub> = 352.8kHz f <sub>S</sub> = 352.8kHz f <sub>S</sub> = 352.8kHz f <sub>S</sub> = 352.8kHz		-88 -74 -34 -94 -76 -36 -98 -80 -40	-82 -68 -28 -88 -74 -34 -92 -74 -34	dB dB dB dB dB dB dB dB dB
CHANNEL SEPARATION		+96	+108		dB
SIGNAL-TO-NOISE RATIO <sup>(5)</sup>	20Hz to 20kHz at BPZ <sup>(6)</sup>		+108		dB
<b>TRANSFER CHARACTERISTICS</b>					
<b>ACCURACY</b> Gain Error Gain Mismatch Bipolar Zero Error BPZ Error Mismatch BPZ Differential Linearity Error <sup>(7)</sup> Gain Drift Bipolar Zero Drift Warm-up Time	Channel to Channel  Channel to Channel		$\pm 1$ $\pm 1$ 10 5 $\pm 1$ 100 20	$\pm 3$ $\pm 3$	% % mV mV LSB ppm/°C ppm of FSR/°C minute
POWER SUPPLY REJECTION	$\pm V_{CC}$ to $V_{OUT}$		+86		dB
<b>ANALOG OUTPUT</b> Voltage: Output Range Output Impedance Current Output Capacitive Load Drive Short Circuit Duration Settling Time Glitch Energy Current: Output Range Output Impedance	R <sub>LOAD</sub> = 1.5k $\Omega$        ( $\pm 2\%$ ) ( $\pm 2\%$ )		$\pm 3$ 0.1 $\pm 2$ TBD Indefinite Meets All THD+N Specs Without External Output Deglitching 1.67		V $\Omega$ mA pF   $\mu A$ k $\Omega$
<b>POWER SUPPLY REQUIREMENTS</b>					
$\pm V_{CC}$ Supply Voltage Supply Current: $+I_{CC}$ $-I_{CC}$ Power Dissipation	$+V_{CC} = +5.0V$ $-V_{CC} = -5.0V$ $\pm V_{CC} = \pm 5.0V$	+4.75	+5.00 +18 -42 280	+5.25 +30 -65 475	V mA mA mW
<b>TEMPERATURE RANGE</b>					
Specification Operating Storage		0 -30 -60		+70 +70 +100	°C °C °C

NOTES: (1) Binary Two's Complement coding. (6) Ratio of (Distortion<sub>RMS</sub> + Noise<sub>eRMS</sub>) / Signal<sub>RMS</sub>. (3) D/A converter input frequency/signal level on both left and right channels. (4) D/A converter sample frequency (8 X 44.1kHz; 8X oversampling per channel). (5) Ratio of Noise<sub>RMS</sub> / Signal<sub>RMS</sub>. Measured using an A-weighted filter. (6) Bipolar zero. (7) Differential non-linearity at bipolar major carry input code. Measured in 16-bit LSBs. Adjustable to zero error.

## PIN ASSIGNMENTS (Plastic PKG)

PIN	DESCRIPTION	MNEMONIC
1	-5V Analog Supply	-V <sub>CC</sub>
2	Left Channel Servo-Amp Decoupling Point	CAP
3	Left Channel MSB Adjustment	MSB ADJ (L)
4	No Connect	NC
5	Left Channel Bipolar Offset Decoupling Point	CAP
6	Left Channel Current Output	I <sub>OUT</sub> (L)
7	Left Channel Analog Common	ACOM
8	Left Channel Summing Junction	SJ (L)
9	Left Channel Voltage Output	VO <sub>UT</sub> (L)
10	No Connect	NC
11	+5V Digital Supply	+V <sub>DD</sub>
12	Left Channel Data Input	DATA
13	Clock Input	CLOCK
14	-5V Logic Supply	-V <sub>DD</sub>
15	Latch Enable Input	LE
16	Right Channel Data Input	DATA (R)
17	Digital Common	DCOM
18	No Connect	NC
19	Right Channel Voltage Output	VO <sub>UT</sub> (R)
20	Right Channel Summing Junction	SJ (R)
21	Right Channel Analog Common	ACOM
22	Right Channel Current Output	I <sub>OUT</sub> (R)
23	Right Channel Bipolar Offset Decoupling Point	CAP
24	Right Channel MSB Adjustment	MSB ADJ (R)
25	Right Channel Servo-Amp Decoupling Point	CAP
26	MSB Adjustment Potentiometer Voltage Output	VPOT
27	+5V Analog Supply	+V <sub>CC</sub>
28	Digital Common	DCOM

## PIN ASSIGNMENTS (SOIC PKG)

PIN	DESCRIPTION	MNEMONIC
9	-5V Analog Supply	-V <sub>CC</sub>
10	Left Channel Servo-Amp Decoupling Point	CAP
11	Left Channel MSB Adjustment	MSB ADJ (L)
19	No Connect	NC
12	Left Channel Bipolar Offset Decoupling Point	CAP
13	Left Channel Current Output	I <sub>OUT</sub> (L)
14	Left Channel Analog Common	ACOM
15	Left Channel Summing Junction	SJ (L)
16	Left Channel Voltage Output	VO <sub>UT</sub> (L)
17	No Connect	NC
18	+5V Digital Supply	+V <sub>DD</sub>
20	Left Channel Data Input	DATA
21	Clock Input	CLOCK
22	-5V Logic Supply	-V <sub>DD</sub>
23	Latch Enable Input	LE
24	Right Channel Data Input	DATA (R)
25	Digital Common	DCOM
26	No Connect	NC
27	Right Channel Voltage Output	VO <sub>UT</sub> (R)
28	Right Channel Summing Junction	SJ (R)
1	Right Channel Analog Common	ACOM
2	Right Channel Current Output	I <sub>OUT</sub> (R)
3	Right Channel Bipolar Offset Decoupling Point	CAP
4	Right Channel MSB Adjustment	MSB ADJ (R)
5	Right Channel Servo-Amp Decoupling Point	CAP
6	MSB Adjustment Potentiometer Voltage Output	V <sub>POT</sub>
7	+5V Analog Supply	+V <sub>CC</sub>
8	Digital Common	DCOM

NOTE: In the SOIC (PCM1700U) package, the die is rotated 90°. Therefore, the pin assignments are different from the DIP. See pin assignments on page 4 for details.

## ORDERING INFORMATION

Basic Model Number _____	PCM1700 ( ) ( )
P: Plastic U: SOIC _____	
Performance Grade Code _____	

## ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages .....	±7.5VDC
Input Logic Voltage .....	-1V to +V <sub>CC</sub>
Power Dissipation .....	500mW
Operating Temperature .....	-25°C to +70°C
Storage Temperature .....	-60°C to +100°C
Lead Temperature (soldering, 10s) .....	+300°C

## PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
PCM1700U	28-Pin SOIC	217
PCM1700U-J	28-Pin SOIC	217
PCM1700U-K	28-Pin SOIC	217
PCM1700P	28-Pin Plastic DIP	126
PCM1700P-J	28-Pin Plastic DIP	126
PCM1700P-K	28-Pin Plastic DIP	126

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

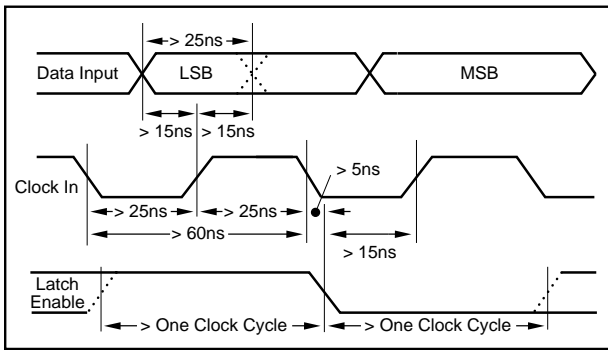


FIGURE 1. PCM1700P Setup and Hold Timing Diagram.

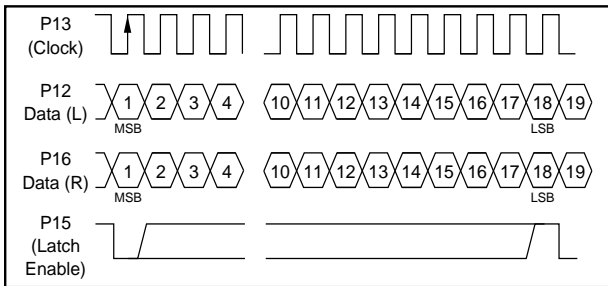


FIGURE 2. Timing Diagram.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V <sub>OUT</sub> Mode	Current (mA) I <sub>OUT</sub> Mode
1FFFF Hex	+ FS	+2.99997711	-0.66999489
00000 Hex	BPZ	0.00000000	0.00000000
3FFFF Hex	BPZ - 1LSB	-0.00002289	+0.00000511
20000 Hex	- FS	-3.00000000	+0.67000000

TABLE I. PCM1700 Input/Output Relationships.

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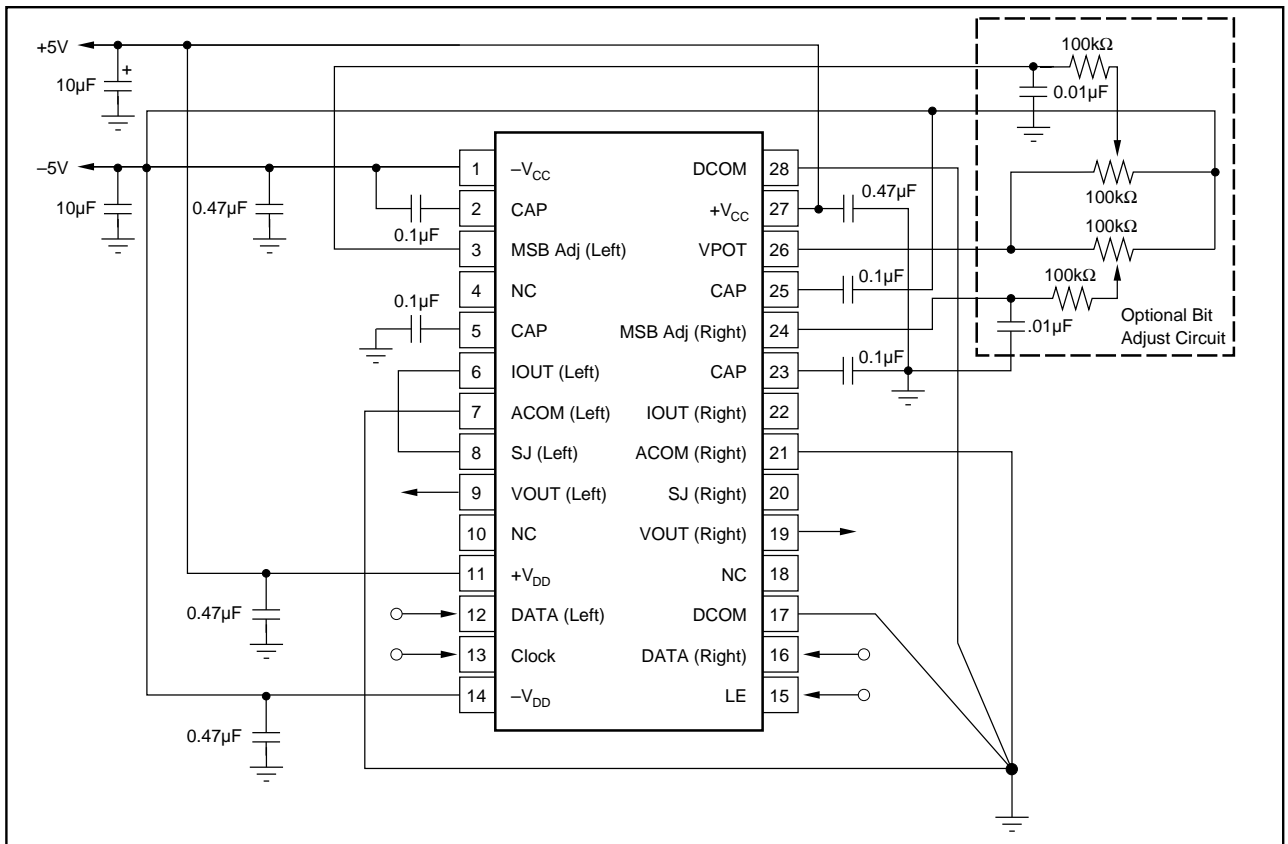


FIGURE 3. Voltage Output Connection Diagram (DIP Package Diagram.)

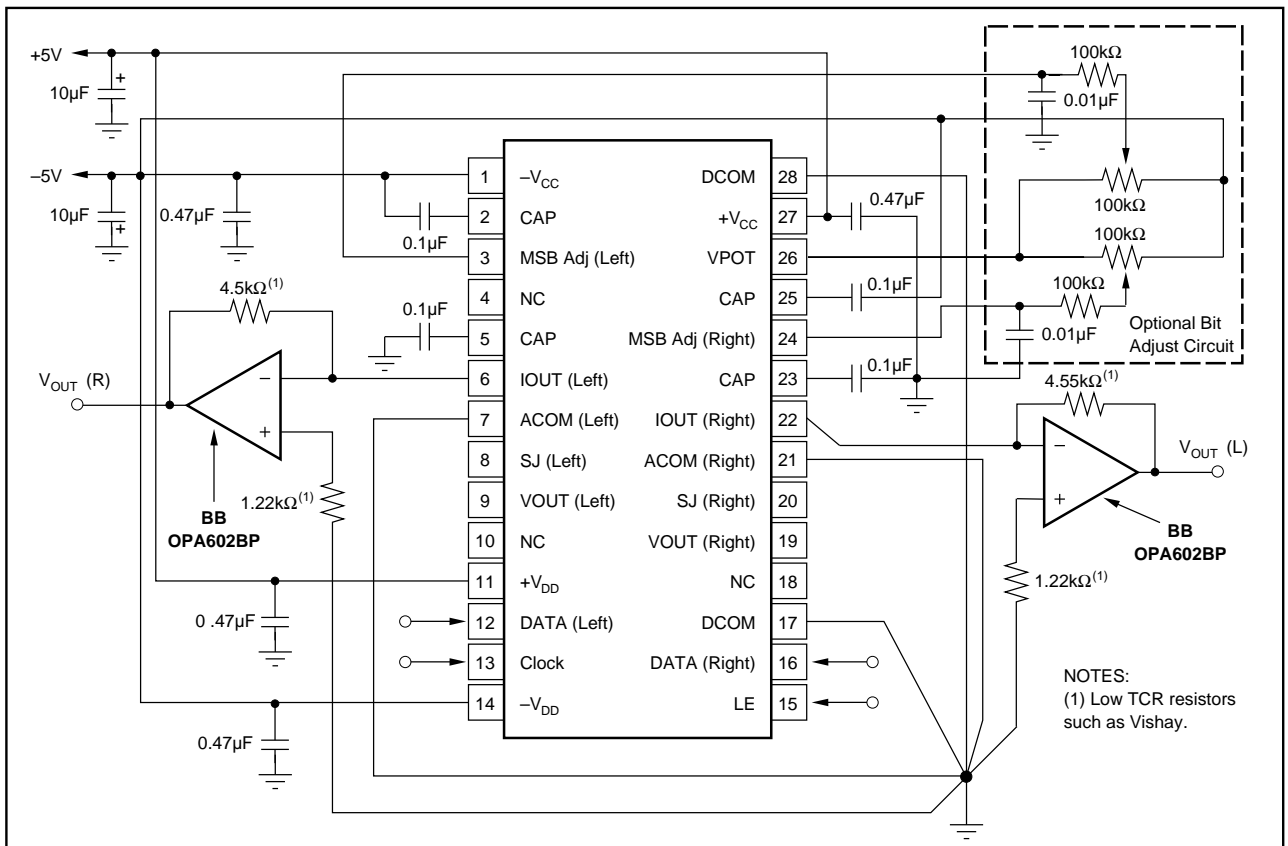


FIGURE 4. Current Output Connection Diagram (DIP Package Diagram.)