



# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted).

V <sub>CC</sub> .....	-0.3V to +14V
GATE* .....	-0.3V to +20V
All Other Pins .....	-0.3V to the lower of (V <sub>CC</sub> + 0.3V) and +14V
SC_DET Current (200ms pulse width, 15% duty cycle) ...	140mA
Continuous Current (all other pins) .....	20mA

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

10-Pin μMAX (derate 6.9mW/°C above +70°C) .....	556mW
16-Pin QSOP (derate 18.9mW/°C above +70°C) .....	1509mW
Operating Temperature Range .....	-40°C to +85°C
Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10s) .....	+300°C

\*GATE is internally driven and clamped. Do not drive GATE with external source.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub>, EN (MAX5924/MAX5925), EN1 (MAX5926) = +2.25V to +13.2V;  $\overline{\text{EN}}2$  (MAX5926) = 0V; V<sub>S</sub> (see Figure 1) = +1.05V to V<sub>CC</sub>; T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = 5V, R<sub>L</sub> = 500Ω from OUT to GND, C<sub>L</sub> = 100μF, SLEW = open, T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>POWER SUPPLIES</b>							
V <sub>CC</sub> Operating Range	V <sub>CC</sub>		2.25		13.20	V	
V <sub>S</sub> Operating Range	V <sub>S</sub>	V <sub>S</sub> as defined in Figure 1	1.05		V <sub>CC</sub>	V	
Supply Current	I <sub>CC</sub>	FET on, SC_DET = V <sub>CC</sub>		1.5	2.5	mA	
<b>UNDERVOLTAGE LOCKOUT (UVLO)</b>							
UVLO Threshold	V <sub>UVLO</sub>	Default value, V <sub>S</sub> and V <sub>CC</sub> increasing, Figure 1	1.86	2.06	2.25	V	
V <sub>CC</sub> UVLO Deglitch Time	t <sub>DG</sub>	(Note 2)		900		μs	
V <sub>CC</sub> UVLO Startup Delay	t <sub>D,UVLO</sub>		123	277	350	ms	
<b>LOAD-PROBE</b>							
Load-Probe Resistance (Note 3)	R <sub>LP</sub>	2.25V < V <sub>CC</sub> < 5V	4	30	65	Ω	
		5V < V <sub>CC</sub> < 13.2V	3	10	20		
Load-Probe Timeout	t <sub>LP</sub>		61	102	163	ms	
Load-Probe Threshold Voltage	V <sub>LP,TH</sub>	(Note 4)	180	200	220	mV	
<b>CIRCUIT BREAKER</b>							
Circuit-Breaker Programming Current	I <sub>CB</sub>	TC = high (MAX5926), MAX5924	35	37	42	μA	
	I <sub>CB25</sub>	TC = low (MAX5926), MAX5925 (Note 5)	V <sub>CC</sub> = 2.25V, T <sub>A</sub> = +25°C	44	51		58
			5V ≤ V <sub>CC</sub> ≤ 13.2V, T <sub>A</sub> = +25°C	49	54		58
	I <sub>CB85</sub>	TC = low (MAX5926), MAX5925 (Note 5)	V <sub>CC</sub> = 2.25V, T <sub>A</sub> = +85°C	47	52		60
5V ≤ V <sub>CC</sub> ≤ 13.2V, T <sub>A</sub> = +85°C			58	63	70		
Circuit-Breaker Programming Current During Startup (No R <sub>SENSE</sub> )	I <sub>CB,SU</sub>		2 × I <sub>CB</sub>			μA	
Circuit-Breaker Enable Threshold (No R <sub>SENSE</sub> )	V <sub>CB,EN</sub>	V <sub>GATE</sub> - V <sub>OUT</sub> , rising gate voltage (Note 6)	4.0			V	

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MAX5924/MAX5925/MAX5926

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC}$ , EN (MAX5924/MAX5925), EN1 (MAX5926) = +2.25V to +13.2V;  $\overline{EN2}$  (MAX5926) = 0V;  $V_S$  (see Figure 1) = +1.05V to  $V_{CC}$ ;  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at  $V_{CC}$  = 5V,  $R_L$  = 500Ω from OUT to GND,  $C_L$  = 100μF, SLEW = open,  $T_A$  = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Circuit-Breaker Comparator Offset Voltage	$V_{CB\_OS}$			0.3	±4.7	mV	
Fast Circuit-Breaker Offset Resistor	$R_{CBF}$	Figure 3	1.2	1.9	2.5	kΩ	
Slow Circuit-Breaker Delay	$t_{CBS}$	$V_{CB} - V_{SENSE} = 10mV$	0.95	1.6	2.80	ms	
Fast Circuit-Breaker Delay	$t_{CBF}$	$V_{CB} - V_{SENSE} = 500mV$		280		ns	
Circuit-Breaker Trip Gate Pulldown Current	$I_{GATE,PD}$	$V_{GATE} = 2.5V$ , $V_{CC} = 13.2V$	20	27		mA	
Circuit-Breaker Temperature Coefficient	$TC_{ICB}$	MAX5924, TC = high (MAX5926)		0		ppm/°C	
		MAX5925, TC = low (MAX5926)		3300			
<b>MOSFET DRIVER</b>							
External Gate Drive	$V_{GS}$	$V_{GATE} - V_{OUT}$	$2.25V \leq V_{CC} \leq 12.6V$	3.46	4.91	6.70	V
			$V_{CC} = 13.2V$ (Note 7)	3.33	5	6.70	
Load Voltage Slew Rate	SR	SLEW = open, $C_{GATE} = 10nF$	2.19	9.5	16.00	V/ms	
		SLEW = 300nF, $C_{GATE} = 10nF$ (Note 8)	0.44	0.84	1.18		
Gate Pullup Current Capacity	$I_{GATE}$	$V_{GATE} = 0V$	239			μA	
<b>ENABLE COMPARATOR</b>							
EN, EN1 Reference Threshold	$V_{EN/UVLO}$	$V_{EN}$ (MAX5924/MAX5925) or $V_{EN1}$ (MAX5926) rising	0.755	0.795	0.836	V	
EN, EN1 Hysteresis	$V_{EN,HYS}$			30		mV	
EN, EN1 Input Bias Current	$I_{EN}$	EN (MAX5924/MAX5925) = $V_{CC}$ , EN1 (MAX5926) = $V_{CC}$		±8	±50	nA	
<b>DIGITAL OUTPUTS (PGOOD, PGOOD)</b>							
Power-Good Output Low Voltage	$V_{OL}$	$I_{OL} = 1mA$		0.3	0.4	V	
Power-Good Output Open-Drain Leakage Current	$I_{OH}$	$PGOOD/\overline{PGOOD} = 13.2V$		0.2	1	μA	
Power-Good Trip Point (% of $V_{GS}$ )	$V_{THPGOOD}$	$V_{GATE} - V_{OUT}$ , rising gate voltage	50	70	99	%	
Power-Good Hysteresis	$V_{PG,HYS}$			0.36		V	
<b>LOGIC AND TIMING (TC, LATCH (MAX5926), EN2 (MAX5926))</b>							
Autoretry Delay	$t_{RETRY}$	Autoretry mode	1.0	1.6	2.6	s	
Input Voltage	$V_{IH}$		2.0			V	
	$V_{IL}$				0.4		
Input Bias Current	$I_{BIAS}$	Logic high at 13.2V		3		μA	

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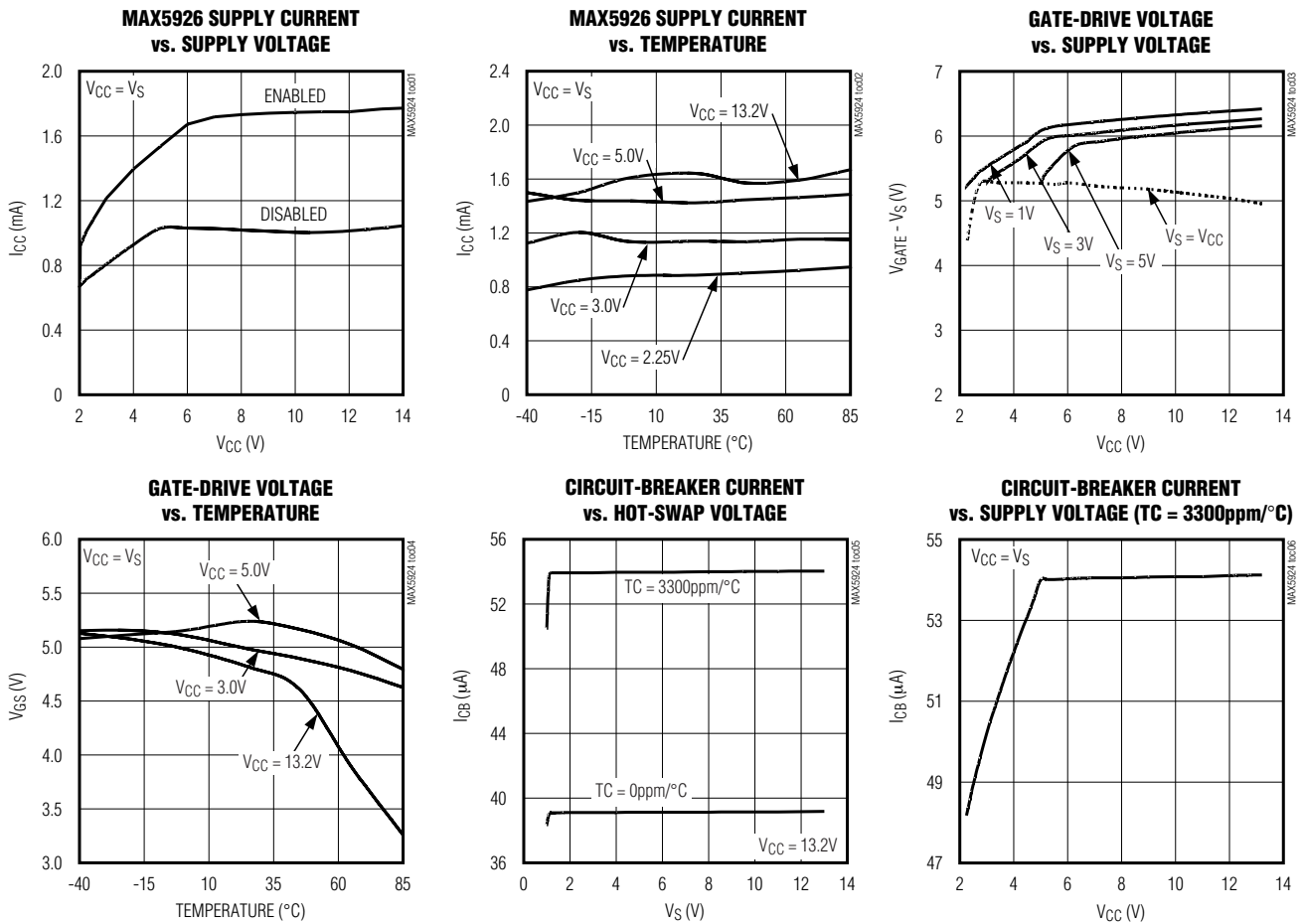
## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC}$ , EN (MAX5924/MAX5925), EN1 (MAX5926) = +2.25V to +13.2V;  $\overline{EN2}$  (MAX5926) = 0V;  $V_S$  (see Figure 1) = +1.05V to  $V_{CC}$ ;  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at  $V_{CC}$  = 5V,  $R_L$  = 500Ω from OUT to GND,  $C_L$  = 100μF, SLEW = open,  $T_A$  = +25°C, unless otherwise noted.) (Note 1)

- Note 1:** All devices are 100% tested at  $T_A$  = +25°C and +85°C. All temperature limits at -40°C are guaranteed by design.
- Note 2:**  $V_{CC}$  drops 30% below the undervoltage lockout voltage during  $t_{DG}$  are ignored.
- Note 3:**  $R_{LP}$  is the resistance measured between  $V_{CC}$  and SC\_DET during the load-probing phase,  $t_{LP}$ .
- Note 4:** Guaranteed by design.
- Note 5:** The circuit-breaker programming current increases linearly from  $V_{CC}$  = 2.25V to 5V. See the Circuit-Breaker Current vs. Supply Voltage graph in the *Typical Operating Characteristics*.
- Note 6:** See the *Startup Mode* section for more information.
- Note 7:**  $V_{GATE}$  is clamped to 17V (typ) above ground.
- Note 8:**  $dv/dt$  =  $330 \times 10^{-9}/C_{SLEW}$  (V/ms), nMOS device used for measurement was IRF9530N. Slew rate is measured at the load.

## Typical Operating Characteristics

( $V_{CC}$  = 5V,  $C_L$  = 100μF,  $C_{SLEW}$  = 330nF,  $C_{GATE}$  = 10nF,  $R_L$  = 500Ω, Figure 1,  $T_A$  = +25°C, unless otherwise noted.)

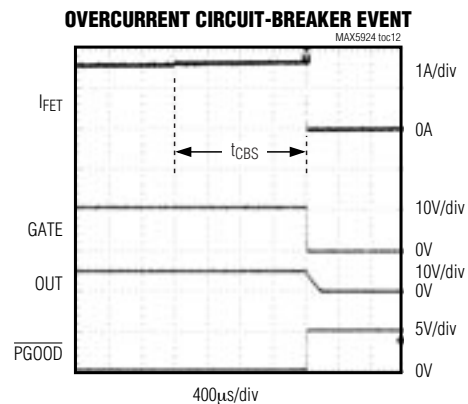
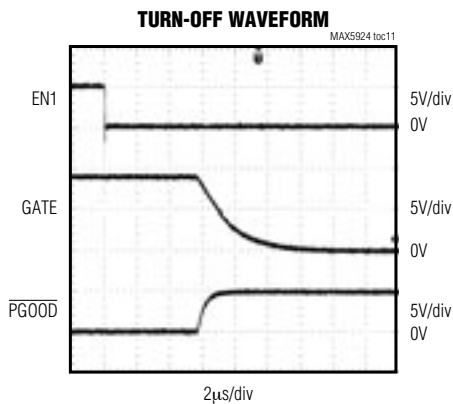
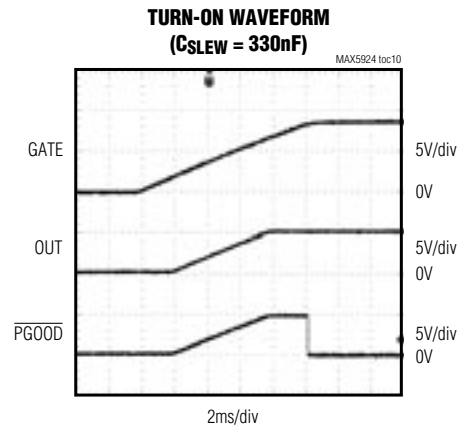
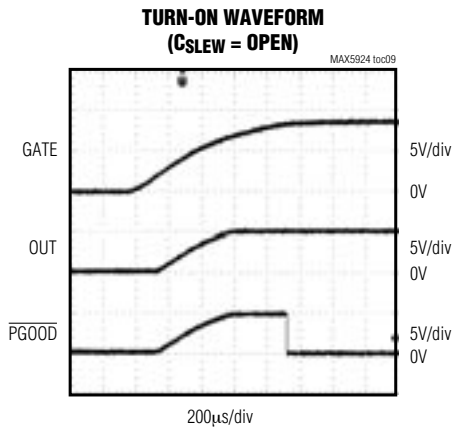
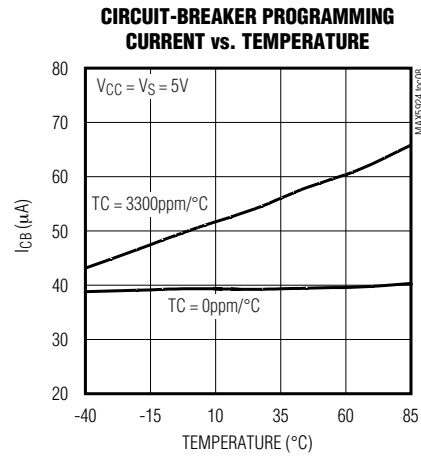
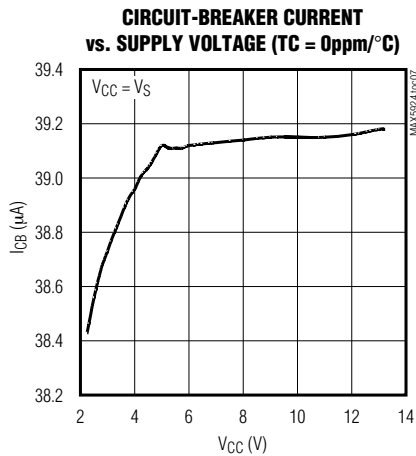


# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

## Typical Operating Characteristics (continued)

( $V_{CC} = 5V$ ,  $C_L = 100\mu F$ ,  $C_{SLEW} = 330nF$ ,  $C_{GATE} = 10nF$ ,  $R_L = 500\Omega$ , Figure 1,  $T_A = +25^\circ C$ , unless otherwise noted.)

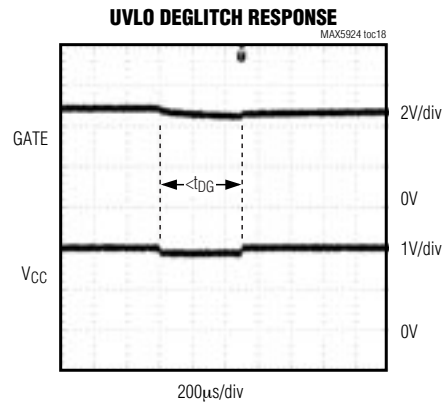
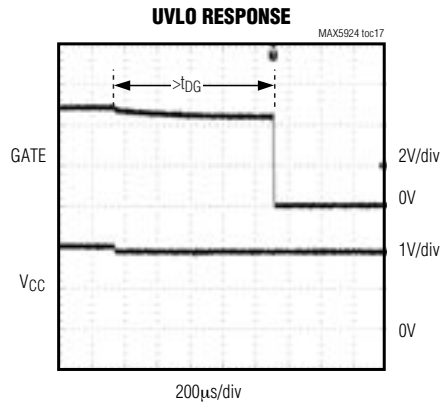
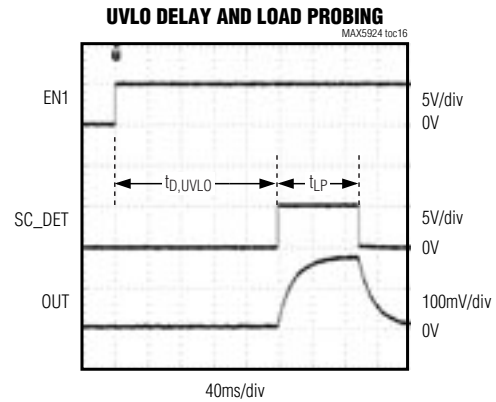
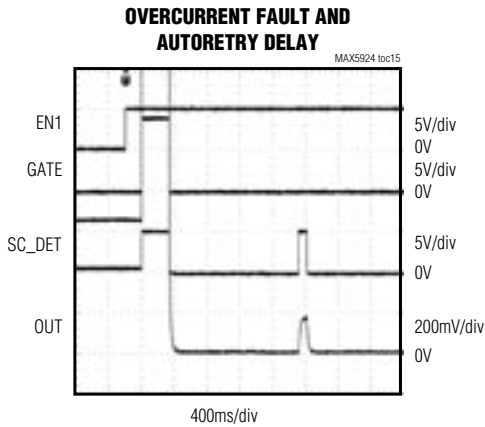
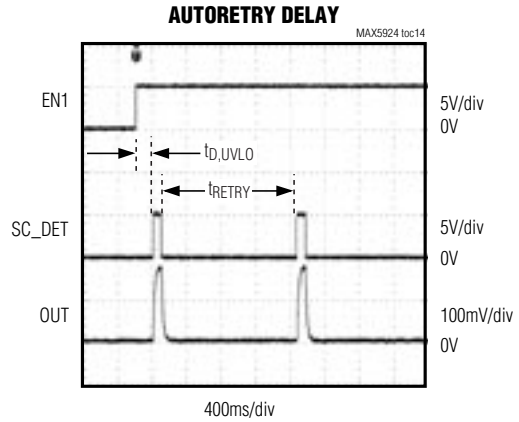
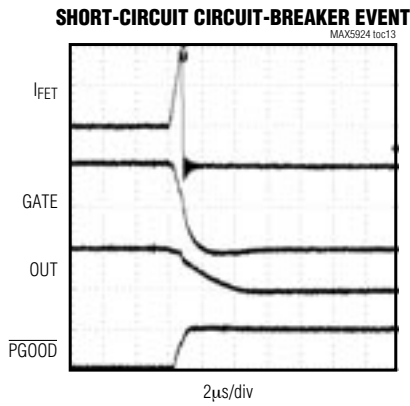
MAX5924/MAX5925/MAX5926



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## Typical Operating Characteristics (continued)

( $V_{CC} = 5V$ ,  $C_L = 100\mu F$ ,  $C_{SLEW} = 330nF$ ,  $C_{GATE} = 10nF$ ,  $R_L = 500\Omega$ , Figure 1,  $T_A = +25^\circ C$ , unless otherwise noted.)



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## Pin Description

MAX5924/MAX5925/MAX5926

PIN			NAME	FUNCTION
MAX5924A/ MAX5924C/ MAX5925A/ MAX5925C	MAX5924B/ MAX5924D/ MAX5925B/ MAX5925D	MAX5926		
1	1	1	V <sub>CC</sub>	Power-Supply Input. Connect V <sub>CC</sub> to a voltage between 2.25V and 13.2V. <b>V<sub>CC</sub> must always be equal to or greater than V<sub>S</sub></b> (see Figure 1).
2	2	2	SC_DET	Short-Circuit Detection Output. SC_DET forces current into the external load through a series resistor, R <sub>SC</sub> , at startup to determine whether there is a short circuit (load probing). Select R <sub>SC</sub> based on the desired slow-comparator trip current (see the <i>Selecting a Circuit-Breaker Threshold</i> section). Connect SC_DET to V <sub>CC</sub> when using R <sub>SENSE</sub> , or to disable load probing when it is not desired.
3	3	—	EN	ON/OFF Control Input. Drive EN high to enable the device. Drive EN low to disable the device. An optional external resistive-divider connected between V <sub>CC</sub> , EN, and GND sets the programmable turn-on voltage.
4	—	4	$\overline{\text{PGOOD}}$	Open-Drain Active-Low Power-Good Output
—	4	7	PGOOD	Open-Drain Active-High Power-Good Output
5	5	5	GND	Ground
6	6	12	SLEW	Slew-Rate Adjustment Input. Connect an external capacitor between SLEW and GND to adjust the gate slew rate. Leave SLEW unconnected for the default slew rate.
7	7	13	GATE	Gate-Drive Output. Connect GATE to the gate of the external n-channel MOSFET.
8	8	14	OUT	Output Voltage. Connect OUT to the source of the external MOSFET.
9	9	15	SENSE	Circuit-Breaker Sense Input. Connect SENSE to OUT when not using an external R <sub>SENSE</sub> (Figure 1). Connect SENSE to the drain of the external MOSFET when using an external R <sub>SENSE</sub> (Figure 2).
10	10	16	CB	Circuit-Breaker Threshold Input. Connect an external resistor, R <sub>CB</sub> , from CB to V <sub>S</sub> to set the circuit-breaker threshold voltage.
—	—	3	EN1	Active-High ON/OFF Control Input. Drive EN1 high to enable the device when $\overline{\text{EN2}}$ is low. Drive EN1 low to disable the device, regardless of the state of $\overline{\text{EN2}}$ . An optional external resistive-divider between V <sub>CC</sub> , EN1, and GND sets the programmable turn-on voltage while $\overline{\text{EN2}}$ is low.
—	—	6	$\overline{\text{EN2}}$	Active-Low ON/OFF Control Input. Drive $\overline{\text{EN2}}$ low to enable the device when EN1 is high. Drive $\overline{\text{EN2}}$ high to disable the device, regardless of the state of EN1.
—	—	8	LATCH	Latch Mode Input. Drive LATCH low for autoretry mode. Drive LATCH high for latched mode.
—	—	9	TC	Circuit-Breaker Temperature Coefficient Selection Input. Drive TC low to select a 3300ppm/°C temperature coefficient. Drive TC high to select a 0ppm/°C temperature coefficient.
—	—	10, 11	N.C.	No Connection. Not internally connected.
—	—	EP	EP	Exposed Pad. Connect EP to GND.

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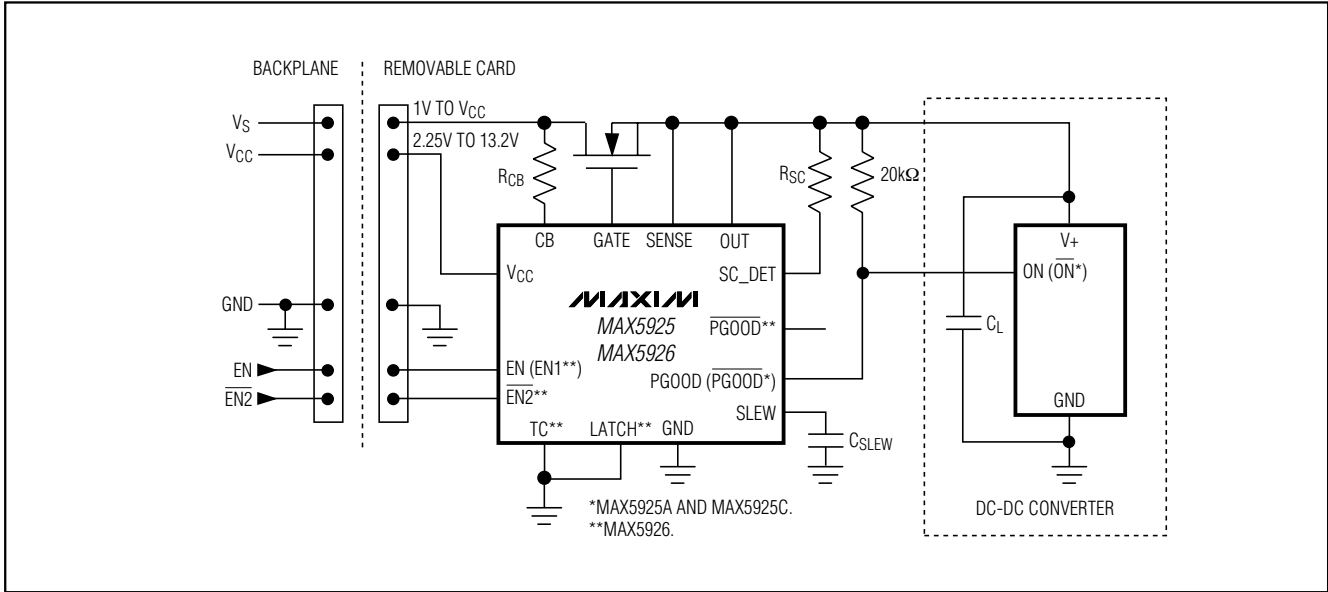


Figure 1. Typical Operating Circuit (Without RSENSE)

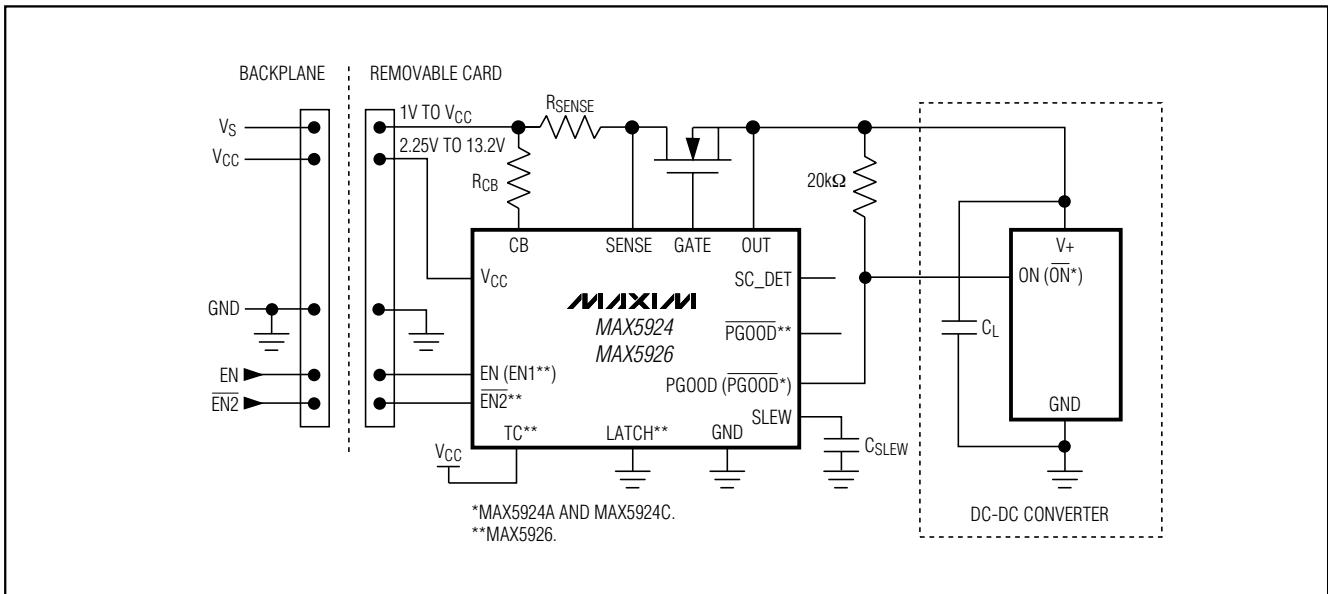


Figure 2. Typical Operating Circuit (With RSENSE)



# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

MAX5924/MAX5925/MAX5926

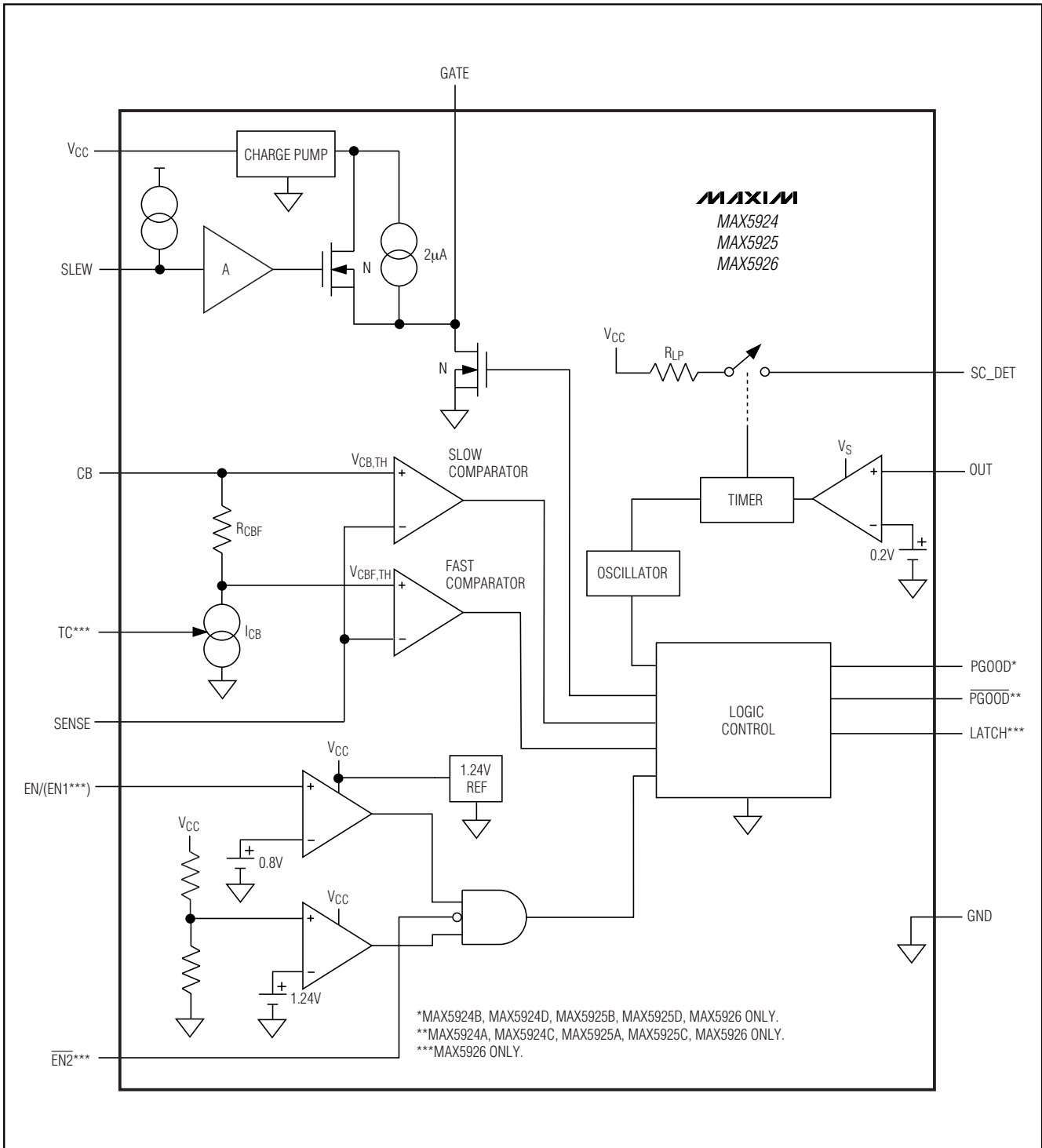


Figure 3. Functional Diagram

# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

## Detailed Description

The MAX5924/MAX5925/MAX5926 are hot-swap controller ICs designed for applications where a line card is inserted into a live backplane. Normally, when a line card is plugged into a live backplane, the card's discharged filter capacitors provide a low impedance that can momentarily cause the main power supply to collapse. The MAX5924/MAX5925/MAX5926 are designed to reside either in the backplane or in the removable card to provide inrush current limiting and short-circuit protection. This is achieved using an external n-channel MOSFET and an optional external current-sense resistor.

Several critical parameters can be programmed:

- Slew rate (inrush current)
- Circuit-breaker threshold
- Turn-on voltage
- Fault-management mode (MAX5926)
- Circuit-breaker temperature coefficient (MAX5926)

See the *Selector Guide* for a device-specific list of factory-preset features and parameters.

### Startup Mode

The MAX5924/MAX5925/MAX5926 control an external MOSFET connected in series with the hot-swapped power supply,  $V_S$ . These devices hold the external MOSFET off while the supply voltage,  $V_{CC}$ , is below the undervoltage lockout threshold or when the device is disabled (see the *EN (MAX5924/MAX5925, EN1/EN2 (MAX5926))* section). When  $V_{CC}$  rises above  $V_{UVLO}$  and the MAX5924/MAX5925/MAX5926 are enabled, an undervoltage lockout timer initiates.  $V_{CC}$  must remain greater than  $V_{UVLO}$  for  $t_{D,UVLO}$  to enter startup.

During the first stage of startup, the MAX5924/MAX5925/MAX5926 detect whether an external sense resistor is present and autoconfigure accordingly (Figure 4). Bilevel fault protection temporarily disables, and load-probing circuitry enables, if no sense resistor is detected (see the *Load Probing* section). During load probing, if  $V_{OUT}$  does not rise above  $V_{LP,TH}$  within  $t_{LP}$ , the device manages the fault according to the selected fault-management mode (see the *Latched and Autoretry Fault Management* section). If  $V_{OUT}$  rises above  $V_{LP,TH}$  within  $t_{LP}$ , the MAX5924/MAX5925/MAX5926 begin startup (Figure 5). If an external  $R_{SENSE}$  is detected, load probing is bypassed and bilevel fault protection enables with a startup circuit-breaker programming current of  $I_{CB,SU} = 2 \times I_{CB}$  to accommodate the higher-than-normal inrush current required to charge board capacitance,  $C_L$ .

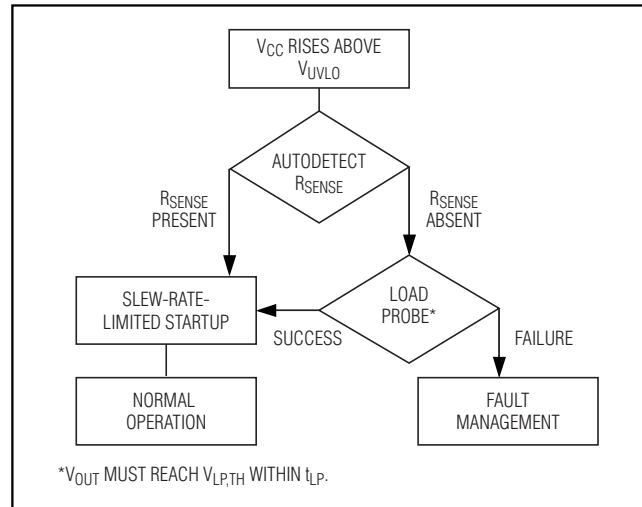


Figure 4. Startup Flow Chart

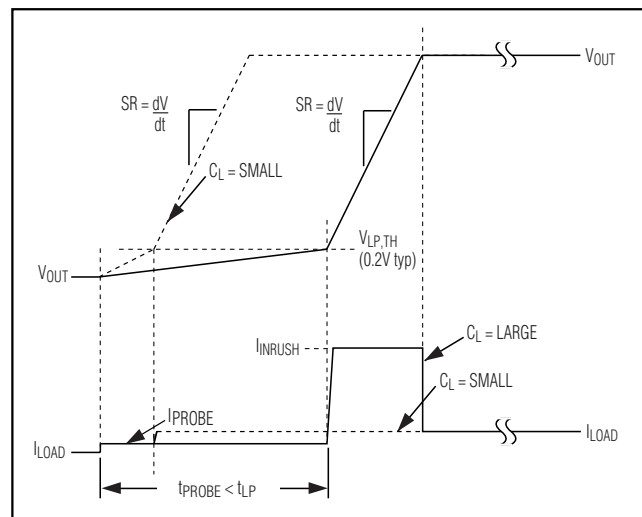


Figure 5. Startup Waveform

During startup, the MAX5924/MAX5925/MAX5926 gradually turn on the MOSFET, and  $V_{OUT}$  rises at a rate determined by the selected slew rate,  $SR$  (see the *Slew Rate* section). The inrush current,  $I_{INRUSH}$ , is limited to a level proportional to the load capacitance,  $C_L$ , and  $SR$ :

$$I_{INRUSH(A)} = C_L \times 1000 \times SR$$

where  $SR$  is in  $V/ms$  and  $C_L$  is the load capacitance in Farads. For operation with and without  $R_{SENSE}$ , once  $V_{GS}$  exceeds  $V_{CB,EN}$ ,  $PGOOD$  and/or  $PGOOD$  assert and the MAX5924/MAX5925/MAX5926 enable standard bilevel fault protection (see the *Bilevel Fault Protection* section).

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## Load Probing

The MAX5924/MAX5925/MAX5926 load-probing circuitry detects short-circuit conditions during startup. As the device begins load probing, SC\_DET is connected to VCC through an internal switch with an on-resistance of RLP (Figure 6). VCC then charges the load with a probe current:

$$I_{PROBE} = (V_{CC} - V_{OUT}) / (R_{LP} + R_{SC}) \quad (\text{Figure 1})$$

If the load voltage does not reach  $V_{LP,TH}$  (0.2V, typ) within  $t_{LP}$ , a short-circuit fault is detected and the channel is turned off according to the selected fault-management mode (see the *Fault Management* section and Figure 5). PGOOD/PGOOD asserts at the end of the startup period, tSTART, if no fault condition is present (see the Turn-On Waveforms in the *Typical Operating Characteristics*).

## Normal Operation

In normal operation, after startup is complete, protection is provided by turning off the external MOSFET when a fault condition is encountered. Dual-speed/bilevel fault protection incorporates two comparators with different thresholds and response times to monitor the current:

- 1) Slow comparator. This comparator has a 1.6ms (typ) response time. The slow comparator ignores low-amplitude momentary current glitches. After an extended overcurrent condition, a fault is acknowledged and the MOSFET gate is discharged.
- 2) Fast comparator. This comparator has a fixed response time and a higher threshold voltage. The fast comparator turns off the MOSFET immediately

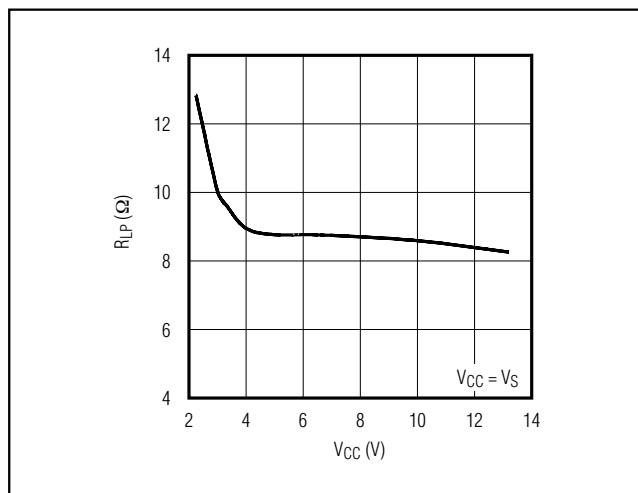


Figure 6. Load-Probe Resistance vs. Supply Voltage

after it detects a large amplitude event such as a short circuit.

In each case, when a fault is encountered, the power-good output deasserts and the device drives GATE low. After a fault, the MAX5924A, MAX5924B, MAX5925A, and MAX5925B latch GATE low and the MAX5924C, MAX5924D, MAX5925C, and MAX5925D enter the autoretry mode. The MAX5926 has selectable latched or autoretry modes. Figure 7 shows the slow comparator response to an overcurrent fault.

## Bilevel Fault Protection

### Bilevel Fault Protection in Startup Mode

Bilevel fault protection is disabled during startup when no RSENSE is detected. The device enables bilevel fault protection when RSENSE is detected, but the overcurrent trip levels are higher than normal during startup because  $I_{CB,SU} = 2 \times I_{CB}$  (see the *Startup Mode* section).

### Slow Comparator

The slow comparator is disabled during startup while the external MOSFET turns on. This allows the MAX5924/MAX5925/MAX5926 to ignore higher than normal inrush currents charging the board capacitors when a card is first plugged in.

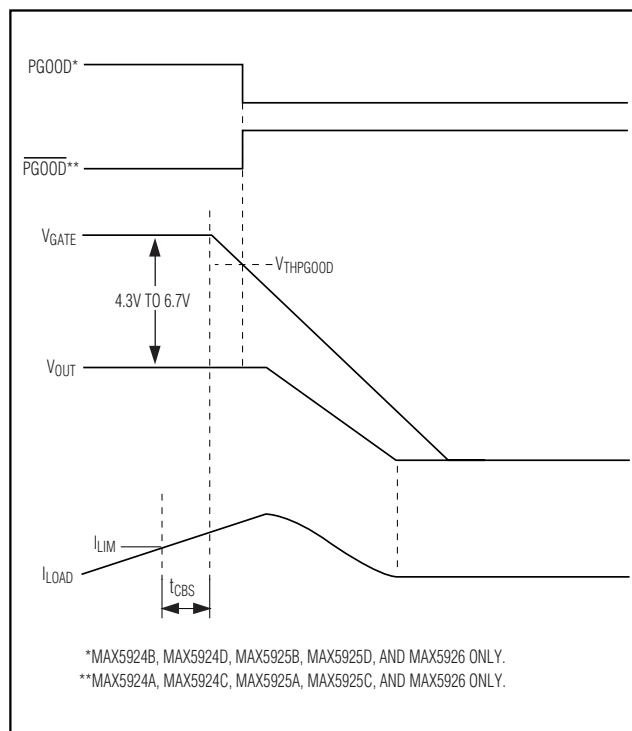


Figure 7. Slow Comparator Response to an Overcurrent Fault

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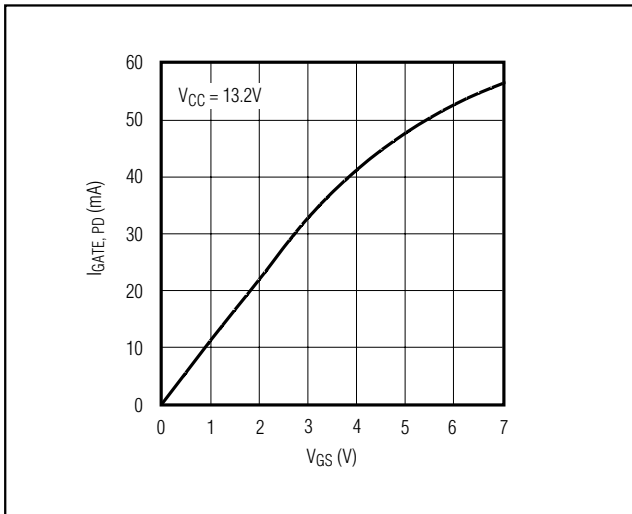


Figure 8a. Gate Discharge Current vs. MOSFET Gate-to-Source Voltage

If the slow comparator detects an overload condition while in normal operation (after startup is complete), it turns off the external MOSFET by discharging the gate capacitance with  $I_{GATE,PD}$ . The magnitude of  $I_{GATE,PD}$  depends on the external MOSFET gate-to-source voltage,  $V_{GS}$ . The discharge current is strongest immediately following a fault and decreases as the MOSFET gate is discharged (Figure 8a).

### Fast Comparator

The fast comparator is used for serious current overloads or short circuits. If the load current reaches the fast comparator threshold, the device quickly forces the MOSFET off. The fast comparator has a response time of 280ns, and discharges GATE with  $I_{GATE,PD}$  (Figure 8a).

### Latched and Autoretry Fault Management

The MAX5924A, MAX5924B, MAX5925A, and MAX5925B latch the external MOSFET off when an overcurrent fault is detected. Following an overcurrent fault, the MAX5924C, MAX5924D, MAX5925C, and MAX5925D enter autoretry mode. The MAX5926 can be configured for either latched or autoretry mode (see Table 1).

In autoretry, a fault turns the external MOSFET off then automatically restarts the device after the autoretry delay,  $t_{RETRY}$ . During the autoretry delay, pull EN or EN1 low to restart the device. In latched mode, pull EN or EN1 low for at least 100 $\mu$ s to clear a latched fault and restart the device.

Table 1. Selecting Fault Management Mode (MAX5926)

LATCH	FAULT MANAGEMENT
Low	Autoretry mode
High	Latched mode

### Power-Good Outputs

The power-good output(s) are open-drain output(s) that deassert:

- When  $V_{CC} < V_{UVLO}$
- During  $t_{D,UVLO}$
- When  $V_{GS} < V_{THPGOOD}$
- During load probing
- When disabled (EN = GND (MAX5924/MAX5925), EN1 = GND or EN2 = high (MAX5926))
- During fault management
- During  $t_{RETRY}$  or when latched off (MAX5924A, MAX5924B, MAX5925A, MAX5925B, or MAX5926 (LATCH = low)).

$\overline{PGOOD}/\overline{PGOOD}$  asserts only if the part is in normal mode and no faults are present.

### Undervoltage Lockout (UVLO)

UVLO circuitry prevents the MAX5924/MAX5925/MAX5926 from turning on the external MOSFET until  $V_{CC}$  exceeds the UVLO threshold,  $V_{UVLO}$ , for  $t_{D,UVLO}$ . UVLO protects the external MOSFET from insufficient gate-drive voltage, and  $t_{D,UVLO}$  ensures that the board is fully plugged into the backplane and  $V_{CC}$  is stable prior to powering the hot-swapped system. Any input voltage transient at  $V_{CC}$  below the UVLO threshold for more than the UVLO deglitch period,  $t_{DG}$ , resets the device and initiates a startup sequence. Device operation is protected from momentary input-voltage steps extending below the UVLO threshold for a deglitch period,  $t_{DG}$ . However, the power-good output(s) may momentarily deassert if the magnitude of a negative step in  $V_{CC}$  exceeds approximately 0.5V, and  $V_{CC}$  drops below  $V_{UVLO}$ . Operation is unaffected and the power-good output(s) assert(s) within 200 $\mu$ s as shown in Figure 8b. This figure also shows that if the UVLO condition exceeds  $t_{DG} = 900\mu$ s (typ), the power-good output(s) again deassert(s) and the load is disconnected.

# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

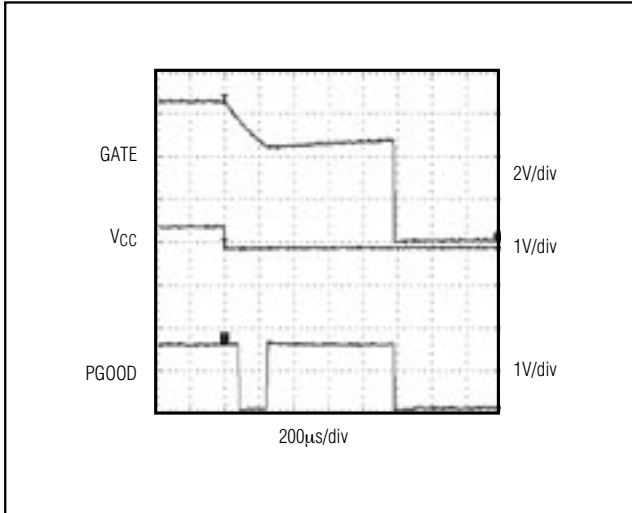


Figure 8b. PGOOD Behavior with Large Negative Input-Voltage Step when  $V_S$  is Near  $V_{S(MIN)}$

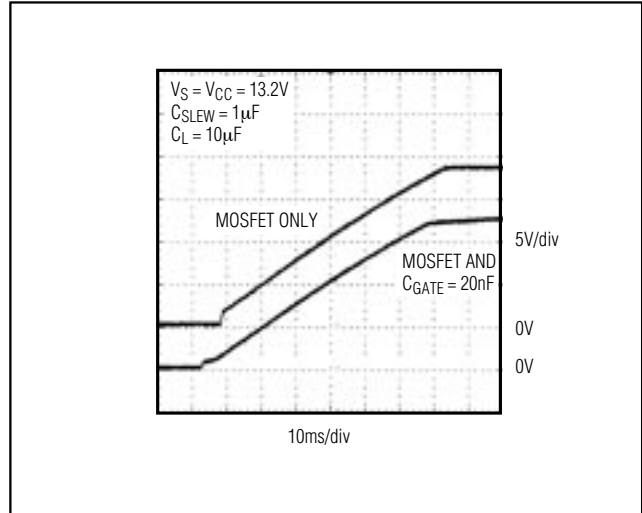


Figure 9. Impact of  $C_{GATE}$  on the  $V_{GATE}$  Waveform

## Determining Inrush Current

Determining a circuit's inrush current is necessary to choose a proper MOSFET. The MAX5924/MAX5925/MAX5926 regulate the inrush current by controlling the output-voltage slew rate, but inrush current is also a function of load capacitance. Determine an anticipated inrush current using the following equation:

$$I_{INRUSH}(A) = C_L \frac{dV_{OUT}}{dt} = C_L \times SR \times 1000$$

where  $C_L$  is the load capacitance in Farads, and  $SR$  is the selected MAX5924/MAX5925/MAX5926 output slew rate in V/ms. For example, assuming a load capacitance of  $100\mu F$  and using the value of  $SR = 10V/ms$ , the anticipated inrush current is 1A. If a  $16V/ms$  output slew rate is used, the inrush current increases to 1.6A. Choose  $SR$  so the maximum anticipated inrush current does not trip the fast circuit-breaker comparator during startup.

## Slew Rate

The MAX5924/MAX5925/MAX5926 limit the slew rate of  $V_{OUT}$ . Connect an external capacitor,  $C_{SLEW}$ , between SLEW and GND to adjust the slew-rate limit. Floating SLEW sets the maximum slew rate to the default value. Calculate  $C_{SLEW}$  using the following equation:

$$C_{SLEW} = 330 \times 10^{-9} / SR$$

where  $SR$  is the desired slew rate in V/ms.

A  $2\mu A$  (typ) pullup current clamped to 1.4V causes an initial jump in the gate voltage,  $V_{GATE}$ , if  $C_{GATE}$  is small

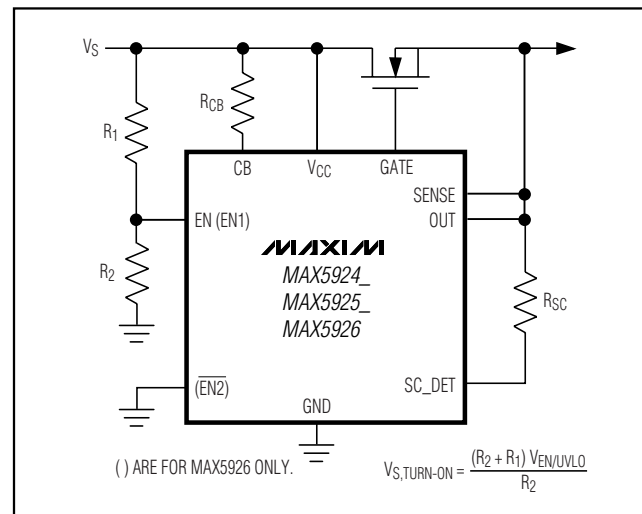


Figure 10. Adjustable Turn-On Voltage

and the slew rate is slow (Figure 3). Figure 9 illustrates how the addition of gate capacitance eliminates this initial jump.  $C_{GATE}$  should not exceed  $25nF$ .

## EN (MAX5924/MAX5925), EN1/EN2 (MAX5926)

The enable comparators control the on/off function of the MAX5924/MAX5925/MAX5926. Enable is also used to reset the fault latch in latch mode. Pull EN or EN1 low for  $100\mu s$  to reset the latch. A resistive divider between EN or EN1,  $V_S$ , and GND sets the programmable turn-on voltage to a voltage greater than  $V_{UVLO}$  (Figure 10).

# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

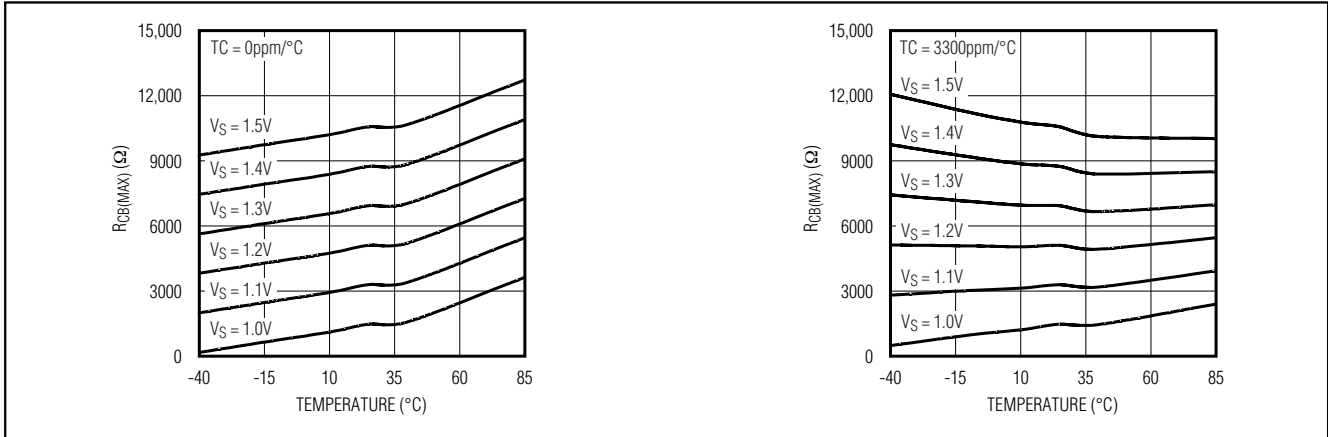


Figure 11. Maximum Circuit-Breaker Programming Resistor vs. Temperature

## Selecting a Circuit-Breaker Threshold

The MAX5924/MAX5925/MAX5926 offer a circuit-breaker function to protect the external MOSFET and the load from the potentially damaging effects of excessive current. As load current flows through R<sub>DS(ON)</sub> (Figure 12) or R<sub>SENSE</sub> (Figure 13), a voltage drop is generated. After V<sub>GS</sub> exceeds V<sub>CB,EN</sub>, the MAX5924/MAX5925/MAX5926 monitor this voltage to detect overcurrent conditions. If this voltage exceeds the circuit-breaker threshold, the external MOSFET turns off and the power-good output(s) deassert(s). To accommodate different MOSFETs, sense resistors, and load currents, the MAX5924/MAX5925/MAX5926 voltage across R<sub>CB</sub> can be set between 10mV and 500mV. The value of the circuit-breaker voltage must be carefully selected based on V<sub>S</sub> (Figure 11).

### No R<sub>SENSE</sub> Mode

When operating without R<sub>SENSE</sub>, calculate the circuit-breaker threshold using the MOSFET's R<sub>DS(ON)</sub> at the worst possible operating condition, and add a 20% overcurrent margin to the maximum circuit current. For example, if a MOSFET has an R<sub>DS(ON)</sub> of 0.06Ω at T<sub>A</sub> = +25°C, and a normalized on-resistance factor of 1.75 at T<sub>A</sub> = +105°C, the R<sub>DS(ON)</sub> used for calculation is the product of these two numbers, or (0.06Ω) × (1.75) = 0.105Ω. Then, if the maximum current is expected to be 2A, using a 20% margin, the current for calculation is (2A) × (1.2) = 2.4A. The resulting minimum circuit-breaker threshold is then a product of these two numbers, or (0.105Ω) × (2.4A) = 0.252V. Using this method to choose a circuit-breaker threshold allows the circuit to operate under worst-case conditions without causing a circuit-breaker fault, but the circuit-breaker function will still detect a short circuit or a gross overcurrent condition.

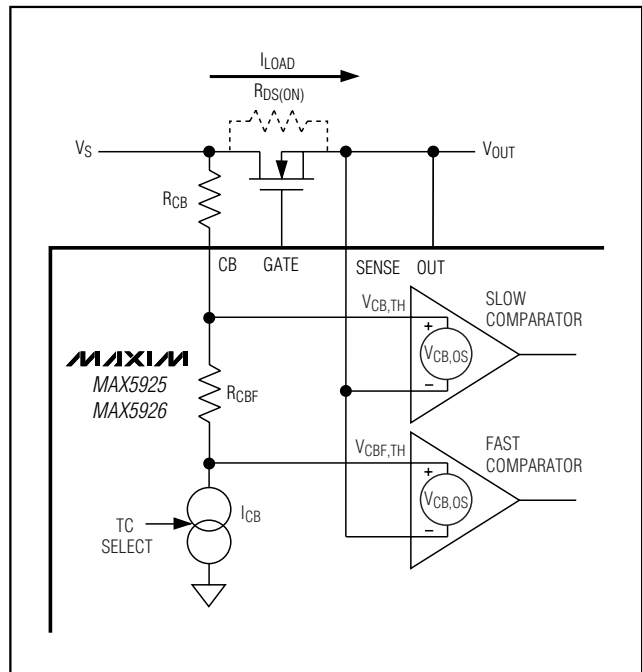


Figure 12. Circuit Breaker Using R<sub>DS(ON)</sub>

To determine the proper circuit-breaker resistor value use the following equation, which refers to Figure 12:

$$R_{CB} = \frac{(I_{TRIPSLow} \times R_{DS(ON)}(T)) + |V_{CB,OS}|}{I_{CB}}$$

where I<sub>TRIPSLow</sub> is the desired slow-comparator trip current.

# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

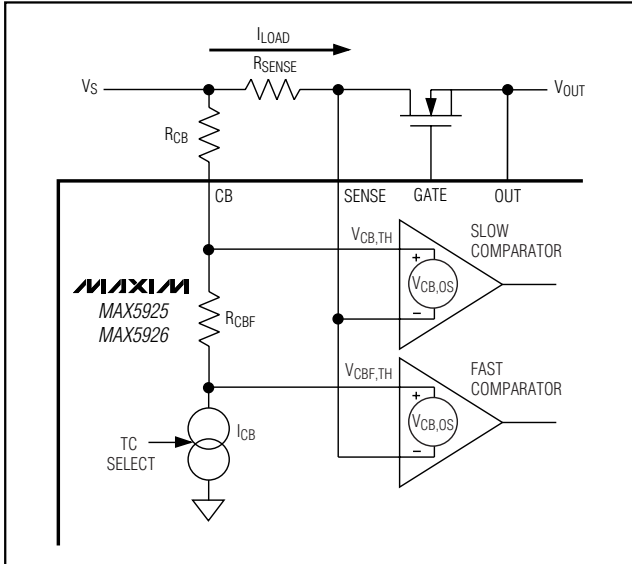


Figure 13. Circuit Breaker Using RSENSE

The fast-comparator trip current is determined by the selected RCB value and cannot be adjusted independently. The fast-comparator trip current is given by:

$$I_{TRIPFAST} = \frac{I_{CB} \times (R_{CBF} + R_{CB}) \pm V_{CB,OS}}{R_{DS(ON)}(T)}$$

### RSENSE Mode

When operating with RSENSE, calculate the circuit-breaker threshold using the worst possible operating conditions, and add a 20% overcurrent margin to the maximum circuit current. For example, with a maximum expected current of 2A, using a 20% margin, the current for calculation is (2A) x (1.2) = 2.4A. The resulting minimum circuit-breaker threshold is then a product of this current and RSENSE = 0.06Ω, or (0.06Ω) x (2.4A) = 0.144V. Using this method to choose a circuit-breaker threshold allows the circuit to operate under worst-case conditions without causing a circuit-breaker fault, but the circuit-breaker function will still detect a short-circuit or a gross overcurrent condition.

**Table 2. Programming the Temperature Coefficient (MAX5926)**

TC	TC <sub>ICB</sub> (ppm/°C)
High	0
Low	3300

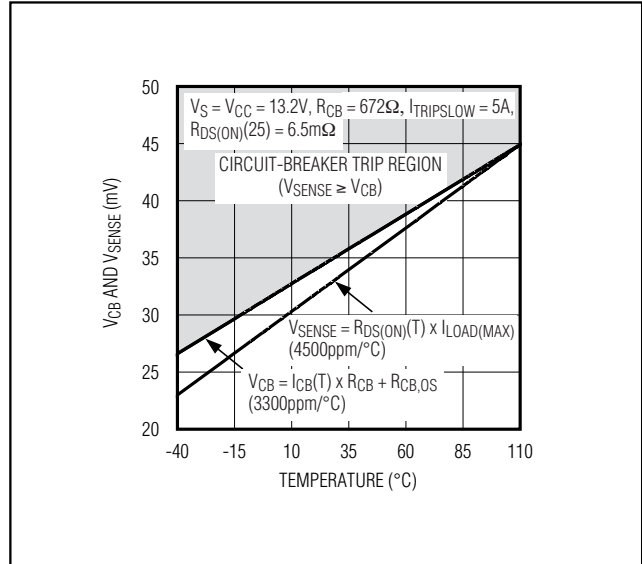


Figure 14. Circuit-Breaker Trip Point and Current-Sense Voltage vs. Temperature

To determine the proper circuit-breaker resistor value, use the following equation, which refers to Figure 12:

$$R_{CB} = \frac{(I_{TRIPSLow} \times R_{SENSE}) + |V_{CB,OS}|}{I_{CB}}$$

where ITRIPSLow is the desired slow-comparator trip current.

The fast-comparator trip current is determined by the selected RCB value and cannot be adjusted independently. The fast-comparator trip current is given by:

$$I_{TRIPFAST} = \frac{I_{CB} \times (R_{CBF} + R_{CB}) \pm V_{CB,OS}}{R_{SENSE}}$$

**Table 3. Suggested External MOSFETs**

APPLICATION CURRENT (A)	PART	DESCRIPTION
1	International Rectifier IRF7401	SO-8
2	Siliconix Si4378DY	SO-8
5	Siliconix SUD40N02-06	DPACK
10	Siliconix SUB85N02-03	D2PAK

# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

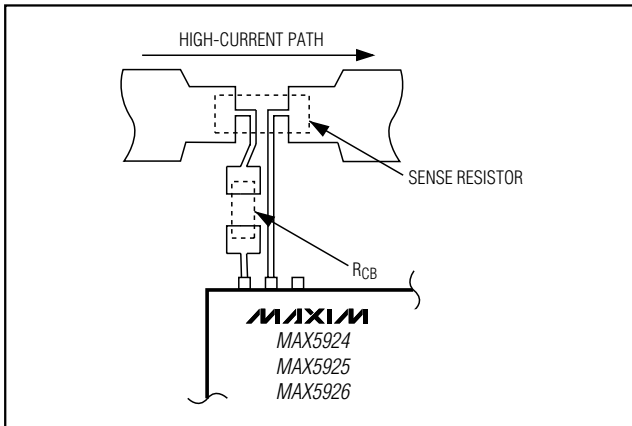


Figure 15. Kelvin Connection for the Current-Sense Resistor

## Circuit-Breaker Temperature Coefficient

In applications where the external MOSFET's on-resistance is used as a sense resistor to determine overcurrent conditions, a 3300ppm/°C temperature coefficient is desirable to compensate for the  $R_{DS(ON)}$  temperature coefficient. Use the MAX5926's TC input to select the circuit-breaker programming current's temperature coefficient,  $TC_{ICB}$  (see Table 2). The MAX5924 temperature coefficient is preset to 0ppm/°C, and the MAX5925's is preset to 3300ppm/°C.

Setting  $TC_{ICB}$  to 3300ppm/°C allows the circuit-breaker threshold to track and compensate for the increase in the MOSFET's  $R_{DS(ON)}$  with increasing temperature. Most MOSFETs have a temperature coefficient within a 3000ppm/°C to 7000ppm/°C range. Refer to the MOSFET data sheet for a device-specific temperature coefficient.

$R_{DS(ON)}$  and  $I_{CB}$  are temperature dependent, and can therefore be expressed as functions of temperature. At a given temperature, the MAX5925/MAX5926 indicate an overcurrent condition when:

$$I_{TRIPSLow} \times R_{DS(ON)}(T) \geq I_{CB}(T) \times R_{CB} + |V_{CB,OS}|$$

where  $V_{CB,OS}$  is the worst-case offset voltage. Figure 14 graphically portrays operating conditions for a MOSFET with a 4500ppm/°C temperature coefficient.

Table 4. Component Manufacturers

COMPONENT	MANUFACTURER	PHONE	WEBSITE
Sense Resistors	Dale-Vishay	402-564-3131	www.vishay.com
	IRC	828-264-8861	www.irctt.com
MOSFETs	Fairchild	888-522-5372	www.fairchildsemi.com
	International Rectifier	310-233-3331	www.irf.com

## Applications Information

### Component Selection

#### n-Channel MOSFET

Select the external n-channel MOSFET according to the application's current and voltage level. Table 3 lists some recommended components. Choose the MOSFET's on-resistance,  $R_{DS(ON)}$ , low enough to have a minimum voltage drop at full load to limit the MOSFET power dissipation. High  $R_{DS(ON)}$  can cause undesired power loss and output ripple if the board has pulsing loads or triggers an external undervoltage reset monitor at full load. Determine the device power-rating requirement to accommodate a short circuit on the board at startup with the device configured in autoretry mode.

Using the MAX5924/MAX5925/MAX5926 in latched mode allows the consideration of MOSFETs with higher  $R_{DS(ON)}$  and lower power ratings. A MOSFET can typically withstand single-shot pulses with higher dissipation than the specified package rating. Low MOSFET gate capacitance is not necessary since the inrush current limiting is achieved by limiting the gate  $dv/dt$ . Table 4 lists some recommended manufacturers and components.

Be sure to select a MOSFET with an appropriate gate drive (see the *Typical Operating Characteristics*). Typically, for  $V_{CC}$  less than 3V or greater than 12V, select a 2.5V  $V_{GS}$  MOSFET.

#### Optional Sense Resistor

Select the sense resistor in conjunction with  $R_{CB}$  to set the slow and fast circuit-breaker thresholds (see the *Selecting a Circuit-Breaker Threshold* section). The sense-resistor power dissipation depends on the device configuration. If latched mode is selected,  $P_{RSENSE} = (I_{OVERLOAD})^2 \times R_{SENSE}$ ; if autoretry is selected, then  $P_{RSENSE} = (I_{OVERLOAD})^2 \times R_{SENSE} \times (t_{ON}/t_{RETRY})$ . Choose a sense-resistor power rating of twice the  $P_{RSENSE}$  for long-term reliable operation. In addition, ensure that the sense resistor has an adequate  $I^2T$  rating to survive instantaneous short-circuit conditions.



# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

MAX5924/MAX5925/MAX5926

## Design Procedure

Given:

- $V_{CC} = V_S = 5V$
- $C_L = 150\mu F$
- Full-Load Current = 5A
- No  $R_{SENSE}$
- $I_{NRUSH} = 500mA$

Procedures:

- 1) Calculate the required slew rate and corresponding  $C_{SLEW}$ :

$$SR = \frac{I_{NRUSH}}{1000 \times C_L} = 3.3 \frac{V}{ms}$$

$$C_{SLEW} = \frac{330 \times 10^{-9}}{SR} = \frac{330 \times 10^{-9}}{3.3 \frac{V}{ms}} = 0.1\mu F$$

- 2) Select a MOSFET and determine the worst-case power dissipation.
- 3) Minimize power dissipation at full load current and at high temperature by selecting a MOSFET with an appropriate  $R_{DS(ON)}$ . Assume a 20°C temperature difference between the MAX5924/MAX5925/MAX5926 and the MOSFET.

For example, at room temperature the IRF7822's  $R_{DS(ON)} = 6.5m\Omega$ . The temperature coefficient for this device is 4000ppm/°C. The maximum  $R_{DS(ON)}$  for the MOSFET at  $T_{J(MOSFET)} = +105^\circ C$  is:

$$R_{DS(ON)105} = 6.5m\Omega \times \left(1 + (105^\circ C - 25^\circ C) \times 4000 \frac{ppm}{^\circ C}\right) = 8.58m\Omega$$

The power dissipation in the MOSFET at full load is:

$$P_D = I^2 R = (5A)^2 \times 8.58m\Omega = 215mW$$

- 4) Select  $R_{CB}$ .

Since the MOSFET's temperature coefficient is 4000ppm/°C, which is greater than  $TC_{ICB}$  (3300ppm/°C), calculate the circuit-breaker threshold at high temperature so the circuit breaker is guaranteed not to trip at lower temperature during normal operation (Figure 15).

$$I_{TRIPSLow} = I_{FULL LOAD} + 20\% = 5A + 20\% = 6A$$

$$R_{DS(ON)105} = 8.58m\Omega \text{ (max), from step 2}$$

$$I_{CB85} = 58\mu A \times (1 + (3300ppm/^\circ C \times (85 - 25)^\circ C)) = 69.5\mu A \text{ (min)}$$

$$R_{CB} = \frac{(I_{TRIPSLow} \times R_{DS(ON)105}) + |V_{CB,OS}|}{I_{CB85}}$$

$$R_{CB} = ((6A \times 8.58m\Omega) + 4.7mV) / 69.5\mu A = 808\Omega$$

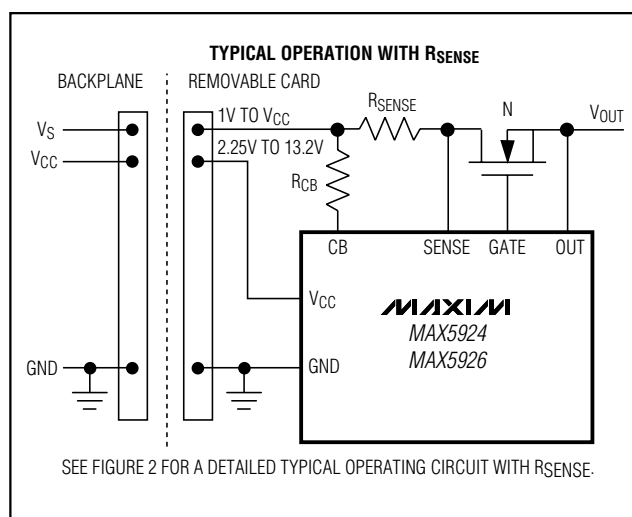
## Layout Considerations

Keep all traces as short as possible and maximize the high-current trace dimensions to reduce the effect of undesirable parasitic inductance. Place the MAX5924/MAX5925/MAX5926 close to the card's connector. Use a ground plane to minimize impedance and inductance. Minimize the current-sense resistor trace length (<10mm), and ensure accurate current sensing with Kelvin connections.

When the output is short circuited, the voltage drop across the external MOSFET becomes large. Hence, the power dissipation across the switch increases, as does the die temperature. An efficient way to achieve good power dissipation on a surface-mount package is to lay out two copper pads directly under the MOSFET package on both sides of the board. Connect the two pads to the ground plane through vias, and use enlarged copper mounting pads on the top side of the board.

It is important to maximize the thermal coupling between the MOSFET and the MAX5925/MAX5926 to balance the device junction temperatures. When the temperatures of the two devices are equal, the circuit-breaker trip threshold is most accurate. Keep the MOSFET and the MAX5925/MAX5926 as close to each other as possible to facilitate thermal coupling.

## Typical Operating Circuits (continued)

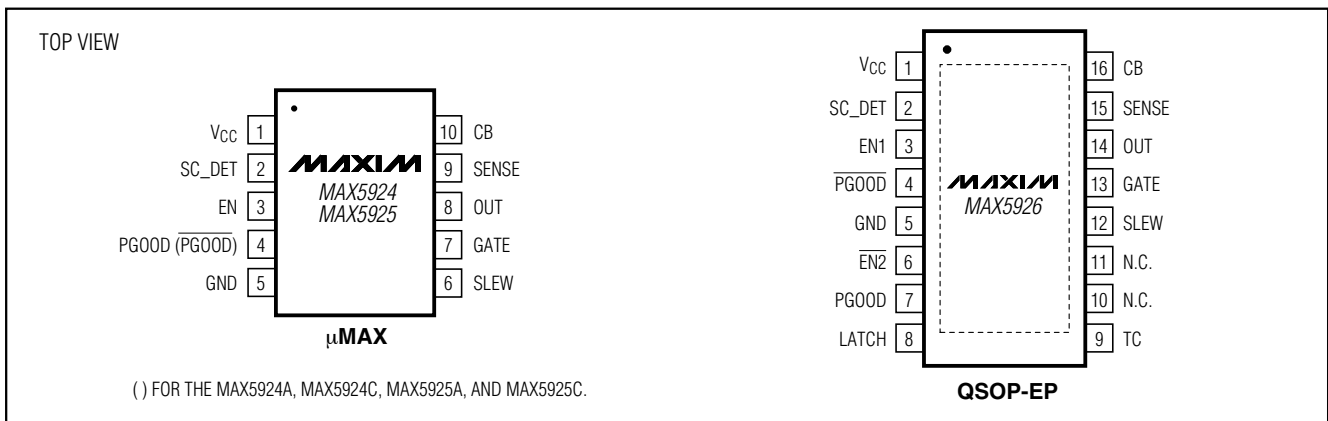


# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

## Selector Guide

PART	CIRCUIT-BREAKER TEMPCO (ppm/°C)	FAULT MANAGEMENT	POWER-GOOD OUTPUT	
			$\overline{\text{PGOOD}}$ (OPEN-DRAIN)	PGOOD (OPEN-DRAIN)
MAX5924A	0	Latched	✓	—
MAX5924B	0	Latched	—	✓
MAX5924C	0	Autoretry	✓	—
MAX5924D	0	Autoretry	—	✓
MAX5925A	3300	Latched	✓	—
MAX5925B	3300	Latched	—	✓
MAX5925C	3300	Autoretry	✓	—
MAX5925D	3300	Autoretry	—	✓
MAX5926	0 or 3300 (Selectable)	Latched or Autoretry (Selectable)	✓	✓

## Pin Configurations



## Chip Information

TRANSISTOR COUNT: 3751

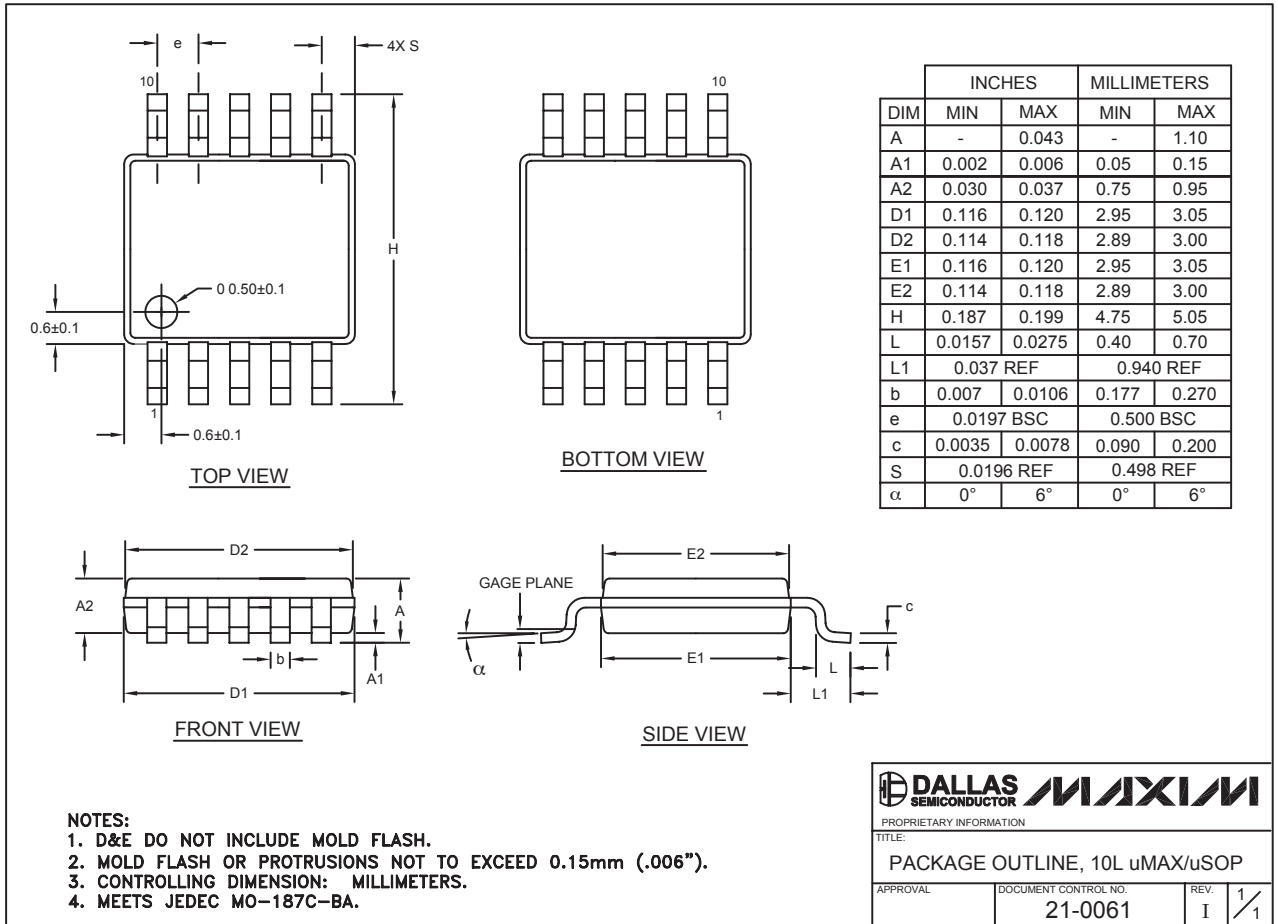
PROCESS: BiCMOS

# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

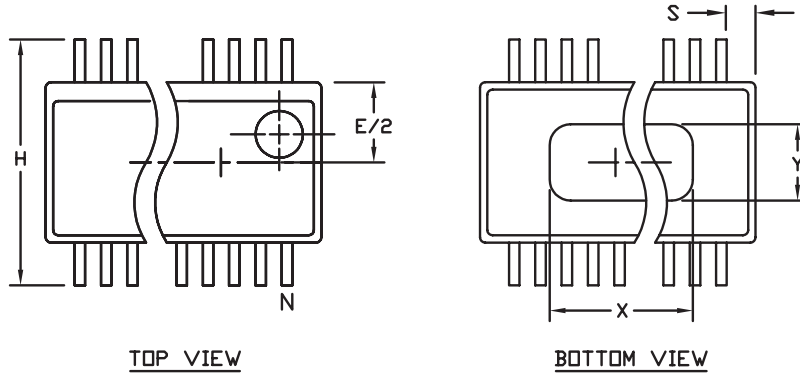
MAX5924/MAX5925/MAX5926



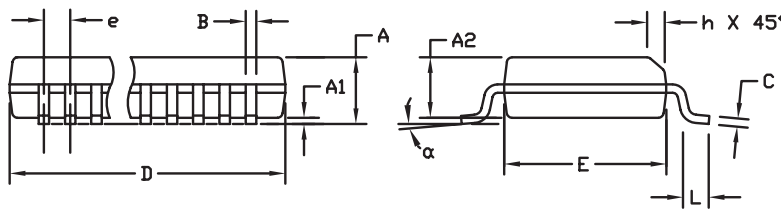
# 1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.055	.065	1.40	1.65
A1	.000	.004	.000	.102
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	16		16	
S	.002	.007	.050	.180
X	SEE VARIATIONS			
Y	SEE VARIATIONS			
α	0°	8°	0°	8°



### VARIATIONS:

	INCHES		MILLIMETERS		PKG.
	MIN.	MAX.	MIN.	MAX.	
X	.086	.106	2.19	2.69	E16E-9
Y	.080	.100	2.04	2.54	
X	.080	.100	2.04	2.54	E16E-10
Y	.120	.140	3.05	3.55	

### NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. DIMENSIONS X AND Y APPLY ONLY TO EXPOSED PAD QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

PROPRIETARY INFORMATION TITLE: PACKAGE OUTLINE, 16L QSOP, .150" EXPOSED PAD			
APPROVAL	DOCUMENT CONTROL NO.	REV.	1/1
	21-0112	C	

QSOP-EXP-PADS-EPS

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