19-4039; Rev 0; 3/08

EVALUATION KIT AVAILABLE

Quad Linear Fan-Speed Controller

MAX6620

General Description

The MAX6620 controls the speeds of up to four fans using four independent linear voltage outputs. The drive voltages for the fans are controlled directly over the I²C interface. Each output drives the base of an external bipolar transistor or the gate of a FET in high-side drive configuration. Voltage feedback at the fan's power-supply terminal is used to force the correct output voltage.

The MAX6620 offers two methods for fan control. In RPM mode, the MAX6620 monitors four fan tachometer logic outputs for precise (±1%) control of fan RPM and detection of fan failure. In DAC mode, each fan is driven with a voltage resolution of 9 bits and the tachometer outputs of the fans are monitored for failure.

The DAC_START input selects the fan power-supply voltage at startup to ensure appropriate fan drive when power is first applied. A watchdog feature turns the fans fully on to protect the system if there are no valid I²C communications within a preset timeout period.

The MAX6620 operates from a 3.0V to 5.5V power supply with low 250µA supply current, and the I²C-compatible interface makes it ideal for fan control in a wide range of cooling applications. The MAX6620 is available in a 28-pin TQFN package and operates over the -40°C to +125°C automotive temperature range.

Applications

Consumer Products

Servers

Communications Equipment

Storage Equipment

Typical Application Circuit appears at end of data sheet.

Features

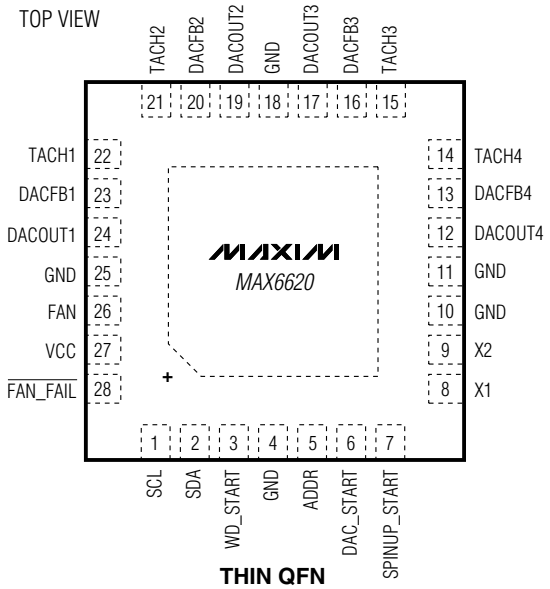
- **Controls Up to Four Independent Fans With Linear (DC) Drive**
- **Uses Four External Low-Cost Pass Transistors**
- **1% Accuracy Precision RPM Control**
- **Controlled Voltage Rate-Of-Change for Best Acoustics**
- **I²C Bus Interface**
- **3.0V to 5.5V Supply Voltage Range**
- **250µA (typ) Operating Supply Current**
- **3µA (typ) Shutdown Supply Current**
- **Small 5mm x 5mm Footprint**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6620ATI+	-40°C to +125°C	28 TQFN-EP*	T2855-8

+Denotes a lead-free package.
**EP = Exposed paddle.*

Pin Configuration



THIN QFN
(5mm × 5mm × 0.8mm)

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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Quad Linear Fan-Speed Controller

ABSOLUTE MAXIMUM RATINGS

VCC to GND .....-0.3V to +6.0V
FAN_FAIL, SDA, SCL to GND .....-0.3V to +6.0V
ADDR, SPINUP_START, DAC_START, WD_START, X1, X2 to GND .....-0.3V to (V_{CC} + 0.3V)
All Other Pins to GND.....-0.3V to +13.5V
Input Current at DACOUT_ Pins (Note 1) .....+5mA/-50mA
Input Current at Any Pin (Note 1).....5mA
ESD Protection (all pins, Human Body Model) (Note 2)...±2000V

Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 34.5mW/°C above +70°C) 2758.6mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Human Body Model, 100pF discharged through a 1.5kΩ resistor.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +125°C, V_{CC} = 3.0V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = 3.3V.) (Note 3)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{CC}			3.0		5.5	V
Operating Supply Current	I_{CC}	V_{CC} = 5.5V			0.25	0.60	mA
Quiescent Supply Current		I^2C inactive			0.2	0.5	mA
		Shutdown mode			3	20	µA
V_{FAN} Supply Voltage	V_{FANHI}			10	12	13.5	V
	V_{FANLO}			4.0	5.0	5.5	
DACOUT_ Output Current	$I_{DACOUT\_}$	V_{GND} + 10V < $V_{DACOUT\_}$ < 11.5V, V_{FAN} = 12V		-18			mA
		V_{GND} + 3V < $V_{DACOUT\_}$ < 10V, V_{FAN} = 12V		-16			
DACOUT_ Output Voltage	$V_{DACOUT\_}$	$I_{DACOUT\_}$ = 5mA		0.05		V_{FAN} - 0.1	V
DAC Feedback Voltage at Half Scale	DAC_{FBHS}	At DACFB_, code = 0x100, $I_{DACOUT\_}$ = 5mA	$V_{FAN} = V_{FANHI}$		256/535		V
			$V_{FAN} = V_{FANLO}$		256/567		
			V_{FAN} = 12V	5.54	5.74	5.94	
			V_{FAN} = 5V	2.05	2.25	2.45	
DAC Feedback Voltage at Full Scale	DAC_{FBFS}	At DACFB_, code = 0x1FF, $I_{DACOUT\_}$ = 5mA	$V_{FAN} = V_{FANHI}$		511/535		V
			$V_{FAN} = V_{FANLO}$		511/567		
	$V_{DACFB511}$		V_{FAN} = 12V	11.25	11.45	11.65	
			V_{FAN} = 5V	4.3	4.5	4.7	
Drive Voltage Resolution					9		Bit
DACFB_ Impedance	R_{DACFB}				1		MΩ
TACH Minimum Input Pulse Width				25			µs
Internal Reference Frequency Accuracy		(Note 4)		-3		+3	%
TACH Count Accuracy (Note 4)		Using 32.768kHz crystal		-0.1		+0.1	%
		Using on-chip oscillator		-2		+2	

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ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +125°C, V_{CC} = 3.0V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = 3.3V.) (Note 3)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Fan Control Accuracy (Note 4)		Using 32.768kHz crystal, test at 850RPM	-1		+1	%
		Using on-chip oscillator	-3		+3	
XTAL Oscillator Startup Time				2		s
X1 Input Threshold				0.7		V
POR Threshold	V_{CC}			2		V
	V_{FAN}			3.5		
LOGIC (SDA, SCL, $\overline{\text{FAN\_FAIL}}$, WD_START, TACH_)						
Input High Voltage	V_{IH}		V_{CC} x 0.7			V
Input Low Voltage	V_{IL}				V_{CC} x 0.3	V
Input High Current	I_{IH}				1.0	µA
Input Low Current	I_{IL}				-1.0	µA
Input Capacitance		All digital inputs		6		pF
Output High Current					100	µA
Output Low Voltage		I_{OL} = 3mA			0.4	V
LOGIC (DAC_START, SPIN_START, ADDR)						
Input High Voltage	V_{IH}		V_{CC} - 0.5			V
Input Low Voltage	V_{IL}				0.5	V
Input High Current	I_{IH}				1.0	µA
Input Low Current	I_{IL}				-1.0	µA
Input Capacitance		All digital inputs		6		pF
I²C-COMPATIBLE TIMING (Notes 5, 6)						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		600			ns
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
START Condition Setup Time	$t_{SU:STA}$		600			ns
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Out Hold Time	t_{DH}		100			ns
Data In Hold Time	$t_{HD:DAT}$	(Note 6)	0		0.9	µs
Maximum Receive SCL/SDA Rise Time	t_R	(Note 8)		300		ns
Minimum Receive SCL/SDA Rise Time	t_R	(Note 7)		20 + 0.1 x C_B		ns

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Quad Linear Fan-Speed Controller

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +125°C, V_{CC} = 3.0V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = 3.3V.) (Note 3)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Maximum Receive SCL/SDA Fall Time	t_F			300		ns
Minimum Receive SCL/SDA Fall Time	t_F	(Note 7)		20 + 0.1 x C_B		ns
Transmit SDA Fall Time	t_F	(Note 7)	20 + 0.1 x C_B		250	ns
Pulse Width of Suppressed Spike	t_{SP}	(Note 8)	0		50	ns
Output Fall Time		C_L = 400pF, I_{OUT} = 3mA			250	ns
SDA Time Low for Reset of Serial Interface	$t_{TIMEOUT}$	(Note 9)	20		50	ms

Note 3: All parts will operate properly over the V_{CC} supply voltage range of 3.0V to 5.5V.
Note 4: Guaranteed by design and characterization.
Note 5: All timing specifications are guaranteed by design.
Note 6: A master device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of SCL's falling edge.
Note 7: C_B = total capacitance of one bus line in pF. Tested with C_B = 400pF.
Note 8: Input filters on SDA and SCL suppress noise spikes less than 50ns.
Note 9: Holding the SDA line low for a time greater than $t_{TIMEOUT}$ will cause the devices to reset SDA to the idle state of the serial bus communication (SDA set high).

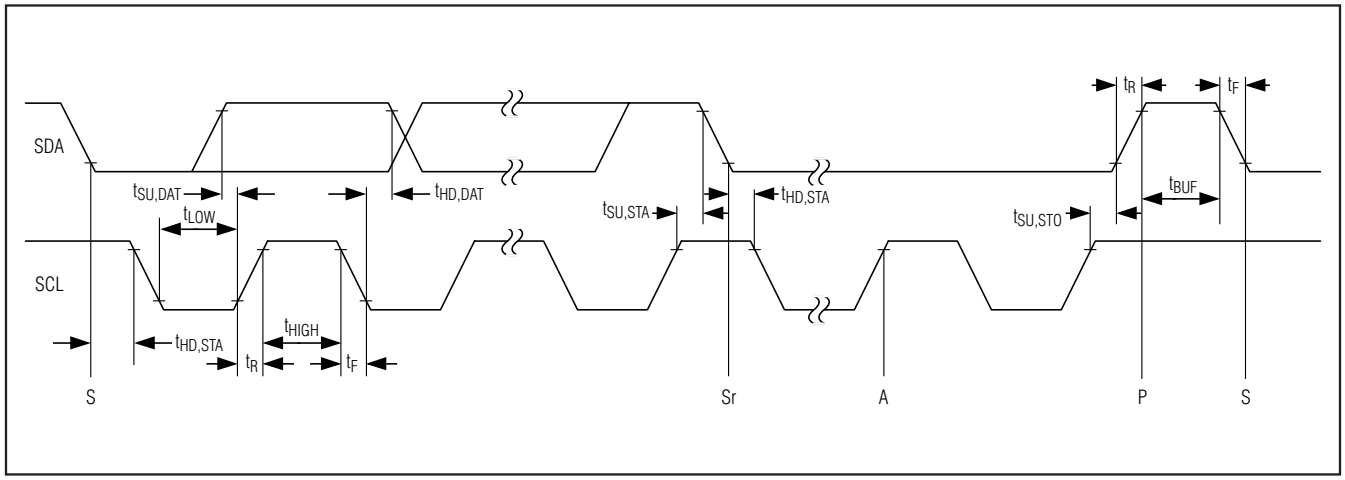

Figure 1. I²C Serial Interface Timing

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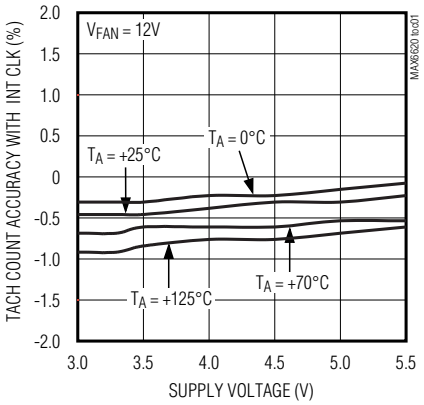
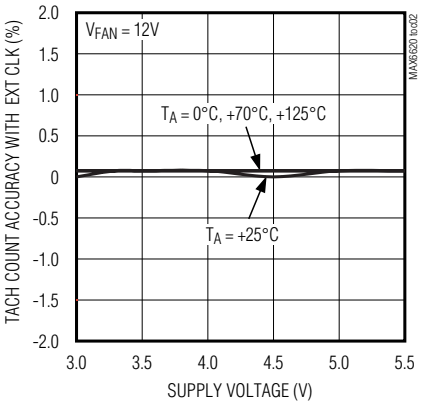
Typical Operating Characteristics

(V_{CC} = 3.3V, V_{FAN} = 12V, T_A = +25°C, unless otherwise noted.)

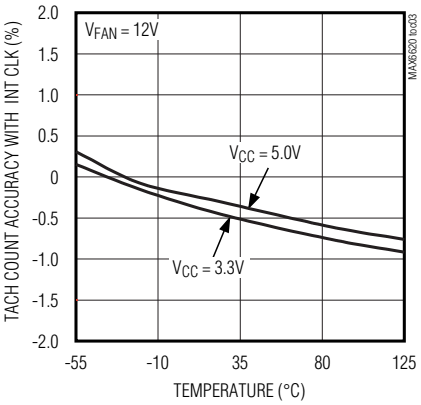
TACH COUNT ACCURACY WITH INT CLK vs. SUPPLY VOLTAGE



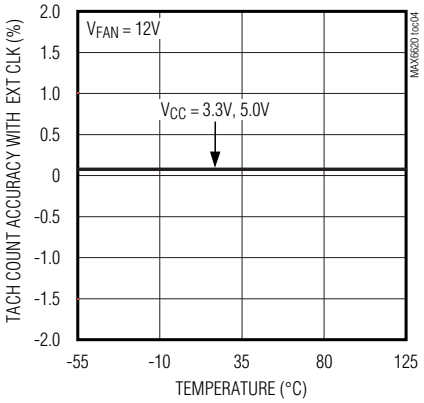
TACH COUNT ACCURACY WITH EXT CLK vs. SUPPLY VOLTAGE



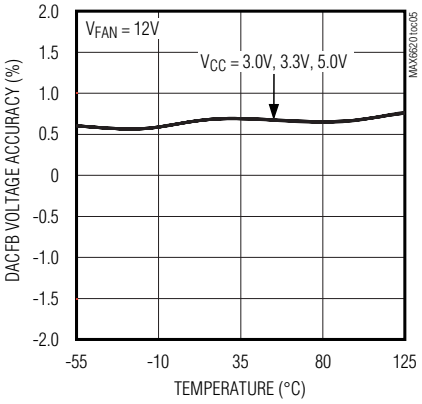
TACH COUNT ACCURACY WITH INT CLK vs. TEMPERATURE



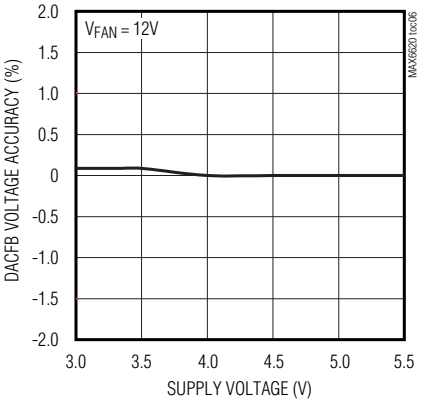
TACH COUNT ACCURACY WITH EXT CLK vs. TEMPERATURE



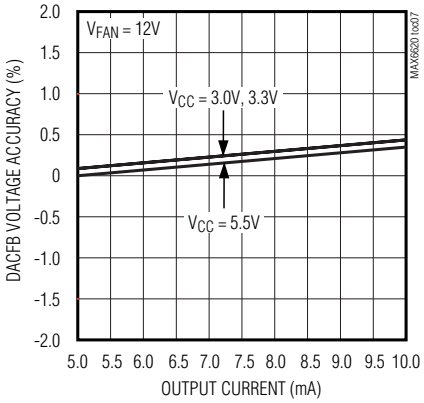
DACFB_ VOLTAGE ACCURACY vs. TEMPERATURE



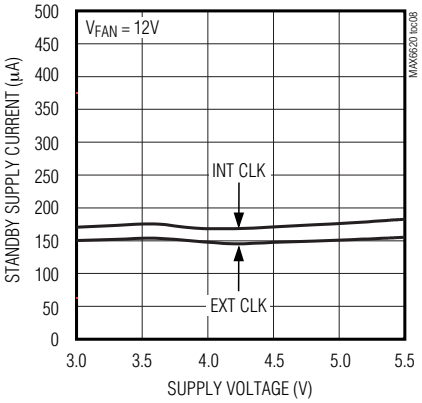
DACFB_ VOLTAGE ACCURACY vs. SUPPLY VOLTAGE



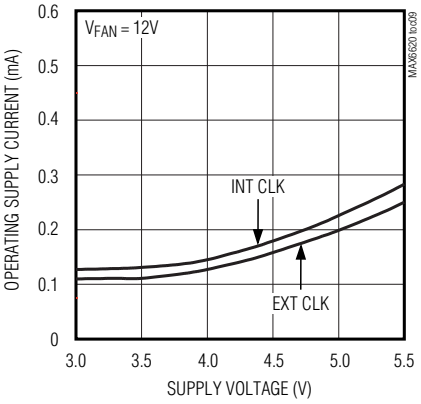
DACFB_ VOLTAGE ACCURACY vs. OUTPUT CURRENT



STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE



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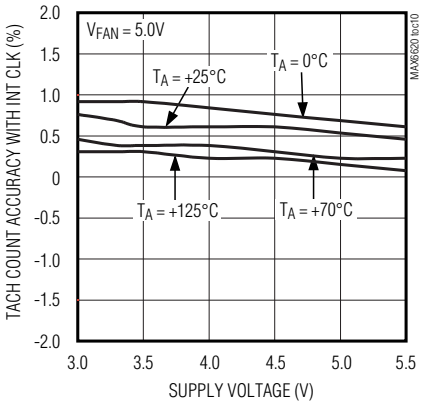
Quad Linear Fan-Speed Controller

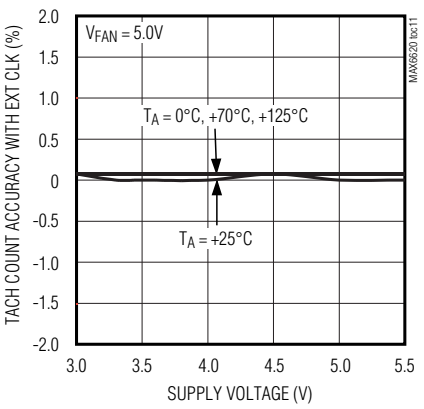
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_{FAN} = 12V, T_A = +25°C, unless otherwise noted.)

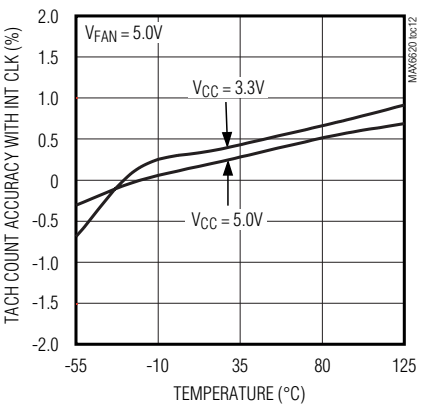
TACH COUNT ACCURACY WITH INT CLK vs. SUPPLY VOLTAGE



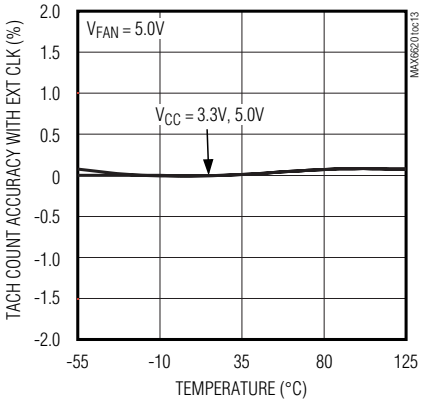
TACH COUNT ACCURACY WITH EXT CLK vs. SUPPLY VOLTAGE



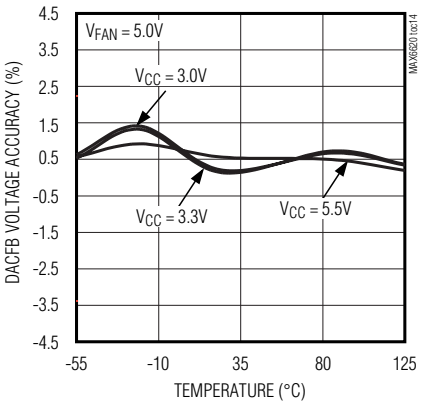
TACH COUNT ACCURACY WITH INT CLK vs. TEMPERATURE



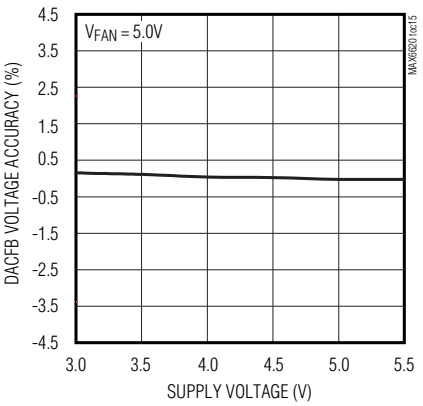
TACH COUNT ACCURACY WITH EXT CLK vs. TEMPERATURE



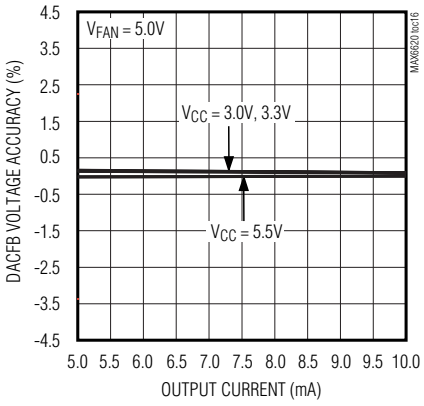
DACFB_ VOLTAGE ACCURACY vs. TEMPERATURE



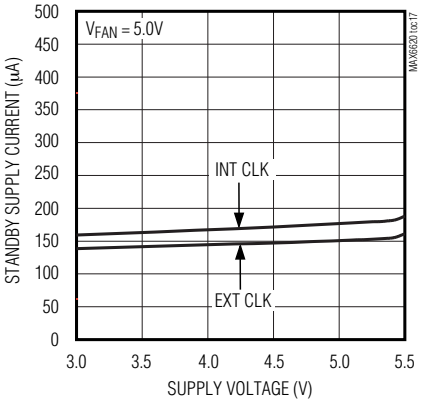
DACFB_ VOLTAGE ACCURACY vs. SUPPLY VOLTAGE



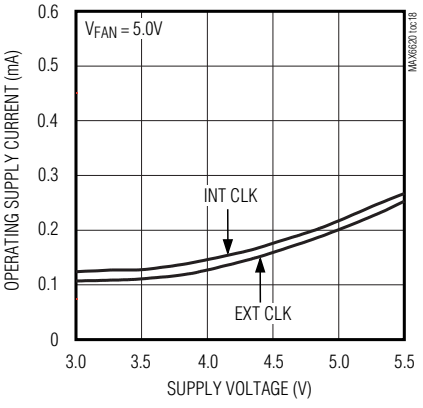
DACFB_ VOLTAGE ACCURACY vs. OUTPUT CURRENT



STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE



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Pin Description

PIN	NAME	FUNCTION
1	SCL	I^2C Serial-Clock Input. Can be pulled up to 5.5V regardless of V_{CC}. Open circuit when V_{CC} = 0V.
2	SDA	Open-Drain, I^2C Serial-Data Input/Output. Can be pulled up to 5.5V regardless of V_{CC}. Open circuit when V_{CC} = 0V.
3	WD_START	Startup Watchdog Set Input. This input is sampled when power is first applied and sets the initial I^2C watchdog behavior. When connected to GND, the watchdog function is disabled. When connected to V_{CC}, the MAX6620 monitors SDA. If 10s elapse without a valid I^2C transaction, the fan drive goes to 100%.
4, 10, 11, 18, 25	GND	Ground
5	ADDR	I^2C Address Set Input. This input is sampled when power is first applied and sets the I^2C slave address. When connected to GND, the slave address will be 0x50. When unconnected, the slave address will be 0x52. When connected to V_{CC}, the slave address will be 0x54.
6	DAC_START	Startup Fan Drive DAC Set Input. This input is sampled when power is first applied and sets the power-up value for the fan drive voltage. When connected to GND, the fan drive voltage will be 0%. When unconnected, the fan drive voltage will be 75%. When connected to V_{CC}, the fan drive voltage will be 100%.
7	SPINUP_START	Startup Spin-Up Set Input. This input is sampled when power is first applied and sets the initial spin-up behavior. When connected to GND, spin-up is disabled. When connected to V_{CC} at power-up, the fan is driven with a full-scale drive voltage until two tachometer pulses have been detected, or 1s has elapsed. When unconnected, the fan is driven with a full-scale drive voltage until two tachometer pulses have been detected, or 0.5s has elapsed. Spin-up behavior may be modified by writing appropriate settings to the MAX6620's registers.
8, 9	X1, X2	Crystal Oscillator Inputs. Connections for a standard 32.768kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 12pF. Connect an external 32.768kHz oscillator across X1 and X2 for operation with the external oscillator. If no crystal or external oscillator is connected, the MAX6620 will use its internal oscillator.
12, 17, 19, 24	DACOUT4–DACOUT1	Fan Drive DAC Outputs. Connect to the gate of a p-channel MOSFET or base of a PNP bipolar transistor.
13, 16, 20, 23	DACFB4–DACFB1	DAC Feedback Inputs. Connect a 0.1µF capacitor between these pins and GND. Connect to the supply pin of the fan and to the drain of a p-channel MOSFET or collector of a PNP bipolar transistor.
14, 15, 21, 22	TACH4–TACH1	Fan Tachometer Logic Inputs. These inputs accept input voltages up to V_{FAN}.
26	FAN	Fan Power-Supply Voltage Input. Connect to the fan power supply (V_{FAN}). Bypass with a 0.1µF capacitor to GND.
27	VCC	Power-Supply Input. 3.3V nominal. Bypass V_{CC} to GND with a 0.1µF capacitor.
28	$\overline{\text{FAN\_FAIL}}$	Active-Low, Open-Drain Fan Failure Output. Active only when fault is present; open-circuit when V_{CC} = 0V. This pin can be pulled up to 5.5V regardless of V_{CC}.
—	EP	Exposed Paddle. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

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Quad Linear Fan-Speed Controller

Detailed Description

The MAX6620 controls the speeds of up to four fans using four independent linear voltage outputs. The drive voltages for the fans are controlled directly over the I²C interface. Each of the outputs (DACOUT1–DACOUT4) drive the base of an external PNP or the gate of a p-channel MOSFET. Voltage feedback at the fan's power-supply terminal is used to force the output voltage.

The MAX6620 monitors fan tachometer logic outputs for precise (1%) control of fan RPM and detection of fan failure. When the MAX6620 is used with 2-wire fans, these inputs are not used, and the fans can be driven to the desired voltage without using tachometer feedback.

Three inputs set the fan drive status on application of power. The DAC_START input selects the fan-supply voltage (100%, 75%, or 0%) at startup to ensure appropriate fan drive when power is first applied. The SPIN_START input selects whether spin-up will be applied to the fans at power-up. WD_START selects whether lack of I²C activity will force the fans to full speed. When the watchdog function is enabled, the fans will be driven to full speed if there is no I²C activity for a period of 2s, 6s, or 10s.

Digital Interface

The MAX6620 features an I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX6620 and the master at rates up to 400kHz. The master (typically a microcontroller) initiates data transfer on the bus and generates SCL. SDA and SCL require 4.7kΩ (typ) pullup resistors.

Bit Transfer

One data bit is transferred during each SCL clock cycle. Nine clock cycles are required to transfer the data into or out of the MAX6620. The data on SDA must remain stable during the high period of the SCL clock pulse, as changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). Both SDA and SCL idle high.

Write Byte Format

S	ADDRESS	WR	A	COMMAND	A	DATA	A	P
	7 bits			8 bits		8 bits		1

Slave Address: equivalent to chip-select line of a 3-wire interface

Command Byte: selects which register you are writing to

Data Byte: data goes into the register set by the command byte (to set thresholds, configuration masks, and sampling rate)

Read Byte Format

S	ADDRESS	WR	A	COMMAND	A	S	ADDRESS	RD	A	DATA	$\overline{A}$	P
	7 bits			8 bits			7 bits			8 bits		

Slave Address: equivalent to chip-select line

Command Byte: selects which register you are reading from

Slave Address: repeated due to change in data-flow direction

Data Byte: reads from the register set by the command byte

Send Byte Format

S	ADDRESS	WR	A	COMMAND	A	P
	7 bits			8 bits		

Command Byte: sends command with no data, usually used for one-shot command

Receive Byte Format

S	ADDRESS	RD	A	DATA	$\overline{A}$	P
	7 bits			8 bits		

Data Byte: reads data from the register commanded by the last read byte or write byte transmission; also used for SMBus alert response return address

S = START CONDITION
P = STOP CONDITION

SHADED = SLAVE TRANSMISSION
$\overline{A}$ = NOT ACKNOWLEDGED

Figure 2. I²C Protocols

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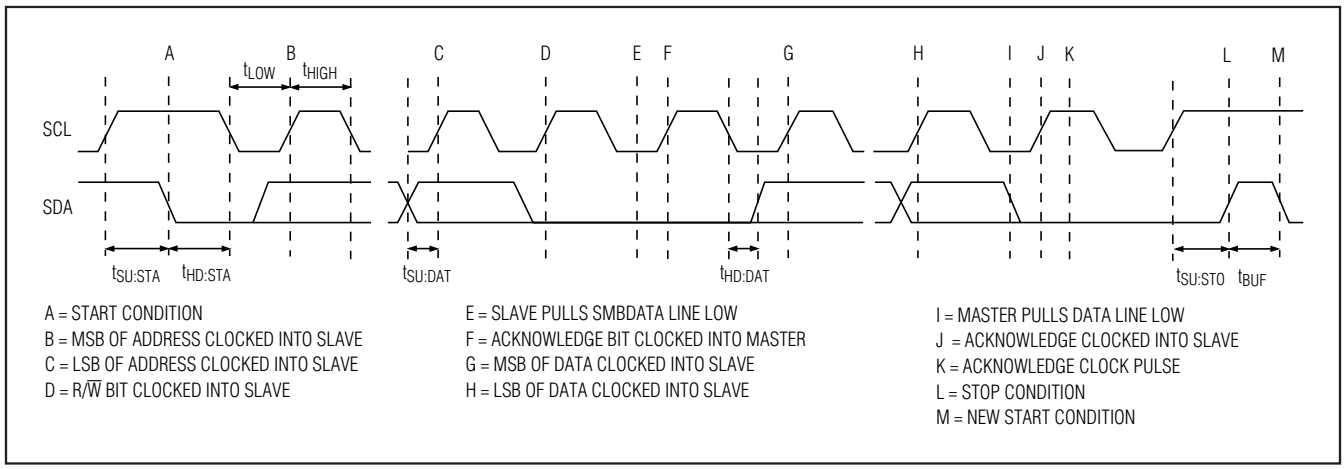

Figure 3. I²C Write Timing Diagram

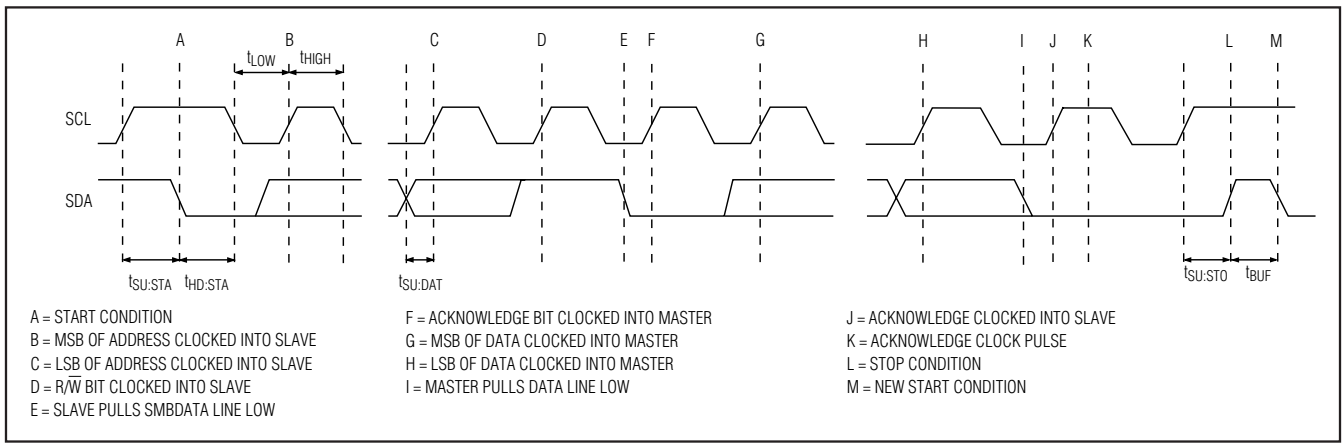

Figure 4. I²C Read Timing Diagram

START and STOP Conditions

The master initiates a transmission with a START condition (S), a high-to-low transition on SDA with SCL high. The master terminates a transmission with a STOP condition (P), a low-to-high transition on SDA while SCL is high (Figure 3). The STOP condition frees the bus and places all devices in F/S mode (Figure 1). Use a repeated START condition (Sr) in place of a STOP condition to leave the bus active and in its current timing mode.

Acknowledge Bits

Successful data transfers are acknowledged with an acknowledge bit (A) or a not-acknowledge bit ($\overline{A}$). Both the master and the MAX6620 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (9th pulse), and keep it low during the high period of the clock pulse (Figure 4). To generate a not acknowledge, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves it high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the master should reattempt communication at a later time.

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Slave Address

A master initiates communication with a slave device by issuing a START condition followed by a slave address byte. As shown in Figure 5, the slave address byte consists of 7 address bits and a read/write bit (R/$\overline{W}$). When idle, the MAX6620 continuously waits for a START condition followed by its slave address. The first four bits (MSBs) of the slave address have been factory programmed and are always **0101** and the seventh bit is **0**. Connect ADDR to GND or V_{CC}, or leave it unconnected to program D2 and D1 of the slave address according to Table 1.

Table 1. Slave Address Setting with ADDR Pin

ADDR CONNECTION	SLAVE ADDRESS	
	HEX	BINARY
GND	0x50	0101 000
Unconnected	0x52	0101 010
V_{CC}	0x54	0101 100

After receiving the address, the MAX6620 (slave) issues an acknowledgement by pulling SDA low for one clock cycle.

Data Byte (Read and Write)

Single Read and Burst Read. A single read begins with the bus master issuing a START condition followed by the seven slave ID address bits and a zero (WR, Figure 2), which is followed by an acknowledge bit (A) from the slave corresponding to the slave ID. Next, the master sends out an 8-bit register address, which is also followed by an acknowledge bit from the slave. The bus master issues another START condition and the same seven slave ID address bits followed by a one (RD, Figure 2), with the slave producing an acknowledge bit. The slave then sends out the 8-bit data corresponding to the register address previously written by the master. The bus master sends back a not-acknowledge bit ($\overline{A}$). This completes the single read process and a STOP condition is issued by the bus master.

In a burst read, the process is the same as a single read except that the bus master issues an acknowledge bit after each byte transmitted by the slave. After each acknowledge bit, the register address increments by one, and the data from the next register is transmitted by the slave. The process continues, with data reads followed by acknowledges. After the register with the highest address is read, the register pointer rolls over to point to the first register. To terminate a burst read, the bus master issues a STOP condition.

Single Write and Burst Write. A single write begins with the bus master issuing a START condition followed by the seven slave ID address bits and a zero (WR, Figure 2), which is followed by an acknowledge bit (A) from the slave corresponding to the slave ID. Next, the master sends out an 8-bit register address, which is also followed by an acknowledge bit from the slave. After the acknowledge bit, 8-bit data is written to the register, and the slave issues a third acknowledgement. A STOP condition is issued by the bus master to complete the single write process.

In a burst write, the process is similar to a single write except that the master does not issue a STOP condition immediately after the first byte has been written. After the first write is completed, the slave issues an acknowledge bit, the register address increments by one, and the data to be written to the next register is transmitted by the master. The process continues, with data writes followed by acknowledges. After the register with the highest available address is written, the register pointer rolls over to point to the first register. To terminate a burst write, the bus master issues a STOP condition.

Fan Drive

The MAX6620 uses external pass transistors to power the fans. DACOUT1–DACOUT4 adjust the power-supply voltage for each fan by driving the base of a PNP bipolar transistor, or the gate of a p-MOSFET. The resulting fan-supply voltage is fed back to DACFB_. This closes the voltage feedback loop. The system power supply for the output devices is V_{FAN}. V_{FAN} is

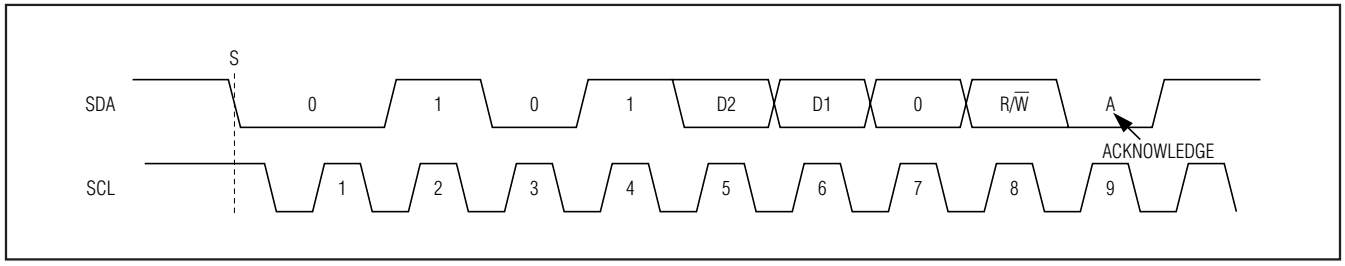

Figure 5. MAX6620 Slave Address Byte

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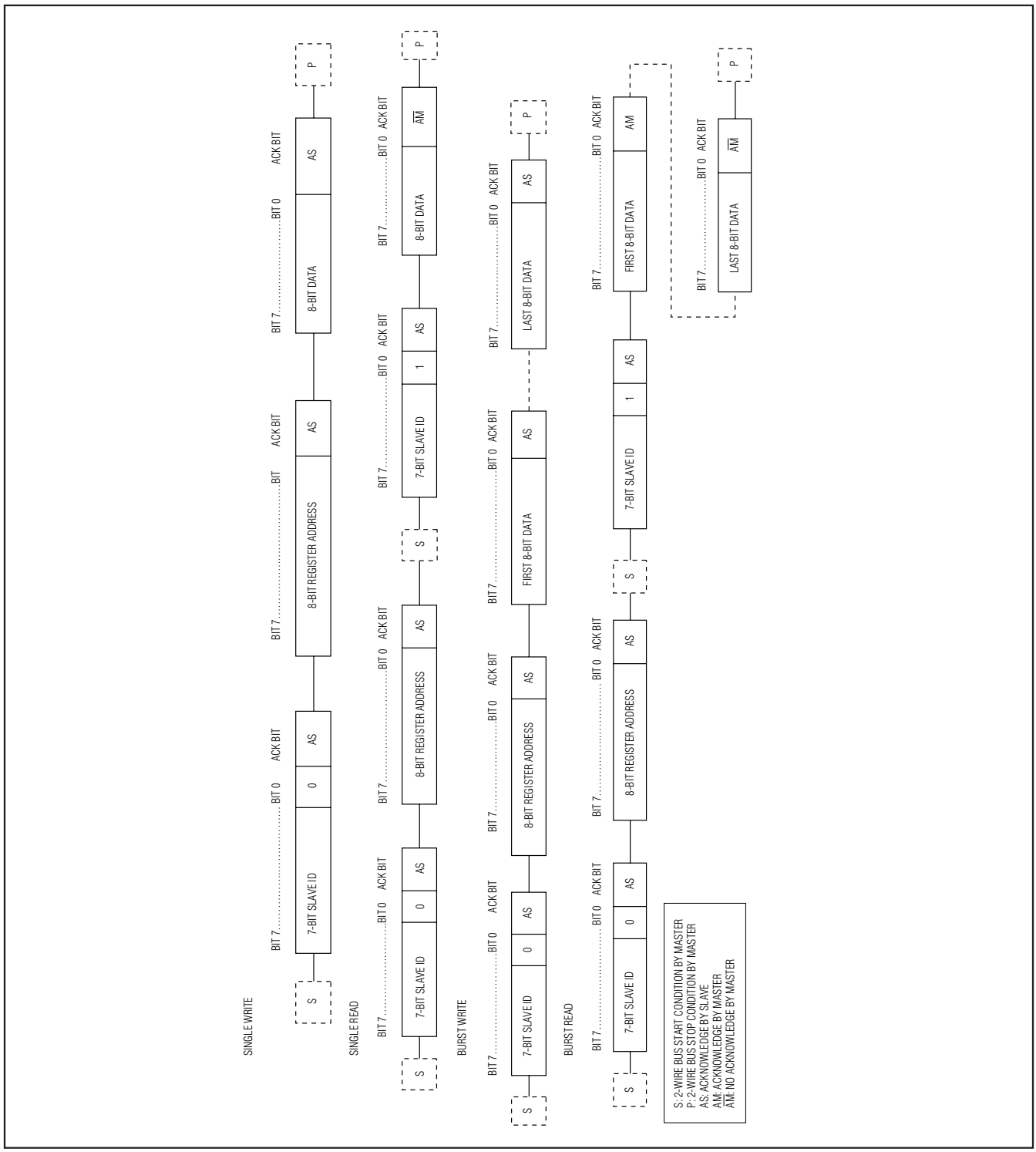

Figure 6. Read and Write Summary

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nominally 12V or 5V. The drive to the fans is proportional to V_{FAN}. See the *Fan_ Target Drive Voltage Registers* and the *Applications Information* sections for more details.

Fan-Speed Control

DAC (Voltage) Mode. In DAC mode, the MAX6620 simply sets the voltage that powers the fan. The fan's speed is related, but not precisely proportional to, the drive voltage. The drive voltage is set by the Fan_ Target Drive Voltage registers and may be read from the Fan_ Drive Voltage registers. Because the output voltage can ramp to new values at a controlled rate, the values in the two registers may be different. See the *Register Descriptions* and *Applications Information* sections for details.

RPM Mode. In RPM mode, the MAX6620 monitors tachometer output pulses from the fan and adjusts the fan drive voltage to force the fan's speed to the desired value. Fan speed is measured by counting the number of internal 8192Hz clock cycles that take place during a selectable number of tachometer periods. The number of clock cycles counted (11-bit value) is stored in the Fan_ TACH Count registers, and the desired number of cycles is stored in the Fan_ Target TACH Count registers. See the *Register Descriptions* and *Applications Information* sections for details.

Rate-of-Change Control. Sudden changes in fan speed can be easily heard by users. The MAX6620 helps reduce the audibility of fan-speed changes by controlling the rate at which the drive to the fan is incremented. Four bits in the Fan_ Dynamics registers set the rate at which the fan drive voltage is incremented. This allows the time required for a change in fan speed to be varied from 0 (in DAC mode only) to several minutes. See the *Register Descriptions* and *Applications Information* sections for details.

Monitoring Tachometer Signals. The TACH_ inputs accept tachometer or "locked-rotor" output signals from 3- or 4-wire fans. When measuring fan speed, the MAX6620 counts the number of internal 8192Hz clock cycles that occur during 1, 2, 4, 8, 16, or 32 tachometer periods. The number of tachometer periods is selectable for each fan by using the appropriate Fan_ Dynamics register. Tachometer pulses <25µs in duration are ignored to minimize the effect of noise on the tachometer lines.

The TACH count for a given RPM can be obtained from the following equation:

$$\text{TACH count} = \frac{60}{NP \times RPM} \times SR \times 8192 = \frac{491520 \times SR}{NP \times RPM}$$

where:

NP = number of tachometer pulses per revolution. Most general-purpose brushless DC fans produce two tachometer pulses per revolution.

SR = 1, 2, 4, 8, 16, or 32. See the Fan_ Speed Range information in the *Fan_ Dynamics Register*s *(06h, 07h, 08h, 09h)—POR = 0100 1100* section.

The tachometer count consists of 11 bits in the Fan_ TACH Count registers and is available in RPM and DAC modes. In RPM mode, the desired fan count is written to the Fan_ Target TACH Count registers.

Fan Failure Detection

When enabled, the MAX6620 monitors the TACH_ inputs to determine when a fan has failed. For fans with tachometer outputs, failure is detected in various ways depending on the fan control mode. In every case, four consecutive fault detections are required to decide whether the fan has failed. In DAC mode, the Fan_ Target TACH Count registers hold the upper limit for tachometer count values; a fault condition is identified when a TACH count exceeds the value written to the Fan_ Target TACH Count registers for more than 1s. In RPM mode, a fault condition is identified when any of the following three conditions occur for more than 1s: 1) the TACH count exceeds the value of the Fan_ Target TACH Count registers while the fan drive voltage is at full-scale, 2) the TACH count exceeds two times the Fan_ Target TACH Count value, or 3) the TACH count reaches its full count of 7FF.

Some fans have locked rotor outputs that produce a logic-level output to indicate that the fan has stopped spinning. These signals can be monitored by setting D2:D1 in the Fan_ Configuration registers. D2 selects locked rotor or tachometer monitoring and D1 selects the polarity of the locked rotor signal. A fan fault has occurred when a locked rotor signal has been present for 1s.

Fan failure is indicated in the Fan Fault register and also with the open-drain $\overline{FAN\_FAIL}$ output. The $\overline{FAN\_FAIL}$ output may be masked using the mask bits in the Fan Fault register. When a fan failure is detected, drive to the affected fan is removed. Drive may be restored by writing a new DAC or fan count target to the fan's control registers. The global configuration regis-

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ter's bit D4 can be used to cause a fan failure to force the remaining fan speeds to 100%.

Watchdog

The MAX6620 includes an optional I²C watchdog function that monitors the I²C bus for transactions. When the watchdog function is enabled, all fans will be forced to full speed if no I²C transactions occur within a selected period (2s, 6s, or 10s).

Spin-Up

When a fan is not spinning, and a voltage less than the nominal fan-supply voltage is applied to its power-supply terminals, it may fail to start spinning. To overcome this, the full nominal supply voltage may be applied to the fan terminals for a short time before a lower voltage is applied. This "spin-up" period allows the fan to overcome inertia and begin operating. Spin-up is controlled using the Fan_ Configuration registers. Spin-up can be disabled, or it can cause the fan to be driven with the full supply voltage until it produces two tachometer pulses, up to a maximum of 0.5s, 1s, or 2s when the fan is started.

POR Options

Three inputs allow set up of the MAX6620's behavior at power-up. These inputs are sampled when power is first applied to the MAX6620:

- **WD_START.** Connect WD_START to V_{CC} to enable, or to ground to disable, the watchdog function. When enabled using WD_START, the timeout period is 10s. After power is applied, the watchdog function may be enabled or disabled through the global configuration register.
- **SPINUP_START.** At power-up, spin-up operation is controlled by the SPINUP_START pin, which can be connected to ground (spin-up disabled), V_{CC} (spin-up for a maximum of 1s), or unconnected (spin-up for a maximum of 0.5s).
- **DAC_START.** This input controls the fan drive voltage (for all four fans) at power-up. When connected to ground, the initial fan drive voltage will be 0V. When connected to V_{CC}, the initial fan drive voltage will be full scale. When unconnected, the initial fan drive voltage will be 75% of V_{FAN}.

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Registers

Register Map

R/W	REGISTER NO./ADDRESS	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R/W	00h	0000 0XXX	Global Configuration	$\overline{\text{Run}}$: 0 = run 1 = standby	POR: 0 = normal 1 = reset	Bus Tmeout (35ms): 0 = enabled 1 = disabled	Fans to 100% on failure: 0 = enabled 1 = disabled	OSC: 0 = internal 1 = XTAL	I^2C Watchdog: 00 = No watchdog 01 = 2s 10 = 6s 11 = 10s		I^2C Watchdog Status (read only): 1 = elapsed
R/W	01h	0000 1111	Fan Fault	Fan 4 Fault	Fan 3 Fault	Fan 2 Fault	Fan 1 Fault	Fan 4 Mask	Fan 3 Mask	Fan 2 Mask	Fan 1 Mask
R/W	02h	0XX0 0000	Fan 1 Configuration	Mode: 0 = DAC 1 = RPM	Spin-Up: 00 = No spin-up 01 = two TACH counts or 0.5s 10 = two TACH counts or 1s 11 = two TACH counts or 2s			TACH input enable	TACH/ Locked Rotor: 0 = TACH 1 = locked rotor	Locked Rotor Polarity: 0 = low 1 = high	
R/W	03h	0XX0 0000	Fan 2 Configuration	Same as Fan 1 Configuration							
R/W	04h	0XX0 0000	Fan 3 Configuration	Same as Fan 1 Configuration							
R/W	05h	0XX0 0000	Fan 4 Configuration	Same as Fan 1 Configuration							
R/W	06h	0100 1100	Fan 1 Dynamics	Speed Range (TACH periods): 000 = 1 001 = 2 010 = 4 011 = 8 100 = 16 101 = 32 110 = 32 111 = 32			DAC Rate-of-Change: 000 = 0s per LSB (DAC mode) 0.0625s per LSB (RPM mode) 001 = 0.015625s per LSB 010 = 0.03125s per LSB 011 = 0.0625s per LSB 100 = 0.125s per LSB 101 = 0.25s per LSB 110 = 0.5s per LSB 111 = 1s per LSB				
R/W	07h	0100 1100	Fan 2 Dynamics	Same as Fan 1 Dynamics							
R/W	08h	0100 1100	Fan 3 Dynamics	Same as Fan 1 Dynamics							
R/W	09h	0100 1100	Fan 4 Dynamics	Same as Fan 1 Dynamics							

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Register Map (continued)

R/W	REGISTER NO./ADDRESS	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R	10h	1111 1111	Fan 1 TACH Count	D10	D9	D8	D7	D6	D5	D4	D3
	11h	1110 0000		D2	D1	D0	—	—	—	—	—
R	12h	1111 1111	Fan 2 TACH Count	Same as Fan 1 TACH Count							
	13h	1110 0000									
R	14h	1111 1111	Fan 3 TACH Count	Same as Fan 1 TACH Count							
	15h	1110 0000									
R	16h	1111 1111	Fan 4 TACH Count	Same as Fan 1 TACH Count							
	17h	1110 0000									
R	18h	0000 0000	Fan 1 Drive Voltage	D8	D7	D6	D5	D4	D3	D2	D1
	19h	0000 0000		D0	—	—	—	—	—	—	Full
R	1Ah	0000 0000	Fan 2 Drive Voltage	Same as Fan 1 Drive Voltage							
	1Bh	0000 0000									
R	1Ch	0000 0000	Fan 3 Drive Voltage	Same as Fan 1 Drive Voltage							
	1Dh	0000 0000									
R	1Eh	0000 0000	Fan 4 Drive Voltage	Same as Fan 1 Drive Voltage							
	1Fh	0000 0000									
R/W	20h	0011 1100	Fan 1 Target TACH Count	D10	D9	D8	D7	D6	D5	D4	D3
	21h	0000 0000		D2	D1	D0	—	—	—	—	—
R/W	22h	0011 1100	Fan 2 Target TACH Count	Same as Fan 1 Target TACH Count							
	23h	0000 0000									
R/W	24h	0011 1100	Fan 3 Target TACH Count	Same as Fan 1 Target TACH Count							
	25h	0000 0000									
R/W	26h	0011 1100	Fan 4 Target TACH Count	Same as Fan 1 Target TACH Count							
	27h	0000 0000									
R/W	28h	XXXX XXXX	Fan 1 Target Drive Voltage	D8	D7	D6	D5	D4	D3	D2	D1
	29h	X000 0000		D0	—	—	—	—	—	—	—
R/W	2Ah	XXXX XXXX	Fan 2 Target Drive Voltage	Same as Fan 1 Target Drive Voltage							
	2Bh	X000 0000									
R/W	2Ch	XXXX XXXX	Fan 3 Target Drive Voltage	Same as Fan 1 Target Drive Voltage							
	2Dh	X000 0000									
R/W	2Eh	XXXX XXXX	Fan 4 Target Drive Voltage	Same as Fan 1 Target Drive Voltage							
	2Fh	X000 0000									

X = Depends on input states at power-up.

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Quad Linear Fan-Speed Controller

Register Descriptions

Global Configuration Register (00h)—POR = 0000 0XXX

BIT	R/W	FUNCTION
7	R/W	**Run:** 0 = run 1 = standby
6	R/W	**POR:** 0 = normal operation 1 = reset all registers to POR values This bit automatically resets itself and will always return a 0 when read.
5	R/W	**I²C Bus Timeout:** 0 = enabled 1 = disabled The I²C interface will reset if SDA is low for more than 35ms.
4	R/W	**Fans to 100% on failure:** 0 = if a fan failure is detected, all other fan channels immediately go to full-scale drive voltage to ensure adequate cooling 1 = disabled
3	R/W	**Oscillator Selection:** Selects on-chip oscillator or 32.768kHz crystal/ceramic resonator. Use crystal if 1% RPM accuracy is required. 0 = internal oscillator (default at power-on) 1 = external 32.768kHz crystal When switching from the internal oscillator to an external crystal, the MAX6620 operates from the internal oscillator until the crystal oscillator has started up. If the crystal is damaged or the oscillator fails to start, the MAX6620 will continue to operate from the internal oscillator.

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Global Configuration Register (00h)—POR = 0000 0XXX (continued)

<table>
<tr><th>BIT</th><th>R/W</th><th>FUNCTION</th></tr>
<tr><td>2</td><td rowspan="2">R/W</td><td rowspan="2">I²C Watchdog:
When active, the watchdog monitors SDA and SCL for valid I²C transactions. If there are no valid transactions between the master and the MAX6620 within the watchdog period, all fan output voltages will go to full-scale drive voltage.

If the watchdog times out and valid I²C transactions begin to occur again, operation will resume with the previous DAC value. The master can then program the output voltages, target TACH counts, or other functions in the normal manner.

When the watchdog function is active, ensure that the master communicates to the MAX6620 periodically, for example reading a status register.

The POR state is set by the state of the WD_START pin at power-up.
<table>
<tr><th>D2:D1</th><th>I²C WATCHDOG PERIOD (s)</th><th>POR CONDITION</th></tr>
<tr><td>00</td><td>Inactive (no watchdog)</td><td>WD_START = GND</td></tr>
<tr><td>01</td><td>2</td><td>—</td></tr>
<tr><td>10</td><td>6</td><td>—</td></tr>
<tr><td>11</td><td>10</td><td>WD_START = V_{CC}</td></tr>
</table>
</td></tr>
<tr><td>1</td></tr>
<tr><td>0</td><td>R</td><td>I²C Watchdog Status:
0 = I²C transactions occurred within watchdog period
1 = time between I²C transaction exceeds watchdog period
This bit is cleared by I²C read from this register.</td></tr>
</table>

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Fan Fault Register (01h)—POR = 0000 1111

<table>
<tr><th>BIT</th><th>R/W</th><th>FUNCTION</th></tr>
<tr><td>7</td><td>R</td><td>Fan 4 Fault Status:
Indicates which fans have had faults detected. When a fan fault is detected, the drive to the fan is disabled and the corresponding fault bit is set. The fault bits latch until they are cleared by reading, thus allowing short-term faults to be identified. After a fault status bit is cleared by reading, the corresponding output voltage will remain zero until a Fan_ Target Drive Voltage register or Fan_ Target TACH Register is written. Writing a new target drive voltage or target TACH count will cause drive to be applied to the fan again, at which time a new failure-detection cycle will begin.
Fault Conditions Are:
<table>
<tr><th>MODE</th><th>FAN_ DRIVE VOLTAGE REGISTER</th><th>CONDITION</th><th>TIME (s)</th></tr>
<tr><td rowspan="2">DAC</td><td rowspan="2">Any</td><td>TACH count exceeds value of Fan_ Target TACH count</td><td rowspan="2">>1</td></tr>
<tr><td>Locked rotor asserts</td></tr>
<tr><td rowspan="3">RPM</td><td>1FF (full)</td><td>TACH count exceeds value of Fan_ Target TACH Count</td><td rowspan="3">>1</td></tr>
<tr><td rowspan="2"><1FF</td><td>TACH count exceeds two times of Fan_ Target TACH Count value</td></tr>
<tr><td>TACH count reaches it full count of 7FF</td></tr>
</table>
$\overline{\text{FAN\_FAIL}}$ will be asserted when four consecutive faults are detected.</td></tr>
<tr><td>6</td><td>R</td><td>Fan 3 Fault Status</td></tr>
<tr><td>5</td><td>R</td><td>Fan 2 Fault Status</td></tr>
<tr><td>4</td><td>R</td><td>Fan 1 Fault Status</td></tr>
<tr><td>3</td><td>R/W</td><td>Fan 4 Fault Mask:
Masks faults on selected fans from asserting the $\overline{\text{FAN\_FAIL}}$ output. Faults will still be indicated by the fault status bits:
0 = not masked
1 = masked</td></tr>
<tr><td>2</td><td>R/W</td><td>Fan 3 Fault Mask</td></tr>
<tr><td>1</td><td>R/W</td><td>Fan 2 Fault Mask</td></tr>
<tr><td>0</td><td>R/W</td><td>Fan 1 Fault Mask</td></tr>
</table>

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Fan_ Configuration Registers (02h, 03h, 04h, 05h)—POR = 0XX0 0000

<table>
<tr><th>BIT</th><th>R/W</th><th>FUNCTION</th></tr>
<tr><td>7</td><td>R/W</td><td>RPM/DAC:
0 = DAC mode. The fan drive voltage is set by the value in the Fan_ Target Drive Voltage register.
1 = RPM mode. The fan drive voltage is adjusted to produce the TACH count value in the Fan_ Target TACH Count register.

When changing from DAC to RPM mode, if the current RPM value is different from the value selected in the Fan_ Target TACH Count register, the drive voltage will start from the current value and increment/decrement toward the desired value at the selected DAC rate-of-change.</td></tr>
<tr><td>6</td><td rowspan="2">R/W</td><td rowspan="2">Spin-Up:
When the fan drive voltage increases from 0V to a value less than the full-scale drive voltage, it may be necessary to drive the fan with the full-scale drive voltage for a brief period to ensure that the fan is spinning before reducing the drive to the selected value.

When spin-up is selected, the fan is driven at the full-scale drive voltage until two tachometer pulses have been detected or locked rotor has been cleared. A maximum spin-up time is also selectable to ensure that the spin-up time is not excessive. After two tachometer pulses have been detected, or locked rotor has been cleared or the spin-up has timed out, the drive voltage goes to the value in the Fan_ Target Drive Voltage register.

The POR state is set by the state of the SPINUP_START pin at power-up.

<table>
<tr><th>D6:D5</th><th>FUNCTION</th><th>POR CONDITION</th></tr>
<tr><td>00</td><td>No spin-up</td><td>SPIN_START pin = ground</td></tr>
<tr><td>01</td><td>Spin-up until two tachometer pulses or clearing of locked rotor, or 0.5s (max)</td><td>SPIN_START pin = open</td></tr>
<tr><td>10</td><td>Spin-up until two tachometer pulses or clearing of locked rotor, or 1s (max)</td><td>SPIN_START pin = V_{CC}</td></tr>
<tr><td>11</td><td>Spin-up until two tachometer pulses or clearing of locked rotor, or 2s (max)</td><td>—</td></tr>
</table></td></tr>
<tr><td>5</td></tr>
<tr><td>4</td><td></td><td>Reserved</td></tr>
<tr><td>3</td><td>R/W</td><td>TACH Input Enable:
Enables TACH input function and fan fault detection (automatically enabled in RPM mode).
0 = disabled. When disabled and TACH input is not used, bit 1 and bit 2 are ignored.
1 = enabled</td></tr>
<tr><td>2</td><td>R/W</td><td>TACH/Locked Rotor:
Selects TACH input function as TACH count or locked rotor. In locked rotor mode, the TACH count stops and assertion of the TACH input indicates that the fan has stopped.
0 = TACH count
1 = locked rotor</td></tr>
<tr><td>1</td><td>R/W</td><td>Locked Rotor Polarity:
0 = low locked rotor. TACH input low in locked rotor mode indicates fan is stopped.
1 = high locked rotor. TACH input high in locked rotor mode indicates fan is stopped.</td></tr>
<tr><td>0</td><td>—</td><td>Reserved</td></tr>
</table>

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Quad Linear Fan-Speed Controller

Fan_ Dynamics Registers (06h, 07h, 08h, 09h)—POR = 0100 1100

<table>
<tr><th>BIT</th><th>R/W</th><th>FUNCTION</th></tr>
<tr><td>7</td><td>R/W</td><td rowspan="3">Fan_ Speed Range:
The MAX6620 determines fan speed by counting the number of internal 8192Hz clock cycles (using an 11-bit counter) during one or more fan tachometer periods. Three bits set the nominal RPM range for the fan, as shown in the table below. As an example, a setting of 010 causes the MAX6620 to count the number of 8192Hz clock cycles that occur during four complete tachometer periods. If the fan has a nominal speed of 2000RPM and two tachometer pulses per revolution, one tachometer period will be nominally 15ms, and four tachometer periods will be 60ms. With an 8192Hz clock, the TACH count will therefore be equal to 491. With a fan speed of 1/3 the nominal value, the count will be 1474. If the fan's nominal speed is 1000RPM, the full-speed TACH count will be 983. At 1/3 the nominal speed, there will be 2948 clock cycles in four tachometer periods. This is greater than the maximum 11-bit count of 2047, so four tachometer periods is too many for this fan; a setting of 001 (two clock cycles) is recommended instead.

The table below shows the full-speed tachometer counts for several combinations of nominal fan speeds and D7:D5 settings. The shaded combinations will provide the best results. When setting D7:D5, the goal is to obtain the highest tachometer count without exceeding the maximum count of 2047 when the fan is at the minimum speed of interest. For example, if the minimum speed of interest is 1/3 of full speed, the maximum tachometer count will be three times the value shown in the table below:

Tachometer Counts/(Counting Period) (8192Hz Clock Used):</td></tr>
<tr><td>6</td><td>R/W</td></tr>
<tr><td>5</td><td>R/W</td></tr>
</table>

D7:D5	NUMBER OF TACH PERIODS COUNTED	RPM					
		500	1000	2000	4000	8000	16000
000	1	**491** (60ms)	**245** (30ms)	**122** (15ms)	**61** (7.5ms)	**30** (3.75ms)	**15** (1.875ms)
001	2	**983** (120ms)	**491** (60ms)	**245** (30ms)	**122** (15ms)	**61** (7.5ms)	**30** (3.75ms)
010	4	**1966** (240ms)	**983** (120ms)	**491** (60ms)	**245** (30ms)	**122** (15ms)	**61** (7.5ms
011	8	**2047** (480ms)	**1966** (240ms)	**983** (120ms)	**491** (60ms)	**245** (30ms)	**122** (15ms)
100	18	**2047** (960ms)	**2047** (480ms)	**1966** (240ms)	**983** (120ms	**491** (60ms)	**245** (30ms
101, 110, 111	32	**2047** (1920ms)	**2047** (960ms)	**2047** (480ms)	**1966** (240ms)	**983** (120ms)	**491** (60ms)

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Fan_ Dynamics Registers (06h, 07h, 08h, 09h)—POR = 0100 1100 (continued)

<table>
<tr><th>BIT</th><th>R/W</th><th>FUNCTION</th></tr>
<tr><td>4

3

2</td><td>R/W

R/W

R/W</td><td>Fan_ DAC Rate-of-Change:
The fan drive voltage (at the DACFB_ inputs) varies from 0 to full scale in 512 increments. The rate-of-change bits determine the time interval between output voltage increments/decrements. In RPM mode, a setting of 0 would result in an unstable feedback loop, so a default value of 0.0625 is in effect when 0 is selected.

Regardless of the settings, there are a few cases for which the rate-of-change is always 0:
• When a target TACH count of 2047 (7FF) is selected, the fan drive voltage immediately goes to 0V. A full-scale target count is assumed to mean that the intent is to shut down the fan, and going directly to 0 drive avoids the possibility of loss of control-loop feedback at high TACH counts. If a slow- speed decrease toward 0 is desired, a target TACH count at the slowest practical value for the fan should be chosen. Once that count has been reached, selecting a count of 2047 (7FF) will then take the drive immediately to 0V.
• When a target fan drive voltage of 0V is selected, the drive voltage immediately goes to 0V. Again, it is assumed that the intent is to shut down the fan. If a slow-speed decrease toward 0 is desired, a target fan drive voltage of the slowest practical value for the fan in question should be chosen. Once that drive voltage has been reached, selecting a target value of 0 will then take the drive immediately to 0V.
• When the current drive level is 0 in DAC mode, selecting a new target fan drive voltage will immediately take the voltage to that value. The fan will spin-up first if spin-up is enabled.
• When the current drive level is 0 in RPM mode, selecting a new target TACH count that is less than 2047 (7FF) will immediately take the drive voltage to the value in the Fan_ Target Drive Voltage register. From this value, the drive voltage will increment as needed to achieve the desired TACH count. The fan will spin-up first if spin-up is enabled.
<table>
<tr><th rowspan="2">D4:D2</th><th colspan="2">TIME BETWEEN OUTPUT VOLTAGE INCREMENTS (s)</th><th rowspan="2">TIME FROM 33% TO 100% (s)</th></tr>
<tr><th>DAC MODE</th><th>RPM MODE</th></tr>
<tr><td>000</td><td>0</td><td>0.0625</td><td>0</td></tr>
<tr><td>001</td><td colspan="2">0.015625</td><td>10</td></tr>
<tr><td>010</td><td colspan="2">0.03125</td><td>20</td></tr>
<tr><td>011</td><td colspan="2">0.0625 (default)</td><td>40</td></tr>
<tr><td>100</td><td colspan="2">0.125</td><td>80</td></tr>
<tr><td>101</td><td colspan="2">0.25</td><td>160</td></tr>
<tr><td>110</td><td colspan="2">0.5</td><td>320</td></tr>
<tr><td>111</td><td colspan="2">1.0</td><td>640</td></tr>
</table>
</td></tr>
<tr><td>1</td><td>—</td><td>Reserved</td></tr>
<tr><td>0</td><td>—</td><td>Reserved</td></tr>
</table>

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Quad Linear Fan-Speed Controller

Fan_ TACH Count Registers (10h, 12h, 14h, 16h)—POR = 1111 1111

BIT	R/W	FUNCTION
7	R	**Fan_ TACH Count D10:D3:** Indicates the number of 8192Hz clock pulses counted during the counting period. The Fan_ TACH Count consists of 11 bits contained in two bytes. To minimize noise from spurious tachometer transitions, pulses less than 25µs are ignored.
6		
5		
4		
3		
2		
1		
0		

Fan_ TACH Count Registers (11h, 13h, 15h, 17h)—POR = 1110 0000

BIT	R/W	FUNCTION
7	R	**Fan_ TACH Count D7:D5**
6		
5		

Fan_ Drive Voltage Registers (18h, 1Ah, 1Ch, 1Eh)—POR = 0000 0000

BIT	R/W	FUNCTION
7	R	**Fan_ Drive Voltage D8:D1:** This is a 9-bit value that ranges from 0 to 511. This register shows the actual fan drive voltage. When the value in this register is 480V, the nominal fan drive voltage of V_{FAN} is supplied to the fan, as shown in the table in the *Fan_ Target Drive Voltage Registers* section.
6		
5		
4		
3		
2		
1		
0		

Fan_ Drive Voltage Registers (19h, 1Bh, 1Dh, 1Fh)—POR = 0000 0000

BIT	R/W	FUNCTION
7	R	**Fan_ Drive Voltage D0**
0	R	**Full-Scale Status:** 0 = DAC is driving with value of D8:D0 that is not at full scale 1 = DAC is driving with full scale voltage

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Fan_ Target TACH Count Registers (20h, 22h, 24h, 26h)—POR = 0011 1100

The Fan_ Target TACH Count consists of 11 bits contained in two bytes. The two bytes must be written in order in one or two I²C transactions, with no other I²C writes in between. These target registers are updated internally at the same time when a second byte (LSB) is written.

BIT	R/W	FUNCTION
7	R/W	**Fan_ Target TACH Count D10:D3:** In RPM mode, write the desired tachometer count to this register. The MAX6620 will then adjust the fan drive voltage to achieve this tachometer count. In DAC mode, this register has no effect. When changing from DAC mode to RPM mode, best results are obtained by loading this register with the desired TACH count before changing to RPM mode. The target TACH count for a given RPM will be obtained by the following equation: $$TargetTACH = \frac{60}{NP \times RPM} \times SR \times 8192$$ where: NP = number of TACH pulses per revolution SR = 1, 2, 4, 8, 16, or 32 (see the fan_ speed range information in the *Fan_ Dynamics Register*s *(06h, 07h, 08h, 09h)—POR = 0100 1100* section)
6		
5		
4		
3		
2		
1		
0		

Fan_ Target TACH Count Registers (21h, 23h, 25h, 27h)—POR = 0000 0000

BIT	R/W	FUNCTION
7	R	**Fan_ Target TACH Count D2:D0**
6		
5		

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Quad Linear Fan-Speed Controller

Fan_ Target Drive Voltage Registers (28h, 2Ah, 2Ch, 2Eh)—POR = XXXX XXXX

The Fan_ Target Drive Voltage consists of 9 bits contained in two bytes. The two bytes must be written in order in one or two I²C transactions with no other I²C writes in between. These target registers are updated internally at the same time when a second byte (LSB) is written.

<table>
<tr><th>BIT</th><th>R/W</th><th>FUNCTION</th></tr>
<tr><td>7
6
5
4
3
2
1
0</td><td>R/W</td><td>
Fan_ Target Drive Voltage D8:D1:
This is a 9-bit value that ranges from 0 to 511 and is contained in two bytes. In DAC mode, write the desired fan drive voltage to these two registers. The MAX6620 will then ramp the fan drive voltage to this value at a rate determined by the DAC rate-of-change bits.

In RPM mode, the value contained in this register will be the voltage applied to the fan immediately after spin-up or after changing the Fan_ Target TACH Count from 2047 (7FF) to a value lower than 2047 (7FF). For example, if the fan is currently stopped with spin-up disabled, and a new Fan_ Target TACH Count corresponding to 60% of the full-scale fan speed is to be selected, the fan voltage can be programmed to immediately go to 60% of the full-scale drive voltage when the new Fan_ Target TACH Count is selected from 2047 (7FF), and then close the RPM control loop starting from that voltage.

The register value is converted to the drive voltage at the fan (or voltage at DACFB_) as follows:
<table>
<tr><th colspan="2">D8:D0</th><th colspan="2">FAN_ DRIVE VOLTAGE (V)</th></tr>
<tr><th>DECIMAL</th><th>HEX</th><th>5V RANGE</th><th>12V RANGE</th></tr>
<tr><td>0</td><td>000h</td><td>0.000</td><td>0.000</td></tr>
<tr><td>200</td><td>0C8h</td><td>1.764</td><td>4.486</td></tr>
<tr><td>300</td><td>12Ch</td><td>2.646</td><td>6.729</td></tr>
<tr><td>400</td><td>190h</td><td>3.527</td><td>8.972</td></tr>
<tr><td>480</td><td>1E0h</td><td>4.232</td><td>10.766</td></tr>
<tr><td>511</td><td>1FFh</td><td>4.506</td><td>11.462</td></tr>
</table>

The value of the Fan_ Target Drive Voltage at POR depends on state of the DAC_START pin, as shown below:
<table>
<tr><th colspan="2">D8:D0</th><th rowspan="2">DAC_START</th></tr>
<tr><th>DECIMAL</th><th>HEX</th></tr>
<tr><td>0</td><td>000h</td><td>GND</td></tr>
<tr><td>384</td><td>180h</td><td>Open</td></tr>
<tr><td>511</td><td>1FF</td><td>VCC</td></tr>
</table>
</td></tr>
</table>

Fan_ Target Drive Voltage Registers (29h, 2Bh, 2Dh, 2Fh)—POR = X000 0000

Bit	R/W	FUNCTION
7	R	**Fan_ Target Drive Voltage D0**

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Applications Information

External Pass Transistors

Match external pass transistors to the fans being used. Ensure that the pass transistor is capable of handling the maximum fan current. For best results, the pass transistor's maximum current rating should be at least 50% greater than the fan's nominal supply current.

The transistor should also be capable of dissipating the worst-case power, which usually occurs when the fan is being driven to approximately 50% of the nominal supply voltage. The maximum power dissipation will depend on the thermal resistance of the transistor, its case, and the printed-circuit board (PCB) to which it is soldered. For example, if the worst-case transistor power dissipation occurs when the fan current is 100mA, and the voltage across the fan is 6.5V, the maximum power dissipation will be 650mW. A BCP69T1-D in a SOT223-4 package is rated at 1.5W at 25°C (about 1W at 70°C) when soldered to a 0.93in^2 (6cm^2) copper PCB pad, and can easily handle this power dissipation. Larger copper pads, packages with lower thermal resistance, or different transistors can give significantly different results.

The MAX6620 uses an advanced output driver design that eliminates the large external capacitors often connected across the fan's power-supply terminals. For stability with a variety of fans, connect a 0.1µF capacitor from DACFB_ to ground.

Using a Low-Dropout Voltage Regulator (LDO) as the Pass Device

Voltage regulators can be used instead of discrete transistors to drive the fans (Figure 7). The voltage feedback loop is closed around the regulator to provide the desired output voltage. When using a voltage regulator, note the following:

- Most regulators require relatively large capacitors at their inputs and outputs for stability.
- Most regulators have a lower output voltage limit that is >0V. If removing the drive from the fan is necessary when using a regulator, choose a regulator that has an on/off control input and drive that input from the system microcontroller.

Fan-Speed Control (DAC and RPM Modes)

The MAX6620 has two main modes for controlling fan speeds. In DAC mode, the MAX6620 produces an output voltage that drives the fan. This voltage is proportional to the main fan power-supply voltage (V_{FAN}). Write the 9-bit desired voltage value in the Fan_ Target Drive Voltage register.

In RPM mode, the MAX6620 monitors the tachometer signals from the fans through the TACH_ inputs and adjusts the drive voltage to yield the desire tachometer count. The tachometer count is the number of internal 8192 clock cycles that are counted during the selected number of tachometer pulses.

Controlling 2-Wire Fans (DAC Mode)

In DAC mode, the MAX6620 sets the fan's supply voltage to the value selected in the Fan_ Target Drive Voltage register. Tachometer monitoring is never done when controlling a 2-wire fan, so the TACH input enable bit in the Fan_ Configuration register should be set to 0. Enabling the TACH input when using a 2-wire fan will result in an erroneous fan failure detection.

Initial Settings:

- Begin with the POR settings. The POR value of the fan_ DAC rate-of-change bits (4:2 of the Fan_ Dynamics Register) can yield slower fan speed changes than desired. If this is the case, choose a faster value, such as 001.

Starting the Fan:

- Write the desired drive voltage value to the Fan_ Target Drive Voltage register.

Changing Speeds:

- Write the new desired drive voltage value to the Fan_ Target Drive Voltage register.

Stopping the Fan:

- Write a voltage value of 0 to the Fan_ Target Drive Voltage register.

Controlling 3-Wire Fans (DAC Mode)

In DAC mode, the MAX6620 sets the fan's supply voltage to the value selected in the Fan_ Target Drive Voltage register. 3-wire fans with tachometer outputs allow monitoring of the fan's speed to detect fan failure. To monitor a fan's speed, the TACH input should be enabled.

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Quad Linear Fan-Speed Controller

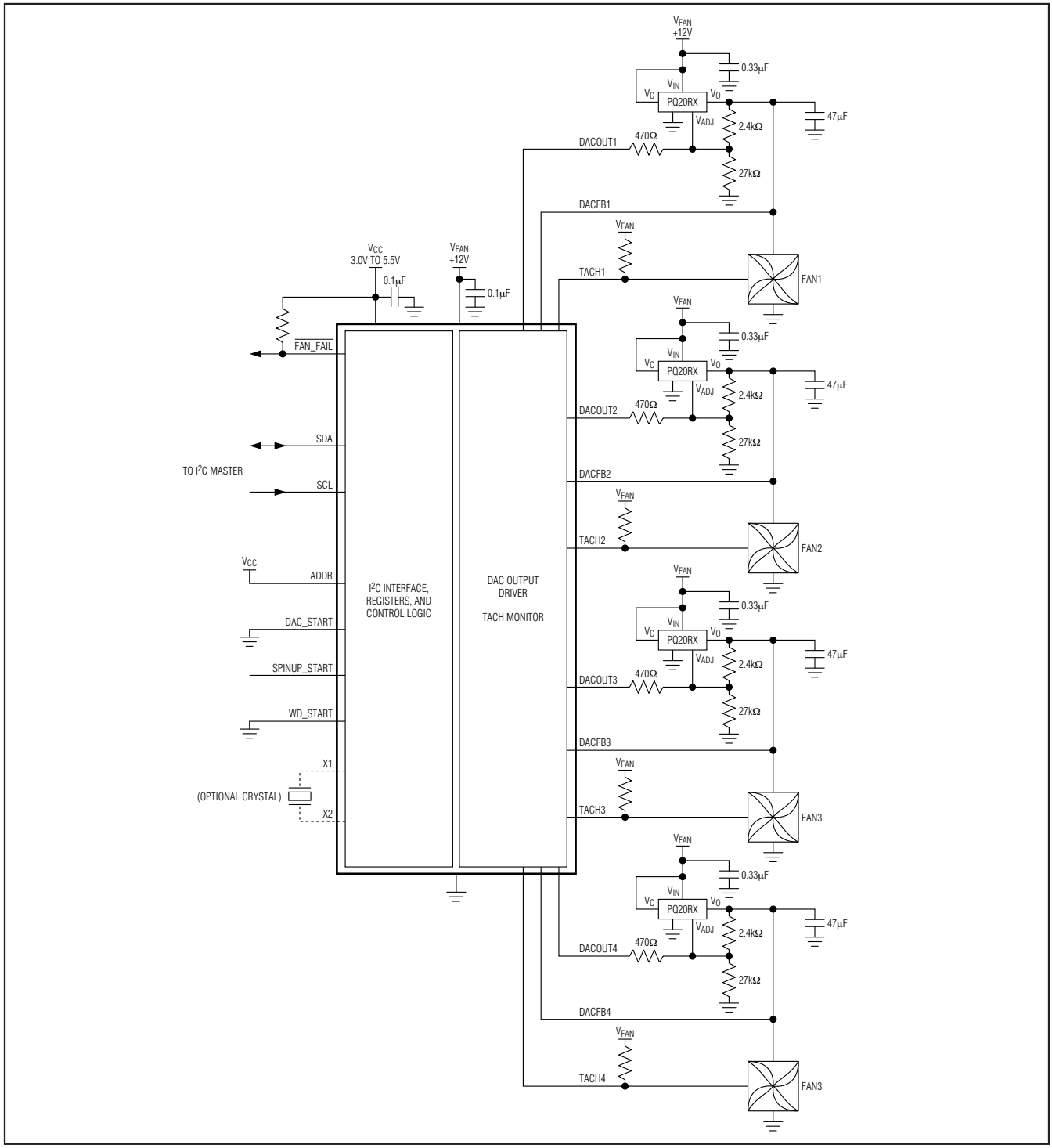

Figure 7. Using Low Dropout Voltage Regulators Instead of Discrete Transistors as the Pass Devices

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Initial Settings:

- Begin with the POR settings. The POR value of the fan_ DAC rate-of-change bits (4:2 of the Fan_ Dynamics register) can yield slower fan speed changes than desired. If this is the case, choose a faster value, such as 001.
- Write the desired number of tachometer periods to be counted in the speed range bits (7:5 of the Fan_ Dynamics register).
- Write the maximum allowable tachometer count to the Fan_ Target TACH Count registers. Tachometer counts greater than this value will result in a fan fault detection. Choose a value that will not be encountered during normal operation, accounting for normal fan speed tolerances.

  Note: Setting a full-scale target count (2047) will result in the fan drive going to 0V.
- Set the TACH input enable bit in the Fan_ Configuration register to 1.

  Note: This bit can be set after the fan has been started, if desired. If the bit is set before writing a target fan drive voltage, the target drive voltage should be set immediately after enabling the TACH input to avoid failure detection before the fan has started spinning.

Starting the Fan:

- Write the desired drive voltage value to the Fan_ Target Drive Voltage register.

Changing Speeds:

- Write the new desired drive voltage value to the Fan_ Target Drive Voltage register.

Stopping the Fan:

- Write a 0 to the TACH input enable bit in the Fan_ Configuration register. This prevents the MAX6620 from deciding that the fan has failed after it has stopped.
- Write a voltage value of 0V to the Fan_ Target Drive Voltage register.
- If a gradual decrease in fan speed is desired, write the lowest drive voltage at which the fan will reliably operate. When the drive voltage reaches that value, write 0V to the Fan_ Target Drive Voltage register.

Controlling 3-Wire Fans (RPM Mode)

Begin as in DAC mode and start the fan.

Changing from DAC Mode to RPM Mode:

- Write the desired tachometer count to the Fan_ TACH Count registers.
- Set bit 7 of the Fan_ Configuration register to 1. This selects RPM mode. The fan will go to the selected speed.

  Note: When the DAC rate-of-change is set to one of the faster values, the fan drive voltage can, depending on the fan's characteristics, undergo a slow oscillation. While this rarely has an audible impact, it can be reduced or eliminated by selecting a slower rate-of-change once the fan's speed has reached or approached its target value.

Changing Speeds:

- Write the desired tachometer count to the Fan_ Target TACH Count registers.

Stopping the Fan:

- Write the current drive voltage into the Fan_ Target Drive Voltage register.
- Write a value greater than the current tachometer count into the Fan_ Target TACH Count register.
- Write a 0 to bit 7 of the Fan_ Configuration register. This selects DAC mode.
- Write a 0 to the TACH input enable bit in the Fan_ Configuration register. This prevents the MAX6620 from detecting a high TACH count and determining that the fan has failed.
- Write a voltage value of 0V to the Fan_ Target Drive Voltage register.
- If a gradual decrease in fan speed is desired, write the lowest drive voltage at which the fan will reliably operate. When the drive voltage reaches that value, write 0 to the Fan_ Target Drive Voltage register.

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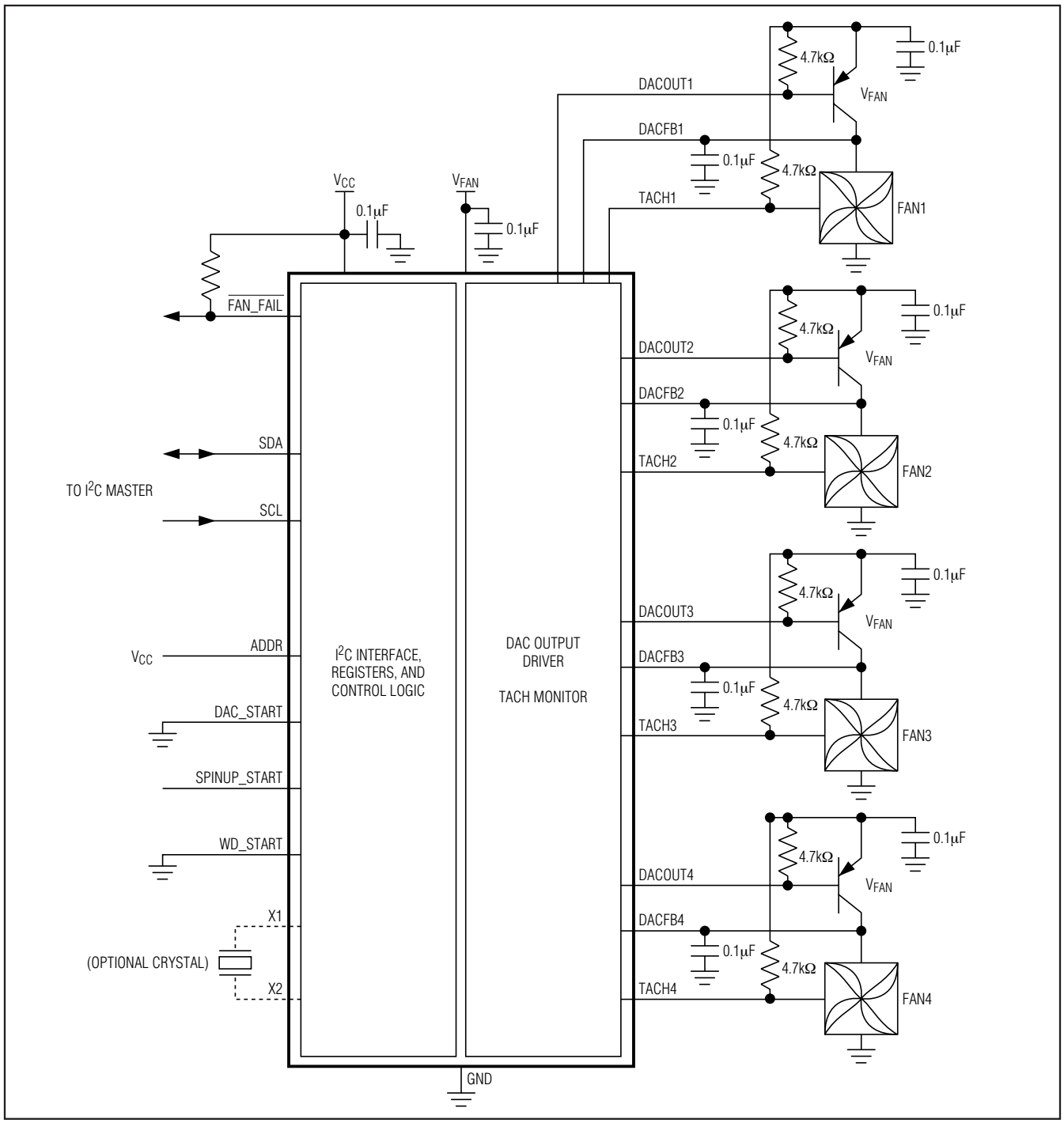
Quad Linear Fan-Speed Controller

Typical Application Circuit



Chip Information

PROCESS: CMOS

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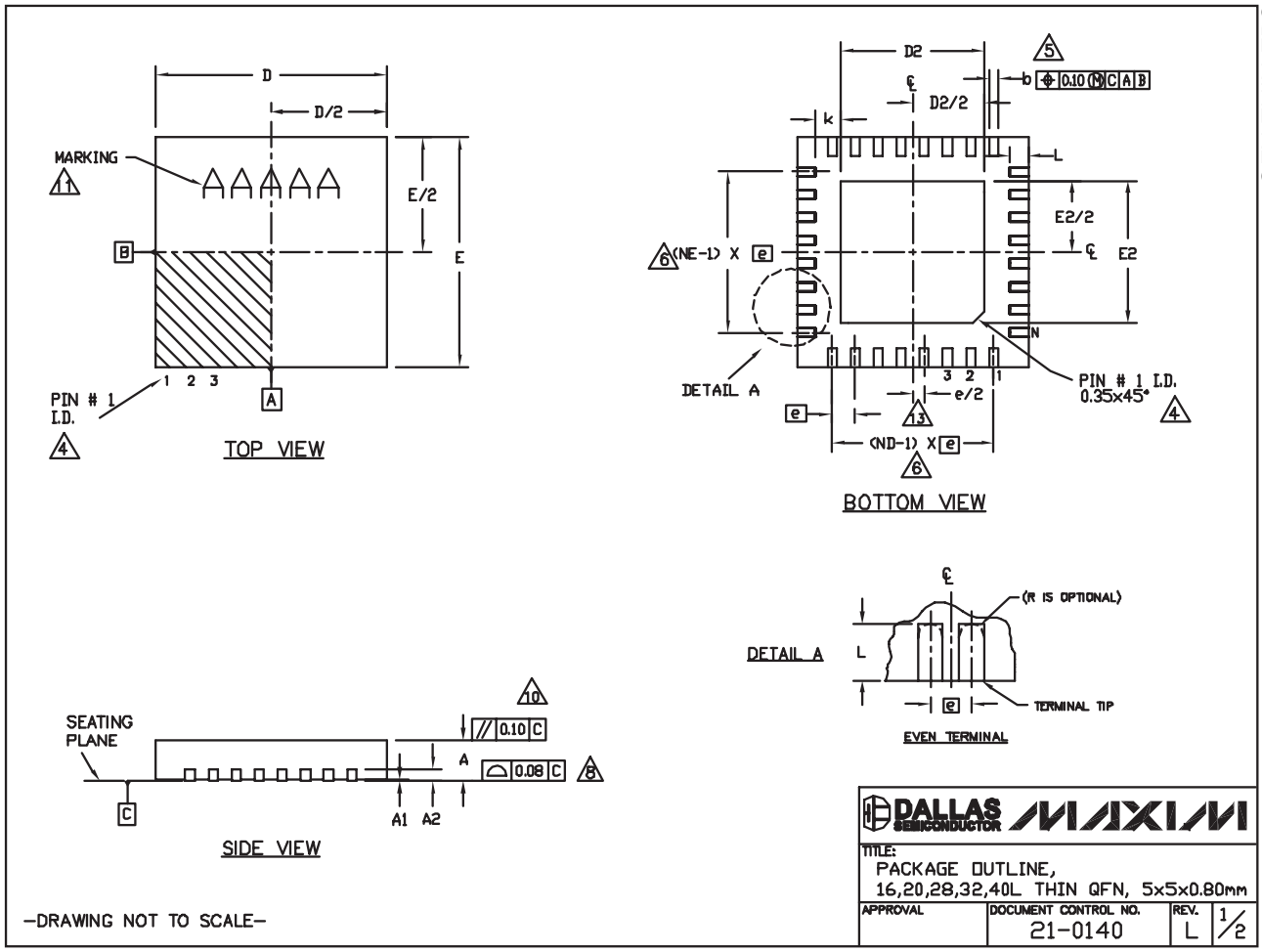
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



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Quad Linear Fan-Speed Controller

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	L	2/2

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