12-Bit Successive Approximation Integrated Circuit A/D Converter

AD572*

FEATURES

PERFORMANCE
- True 12-Bit Operation: Max Nonlinearity <±0.012%
- Low Gain T.C.: < ±15 ppm/°C (AD572B)
- Low Power: 900 mW
- Fast Conversion Time: < 25 µs
- Monotonic Feedback DAC Guarantees No Missing Codes

VERSATILITY
- Aerospace Temperature Range: −55°C to +125°C (AD572S)
- Positive-True Serial or Parallel Logic Outputs
- Short-Cycle Capability

VALUE
- Precision +10 V Reference for External Application
- Internal Buffer Amplifier
- High Reliability Package

GENERAL DESCRIPTION

The AD572 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier. Its hybrid IC design utilizes MSI digital and linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide superior performance, flexibility and ease of use, combined with IC size, price, and reliability.

Important performance characteristics of the AD572 include a maximum linearity error at 25°C of ±0.012%, gain T.C. below 15 ppm/°C, typical power dissipation of 900 mW, and conversion time of less than 25 µs. Of considerable significance in aerospace applications is the guaranteed performance from −55°C to +125°C of the AD572S. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0°C to +70°C, −25°C to +85°C, and −55°C to +125°C.

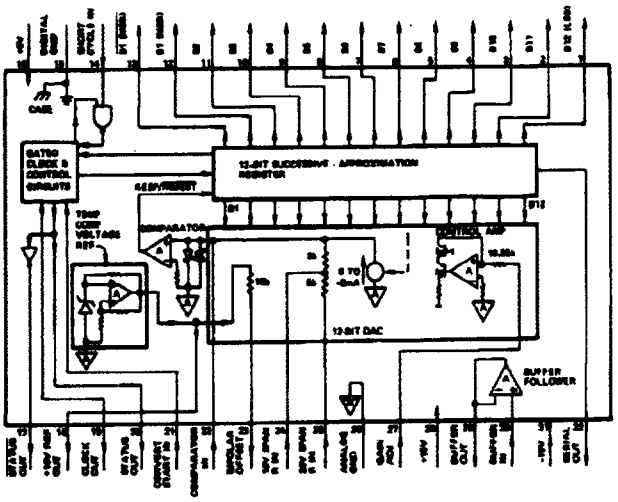
The design of the AD572 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5.0, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +10 V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully TTL compatible, and the data output is positive-true and available in either serial or parallel form.

The AD572 is available in three versions with differing guaranteed performance characteristics and operating temperature ranges; the "A" and "B" are specified from −25°C to +85°C, and the "S" from −55°C to +125°C.

Protected by U.S. Patent Nos. 3,961,326; 3,803,590; and 3,747,088.

REV. A

AD572 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD572 functional diagram and pinout are shown above. The device consists of the following monolithic bipolar circuit elements:

1. Twelve-bit successive-approximation register
2. Twelve-bit DAC
3. Low-drift comparator
4. Temperature-compensated precision +10 V reference
5. High-impedance buffer follower
6. Gated clock and digital control circuits

The +10 V reference is derived from a low drift Zener reference diode which has its Zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10 V, ±10 mV, by active laser trimming of thin-film resistors.

The DAC chip uses 12 precision, high speed bipolar current steering switches, a control amplifier and a laser-trimmed thin-film resistor network to produce a very fast, high accuracy analog output current. The DAC is laser-trimmed to calibrate all bit ratio scale factors to a precision of 0.005% of FSR (full-scale range) to guarantee no missing codes over the appropriate temperature ranges specified for the AD572A, AD572B, and AD572S versions.

Different unipolar and bipolar analog input ranges can be selected by changing connections at the device terminal pins. The analog voltage input can be applied to either of the span (direct input) resistors. Alternatively, the unity gain buffer follower can be connected between the analog signal and either direct input terminal when a high impedance input is required.

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AD572—SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

Model	AD572AD	AD572BD	AD572SD
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5.0, ±10.0 V	*	*
Unipolar	0 to +5, 0 to +10 V	*	*
Impedance (Direct Input)			
0 to +5 V, ±2.5 V	2.5 kΩ	*	*
0 to +10 V, ±5 V	5.0 kΩ	*	*
±10 V	10 kΩ	*	*
Buffer Amplifier			
Impedance (min)	100 MΩ	*	*
Bias Current	50 nA	*	*
Settling Time			
to 0.01% of FSR for 20 V Step	2 µs	*	*
DIGITAL INPUTS			
Convert Command	Note 1	*	*
Logic Loading	1 TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error (Note 2)	±0.05% FSR (Adj to Zero)	*	*
Unipolar Offset Error	±0.05% FSR (Adj to Zero)	*	*
Bipolar Offset Error	±0.1% FSR (Adj to Zero)	*	*
Linearity Error (max)	±0.012% FSR	*	*
Inherent Quantization Error	±1/2 LSB	*	*
Differential Linearity Error	±1/2 LSB	*	*
No Missing Codes	Guaranteed: 0°C to +70°C	Guaranteed: −25°C to +85°C	Guaranteed: −55°C to +125°C
Power Supply Sensitivity			
±15 V	±0.002% FSR/%ΔV_S	*	*
±5 V	±0.001% FSR/%ΔV_S	*	*
TEMPERATURE COEFFICIENTS			
Gain (max)	±30 ppm/°C (−25°C to +85°C)	±15 ppm/°C (−25°C to +85°C)	±15 ppm/°C (−25°C to +85°C) ±25 ppm/°C (−55°C to +125°C)
Unipolar Offset	±3 ppm FSR/°C	±5 ppm FSR/°C (max)	**
Bipolar Offset (max)	±15 ppm FSR/°C	±7 ppm FSR/°C	**
Linearity	±3 ppm FSR/°C	±2 ppm FSR/°C	**
CONVERSION TIME (max)	25 µs	*	*
DIGITAL OUTPUTS (All Codes Positive-True)			
Parallel Data			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Twos Complement	*	*
Output Drive	2 TTL Loads	*	*
Serial Data (NRZ format)			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary	*	*
Output Drive	2 TTL Loads	*	*
Status	Logic "1" during Conversion	*	*
Status	Logic "0" during Conversion	*	*
Output Drive	2 TTL Loads	*	*
Internal Clock			
Output Drive	2 TTL Loads	*	*
Frequency	500 kHz	*	*
INTERNAL REFERENCE VOLTAGE	+10.00 V, ±10 mV typ	*	*
Max External Current	±1 mA	*	*
Voltage Temperature Coefficient (max)	±20 ppm/°C	±10 ppm/°C	*
POWER REQUIREMENTS			
Supply Voltages/Currents	+15 V, ±5% @ +25 mA (40 max)	*	*
	−15 V, ±5% @ −20 mA (35 max)	*	*
	+5 V, ±5% @ +80 mA (150 max)	*	*
Total Power Dissipation	925 mW	*	*
TEMPERATURE RANGE			
Specification	−25°C to +85°C	*	−55°C to +125°C
Operating	−55°C to +125°C	*	*
Storage	−55°C to +150°C	*	*

NOTES

*Same specification as AD572AD.

**Same specifications as AD572BD.

Note 1 Positive pulse 200 ns wide (min). Leading edge ("0" to "1") resets registers. Trailing edge ("1" to "0") initiates conversion.

Note 2 With 50 Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 4 and 5.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Specification Temp Range	Max Gain TC	Max Reference TC	Guaranteed Temp Range No Missing Codes	Package Option*
AD572AD	−25°C to +85°C	±30 ppm/°C	±20 ppm/°C	0°C to +70°C	DH-32C
AD572BD	−25°C to +85°C	±15 ppm/°C	±10 ppm/°C	−25°C to +85°C	DH-32C
AD572SD	−55°C to +125°C	±15 ppm/°C (−25°C to +85°C) ±25 ppm/°C (−55°C to +125°C)	±20 ppm/°C	−55°C to +125°C	DH-32C
AD572SD/883B	Meets all specifications after processing to the requirements of MIL-STD-883, Method 5008, Class B. Refer to Analog Devices Military Databook for details.				

*DH-32C = Size Brazed Ceramic Dip for Hybrid (Medium Cavity).

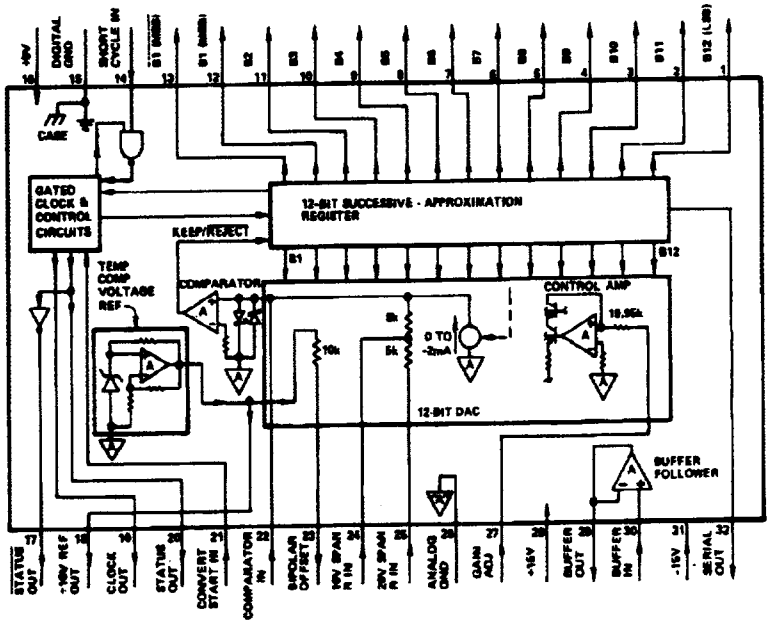


Figure 1. AD572 Functional Diagram and Pinout

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD572 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{12}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep or reject) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision is made at t_{12}. After a 100 ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges. Serial data can be transferred by clocking it into a receiving shift register on these edges.

Incorporation of the 100 ns delay period guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

AD572

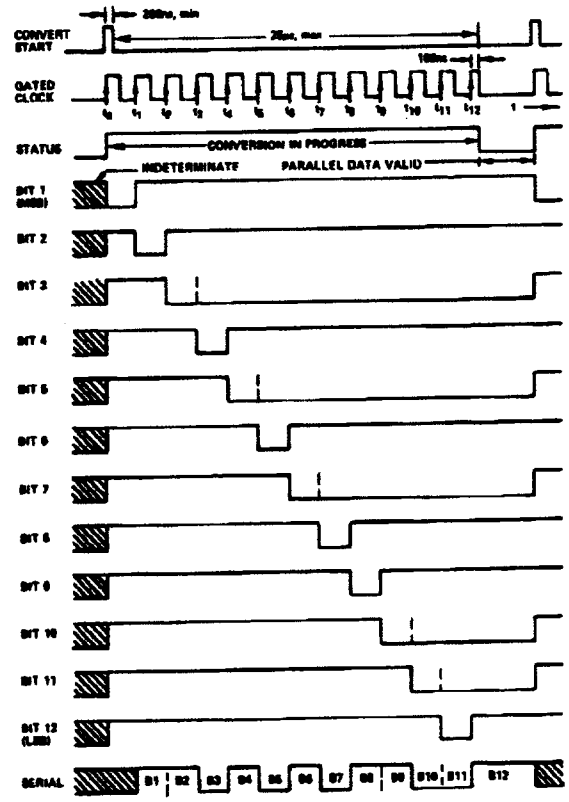


Figure 2. Timing Diagram (Binary Code 110101011001)

BINARY CODING

The AD572 binary output number $N_o = B_1\ B_2\ B_3\ \ldots\ B_{12}$ is related to the analog input voltage E_{IN} for all unipolar ranges by the expression:

$$\frac{B_1\,2^{11} + B_2\,2^{10} + B_3\,2^9 \ldots + B_{12}\,2^0}{2^{12}} = \frac{E_{IN}}{FSR} \qquad (1)$$

. . .where B_1 = MSB, B_{12} = LSB, and FSR = full-scale range. For all bipolar ranges a fixed bipolar offset equal to $\frac{+FSR}{2}$ is internally summed with E_{IN} so that the sum of E_{IN} plus this offset will be positive over the rated operating range. For bipolar ranges, expression (1) becomes:

$$\frac{B_1\,2^{11} + B_2\,2^{10} + B_3\,2^9 + \ldots + B_{12}\,2^0}{2^{12}} = \frac{E_{IN} + \frac{FSR}{2}}{FSR} \qquad (2)$$

Expressions (1) and (2) can be put in an alternate form:

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR = E_{IN} \qquad (3)$$

Unipolar (Binary Coding)

. . . and . . .

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR - \frac{FSR}{2} = E_{IN} \qquad (4)$$

Bipolar (Offset Binary Coding)

Several examples will illustrate how this binary coding works.

0 TO +10 V INPUT RANGE

Assume FSR = 10 V and $B_1\ B_2\ B_3\ \ldots\ B_{12}$ = 110001000001, then from (3), E_{IN} = +5 V +2.5 V +0.1563 V + 0.0024 V = +7.6587 V.

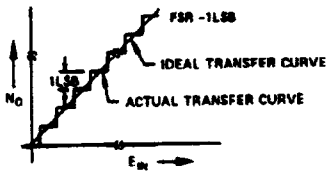
−5 V TO +5 V INPUT RANGE

Assume FSR = 10 V as above, but that the bipolar offset is connected and $B_1\ B_2\ B_3\ \ldots\ B_{12}$ = 011000000001. Then from (4), E_{IN} = (+2.5 V + 1.25 V + 0.0024 V) − 5 V = −1.2476 V.

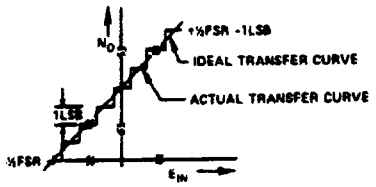
−10 V TO +10 V INPUT RANGE

Assume the bipolar offset is connected as above, but that the input span is now 20 V. Assuming the same digital output code as in the −5 V to +5 V input range example, from (4), E_{IN} = (+5 V +2.5 V +0.0049 V) −10 V = −2.4951 V, or twice the value of the previous example (neglecting round-off errors).

The encoding process defined by the previous relations (1) and (2) or (3) and (4) determines that the analog input lies within one of the 2^{12} = 4096 quantization levels between 0 and FSR (or −FSR/2 and +FSR/2). Figures 3 (A) and 3 (B) show the actual device transfer curves for unipolar and bipolar ranges (offset binary coding). They also show the ideal straight-line transfer curves which pass through the center of each quantization level. As can be seen from these figures, the actual and ideal transfer curves differ by exactly ±1/2 LSB at the end of each quantization interval, giving rise to the fundamental ±1/2 LSB quantization error inherent in the digitizing process.



(A) Unipolar Range (Binary Coding)



(B) Bipolar Range (Offset Binary Coding)

Figure 3. Unipolar and Bipolar Range Transfer Curves

ANALOG INPUT AND POWER CONNECTIONS

Offset Adjust: Analog and power connections for 0 to +10 V unipolar and −10 V to +10 V bipolar input ranges are shown in Figure 4 and 5, respectively. Bipolar Offset (Pin 23) is open-circuited for all unipolar input ranges, and connected to Comparator Input (Pin 22) for all bipolar input ranges. The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 3.9 MΩ resistor to Comparator Input (Pin 22) for all ranges. The tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200 ppm/°C tempco contributes a worst-case offset drift of $8 \times 244 \times 10^{-6}\ \Omega \times 1200$ ppm/°C = 2.3 ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4 LSB, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset drift.

Analog Input – Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10 V Range	−5 V to +5 V Range	−10 V to +10 V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB) B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR−1 LSB	+1/2 FSR−1 LSB	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+4.9952	+9.9902	+FSR−2 LSB	+1/2 FSR−2 LSB	1 1 1 1 1 1 1 1 1 1 1 0
.	.	.	.	.	.
.	.	.	.	.	.
+5.0024	+0.0024	+0.0049	+1/2 FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+0.0000	+0.0000	+1/2 FSR	ZERO	1 0 0 0 0 0 0 0 0 0 0 0
.	.	.	.	.	.
.	.	.	.	.	.
+0.0024	−4.9976	−9.9951	+1 LSB	−1/2 FSR+1 LSB	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	−5.0000	−10.0000	ZERO	−1/2 FSR	0 0 0 0 0 0 0 0 0 0 0 0

Table I. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

RANGE AND BUFFER FOLLOWER PIN CONNECTIONS

Analog pin connections for each of the ranges, with and without the buffer follower being used, are shown in Table II.

Range	Buffer Follower	Connect Analog Input to Pin:	Connect Span Pin:	Connect Bipolar Pin 23 to:
0 to +5 V	Used	30, and 29 to 24	25 to 22	——
	Not Used	24		
0 to +10 V	Used	30, and 20 to 24	——	——
	Not Used	24		
−2.5 V to +2.5 V	Used	30, and 29 to 24	25 to 22	22
	Not Used	24		
−5 V to +5 V	Used	30, and 29 to 24	——	
	Not Used	24		
−10 V to +10 V	Used	30, and 29 to 25	——	
	Not Used	25		

Table II. Range and Buffer Follower Pin Connections

When the analog signal source has a low impedance (as would be the case if it were the output of the sample-hold amplifier of Figure 8), it can be connected to either of the direct input pins 24 and 25. The buffer follower is used in the application as shown in Figure 6, in which the analog input to the converter comes directly from the output of a FET analog multiplexer. The selected channel has a typical r_{on} = 200 Ω which has a 3000 ppm/°C tempco. If the multiplexer output were connected to the 0 to +10 V direct input Pin 24 (5 kΩ input impedance, nominal), this r_{on} would introduce a 4% gain scale-factor loading error, which is well beyond the normal ±0.25% FSR external gain adjustment range, and a tempco of approximately 3000 ppm/°C × 4% = 120 ppm/°C. By connecting the buffer between the multiplexer output and direct input, these errors are eliminated. The buffer amplifier input bias current (50 nA typical) must flow through the analog signal source, however. This limits the upper practical source impedance to several kilohms so that the offset voltage I_{BIAS} R_{SOURCE} can be kept negligible, even though the buffer amplifier dynamic input impedance ≥ 100 MΩ. The buffer amplifier has a 2 µs settling

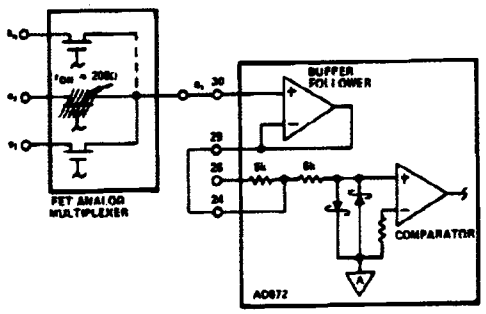


Figure 7. Using Buffer Follower with Multiplexed Analog Input

time to 0.01% FSR for a 20 V input step. This must be added to the conversion time when the input voltage can change significantly between successive conversions (as could be the case in the circuit of Figure 7).

Short Cycle Input: A Short Cycle input (Pin 14) permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits have been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, Pin 14 is connected to +5 V (Pin 16). When 10-bit resolution is desired, Pin 14 is connected to Bit 11 output Pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +100 ns in timing diagram of Figure 2). Short cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table III.

Connect Short Cycle Pin 14 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (µs)	Status Flag Reset at: (Figure 2)
16	12	0.024	25	t_{12} + 100 ns
2	10	0.10	21	t_{10} + 100 ns
4	8	0.39	17	t_8 +100 ns

Table III. Short Cycle Connections

(One should note that the calibration voltages listed in Table I are for 12-bit resolution only, and are those corresponding to the center of each discrete quantization interval at reduced bit resolutions.)

DIGITAL OUTPUT DATA

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary or twos complement binary depending on whether Bit 1 (Pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (Pin 13) is used as the MSB. Parallel data becomes valid approximately 200 ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of STATUS flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (nonreturn-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 2. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations at the completion of the conversion period.

APPLICATIONS

Sample-Hold Amplifier: A sample-hold amplifier (SHA) is normally connected between the analog signal source and AD572 analog input when the analog signal can change by more than 1/2 LSB during conversion. Typical SHA-AD572 interconnections are shown in Figure 8. The STATUS output drives the SHA SAMPLE/HOLD input directly. On receipt of a CONVERT START pulse, the $\overline{\text{STATUS}}$ flag changes from "1" to "0" causing SHA mode to change from SAMPLE to HOLD. The SHA output voltage $e_{o\ S-H}$ is then held constant at the value existing just prior to application of the HOLD command for the complete conversion period. At the end of conversion, the $\overline{\text{STATUS}}$ flag returns to "1," restoring the SHA mode to SAMPLE, $e_{o\ S-H}$ again tracks the analog signal voltage $e_{in\ S-H}$ (after the signal acquisition transient has subsided).

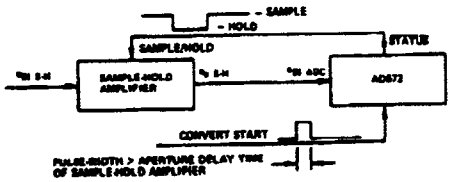


Figure 8. Sample-Hold Amplifier – AD572 Interconnections

Note that the internal (gated) clock is inhibited for the duration of the CONVERT START pulse and does not start running until the termination of this pulse (see timing). This can be used to simplify control signal timing requirements. In the circuit of Figure 8, for example, the CONVERT START signal pulsewidth can be extended beyond the aperture delay time of the SHA to assure that $e_{o\ S-H}$ is in stead state before conversion is initiated. This assured accurate conversion without requiring additional delay timing circuitry. The effect of varying the CONVERT START pulse width on the conversion timing cycle is shown in Figure 9.

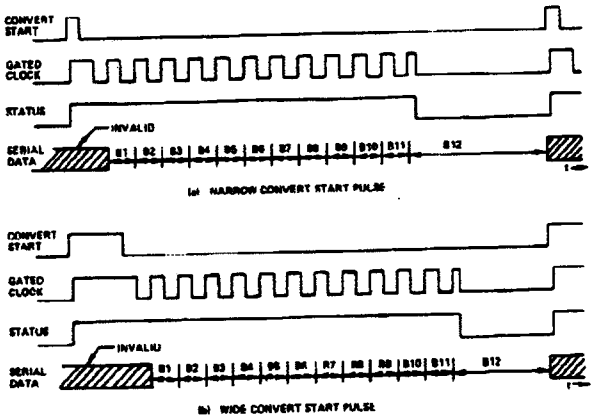


Figure 9. Effect of Convert Start Pulse-Width on Timing

Custom Input Ranges: The AD572's internal buffer makes it easy to create custom input ranges while maintaining normal operation of the gain and offset adjustments. The AD572 should be configured for the standard input range nearest to the desired custom range. Additional scaling is done with external resistors.

The connections required for 10.24 V unipolar operation, which provides a convenient 2 mV LSB size, are shown in Figure 10. The nearest standard input range is 10 V unipolar. Two resistors attenuate the input by a factor of 1000/1024 to match the 10.24 V signal to the converter's 10 V span. The AD572's internal buffer prevents loading of this attenuator by the A/D's 5 kΩ (typical) input impedance.

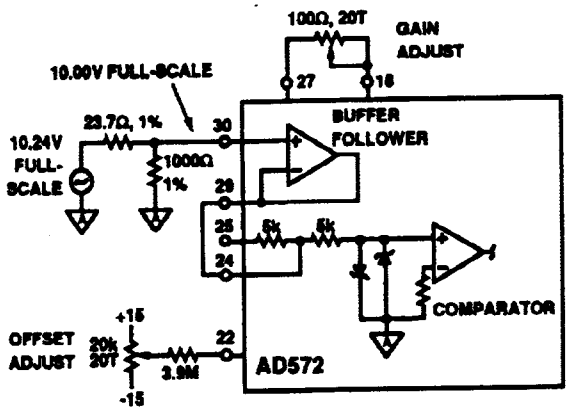


Figure 10. Analog Input Connections for Unipolar 0 to +10.24 V Input Range

Shielding: Sometimes significant electromagnetic interference in the vicinity of the AD572 cannot be avoided. The AD572SD/883B with its all metal cavity and lid, will provide superior performance in such environments.

AD572

Digital Gain Control: Figure 11 shows a method of varying the AD572 gain digitally, using an 8-bit DAC. The 100 Ω GAIN ADJ potentiometer is replaced by a 15 Ω fixed resistor. This biases full-scale high by approximately 35 Ω/20,000 Ω = +0.18% of FSR. The AD559 has a large positive compliance voltage which permits its current out Pin 4 to be connected directly to the AD572 reference input Pin 27. The AD559 2.5 mA output current is established by the AD580 +2.5 V voltage reference connected through a 1 kΩ resistor to reference current input Pin 14. The 2.5 mA DAC full-scale output current removed from the AD572 Pin 27 node changes the Pin 27 input current −2.5 mA × 15 Ω/20 kΩ = −1.88 μA, or −0.38% of FSR; this permits a digital gain adjustment range of approximately ±0.2% FSR from nominal.

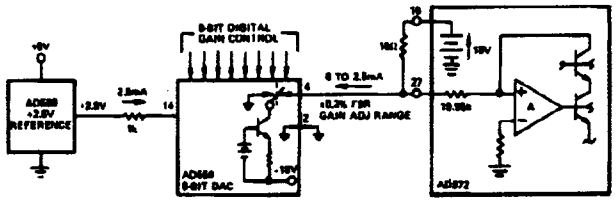


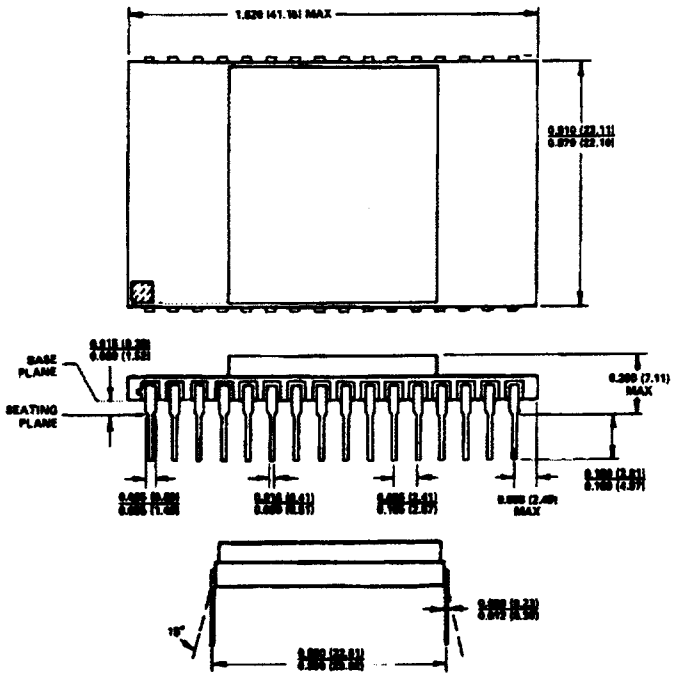
Figure 11. Digital Gain Control Using 8-Bit DAC

C4086c–3–1/91

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).

32-Pin Ceramic Package



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