

# DATA SHEET

## **TDA8822** Universal I<sup>2</sup>C-bus programmable RF modulator

Preliminary specification  
File under Integrated Circuits, IC02

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# Universal I<sup>2</sup>C-bus programmable RF modulator

## TDA8822

### FEATURES

- 5 V power supply
- Video amplifier with clamp and white clip circuits
- Programmable video modulation depth
- FM sound modulator (4.5, 5.5, 6.0 and 6.5 MHz)
- Programmable picture-to-sound ratio
- Programmable deviation of the sound subcarrier
- Input for modulated NICAM sound subcarrier or second frequency modulated sound subcarrier
- Asymmetrical or symmetrical RF output buffer
- Symmetrical RF oscillator for UHF or VHF band according to the application
- One I<sup>2</sup>C-bus programmable output port
- On-chip Phase-Locked Loop (PLL) frequency synthesizer for the RF carrier
- On-chip PLL frequency synthesizer for the sound carrier
- On-chip power supply regulator
- On-chip I<sup>2</sup>C-bus and/or hardware controlled Test Pattern Signal Generator (TPSG) with LED driver
- RF output switch-off during tuning.

### APPLICATIONS

- Video recorders
- Cable converters
- Satellite receivers
- Set top boxes.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8822T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA8822M	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1



### GENERAL DESCRIPTION

The TDA8822 is a programmable modulator which generates an RF TV channel from a baseband video signal and a baseband audio signal in the event of negative video and FM sound standards (B/G, I, D/K, M and N standards).

Two PLL frequency-synthesizers set the picture carrier frequency and the sound subcarrier frequency to the required frequencies. These PLL frequency-synthesizers are programmed via the I<sup>2</sup>C-bus.

The I<sup>2</sup>C-bus controls these features:

- Video modulation depth
- Sound subcarrier modulation deviation
- Picture-to-sound ratio.

This makes the IC suitable for multistandard applications without any adjustment into the application.

Additional features are provided like an input for the NICAM or second FM carrier, a test pattern signal generator with a LED driver and a general purpose output port.

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**QUICK REFERENCE DATA**

$V_{CCA} = V_{CCD} = 5\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; in PAL B/G, PAL I, PAL D/K or NTSC; MD setting = 4; DEV setting = 2; PS setting = 1; video input signal = 500 mV (p-p) EBU colour bars; audio input signal = 45 mV (p-p); 1 kHz sine wave; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CCA}$	analog supply voltage		4.5	5.0	5.5	V
$V_{CCD}$	digital supply voltage		4.5	5.0	5.5	V
$I_{CC(\text{tot})}$	total supply current		–	60	72	mA
$m_d$	modulation depth adjustment range	typical value for MD setting between 0 and 7	72.5	–	90.0	%
P/S	picture-to-sound ratio adjustment range	typical value for PS setting between 0 and 7	–18	–	–11	dB
$V_{RF}$	RF output voltage level asymmetrical on a 75 $\Omega$ load	frequency between 45 and 860 MHz	77	80	83	$\text{dB}\mu\text{V}$
$f_{sc}$	sound subcarrier frequency		4.5	–	6.5	MHz
$\Delta f_{sc}$	sound subcarrier frequency deviation range	for B/G, I, D/K, SC setting = 1, 2 or 3; typical value for DEV setting between 0 and 7	20	–	45	kHz
		for M, N, SC setting = 0; typical value for DEV setting between 0 and 7	10	–	22.5	kHz

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## BLOCK DIAGRAM

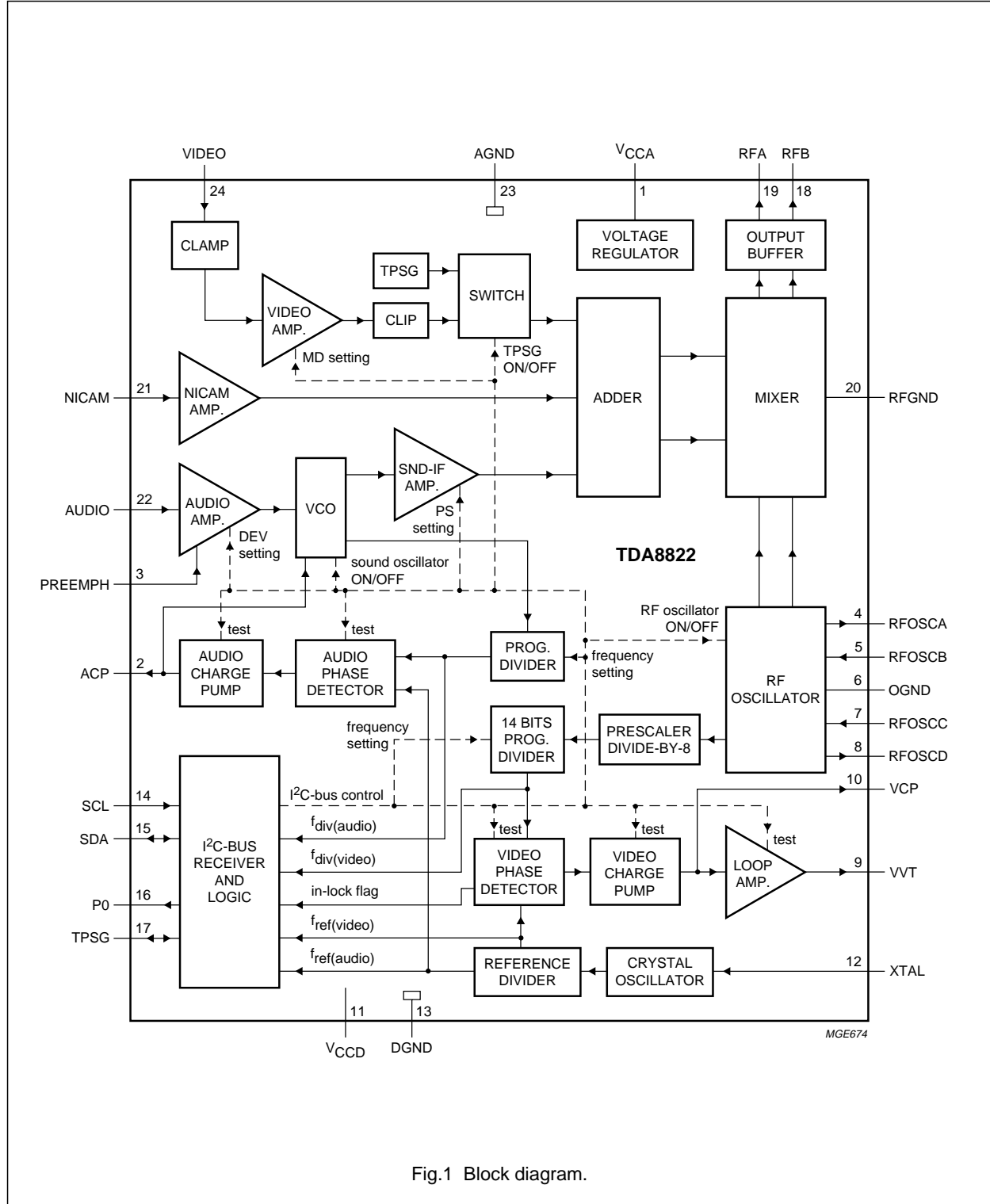


Fig.1 Block diagram.

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## PINNING

SYMBOL	PIN	DESCRIPTION
V <sub>CCA</sub>	1	analog power supply
ACP	2	audio charge pump output
PREEMPH	3	audio pre-emphasis network
RFOSCA	4	RF oscillator A (collector) output
RFOSCB	5	RF oscillator B (base) input
OGND	6	RF oscillator ground
RFOSCC	7	RF oscillator C (base) input
RFOSCD	8	RF oscillator D (collector) output
VVT	9	video tuning voltage output
VCP	10	video charge pump output
V <sub>CCD</sub>	11	digital power supply
XTAL	12	crystal oscillator input
DGND	13	digital ground
SCL	14	serial clock (I <sup>2</sup> C-bus) input
SDA	15	serial data (I <sup>2</sup> C-bus) input/output
P0	16	general purpose output
TPSG	17	test pattern signal generator input/output pin
RFB	18	RF output B
RFA	19	RF output A
RFNGND	20	ground for the RF outputs
NICAM	21	NICAM input
AUDIO	22	audio input
AGND	23	analog ground
VIDEO	24	video input

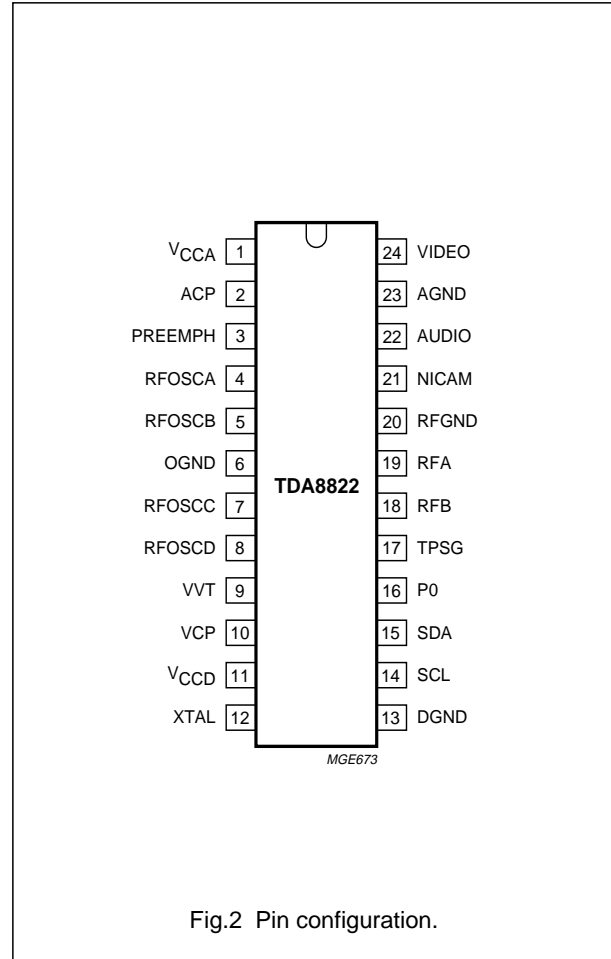


Fig.2 Pin configuration.

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## FUNCTIONAL DESCRIPTION

The TDA8822 is a programmable RF modulator which can be divided into the following parts:

- Video part
- Audio part
- RF part.

### Video part

The video part provides the following:

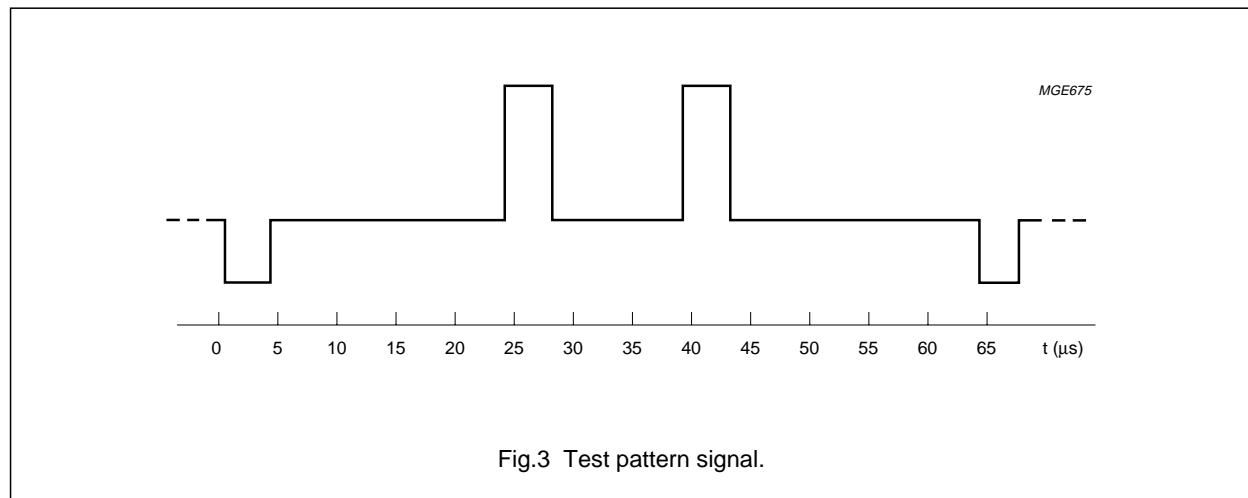
- The video part includes a clamping circuit which sets the internal reference voltage to the bottom of the synchronizing pulse. The modulation depth is adjusted using 3 bits of the I<sup>2</sup>C-bus programming, called MD2, MD1 and MD0. These 3 bits make 8 different values for the modulation depth possible (see Table 1).
- After the modulation depth is set, the signal is fed through a clip control circuit that clips the video signal to avoid that the modulation depth becomes higher than 100%.
- The video part also contains a TPSG. This TPSG generates a pattern that helps to tune the TV set to the programmed channel of the modulator. The pattern consists of a sync pulse and two vertical white bars on the screen (see Fig.3)

The TPSG is activated in two ways:

- Forcing the pin TPSG to DGND in the application (see Fig.8)
- Setting the TPSG bit to 1 via the I<sup>2</sup>C-bus, then the TPSG pin acts as an output port, sinking current to allow the indication of the use of the TPSG in the application e.g. with an LED (see Fig.9).

**Table 1** Modulation depth setting (typical values)

MD SETTING	BIT			MODULATION DEPTH (%)
	MD2	MD1	MD0	
0	0	0	0	72.5
1	0	0	1	75.0
2	0	1	0	77.5
3	0	1	1	80.0
4	1	0	0	82.5
5	1	0	1	85.0
6	1	1	0	87.5
7	1	1	1	90.0



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## Audio part

The audio part provides the following:

- The sound subcarrier is created in an integrated VCO. The signal at the output of this VCO is fed to a stage that adjusts the picture-to-sound ratio and to the audio programmable divider.
- The frequency of the sound subcarrier is set by programming the bits SC1 and SC0 of the I<sup>2</sup>C-bus (see Table 2). These two bits set the dividing ratio of the audio programmable divider to get the divided frequency  $f_{\text{div}(\text{audio})}$ .
- The audio phase detector compares the phase/frequency of the divided audio frequency  $f_{\text{div}(\text{audio})}$  and the reference frequency for the audio,  $f_{\text{ref}(\text{audio})}$  and drives the Charge Pump (CP) that charges or discharges the audio loop filter connected between pins ACP and AGND to get the VCO oscillating to the programmed frequency.
- $f_{\text{ref}(\text{audio})}$  and  $f_{\text{div}(\text{audio})}$  can be monitored on the general purpose output port during a special test mode.
- The frequency deviation of the sound subcarrier is set using 3 bits DEV2, DEV1 and DEV0 of the I<sup>2</sup>C-bus programming (see Table 3), when a signal of 1 kHz with a level of 50 mV (p-p) is applied on the audio input pin.
- The difference between the picture carrier level and the sound subcarrier level is adjusted using 3 bits PS2, PS1 and PS0 (see Table 4).
- The NICAM amplifier has a constant gain, and is designed for adding a second sound subcarrier in the TV channel. This subcarrier can be either a second FM carrier for dual-sound/stereo system used in PAL B/G or a modulated NICAM carrier. The level between the picture carrier and the NICAM carrier (P/N) will depend on the input level on the NICAM input.

**Table 2** Sound subcarrier frequency setting

SC SETTING	BIT		SOUND SUBCARRIER FREQUENCY (MHz)	STANDARD
	SC1	SC0		
0	0	0	4.5	M, N
1	0	1	5.5	B, G
2	1	0	6.0	I
3	1	1	6.5	D, K

**Table 3** Sound subcarrier frequency deviation setting (typical values)

DEV SETTING	BIT			DEVIATION (%)	DEVIATION (kHz)	
	DEV2	DEV1	DEV0		B, G, I, D, K	M, N
0	0	0	0	40.0	20.0	10.0
1	0	0	1	45.0	22.5	11.3
2	0	1	0	50.5	25.3	12.6
3	0	1	1	56.5	28.3	14.1
4	1	0	0	63.5	31.8	15.9
5	1	0	1	71.5	35.8	17.9
6	1	1	0	80.0	40.0	20.0
7	1	1	1	90.0	45.0	22.5

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**Table 4** Picture-to-sound ratio setting (typical values)

PS SETTING	BIT			P/S RATIO (dB)
	PS2	PS1	PS0	
0	0	0	0	-11
1	0	0	1	-12
2	0	1	0	-13
3	0	1	1	-14
4	1	0	0	-15
5	1	0	1	-16
6	1	1	0	-17
7	1	1	1	-18

**RF part**

The RF part provides the following:

- The RF oscillator can produce any frequency used for TV transmission, from 35 to 890 MHz. The frequency range depends on the components used in the application (see Table 11).
- The RF mixer combines the video signal, the sound subcarrier and the carrier from the NICAM input to build a baseband TV channel. This baseband signal is then mixed with the RF oscillator signal to get the RF TV channel.
- The two signals from the RF mixer are sent to the output buffer. This output buffer can be used either as two asymmetrical outputs or as one symmetrical output.
- The output buffer is switched-off while the PLL is not in-lock, to avoid parasitic output signal during the tuning of the RF oscillator. The in-lock information is given by the phase detector of the loop.
- The signal from the RF oscillator is fed to the PLL which controls the picture carrier frequency. The RF signal is first divided by 8 in the prescaler, and then divided in the programmable 14-bits divider. The dividing ratio of this divider is programmed via the I<sup>2</sup>C-bus. The minimum frequency that can be synthesized is 16 MHz, and the maximum frequency is 1023.9375 MHz.
- The divided frequency called  $f_{\text{div}(\text{video})}$  is compared to the reference frequency called  $f_{\text{ref}(\text{video})}$  coming from the crystal oscillator and divided in the reference divider. The crystal oscillator is intended to be used with a crystal of 4 MHz.
- The comparison between  $f_{\text{ref}(\text{video})}$  and  $f_{\text{div}(\text{video})}$  is done in the video phase detector. The resulting signal is fed via the video charge pump to the loop amplifier, including the tuning voltage drive (33 V) inside the IC.
- $f_{\text{ref}(\text{video})}$  and  $f_{\text{div}(\text{video})}$  can also be monitored on the output port during a special test mode.
- The I<sup>2</sup>C-bus receiver and control logic includes the control of:
  - Picture carrier frequency
  - Sound subcarrier frequency
  - Sound subcarrier frequency deviation
  - Video modulation depth
  - Picture-to-sound ratio
  - TPSG on/off and LED drive control
  - RF oscillator on/off
  - Sound oscillator on/off
  - General purpose output port on/off
  - Test modes setting.

**Software information**

The transmission is made using 4 words in I<sup>2</sup>C-bus format. First the address CA has to be sent, then at least two consecutive words have to be sent, either the two words F1 and F0, or the two words C1 and C0.

The two words C1 and F1 are differentiated inside the IC by the first bit being logic 1 or logic 0 respectively. The contents of the 4 bytes is shown in Table 5.

At the power-up of the TDA8822, the I<sup>2</sup>C-bus state is the following:

- N13 to N0 are not fixed
- SC setting = 1: the sound carrier is fixed to 5.5 MHz
- MD is set to 4 (82.5%), PS is set to 1 (-12 dB) and DEV is set to 2 (50.5%)



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- T0 is set to logic 1, RF0 is set to logic 1, TPSG is set to logic 1 and P0 is set to logic 0 to select the video high impedance test mode because it is in this mode that the RF oscillator starts in the best conditions.

The TPSG bit is used to switch on or off the TPSG using the I<sup>2</sup>C-bus. It is also possible to switch the TPSG on in the application, connecting the pin TPSG to DGND. This pin TPSG has a double function and acts as an input or as an output.

These are the two functions:

- Output: if the TPSG is set using the I<sup>2</sup>C-bus, the pin TPSG is used as an output open collector NPN port. This port can be used to indicate with an LED that the TPSG is on. This is especially useful in systems using an on-screen display. If the TV set is not tuned to the right channel there is an alternate indication that the TPSG is on (see Fig.9).
- Input: if the TPSG is set with a hardware switch in the application, the TPSG pin is used as one of the inputs to select the TPSG mode (see Fig.8).

Notice that if the TPSG bit is set to logic 1 while the RF0 bit is set to logic 0, the TPSG is turned off, and the sound oscillator is off (see Table 8).

N13 to N0 are the 14 bits to set the video programmable divider ratio and then to set the picture carrier frequency following the formula:  $f_{osc} = f_{ref(video)} \times 8 \times N$ ,

where:

- $f_{ref(video)}$  is the frequency on pin XTAL divided by the reference divider ratio. For example, with a 4 MHz crystal connected to

$$\text{pin XTAL, } f_{ref(video)} = \frac{4\,000\,000}{512} = 7812.5 \text{ Hz}$$

- N is the programmable divider ratio:  
 $N = N_{13} \times 2^{13} + N_{12} \times 2^{12} + \dots + N_1 \times 2 + N_0$
- $f_{osc}$  is the RF oscillator frequency.

DEV2, DEV1 and DEV0 are the bits to set the sound subcarrier frequency deviation (see Table 3).

PS2, PS1 and PS0 are the bits to set the picture-to-sound ratio (see Table 4).

MD2, MD1 and MD0 are the bits to set the modulation depth (see Table 1).

SC1 and SC0 are the bits to set the sound subcarrier frequency according to Table 2.

RF0 is a bit that controls the RF oscillator on/off. In normal mode, it should be set to logic 1. If the modulator is not used and may create some interferences with other signals in the application, it should be set to logic 0 (see Table 6).

Notice that if the bit RF0 is logic 0 while the bit TPSG is logic 1, then the RF oscillator is still running, but the sound oscillator is off, and the TPSG is also off (see Table 8).

The bit P0 controls the output port P0, which is an open collector NPN port, able to drive up to 10 mA (see Table 7).

T0 is a bit used for test purposes. If this bit is set to logic 0, the IC operates in normal configuration. If it is set to logic 1, then the use of bits TPSG, RF0 and P0 is changed to select 1 of the 8 test modes as explained in Table 9.

**Table 5** Contents of programming words

BYTE	MSB							LSB		ACKNOWLEDGE BIT
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
Address byte CA	1	1	0	0	1	0	1	0	ACK	
F1: frequency byte 1	0	TPSG	N13	N12	N11	N10	N9	N8	ACK	
F0: frequency byte 0	N7	N6	N5	N4	N3	N2	N1	N0	ACK	
C1: control byte 1	1	DEV2	DEV1	DEV0	PS2	PS1	PS0	0	ACK	
C0: control byte 0	MD2	MD1	MD0	SC1	SC0	RF0	P0	T0	ACK	

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**Table 6** RF oscillator on/off setting (see note 1)

STATE OF RF0	ACTION ON RF OSCILLATOR
0	stopped; no RF carrier
1	operating; normal use

**Note**

1. This table is valid only if bit TPSG is set to logic 0.

**Table 7** Output port programming

STATE OF P0	PORT STATE	VOLTAGE ON PORT (with a pull-up resistor to V <sub>CCD</sub> )
0	high impedance	close to V <sub>CCD</sub>
1	sinking current	close to 0 V

**Table 8** Overview of the normal modes

T0	RF0	TPSG	P0	PIN TPSG	MODE
0	1	0	X <sup>(1)</sup>	input: open	RF on; TPSG off
0	1	0	X <sup>(1)</sup>	input: to DGND	RF on; TPSG on
0	1	1	X <sup>(1)</sup>	output: sinking current	RF on; TPSG on
0	0	0	X <sup>(1)</sup>	input: open or to DGND	RF off
0	0	1	X <sup>(1)</sup>	input: open	RF on; TPSG off; sound oscillator off
0	0	1	X <sup>(1)</sup>	input: to DGND	RF on; TPSG on; sound oscillator off
0	X <sup>(1)</sup>	X <sup>(1)</sup>	0	X <sup>(1)</sup>	Port P0 off (high impedance)
0	X <sup>(1)</sup>	X <sup>(1)</sup>	1	X <sup>(1)</sup>	Port P0 on (sinking current)

**Note**

1. X means logic 0 or logic 1, don't care.

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**Table 9** Overview of the test modes

T0	RF0	TPSG	P0	PIN <sup>(1)</sup> TPSG	TEST MODES
1	0	0	0	X	f <sub>ref(audio)</sub> on P0; both CP sinking current; notes 2 and 6
1	0	0	1	X	f <sub>div(audio)</sub> on P0; note 3
1	0	1	0	X	f <sub>ref(video)</sub> on P0; both CP sourcing current; notes 4 and 6
1	0	1	1	X	f <sub>div(video)</sub> on P0; note 5
1	1	0	0	X	video charge pump off; note 7
1	1	0	1	X	audio charge pump off and balance test; notes 8 and 11
1	1	1	0	X	video high impedance test; note 9
1	1	1	1	X	baseband signal on RF outputs; note 10

**Notes**

1. During the test mode (bit T0 set to logic 1), the pin TPSG is unused, meaning that the input information does not have any effect, and that the output port does not sink any current.
2. In 'f<sub>ref(audio)</sub> on P0' mode, the reference frequency of the audio PLL is available on the port P0.
3. In 'f<sub>div(audio)</sub> on P0' mode,  $\frac{f_{div(audio)}}{2}$  is available on the port P0 (f<sub>div(audio)</sub> is the frequency from the sound oscillator divided by the dividing ratio of the audio programmable divider).
4. In 'f<sub>ref(video)</sub> on P0' mode, the reference frequency of the video PLL is available on the port P0.
5. In 'f<sub>div(video)</sub> on P0' mode,  $\frac{f_{div(video)}}{2}$  is available on the port P0 (f<sub>div(video)</sub> is the frequency of the RF oscillator divided by the dividing ratio of the video programmable divider).
6. In 'both CP sinking or sourcing current' modes, the charge pump of the audio PLL and the one of the video PLL are sinking or sourcing their nominal current.
7. The 'video charge pump off' mode allows to measure the leakage current on the video PLL charge pump.
8. The 'audio charge pump off' mode allows to measure the leakage current on the audio PLL charge pump.
9. In the 'video high-impedance' mode, it is possible to inject an external tuning voltage for the RF carrier setting. In this mode, the video PLL is off.
10. In the 'baseband signal on RF outputs' mode, the RF oscillator is off, and it is possible to measure the baseband video and audio subcarrier signals on the RF output pins.
11. During the 'balance test' mode the picture carrier is over-modulated allowing the measurement of the residual carrier.

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## Example of programming

We want to program the TDA8822 in a UHF application, on channel 21 (picture carrier at 471.25 MHz) in a B/G standard (sound carrier at 5.5 MHz from the picture carrier) with a Picture-to-Sound ratio of -12 dB, a modulation depth of 82.5% and a deviation set to 50.5% in normal mode, without TPSG, output port on.

These are the values of the bits that must be programmed:

- The video dividing ratio will be  $N = \frac{f_{osc}}{f_{ref} \times 8} = \frac{471\,250\,000}{7\,812.5 \times 8} = 7540 = 01110101110100$
- TPSG bit will be set to logic 0
- DEV2 will be set to logic 0, DEV1 to logic 1 and DEV0 to logic 0
- PS2 will be set to logic 0, PS1 to logic 0 and PS0 to logic 1
- MD2 will be set to logic 1, MD1 to logic 0 and MD0 to logic 0
- SC1 will be set to logic 0 and SC0 to logic 1
- P0 will be set to logic 1
- RF0 will be set to logic 1
- T0 will be set to logic 0.

The protocol to the TDA8822 is illustrated in Table 10.

**Table 10** Example of programming for the TDA8822.

BYTE	MSB							LSB		ACKNOWLEDGE
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
Address byte CA	1	1	0	0	1	0	1	0	ACK	
F1: frequency byte 1	0	0	0	1	1	1	0	1	ACK	
F0: frequency byte 0	0	1	1	1	0	1	0	0	ACK	
C1: control byte 1	1	0	1	0	0	0	1	0	ACK	
C0: Control byte 0	1	0	0	0	1	1	1	0	ACK	

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>CCA</sub>	analog supply voltage	-0.3	+7.0	V
V <sub>CCD</sub>	digital supply voltage	-0.3	+7.0	V
V <sub>CC</sub>	operating supply voltage	4.5	5.5	V
V <sub>max</sub>	maximum voltage on all pins except SCL, SDA and VVT	-0.3	V <sub>CC</sub>	V
V <sub>BUS(max)</sub>	maximum voltage on SCL and SDA pins	-0.3	+7.0	V
V <sub>VVT(max)</sub>	maximum voltage on VVT pin	-0.3	+35.0	V
T <sub>stg</sub>	storage temperature	-40	+125	°C
T <sub>amb</sub>	operating ambient temperature	-20	+85	°C

## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits. The IC withstands the ESD test in accordance with the "UZW-B0/FQ-A302" specification equivalent to the "MIL-STD-883C category B" (2000 V). The IC withstands the ESD test in accordance with Philips Semiconductors Machine Model (MM), specification "UZW-B0/FQ-B302", issue date November 6<sup>th</sup>, 1990, (0 Ω, 200 pF, 200 V).

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient in free air		
	SO24; SOT137-1	74	K/W
	SSOP24; SOT340-1	120	K/W

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## CHARACTERISTICS

$V_{CCA} = V_{CCD} = 5\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; in PAL B/G, PAL I, PAL D/K, or NTSC; MD setting = 4; DEV setting = 2; PS setting = 1; video input signal = 500 mV (p-p) EBU colour bars; audio input signal = 45 mV (p-p) 1 kHz sine wave; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$I_P$	power supply current	analog and digital parts	–	60	72	mA
<b>Video characteristics</b>						
$I_{VIDEO}$	video input current		–	0.5	2.0	$\mu\text{A}$
$Z_{VIDEO}$	video input impedance		30	–	–	$\text{k}\Omega$
$m_d$	modulation depth	part-to-part variation; MD setting = 4	77.5	82.5	87.5	%
$m_{d(\text{clip})}$	modulation depth during clipping condition	video input level lower than 1 V (p-p)	–	–	99	%
$m_{d(\text{TPSG})}$	modulation depth when TPSG mode on	part to part variation, MD setting = 4	72.5	82.5	92.5	%
$m_{d(\text{APL})}$	variation of the modulation depth with change of APL between 10 and 90%	reference for APL = 50%	–2	0	+2	%
S/N	video signal-to-noise ratio	note 1	48	52	–	dB
$G_{\text{diff}}$	differential gain	note 2	–	3	6	%
$\phi_{\text{diff}}$	differential phase	note 2	–	3	6	deg
V/S	video-to-sync ratio	input signal: V/S = 7 : 3	6.9 : 3.1	7 : 3	7.1 : 2.9	
$f_{\text{video}}$	frequency response for the video signal	note 3	–1	–	+1	dB
<b>Audio characteristics</b>						
$Z_{\text{AUDIO}}$	audio input impedance	without any resistor between AUDIO and AGND	30	–	–	$\text{k}\Omega$
$\Delta f_m$	modulation deviation	SC setting = 1, 2 or 3; DEV setting = 2	20	25	30	kHz
		SC setting = 0; DEV setting = 2	10	12.5	15	kHz
$\Delta f_{m(\text{max})}$	maximum modulation deviation	$V_{\text{AUDIO}} = 500\text{ mV (p-p)}$ ; note 4	180	250	–	kHz
THD	total harmonic distortion	50 mV (p-p) sine wave at 1 kHz on AUDIO pin	–	0.4	1.0	%
S/N	audio signal-to-noise ratio	note 5	44	47	–	dB
$f_{\text{AUDIO}}$	frequency response of the audio signal	note 6	–1	–	+1	dB
$\Delta f_{\text{sc}(\text{acc})}$	sound subcarrier accuracy	note 7	–1	0	+1	kHz
P/S	picture-to-sound ratio	no audio signal; no video signal; PS setting = 1	–15	–12	–9	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>NICAM characteristics</b>						
Z <sub>NICAM</sub>	NICAM input impedance		10	–	–	kΩ
P/N	level between picture carrier and NICAM carrier	NICAM input level = 150 mV (p-p); no video signal	–23	–20	–17	dB
f <sub>NICAM</sub>	frequency response of the NICAM input	for frequencies between 5 and 8 MHz; reference for 6.5 MHz	–1	–	+1	dB
BER	bit error rate	note 11	–	10 <sup>–6</sup>	–	
EHD	eye-height degradation	note 11	–	4	–	%
<b>Channel characteristics</b>						
f <sub>RF</sub>	RF frequency range	with application VHF 1	47	–	88	MHz
		with application VHF 3	174	–	230	MHz
		with application UHF	470	–	860	MHz
f <sub>RF(acc)</sub>	picture carrier accuracy	note 7	–75	–	+75	kHz
V <sub>RF</sub>	output level on RF outputs during sync. pulse, loaded with 75 Ω	between 45 and 860 MHz	77	80	83	dBμV
V <sub>RF(flat)</sub>	flatness of the RF output level across each band	reference is centre of each band	–2	0	2	dB
Z <sub>o(RF)</sub>	RF output impedance	single ended	–	75	–	Ω
SPU <sub>o</sub>	spurious outside channel	note 8	–	–	–40	dBc
SPU <sub>2PC</sub>	RF second harmonic level	on asymmetrical output at low end of UHF band	–	–	–10	dBc
SPU <sub>2SC</sub>	sound carrier second harmonic level		–	–65	–60	dBc
SPU <sub>3SC</sub>	sound carrier third harmonic level		–	–65	–60	dBc
SPU <sub>fref</sub>	reference frequency spurious	measured with Philips application board	–	–	–40	dBc
CHR <sub>BEAT</sub>	chroma beat	note 9	–	–	–63	dBc
NIC <sub>BEAT</sub>	NICAM beat	note 10	–	–	–63	dBc
<b>Video charge pump output and video tuning amplifier: VCP and VVT</b>						
I <sub>VCP</sub>	output current		–	50	–	μA
I <sub>VCP(Ik)</sub>	off-state leakage current		–10	–	10	nA
V <sub>VVT(min)</sub>	minimum tuning voltage on pin VVT	27 kΩ resistor between pin VVT and +33 V	–	–	0.2	V
I <sub>VVT(Ik)</sub>	leakage current on pin VVT	27 kΩ resistor between pin VVT and +33 V; high impedance test mode	–	–	10	μA
<b>Audio charge pump output: ACP</b>						
I <sub>ACP</sub>	output current		–	3	–	μA
I <sub>ACP(Ik)</sub>	off-state leakage current		–10	–	10	nA
V <sub>ACP</sub>	tuning voltage range for the audio PLL, on pin ACP		1.5	–	4.5	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>XTAL characteristics</b>						
Z <sub>XTAL</sub>	XTAL input impedance	absolute value; with a 4 MHz crystal	600	1200	–	Ω
<b>Output Port characteristics</b>						
V <sub>PORT</sub>	low voltage	port on; I <sub>PORT</sub> = 10 mA	–	150	400	mV
I <sub>PORT(IK)</sub>	off-state leakage current	port off; V <sub>CCD</sub> = 5.5 V	–	–	10	μA
I <sub>PORT(sink)</sub>	sinking current in the port	port on	10	–	–	mA
<b>TPSG pin characteristics</b>						
V <sub>TPSG(on)</sub>	voltage on pin TPSG to switch the TPSG on		0	–	1.5	V
V <sub>TPSG(off)</sub>	voltage on pin TPSG to switch the TPSG off		3.0	–	V <sub>CCD</sub>	V
I <sub>TPSGL</sub>	LOW input current in pin TPSG	TPSG to DGND	–100	–	–	μA
I <sub>TPSGH</sub>	HIGH input current in pin TPSG	TPSG to V <sub>CCD</sub>	–	–	100	μA
I <sub>TPSG(sink)</sub>	output sinking current in pin TPSG	TPSG set on using I <sup>2</sup> C-bus	10	–	–	mA
V <sub>TPSG(sink)</sub>	voltage on pin TPSG used as output	TPSG set on using I <sup>2</sup> C-bus	–	150	400	mV
<b>I<sup>2</sup>C-bus receiver characteristics, pins SCL and SDA</b>						
f <sub>SCL</sub>	frequency on SCL line		–	–	100	kHz
V <sub>IH</sub>	HIGH level input voltage		3	–	5.5	V
V <sub>IL</sub>	LOW level input voltage		0	–	1.5	V
I <sub>IH</sub>	HIGH level input current	V <sub>IH</sub> = 5 V; V <sub>CCD</sub> = 0 or 5 V	–	–	10	μA
I <sub>IL</sub>	LOW level input current	V <sub>IL</sub> = 0 V; V <sub>CCD</sub> = 0 or 5 V	–10	–	–	μA
V <sub>SDA(ack)</sub>	acknowledge output voltage on SDA	during acknowledge pulse; I <sub>IL</sub> = 3 mA	–	–	0.4	V

**Notes**

- Ratio between the CCIR 17-line bar amplitude (corresponding to the level difference between black and white; see Fig.4) and the RMS value of the noise on a black line (line 22 or 335) measured on the video signal after demodulation. Measurement is done for frequencies between 200 kHz and 5 MHz. Measurement is unweighted.
- Measured on CCIR 330 line, corresponding to a 5-step staircase with a chroma carrier of amplitude equal to 0.3 times the voltage between sync pulse and white (see Fig.5). The video signal is 500 mV (p-p). The modulation depth is adjusted using the I<sup>2</sup>C-bus to MD setting = 4 (82.5% typical modulation depth).
- Measured with a spectrum analyser with 'peak hold' function, applying a 500 mV (p-p) sine wave at the video input of the IC, with a sweeping frequency between 0.5 and 6.0 MHz. The reference is the value measured at 1.0 MHz.
- To have a deviation between 50 and 250 kHz, the audio frequency must be higher than 100 Hz.
- Measured with an audio frequency of 1 kHz with a level adjusted to get a deviation of 50 kHz with DEV setting = 2, using CCIR 468-3 weighting filter, with a quasi-peak detection. The input signal has pre-emphasis and the receiver has de-emphasis. Video signal is 500 mV (p-p) EBU colour bars on pin VIDEO.



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## Universal I<sup>2</sup>C-bus programmable RF modulator

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6. Measured with no pre-emphasis on the audio input and no de-emphasis in the receiver. Measurement is done for frequencies between 50 Hz and 15 kHz, reference is the level measured at 1 kHz.
7. The accuracy only depends on the accuracy of the reference frequency (accuracy of the crystal). Notice that the value of the capacitor in series with the crystal must be chosen to be as close as possible to the load capacitance of the crystal.
8. Except for the harmonics of the RF oscillator frequency and for the combinations between the RF oscillator frequency and the sound oscillator frequency ( $f_{RF} + 2f_s$ ,  $2f_{RF} + f_s$ , etc.). This measurement includes the spurious at the  $\frac{1}{4}f_{RF}$ ,  $\frac{1}{2}f_{RF}$  and  $\frac{3}{4}f_{RF}$ .
9. Chroma beat
  - a) For PAL: measured applying a 4.43 MHz sine wave of 200 mV (p-p) at the video input. Measurement is the difference between the level of the unmodulated picture carrier and the level of the spike appearing at the frequency of the picture carrier plus 1.07 MHz for PAL B/G, 1.57 MHz for PAL I and 2.07 MHz for PAL D/K.
  - b) For NTSC: measured applying a 3.58 MHz sine wave of 200 mV (p-p) at the video input. Measurement is the difference between the level of the unmodulated picture carrier and the level of the spike appearing at the frequency of the picture carrier plus 920 kHz.
10. NICAM beat
  - a) For PAL B/G: measured applying a sine wave of 150 mV (p-p) at 5.85 MHz on the NICAM input. Measurement is the difference between the level of the unmodulated picture carrier and the level of the spike appearing at the frequency of the picture carrier plus 350 kHz or 5.15 MHz.
  - b) For PAL I: measured applying a sine wave of 150 mV (p-p) at 6.552 MHz on the NICAM input. Measurement is the difference between the level of the unmodulated picture carrier and the level of the spike appearing at the frequency of the picture carrier plus 552 kHz or 5.448 MHz.
11. NICAM eye height and Bit Error Rate measurement conditions:
  - a) A NICAM frame is applied from a Textronix 728E in B/G mode on the NICAM input of the TDA8822 through an attenuator to get 150 mV (p-p). The sound subcarrier is set to 5.5 MHz (SC = 1) and the picture to sound ratio is set to -12 dB (PS = 1). There is no video signal applied to the video input and no audio signal on the audio input.
  - b) The RF carrier is demodulated with a Rohde & Schwartz EMFP demodulator for PAL B/G, the sound trap filter is set off, and the video signal is fed to a Textronix 728D NICAM demodulator for B/G. Measurements of the eye height and bit error rate are done on the 728D.

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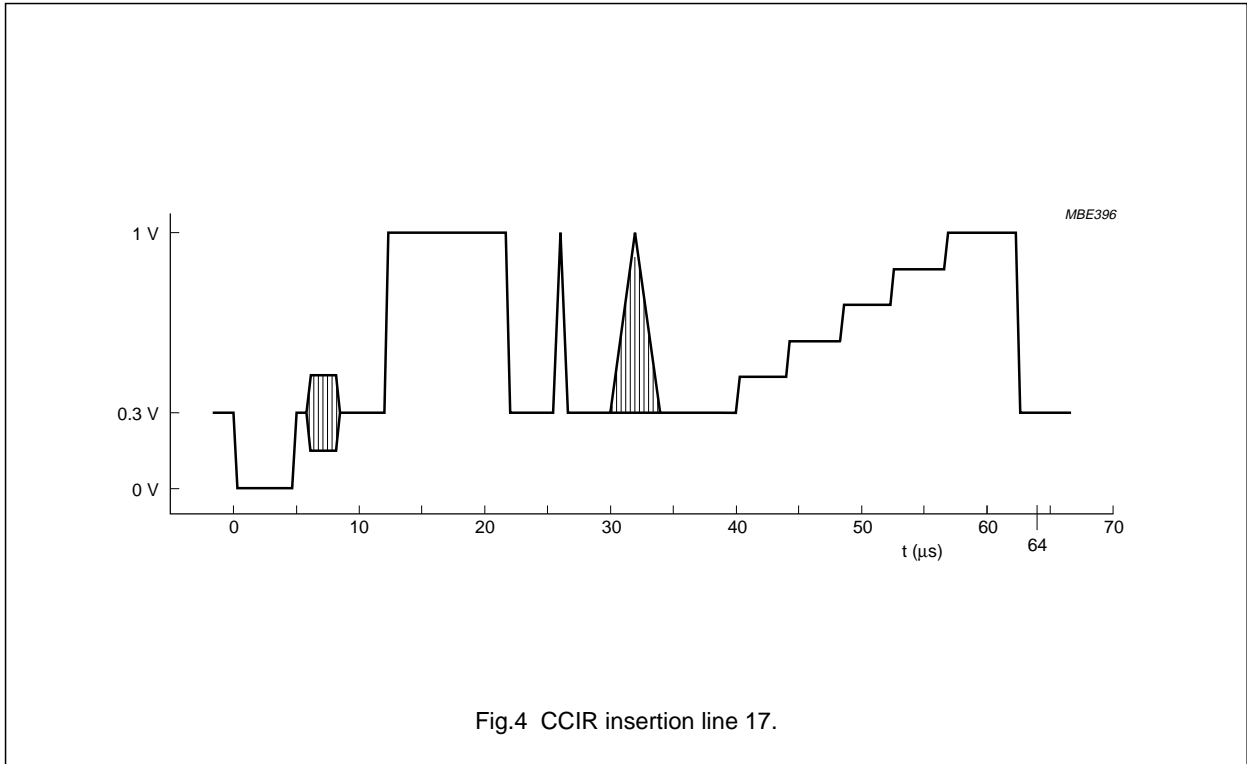


Fig.4 CCIR insertion line 17.

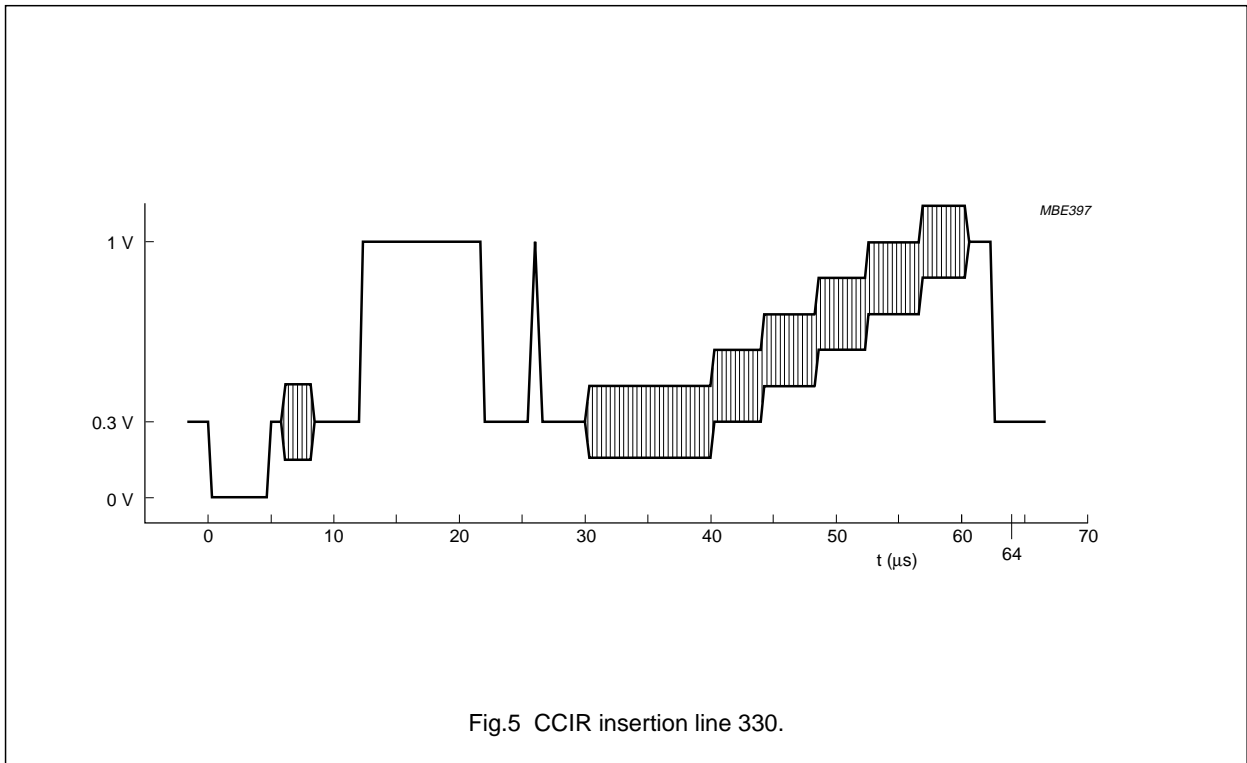


Fig.5 CCIR insertion line 330.

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## INTERNAL PIN CONFIGURATION

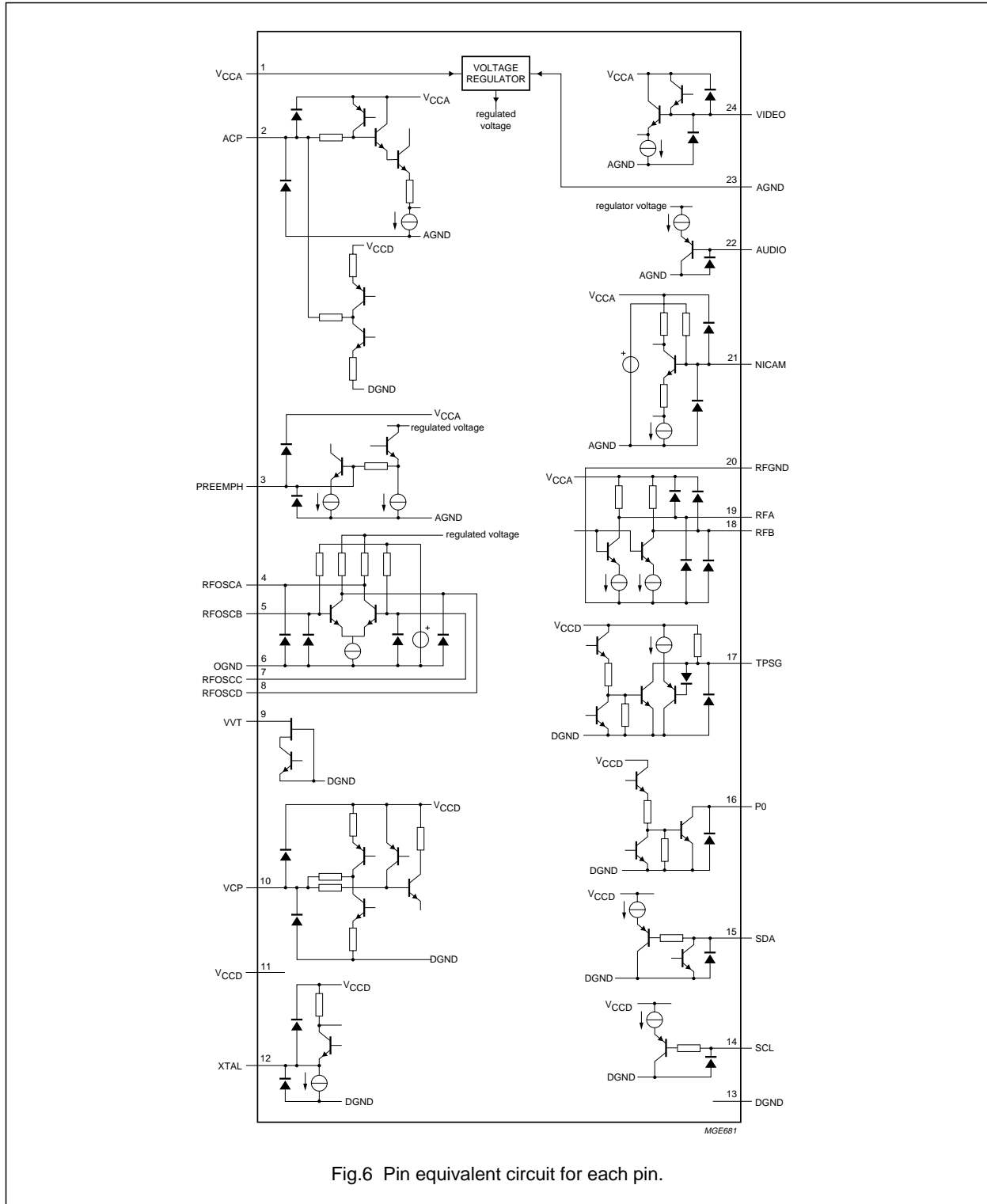


Fig.6 Pin equivalent circuit for each pin.

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## TDA8822

### APPLICATION INFORMATION

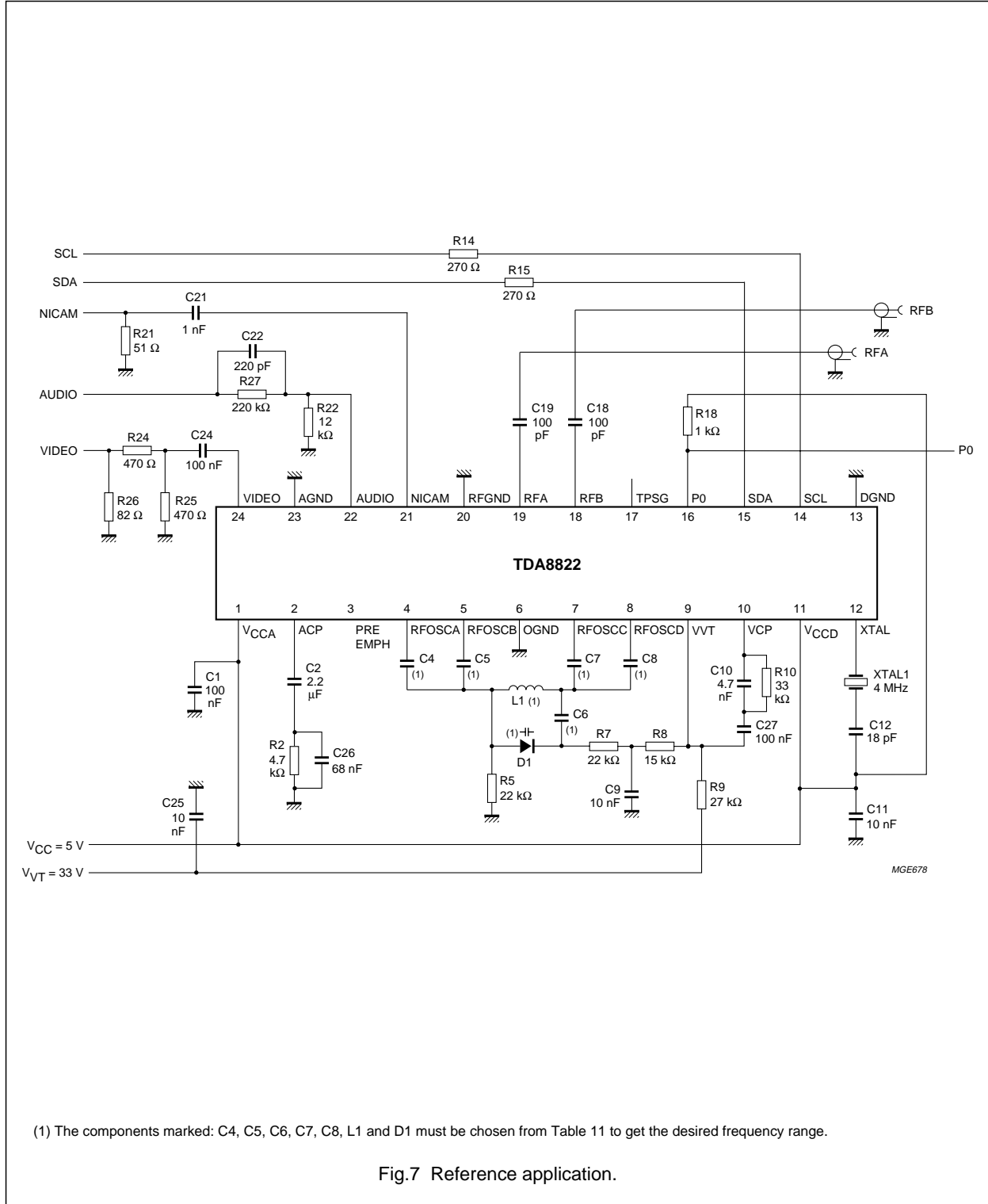


Fig.7 Reference application.

# Universal I<sup>2</sup>C-bus programmable RF modulator

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## Application design

In the design of the application, it is highly recommended to separate the part of the RF oscillator as much as possible from the part of the RF outputs in order to avoid parasitic coupling between these two parts.

A good solution is shielding the RF oscillator part to avoid radiation from and to this part. The pin OGND must be connected to the shielding box and to ground.

The frequency range the IC covers is fixed by the choice of the components marked with a note (1) in Fig.7. For these components, it is recommended to use the values indicated in Table 11.

**Table 11** Components to be used for the RF oscillator

BAND	FREQUENCY RANGE	VALUE FOR C4, C5, C7, C8	VALUE FOR C6	D1	L1: NUMBER OF TURNS	L1: COIL DIAMETER	L1: WIRE DIAMETER
VHF1	47 to 130 MHz	5.6 pF	100 pF	BB132	14.5	3.0 mm	0.3 mm
VHF3	130 to 350 MHz	4.7 pF	150 pF	BB133	4.5	3.0 mm	0.4 mm
UHF	470 to 860 MHz	1.8 pF	22 pF	BB134	1.5	2.5 mm	0.5 mm

## Video input (pin 24)

The video input level on the IC is of 500 mV (p-p). In most of the cases, the available video signals are of 1 V (p-p) with a source impedance of 75 Ω.

To handle this kind of signal, we use a resistive divider with two 470 Ω resistors (R24 and R25 in Fig.7) to divide the 1 V (p-p) signal down to 500 mV (p-p). In order to get an input impedance of 75 Ω, a resistor of 82 Ω is implemented in parallel to the divider (R26 in Fig.7).

## Audio pre-emphasis

The capacitor C22 connected in parallel with R27 is defining the time constant for the pre-emphasis following Table 12.

**Table 12** Choice of the pre-emphasis constant

STANDARD	CAPACITOR C22	TIME CONSTANT
NTSC	330 pF	75 μs
PAL	220 pF	50 μs
special; note 1	no capacitor	—

## Note

1. This mode has to be considered if the pre-emphasis is applied else-where on the path of the audio signal, or if there is no need for pre-emphasis in specific applications. Note also that the pre-emphasis can be done by connecting a capacitor between pin PREEMPH (pin 3) and ground. The value for this capacitor is 10 nF for PAL and 15 nF for NTSC.

## Audio input (pin 22)

The IC is sensitive to 45 mV (p-p) on pin AUDIO and the DC voltage on this pin is close to 0 V.

This pin needs to be grounded through a 12 kΩ resistor (R22 in Fig.7). Care must then be taken if a coupling capacitor needs to be implemented on the audio path to connect it between the signal source and the input, with the resistor of 12 kΩ still connected to the AUDIO pin.

## NICAM input (pin 21)

The NICAM pin is sensitive to 150 mV (p-p) to reach a level between picture carrier and NICAM carrier of typical -20 dBc.

It is possible to put on this pin either a NICAM modulated carrier for a NICAM application or a frequency modulated carrier for the stereo system with a second FM carrier used e.g. in Germany.

In a specific application where the main sound subcarrier would be generated outside the IC, it is also possible to inject the main sound carrier to this pin, with a level depending on the wanted P/S. In this event, it is necessary to stop the internal sound oscillator by setting RF0 to logic 0 and TPSG to logic 1 (see Table 8).

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### TPSG input/output (pin 17)

As already mentioned, this pin can be used either as an input or as an output.

- As an input, it allows to turn on the TPSG, without changing anything to the word the TDA8822 is programmed through the I<sup>2</sup>C-bus.

In this mode, it is simply necessary to connect a switch between the pin TPSG and DGND (see Fig.8). If the switch is open, then the TPSG is selected corresponding to the I<sup>2</sup>C-bus programming; if the switch is closed, then the TPSG is on.

- As an output, it allows to indicate e.g. with an LED that the TPSG has been programmed on using the I<sup>2</sup>C-bus.

In this mode, the pin acts as an open-collector output port, it is possible to connect a LED to the 5 V power supply with a series resistor to limit the current to about 10 mA (see Fig.9).

### XTAL pin (pin 12)

This pin is connected to a 4 MHz crystal in series with a capacitor. The value of this capacitor has to be as close as possible to the load capacitance of the crystal.

It is also possible to drive the IC with an external 4 MHz signal from a voltage source. A level of 50 mV(RMS) insures stable operation. A capacitor of about 18 pF and a resistor of 680 Ω needs to be placed in series with the voltage source.

### ACP pin (pin 2)

This pin is the charge pump output for the sound subcarrier PLL as well as the input of the sound subcarrier VCO.

It is necessary to connect the loop filter between this pin and ground. The loop filter indicated in Fig.7 gives a cut-off frequency lower than 20 Hz.

If a cutoff frequency slightly higher than 20 Hz can be accepted, it is possible to reduce the value of the 2.2 μF capacitor (C2) to 220 nF. In this case C26 needs to be changed from 68 nF to 22 nF and R3 needs to be changed from 4.7 kΩ to 33 kΩ.

### RF outputs (pins 18 and 19)

For inexpensive applications, it is possible to use the IC with an asymmetrical output.

In an asymmetrical application, the unused output pin must be loaded with a load as close as possible to the load connected to the used pin.

A good improvement in performance is obtained using a symmetrical to asymmetrical transformer (balun; balance-to-unbalance) connected between the two outputs. In this event both outputs have their loads matched. The level of the RF second harmonic, and the spurious outside channel is decreasing. The parasitic coupling between RF outputs and RF oscillator is also reduced.

### RF harmonics

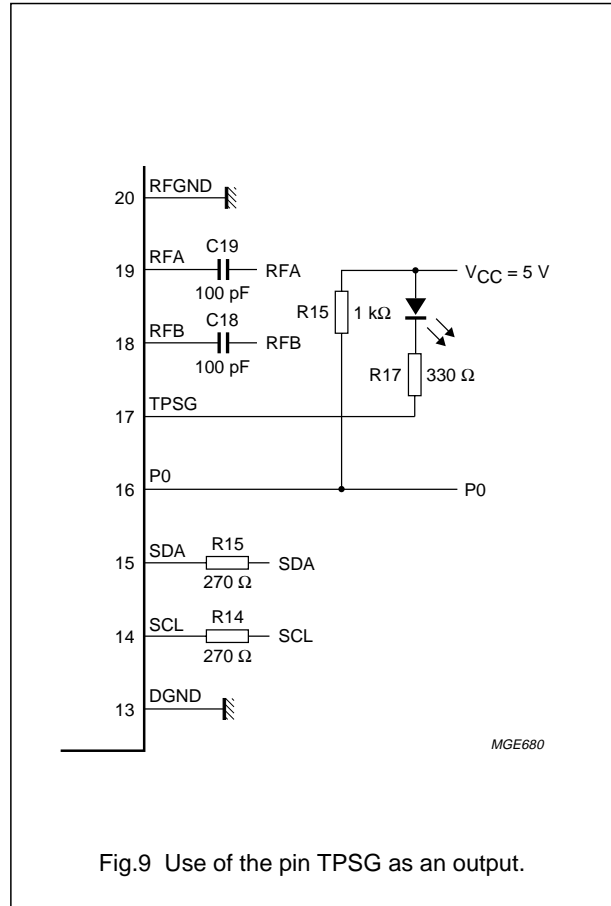
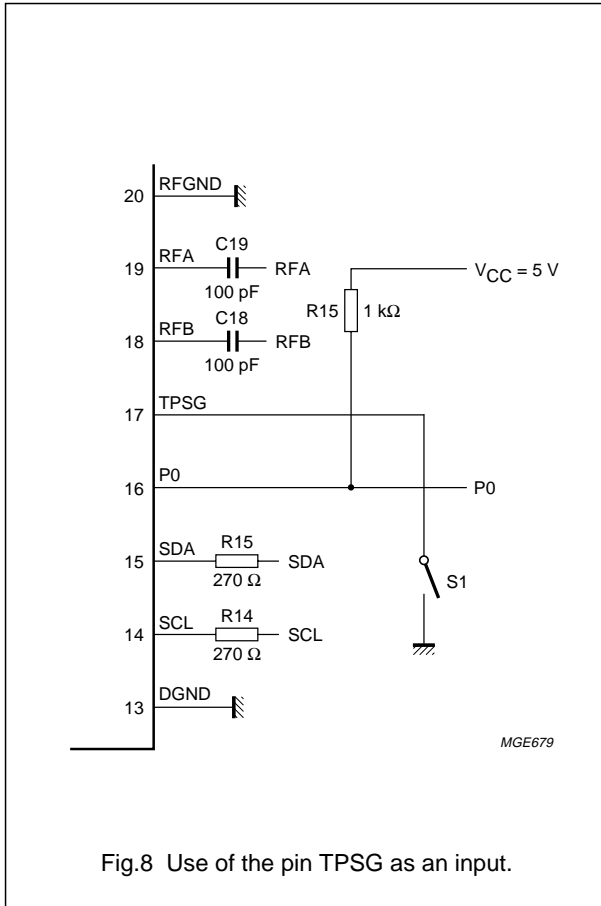
This IC has been designed to have the lowest level of unwanted RF harmonics at the frequencies where these are the hardest to be filtered out, especially for the second harmonic of the RF carrier at the lowest frequencies of the UHF band.

It is possible to reduce the level of the second harmonic by using a wide-band transformer at the output of the IC and create a symmetrical application.

To reduce the out-of-band harmonics and especially the third one, it is necessary to use a low-pass filter at the output of the IC.

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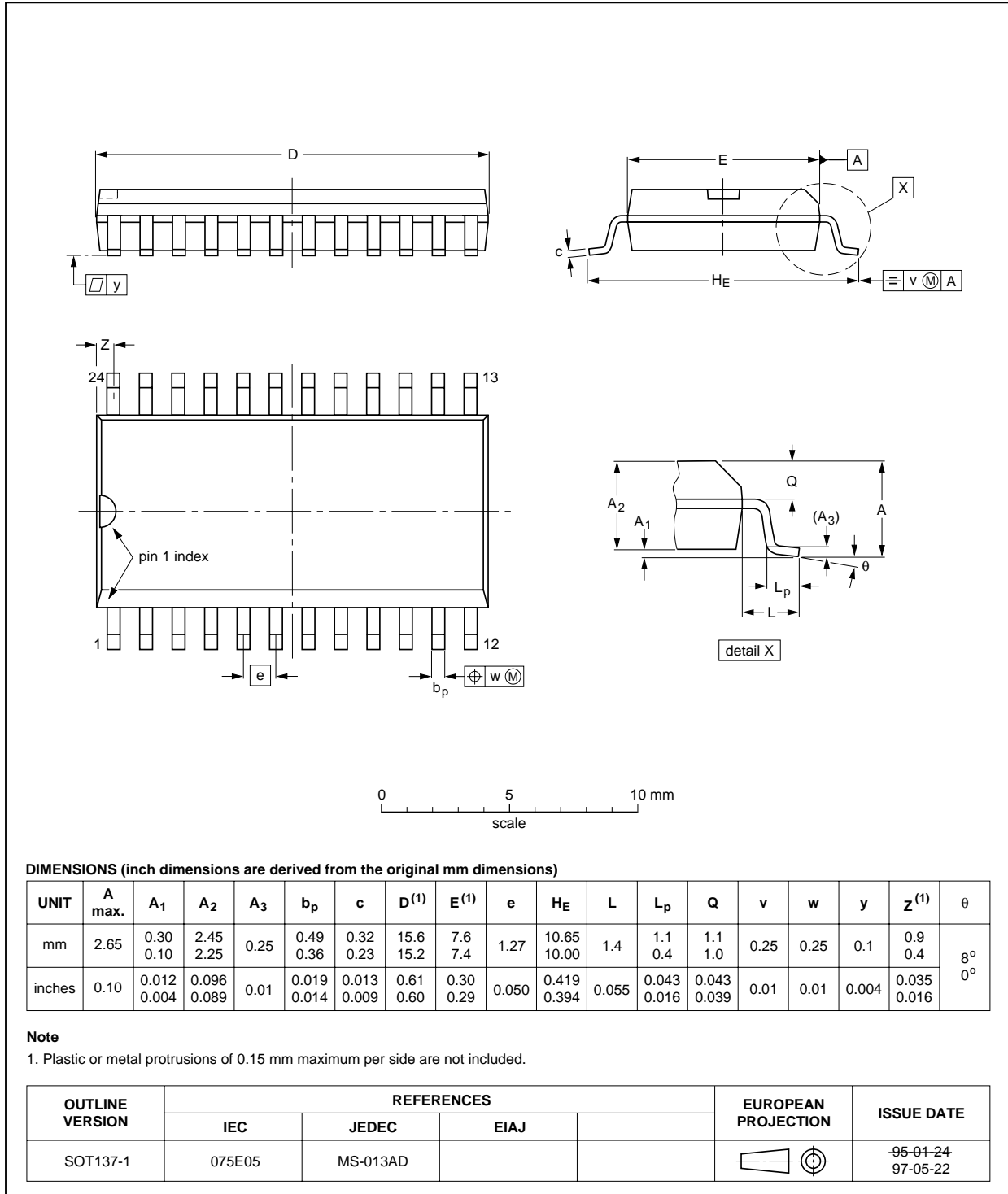
# Universal I<sup>2</sup>C-bus programmable RF modulator

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## PACKAGE OUTLINES

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



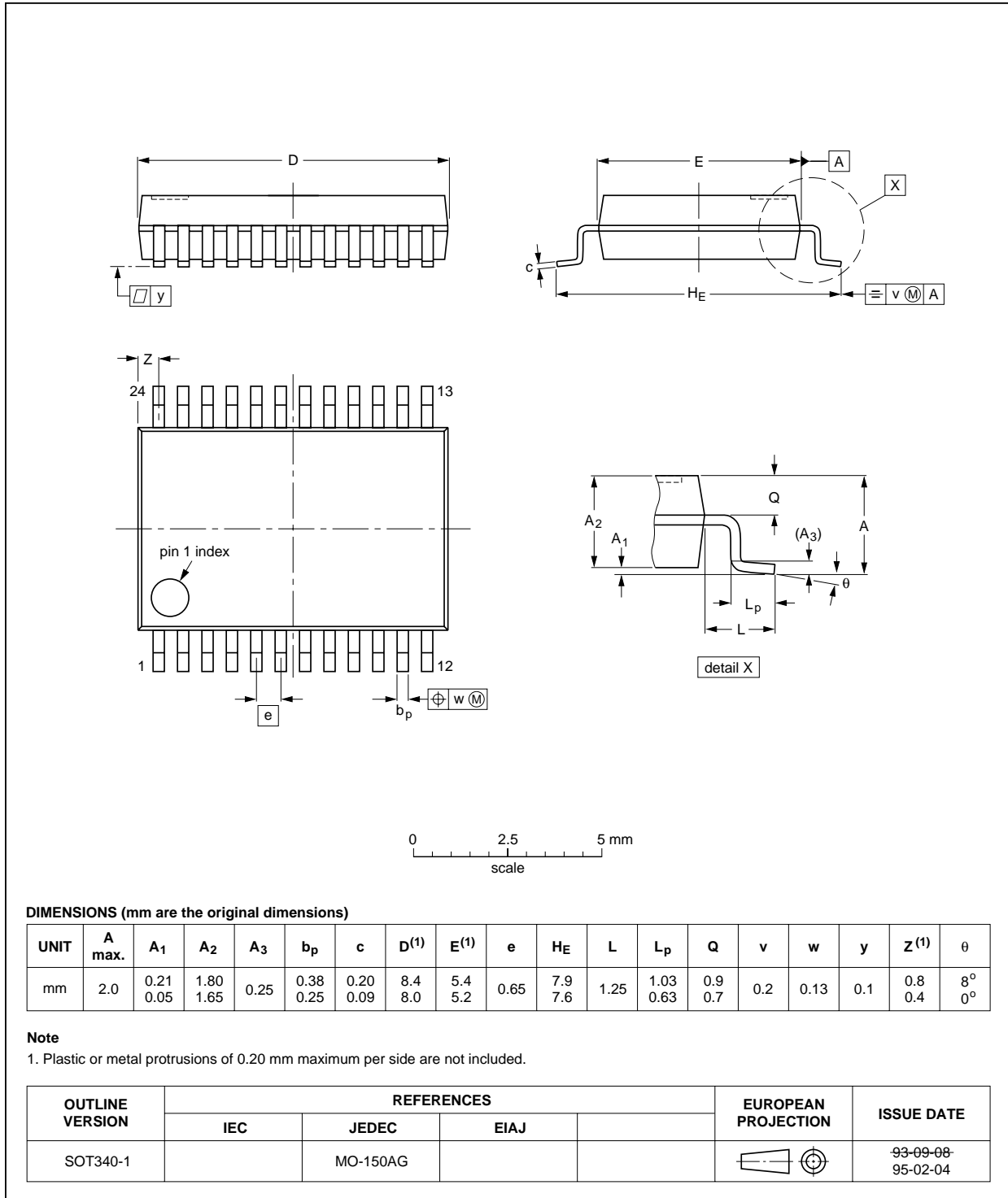


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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



# Universal I<sup>2</sup>C-bus programmable RF modulator

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## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

### Reflow soldering

Reflow soldering techniques are suitable for all SO and SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

### Wave soldering

#### SO

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

#### SSOP

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

**Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**

#### METHOD (SO AND SSOP)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

# Universal I<sup>2</sup>C-bus programmable RF modulator

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## DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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