

# 74LVX74

## Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

### Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

### General Description

The LVX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.


Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  (Set) sets Q to HIGH level
- LOW input to  $\bar{C}_D$  (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

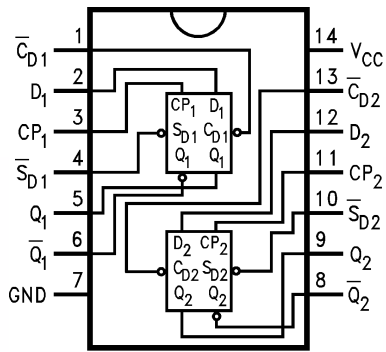
### Ordering Information

Order Number	Package Number	Package Description
74LVX74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

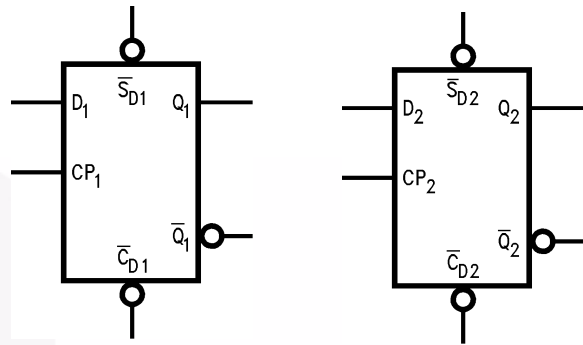
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

### Connection Diagram



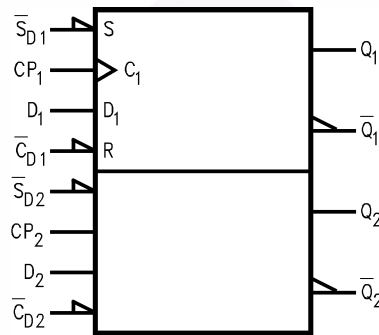
### Logic Symbols



### Pin Description

Pin Names	Description
D <sub>1</sub> , D <sub>2</sub>	Data Inputs
CP <sub>1</sub> , CP <sub>2</sub>	Clock Pulse Inputs
$\overline{C}_{D1}$ , $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$ , $\overline{S}_{D2}$	Direct Set Inputs
Q <sub>1</sub> , $\overline{Q}_1$ , Q <sub>2</sub> , $\overline{Q}_2$	Outputs

### IEEE/IEC



### Truth Table

(Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q <sub>0</sub>	$\overline{Q}_0$

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

Q<sub>0</sub>( $\overline{Q}_0$ ) = Previous Q( $\overline{Q}$ ) before LOW-to-HIGH Transition of Clock

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$I_{IK}$	DC Input Diode Current, $V_I = -0.5V$	-20mA
$V_I$	DC Input Voltage	-0.5V to 7V
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$	-20mA
	$V_O = V_{CC} + 0.5V$	+20mA
$V_O$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	$\pm 25mA$
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
P	Power Dissipation	180mW

## Recommended Operating Conditions<sup>(1)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	2.0V to 3.6V
$V_I$	Input Voltage	0V to 5.5V
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0ns/V to 100ns/V

### Note:

- Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V <sub>IH</sub>	HIGH Level Input Voltage	2.0		1.5			1.5		V
		3.0		2.0			2.0		
		3.6		2.4			2.4		
V <sub>IL</sub>	LOW Level Input Voltage	2.0				0.5		0.5	V
		3.0				0.8		0.8	
		3.6				0.8		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -50μA	1.9	2.0		1.9		V
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -50μA	2.9	3.0		2.9		
			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -4mA	2.58			2.48		
V <sub>OL</sub>	LOW Level Output Voltage	2.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 50μA		0.0	0.1		0.1	V
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 50μA		0.0	0.1		0.1	
			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 4mA			0.36		0.44	
I <sub>IN</sub>	Input Leakage Current	3.6	V <sub>IN</sub> = 5.5V or GND			±0.1		±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	3.6	V <sub>IN</sub> = V <sub>CC</sub> or GND			2.0		20.0	μA

Noise Characteristics<sup>(2)</sup>

Symbol	Parameter	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C		Units
				Typ.	Limit	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	50	0.3	0.5	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	50	-0.3	-0.5	V
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	3.3	50		2.0	V
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage	3.3	50		0.8	V

## Note:

2. Input  $t_r = t_f = 3ns$

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, CP <sub>n</sub> to Q <sub>n</sub> or $\bar{Q}_n$	2.7	15		7.3	15	1.0	18.5	ns
			50		9.8	18.5	1.0	22	
		3.3 ± 0.3	15		5.7	9.7	1.0	11.5	
			50		8.2	13.2	1.0	15	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, $\bar{C}_{Dn}$ to $\bar{S}_{Dn}$ to Q <sub>n</sub> or $\bar{Q}_n$	2.7	15		8.4	15.6	1.0	18.5	ns
			50		10.9	19.1	1.0	22	
		3.3 ± 0.3	15		6.6	10.1	1.0	12	
			50		9.1	13.6	1.0	15.5	
t <sub>W</sub>	CP <sub>n</sub> or $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ Pulse Width	2.7		8.5		10		ns	
		3.3 ± 0.3		6		7			
t <sub>S</sub>	Setup Time, D <sub>n</sub> to CP <sub>n</sub>	2.7		8.0		9.5		ns	
		3.3 ± 0.3		5.5		6.5			
t <sub>H</sub>	Hold Time, D <sub>n</sub> to CP <sub>n</sub>	2.7		0.5		0.5		ns	
		3.3 ± 0.3		0.5		0.5			
t <sub>REC</sub>	Recovery Time, $\bar{C}_{Pn}$ or $\bar{S}_{Dn}$ to CP <sub>n</sub>	2.7		6.5		7.5		ns	
		3.3 ± 0.3		5.0		5.0			
f <sub>MAX</sub>	Maximum Clock Frequency	2.7	15	55	135	50		MHz	
			50	45	60	40			
		3.3 ± 0.3	15	95	145	80			
			50	60	85	50			
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew <sup>(3)</sup>	2.7	50			1.5	1.5	ns	
		3.3				1.5	1.5		

## Note:

3. Parameter guaranteed by design  $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

## Capacitance

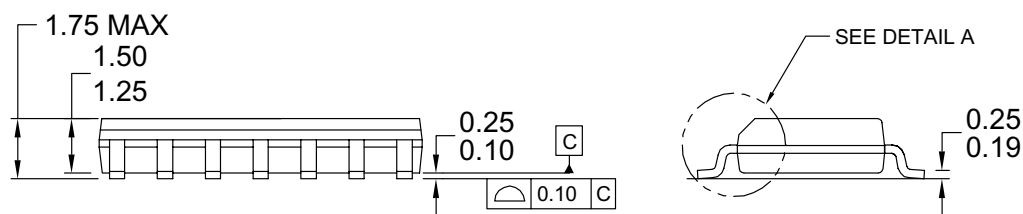
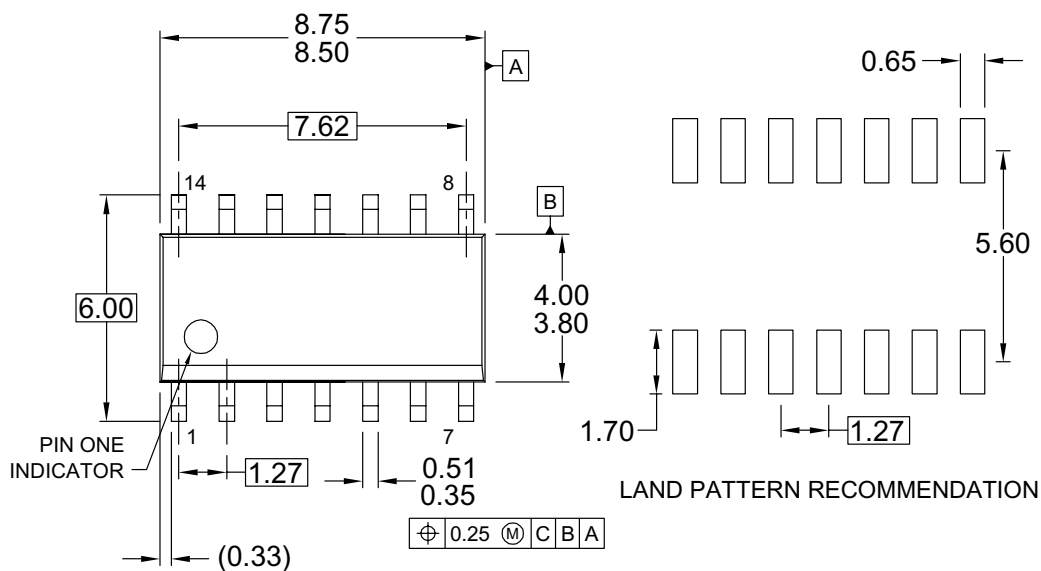
Symbol	Parameter	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
		Min.	Typ.	Max.	Min.	Max.	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance <sup>(4)</sup>		25				pF

## Note:

4. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

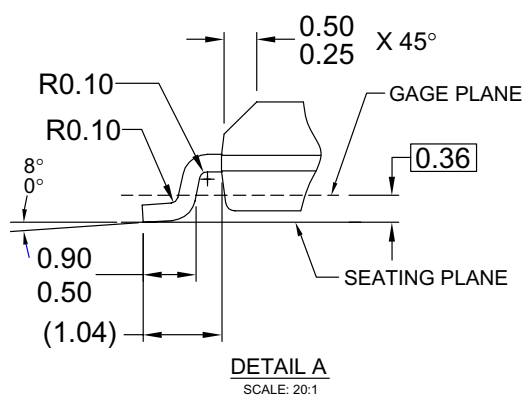
Average operating current can be obtained by the equation:  $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{2 \text{ (per F/F)}}$

### Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13



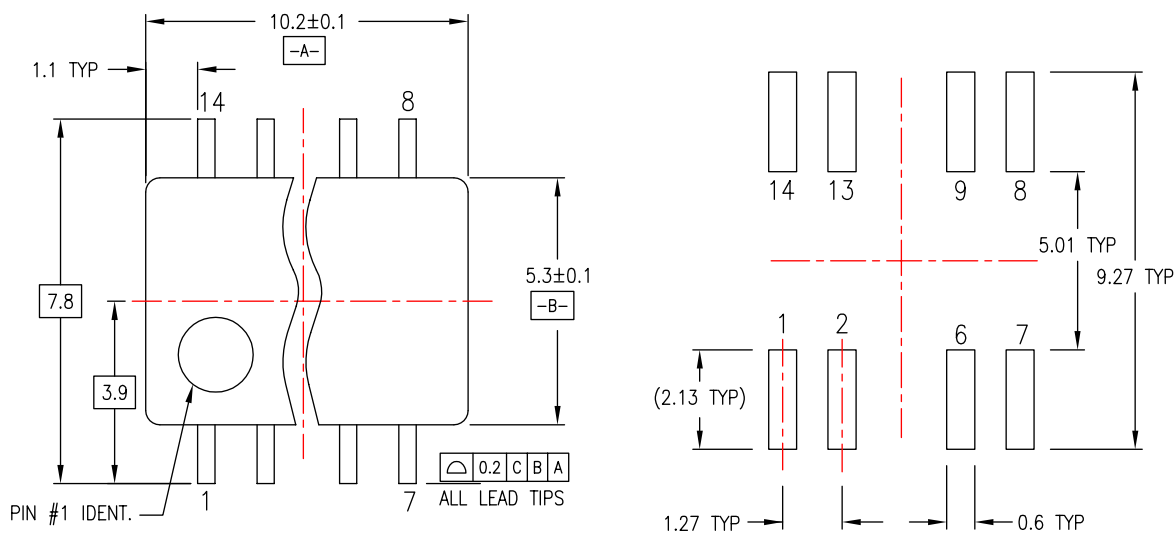
**Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

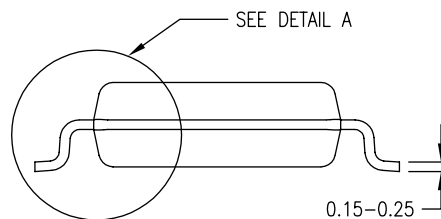
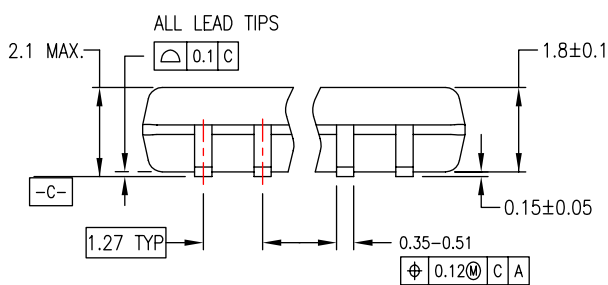
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**Physical Dimensions (Continued)**



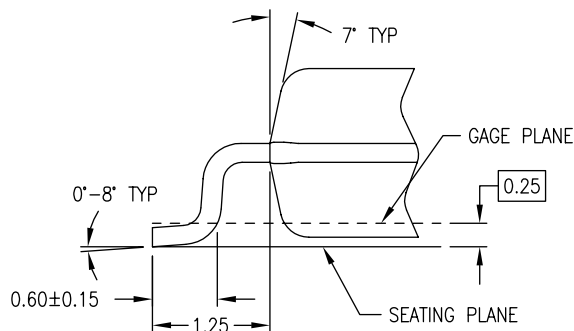
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



DETAIL A

M14DREVC

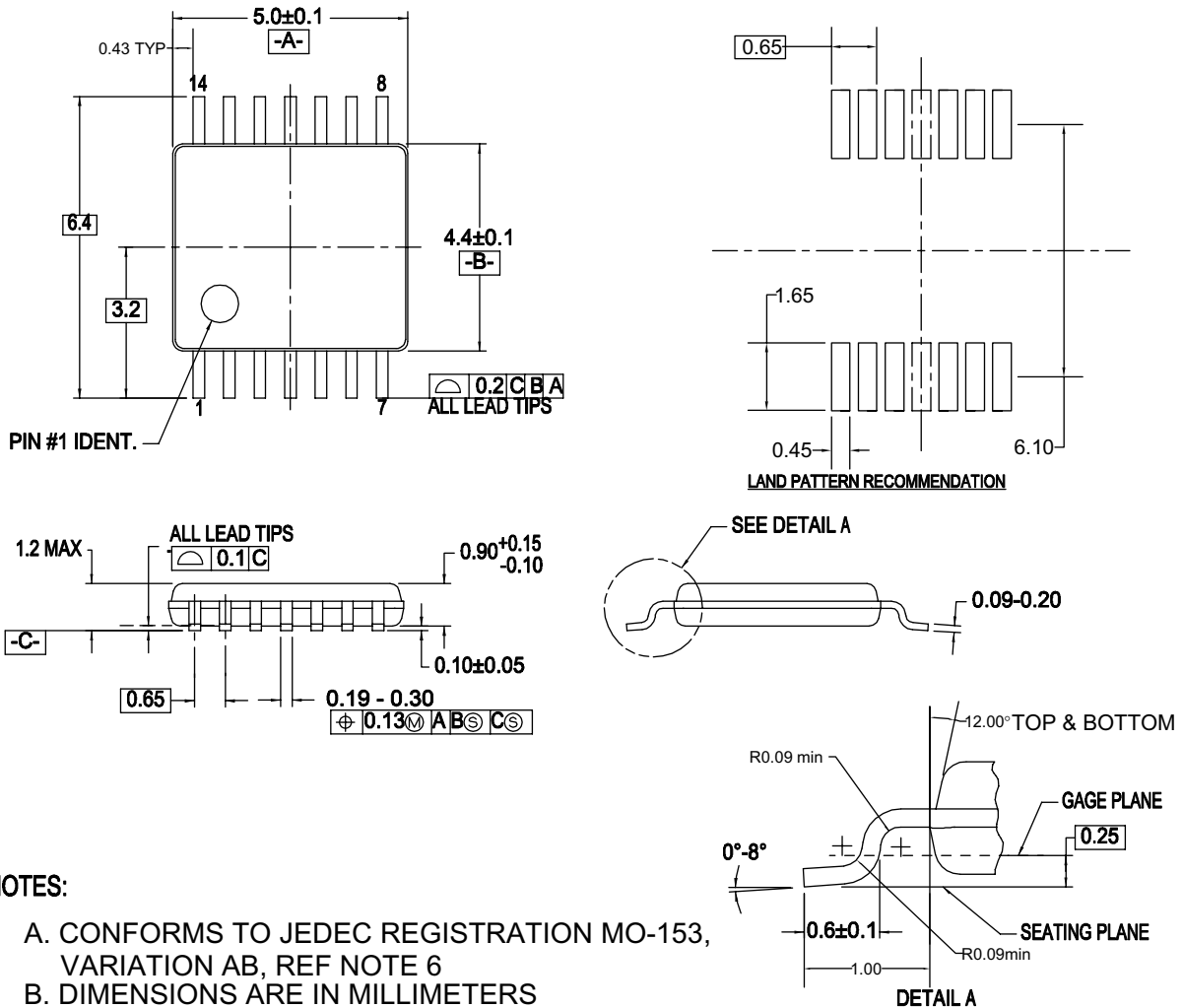
**Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

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**Physical Dimensions** (Continued)



**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

**Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**

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