12-Bit, 65 MSPS, Dual ADC

AD15252

FEATURES

12-bit, 65 MSPS dual ADC
Differential input with 100 Ω input impedance
Full-scale analog input: 296 mV p-p
170 MHz, 3 dB bandwidth
SNR (–9 dBFS): 64 dBFS (70 MHz AIN), 64 dBFS (140 MHz AIN)
SFDR (–9 dBFS): 77 dBFS (70 MHz AIN), 73 dBFS (140 MHz AIN)
435 mW per channel
Dual parallel output buses
Out-of-range indicators
Independent clocks
Duty cycle stabilizer
Twos complement or offset binary data format

APPLICATIONS

Antijam GPS receivers
Wireless and wired broadband communications
Communications test equipment

FUNCTIONAL BLOCK DIAGRAM

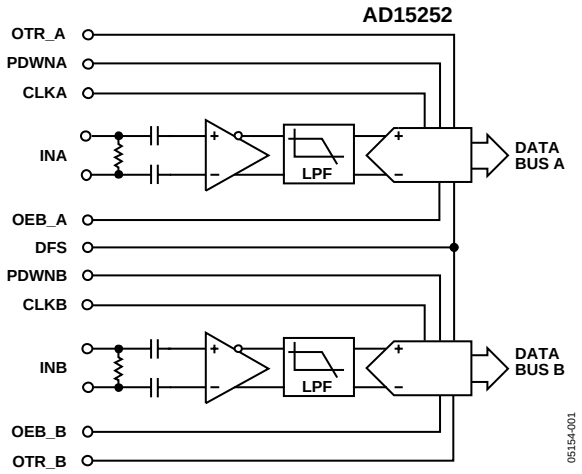

Figure 1.

GENERAL DESCRIPTION

The AD15252 is a dual, 12-bit, 65 MSPS, analog-to-digital converter (ADC). It features a differential front-end amplification circuit followed by a sample-and-hold amplifier and multistage pipeline ADC. It is designed to operate with a 3.3 V analog supply and a 2.5 V/3.3 V digital supply. Each input is fully differential, ac-coupled, and terminated in 100 Ω input impedances. The full-scale differential signal input range is 296 mV p-p.

Two parallel, 12-bit digital output buses provide data flow from the ADCs. The digital output data is presented in either straight binary or twos complement format. Out-of-range (OTR) signals indicate an overflow condition, which can be used with the most significant bit to determine low or high overflow. Dual single-ended clock inputs control all internal conversion cycles. A duty cycle stabilizer allows wide variations in the clock duty cycle while maintaining excellent performance. The AD15252 is optimized for applications in antijam global positioning receivers and is well suited for communications applications.

PRODUCT HIGHLIGHTS

1. Dual 12-bit, 65 MSPS ADC with integrated analog signal conditioning optimized for antijam global positioning system receiver (AJ-GPS) applications.
2. Operates from a single 3.3 V power supply and features a separate digital output driver supply to accommodate 2.5 V and 3.3 V logic families.
3. Packaged in a space-saving 8 mm × 8 mm chip scale package ball grid array (CSP_BGA) and is specified over the industrial temperature range (–40°C to +85°C).

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

8/05—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

AVDD = 3.3 V, DRVDD = 2.5 V, encode = 65 MSPS, CLK_A = CLK_B, AIN = −9 dBFS differential input, T_A= 25°C, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION				12		Bits
ACCURACY						
No Missing Codes	25°C	IV		Guaranteed		
Offset Error	25°C	I	−6	±1.7	+6	% FSR
Gain Error	25°C	I	−12.5	±2.0	+12.5	% FSR
Differential Nonlinearity (DNL)	Full	V		±0.35		LSB
Integral Nonlinearity (INL)	Full	V		±0.8		LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		±9		ppm/°C
Gain Error	Full	V		±172		ppm/°C
MATCHING CHARACTERISTICS						
Offset Error	Full	V		±2.0		% FSR
Gain Error	Full	V		±1.0		% FSR
Input Referred Noise	Full	V		0.87		LSB rms
ANALOG INPUT						
Input Range	Full	IV		296		mV p-p
Input Resistance (R_{IN})[1]	25°C	V		100		Ω
Input Capacitance (C_{IN})[1]	25°C	V		1.8		pF
CLOCK INPUTS						
High Level Input Voltage (V_{IH})	Full	IV	2.0			V
Low Level Input Voltage (V_{IL})	Full	IV			0.8	V
High Level Input Current (I_{IH})	Full	IV	−10		+10	µA
Low Level Input Current (I_{IL})	Full	IV	−10		+10	µA
Input Capacitance (C_{IN})	Full	V		2		pF
LOGIC OUTPUTS						
High Level Output Voltage (V_{OH})	Full	IV	2.49			V
Low Level Output Voltage (V_{OL})	Full	IV			0.2	V
INTERFACE TIMING						
Maximum Conversion Rate	Full	VI	65			MSPS
Minimum Conversion Rate	Full	IV			1	MSPS
Clock Period (t_C)	Full	V		15.4		ns
Clock Width High (t_{CH})	Full	IV	6.2			ns
Clock Width Low (t_{CL})	Full	IV	6.2			ns
Clock to Data (t_{OD})	Full	IV	2		6	ns
Pipeline Delay (Latency)	Full	V		7		Cycles
POWER SUPPLIES						
Supply Voltages						
AVDD	Full	IV	3.0	3.3	3.6	V
DRVDD	Full	IV	2.25	2.5	3.6	V
Supply Currents						
AVDD	Full	VI		254	280	mA
DRVDD	Full	VI		12	15	mA
Total Power Dissipation	Full	VI		0.87	1.0	W

Parameter	Temp	Test Level	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)						
f_{INPUT} = 70 MHz	25°C	I	62.7	64.2		dBFS
f_{INPUT} = 110 MHz	25°C	V		64.1		dBFS
f_{INPUT} = 140 MHz	25°C	I	62.5	64		dBFS
SINAD						
f_{INPUT} = 70 MHz	25°C	I	62.4	63.9		dBFS
f_{INPUT} = 110 MHz	25°C	V		63.7		dBFS
f_{INPUT} = 140 MHz	25°C	I	61.9	63.3		dBFS
THD						
f_{INPUT} = 70 MHz	Full	V		−76		dBFS
f_{INPUT} = 110 MHz	Full	V		−74		dBFS
f_{INPUT} = 140 MHz	Full	V		−72		dBFS
SPURIOUS-FREE DYNAMIC RANGE (SFDR)						
f_{INPUT} = 70 MHz	25°C	I	72.7	77.8		dBFS
f_{INPUT} = 110 MHz	25°C	V		75.9		dBFS
f_{INPUT} = 140 MHz	25°C	I	68	73.8		dBFS
CROSSTALK	25°C	V		−70		dB

[1] Input resistance and capacitance shown as differential.

Table 2. Explanation of Test Levels

Test Level	Description
I	100% production tested.
II	100% production tested at 25°C, and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	All devices are 100% production tested at 25°C, guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
AVDD to AGND	−0.3 V, +3.9 V
DRVDD to DRGND	−0.3 V, +3.9 V
DRGND to AGND	−0.3 V, +0.3 V
DRVDD to AVDD	−3.9 V, +3.9 V
Analog Inputs	−0.3 V, AVDD + 0.3 V
Digital Outputs	−0.3 V, DRVDD + 0.3 V
CLK	−0.3 V, AVDD + 0.3 V
Operational Case Temperature	−40°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature: Infrared, 15 sec	230°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

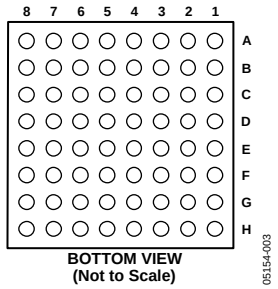

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VINA	Analog Input Pin (+) for Channel A.
A2	$\overline{\text{VINA}}$	Analog Input Pin (–) for Channel A.
H1	VINB	Analog Input Pin (+) for Channel B.
H2	$\overline{\text{VINB}}$	Analog Input Pin (–) for Channel B.
B4	CLK_A	Clock Input Pin for Channel A.
G4	CLK_B	Clock Input Pin for Channel B.
C4	PDWN_A	Power-Down Function Selection for Channel A (Active High).
F4	PDWN_B	Power-Down Function Selection for Channel B (Active High).
A4	OTR_A	Out-of-Range Indicator for Channel A.
E8	OTR_B	Out-of-Range Indicator for Channel B.
A3	VCM_A	Channel A Common Mode.
H3	VCM_B	Channel B Common Mode.
D4	OEB_A	Output Enable for Channel A. Logic 0 enables Data Bus A; Logic 1 sets outputs to high-Z.
E4	OEB_B	Output Enable for Channel B. Logic 0 enables Data Bus B; Logic 1 sets outputs to high-Z.
C5	D11_A(MSB)	Channel A Data Output Bit 11 (MSB).
A5	D10_A	Channel A Data Output Bit 10.
B5	D09_A	Channel A Data Output Bit 9.
A6	D08_A	Channel A Data Output Bit 8.
B6	D07_A	Channel A Data Output Bit 7.
A7	D06_A	Channel A Data Output Bit 6.
B7	D05_A	Channel A Data Output Bit 5.
A8	D04_A	Channel A Data Output Bit 4.
C6	D03_A	Channel A Data Output Bit 3.
B8	D02_A	Channel A Data Output Bit 2.
C7	D01_A	Channel A Data Output Bit 1.
C8	D00_A(LSB)	Channel A Data Output Bit 0 (LSB).
E3	DFS	Data Output Format Select Bit (Logic 0 for offset binary, Logic 1 for twos complement).
E7	D11_B(MSB)	Channel B Data Output Bit 11 (MSB).
F8	D10_B	Channel B Data Output Bit 10.
F7	D09_B	Channel B Data Output Bit 9.
G8	D08_B	Channel B Data Output Bit 8.

Pin No.	Mnemonic	Description
F6	D07_B	Channel B Data Output Bit 7.
H8	D06_B	Channel B Data Output Bit 6.
G7	D05_B	Channel B Data Output Bit 5.
H7	D04_B	Channel B Data Output Bit 4.
G6	D03_B	Channel B Data Output Bit 3.
H6	D02_B	Channel B Data Output Bit 2.
G5	D01_B	Channel B Data Output Bit 1.
H5	D00_B	Channel B Data Output Bit 0 (LSB).
C1 to C3, F1 to F3	AVDD	Analog Power Supply.
B1 to B3, D3, G1 to G3	AGND	Analog Ground.
D6, E6	DRVDD	Digital Output Driver Supply.
D5, E5	DRGND	Digital Output Ground.
E1	REFT	Differential Reference (+).
E2	REFB	Differential Reference (–).
D1	VREF	Voltage Reference.
D2	REF_RTN	Voltage Reference Return
H4, F5, D7, D8	DNC1 to DNC4	No Connect.

TYPICAL PERFORMANCE CHARACTERISTICS

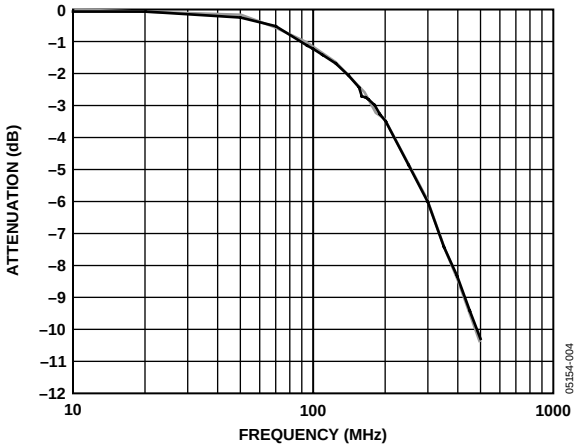

Figure 3. Gain Flatness

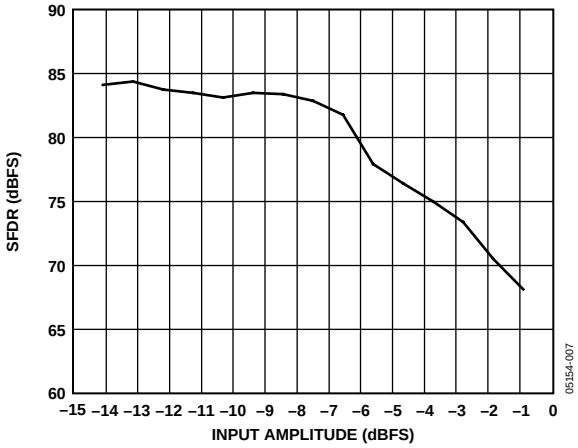

Figure 6. Single-Tone SFDR vs. AIN with f_{IN} = 70 MHz

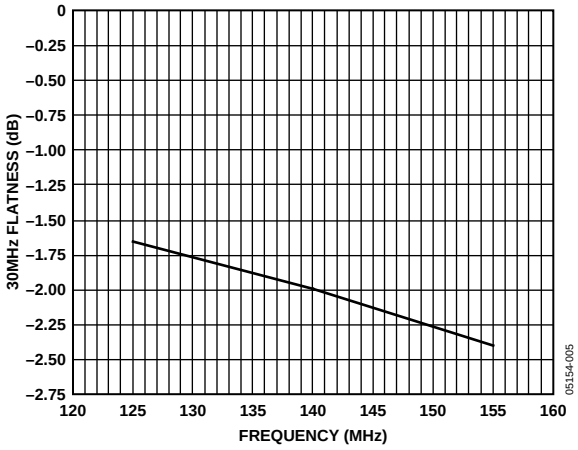

Figure 4. Gain Flatness f_{IN} =125MHz to 155 MHz

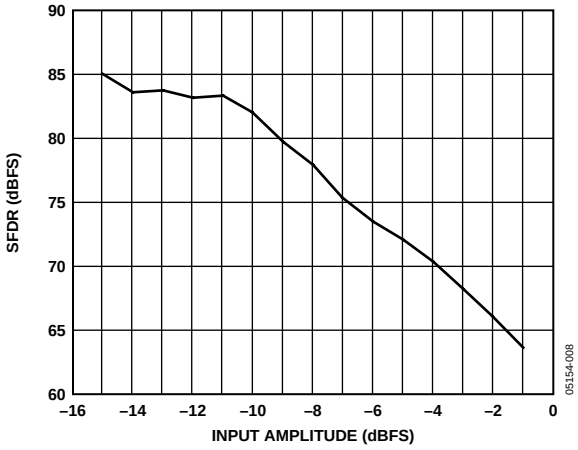

Figure 7. Single-Tone SFDR vs. AIN with f_{IN} = 110 MHz

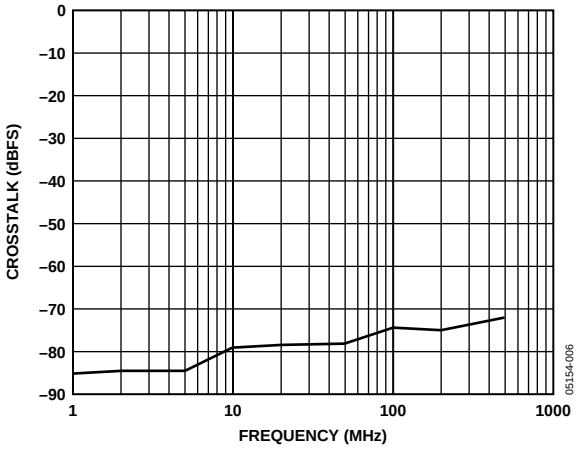

Figure 5. Typical Crosstalk

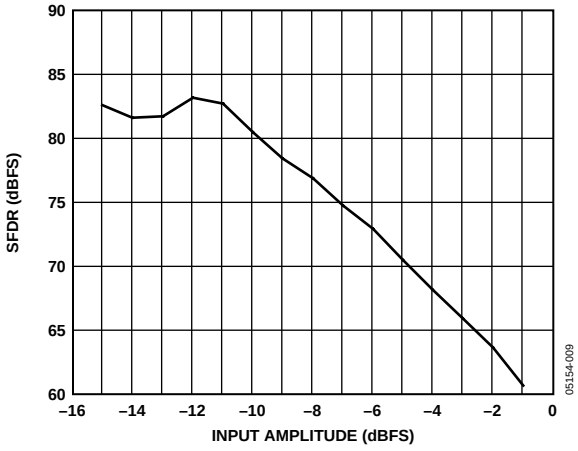

Figure 8. Single-Tone SFDR vs. AIN with f_{IN} = 140 MHz

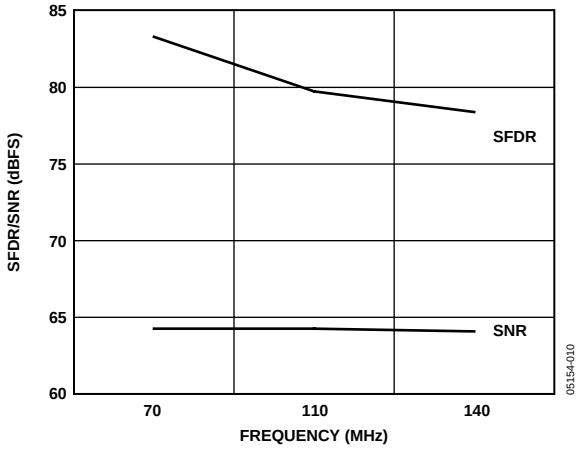

Figure 9. Single-Tone SNR/SFDR vs. f_{IN}

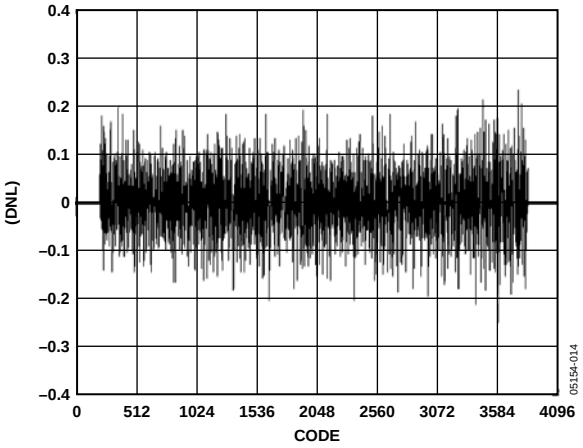

Figure 12. Typical DNL

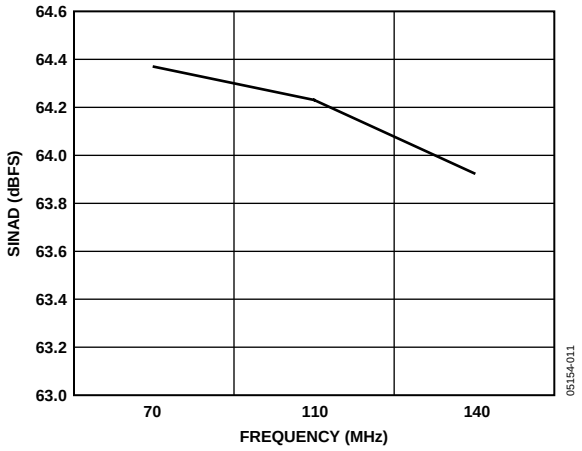

Figure 10. Single-Tone SINAD vs. f_{IN}

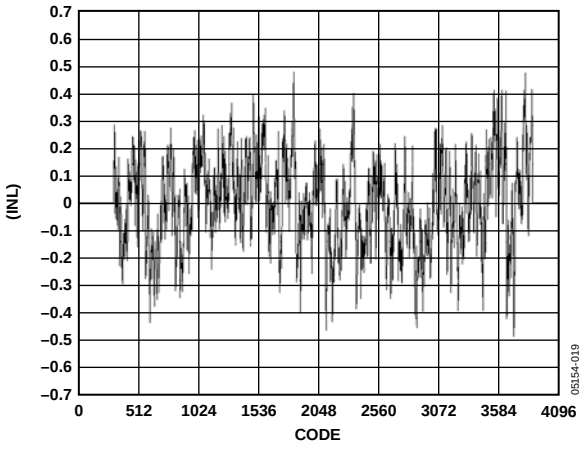

Figure 13. Typical INL

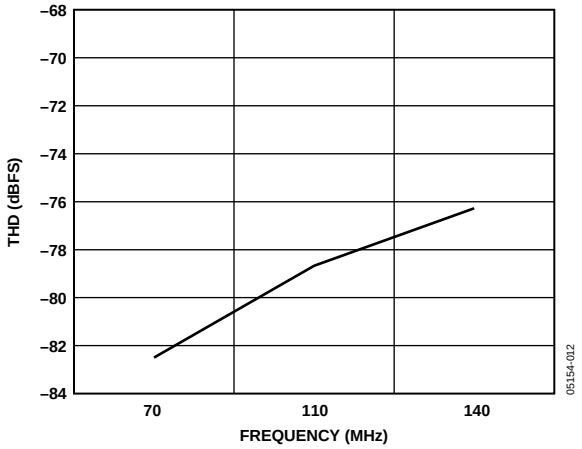

Figure 11. Single-Tone THD vs. f_{IN}

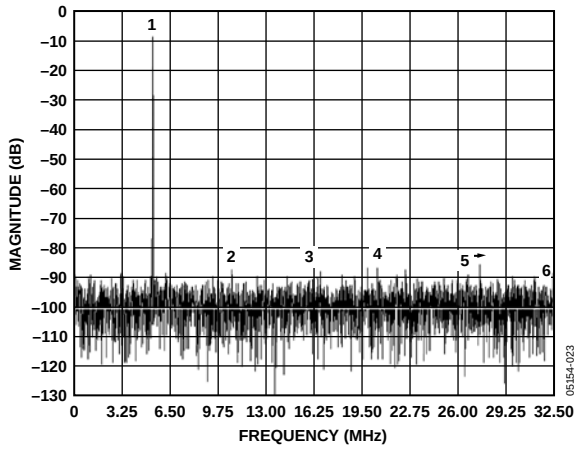

Figure 14. Single-Tone FFT of Channel A Digitizing f_{IN} = 70 MHz @ –9 dBFS While Channel B Digitizes f_{IN} = 70 MHz @ –9 dBFS

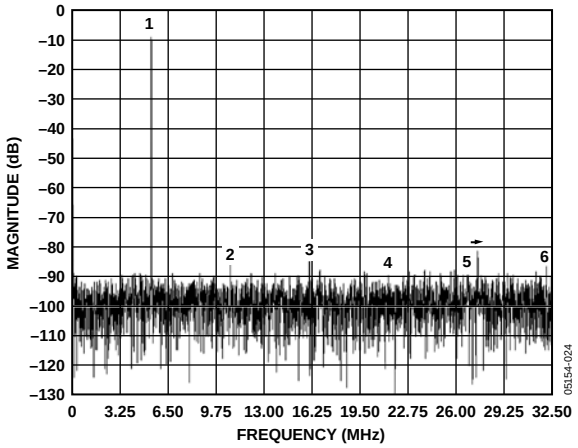

Figure 15. Single-Tone FFT of Channel B Digitizing f_{IN} = 70 MHz @ –9 dBFS While Channel A Digitizes f_{IN} = 70 MHz @ –9 dBFS

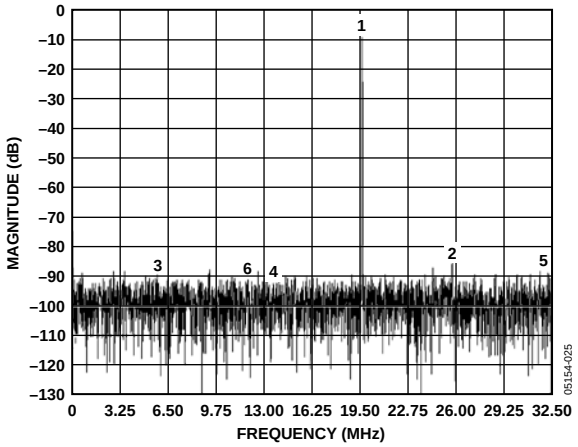

Figure 16. Single-Tone FFT of Channel A Digitizing f_{IN} = 110 MHz @ –9 dBFS While Channel B Digitizes f_{IN} = 110 M z @ –9 dBFS

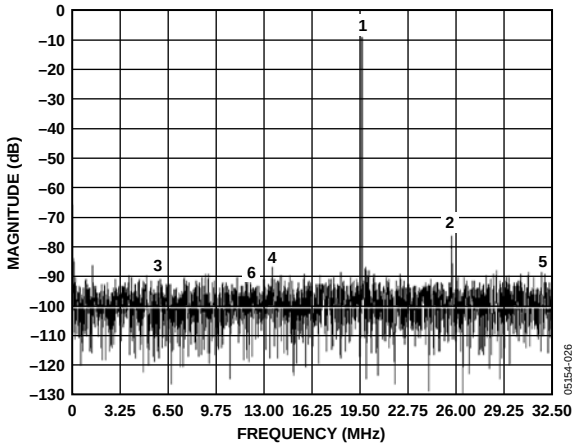

Figure 17. Single-Tone FFT of Channel B Digitizing f_{IN} = 110 MHz @ –9 dBFS While Channel A Digitizes f_{IN} = 110 MHz @ –9 dBFS

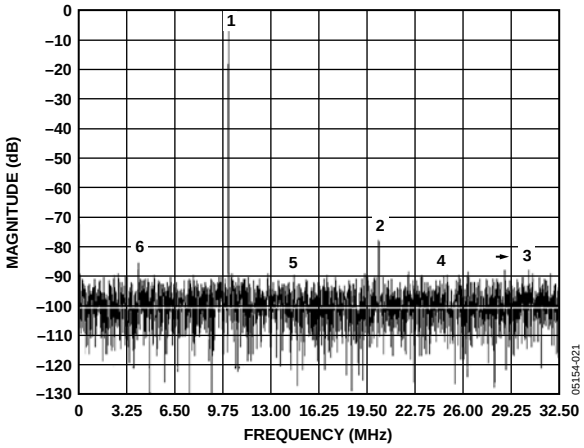

Figure 18. Single-Tone FFT of Channel A Digitizing f_{IN} = 140 MHz @ –9 dBFS While Channel B Digitizes f_{IN} = 140 MHz @ –9 dBFS

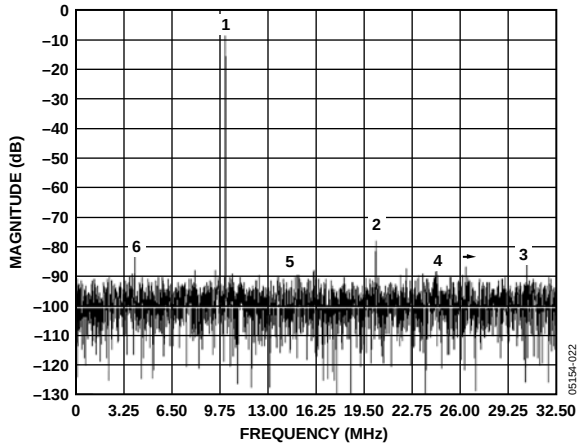

Figure 19. Single-Tone FFT of Channel B Digitizing f_{IN} = 140 MHz @ –9 dBFS While Channel A Digitizes f_{IN} = 140 MHz @ –9dBFS

THEORY OF OPERATION

The AD15252 consists of two high performance ADC channels. The dual ADC paths are independent, except for a shared internal band gap reference source, VREF. Each path consists of a differential front end amplification circuit followed by a sample-and-hold amplifier and multistage pipeline ADC.

The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing.

ANALOG INPUT

Each analog input is fully differential, allowing sampling of differential input signals. The differential input signals are ac-coupled and terminated in 100 Ω input impedances. The full-scale differential signal input range is 296 mV p-p.

VOLTAGE REFERENCE

The internal voltage reference of the ADC is pin strapped to a fixed value of 0.5 V. A 10 µF capacitor should be used between REFT and REFB.

CLOCK INPUT AND CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, can be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD15252 provides separate clock inputs for each channel. The optimum performance is achieved with the clocks operated at the same frequency and phase. Clocking the channels asynchronously can significantly degrade performance. In some applications, it is desirable to skew the clock timing of adjacent channels. The AD15252's separate clock inputs allow clock timing skew (typically ±1 ns) between the channels without significant performance degradation.

The AD15252 contains two internal clock duty cycle stabilizers (DCS), one for each converter, which retime the nonsampling edge, providing an internal clock with a nominal 50% duty cycle. Input clock rates of over 40 MHz can use the DCS so that a wide range of input clock duty cycles can be accommodated. Maintaining a 50% duty cycle clock is particularly important in high speed applications, when proper track-and-hold times for the converter are required to maintain high performance.

The duty cycle stabilizer uses a delay-locked loop to create the nonsampling edge. As a result, any change to the sampling frequency requires approximately 2 µs to 3 µs to allow the DLL to acquire and settle to the new rate.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \times \log 10\ (1/2 \times p \times f_{INPUT} \times t_J)$$

In the equation, the rms aperture jitter, t_J, represents the root-sum square of all jitter sources, which includes the clock input, analog input signal, and ADC aperture jitter specification.

Undersampling applications are particularly sensitive to jitter.

For optimal performance, especially in cases where aperture jitter can affect the dynamic range of the AD15252, it is important to minimize input clock jitter. The clock input circuitry should use stable references, for example, using analog power and ground planes to generate the valid high and low digital levels for the AD15252 clock input. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

POWER DISSIPATION AND STANDBY MODE

The power dissipated by the AD15252 is proportional to its sampling rates. The digital (DRVDD) power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The digital drive current can be calculated by

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLOCK} \times N$$

where:
N is the number of bits changing.
C_{LOAD} is the average load on the digital pins that changed.

The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates that increase with clock frequency.

Either channel of the AD15252 can be placed into standby mode independently by asserting the PDWN_A or PDWN_B pins.

The minimum standby power is achieved when both channels are placed into full power-down mode using PDWN_A = PDWN_B = high. Under this condition, the internal references are powered down. When either or both of the channel paths are enabled after a power-down, the wake-up time is directly related to the recharging of the REFT and REFB decoupling capacitors and to the duration of the power-down. Typically, it takes approximately 5 ms to restore full operation with fully discharged 10 µF decoupling capacitors on REFT and REFB.

A single channel can be powered down for moderate power savings. The powered-down channel shuts down internal circuits, but both the reference buffers and shared reference remain powered. Because the buffer and voltage reference remain powered, the wake-up time is reduced to several clock cycles.

When using only one channel of the AD15252, the clock for the disabled channel should also be disabled, or distortion occurs in the channel in use.

DIGITAL OUTPUTS

The AD15252 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies, which can affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fan-outs can require external buffers or latches.

The data format can be selected for either offset binary or twos complement. This is discussed later in the Data Format section.

TIMING

The AD15252 provides latched data outputs with a pipeline delay of seven clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal. Refer to Figure 20 for a detailed timing diagram.

The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD15252. These transients can detract from the converter's dynamic performance.

The lowest typical conversion rate of the AD15252 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance can degrade.

DATA FORMAT

The AD15252 data output format can be configured for either twos complement or offset binary. This is controlled by the data format select pin (DFS). Connecting DFS to AGND produces offset binary output data. Conversely, connecting DFS to AVDD formats the output data as twos complement.

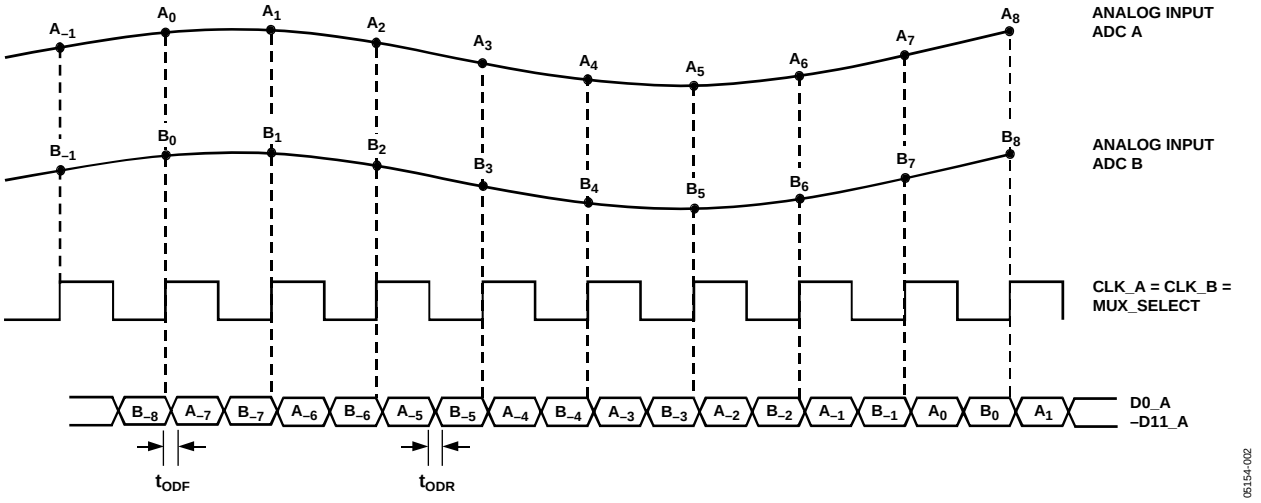

Figure 20. Example of Multiplexed Data Format Using the Channel A Output and the Same Clock Tied to CLK_A, CLK_B, and MUX_SELECT

PCB AND EVALUATION BOARD

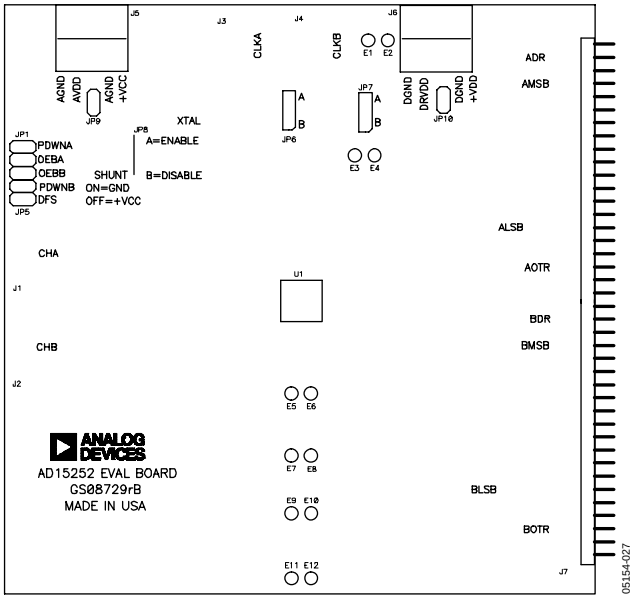

Figure 21. AD15252 Evaluation Board Top Silk

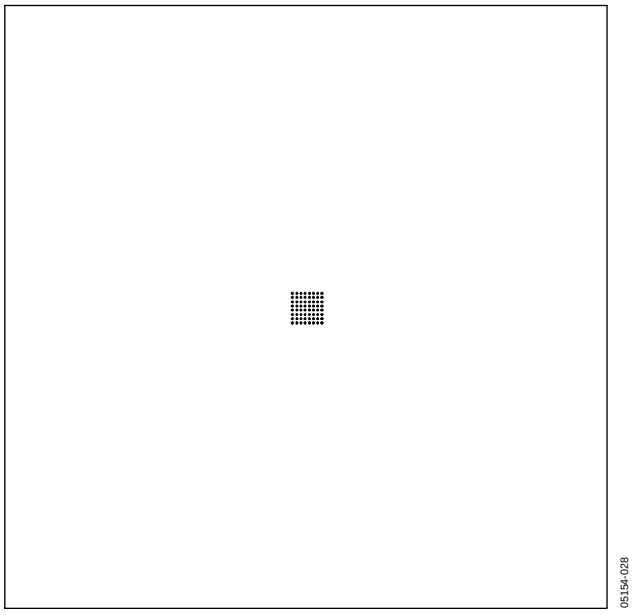

Figure 22. AD15252 Evaluation Board Top Paste

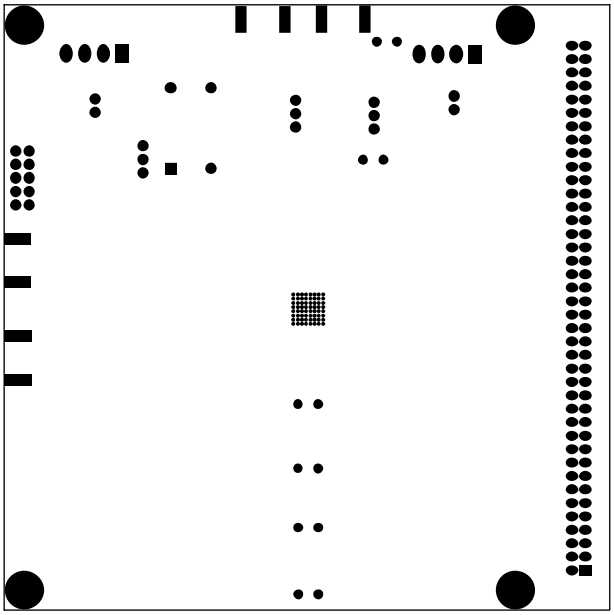

Figure 23. AD15252 Evaluation Board Top Mask

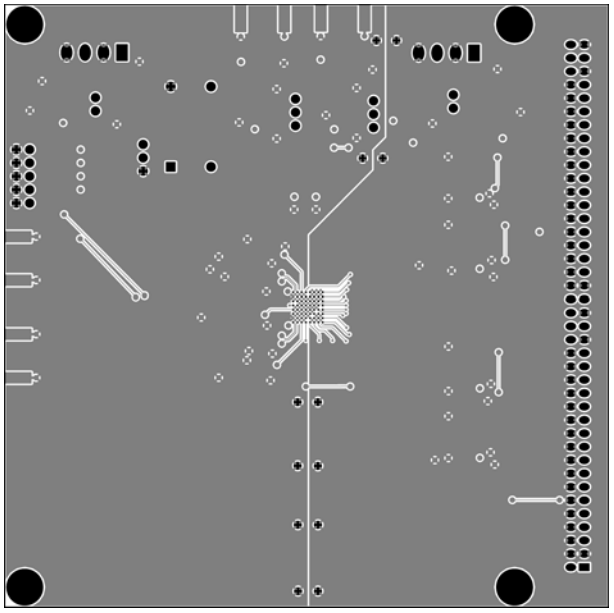

Figure 24. AD15252 Evaluation Board Top Signal

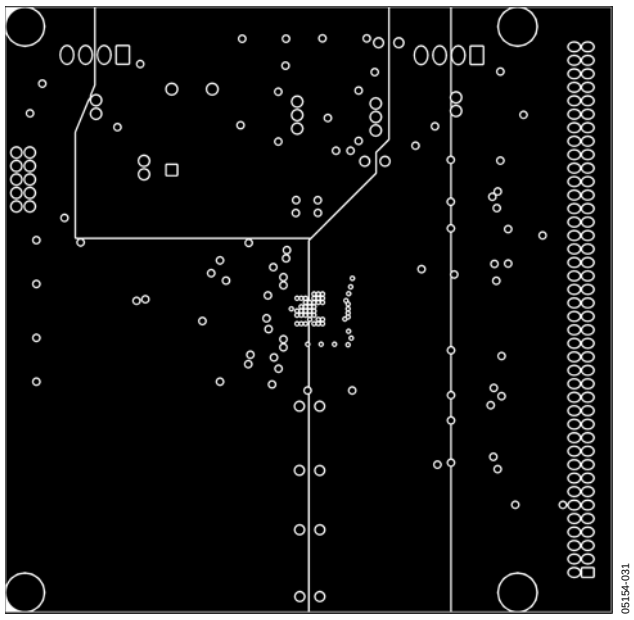

Figure 25. AD15252 Evaluation Board Power Plane

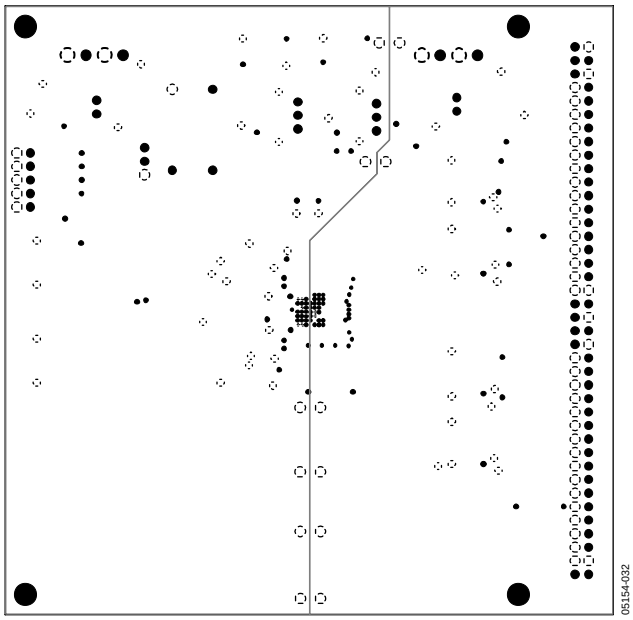

Figure 26. AD15252 Evaluation Board Ground Plane

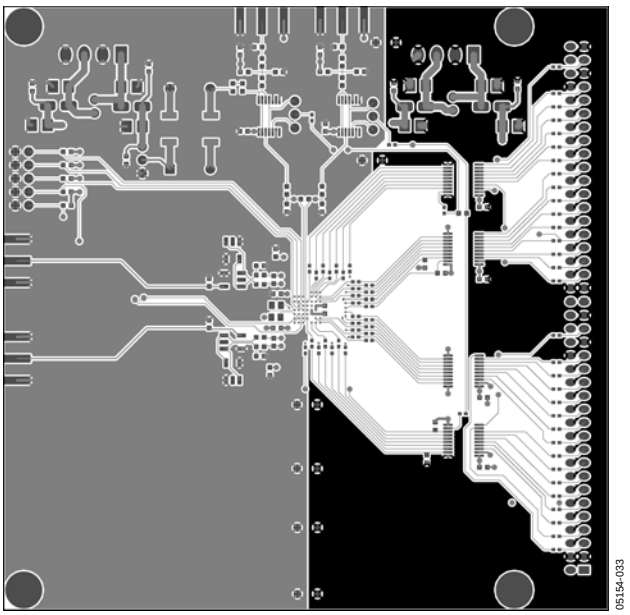

Figure 27. AD15252 Evaluation Board Bottom Signal

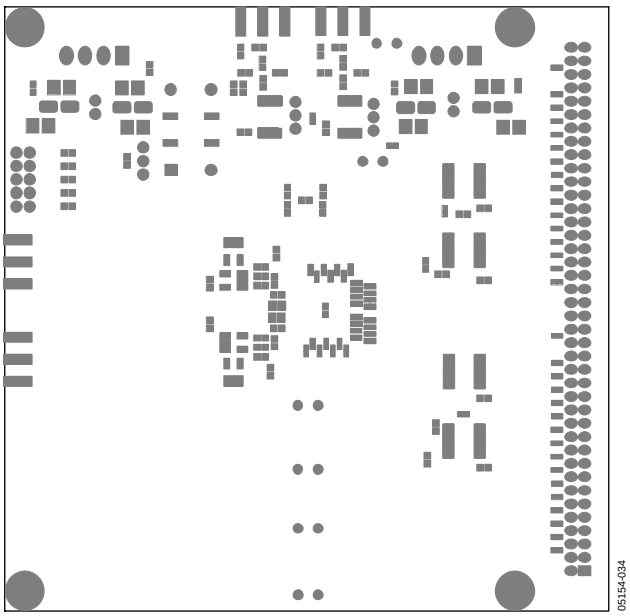

Figure 28. AD15252 Evaluation Board Bottom Mask

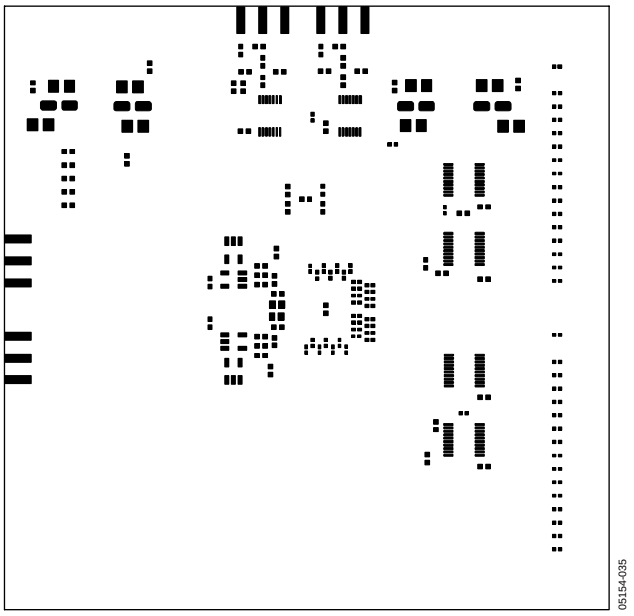

Figure 29. AD15252 Evaluation Board Bottom Paste

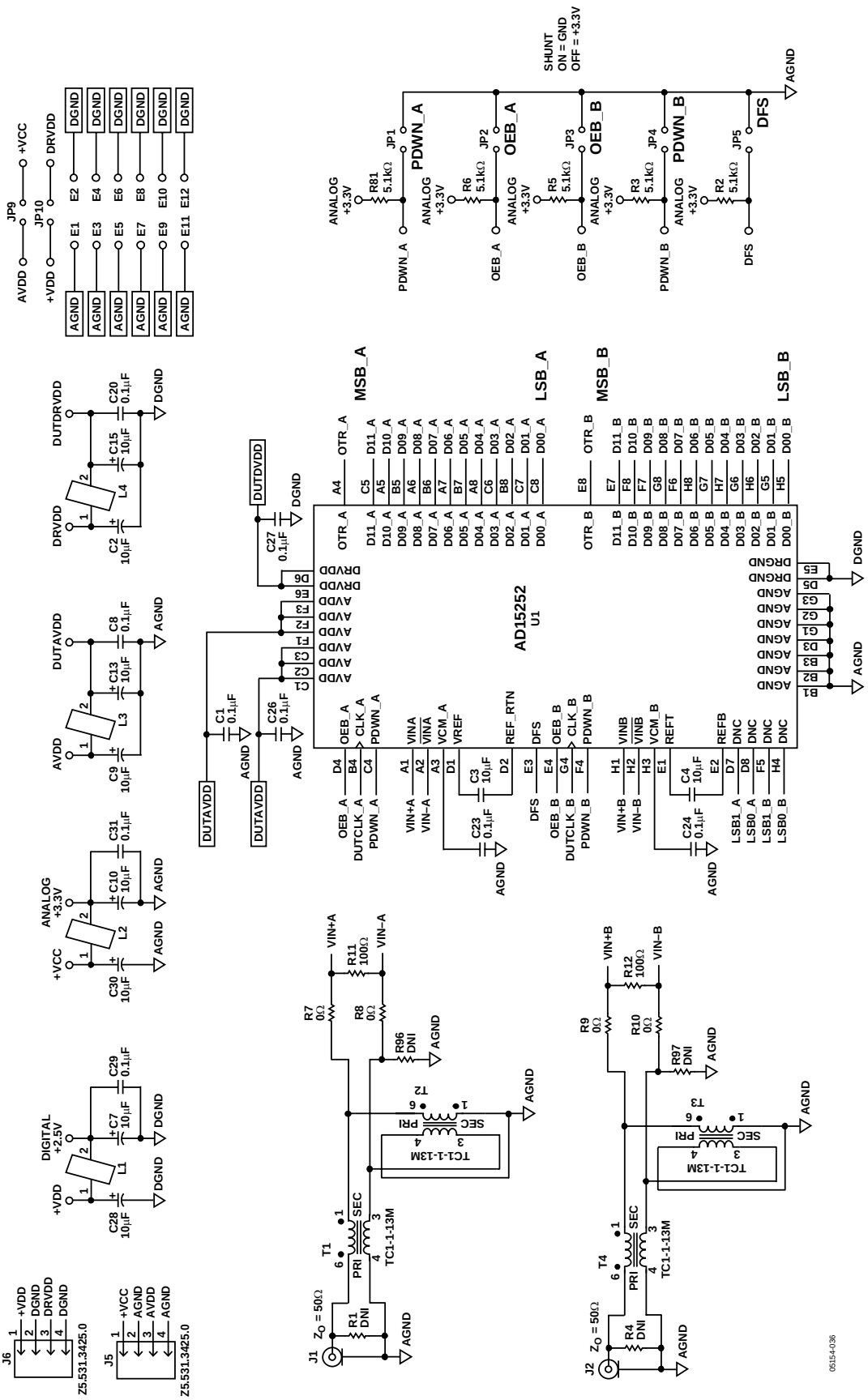

Figure 30. AD15252 Evaluation Board Schematic: Analog Front End ADC

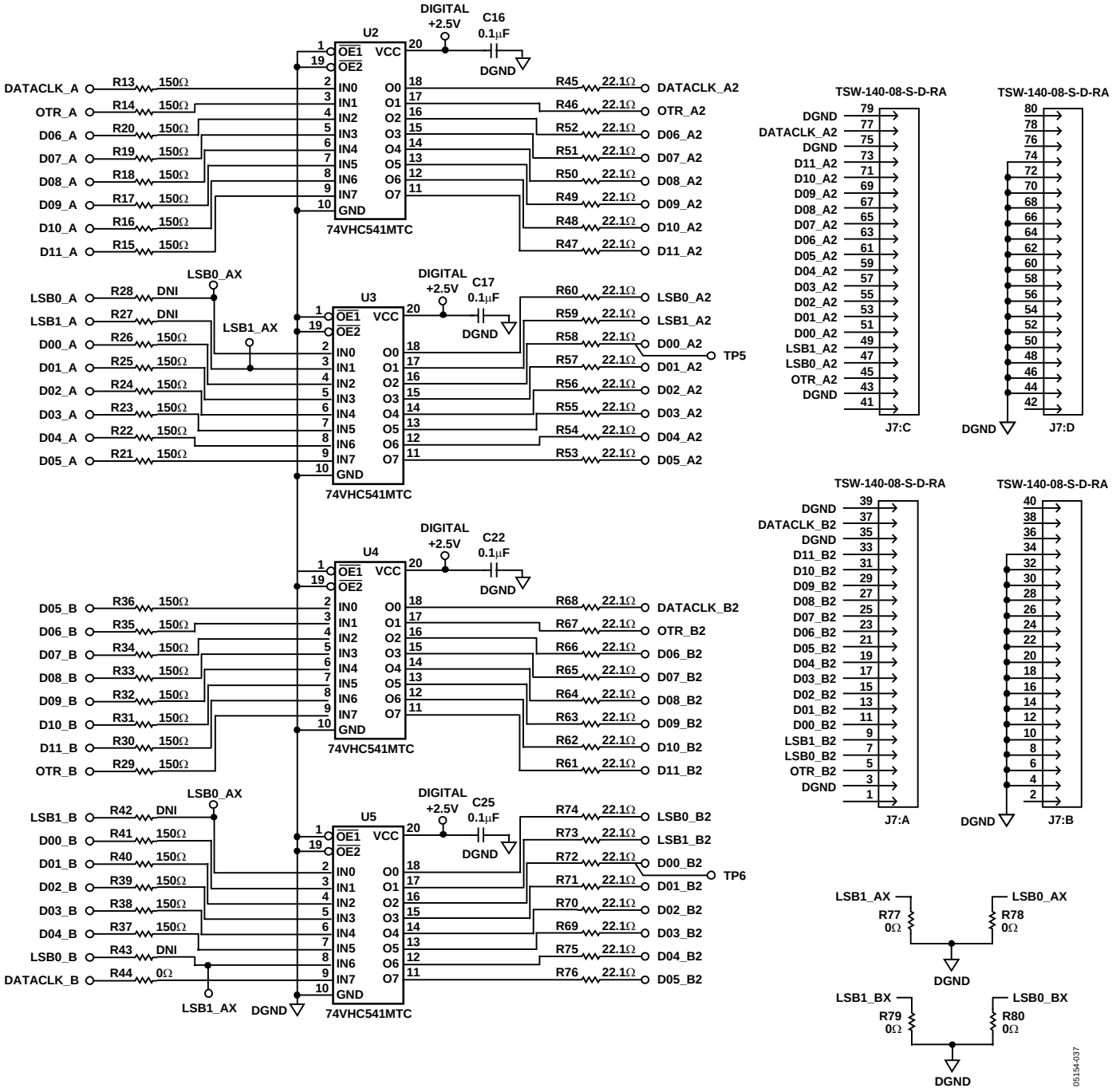

Figure 31. AD15252 Evaluation Board Schematic: Digital Outputs

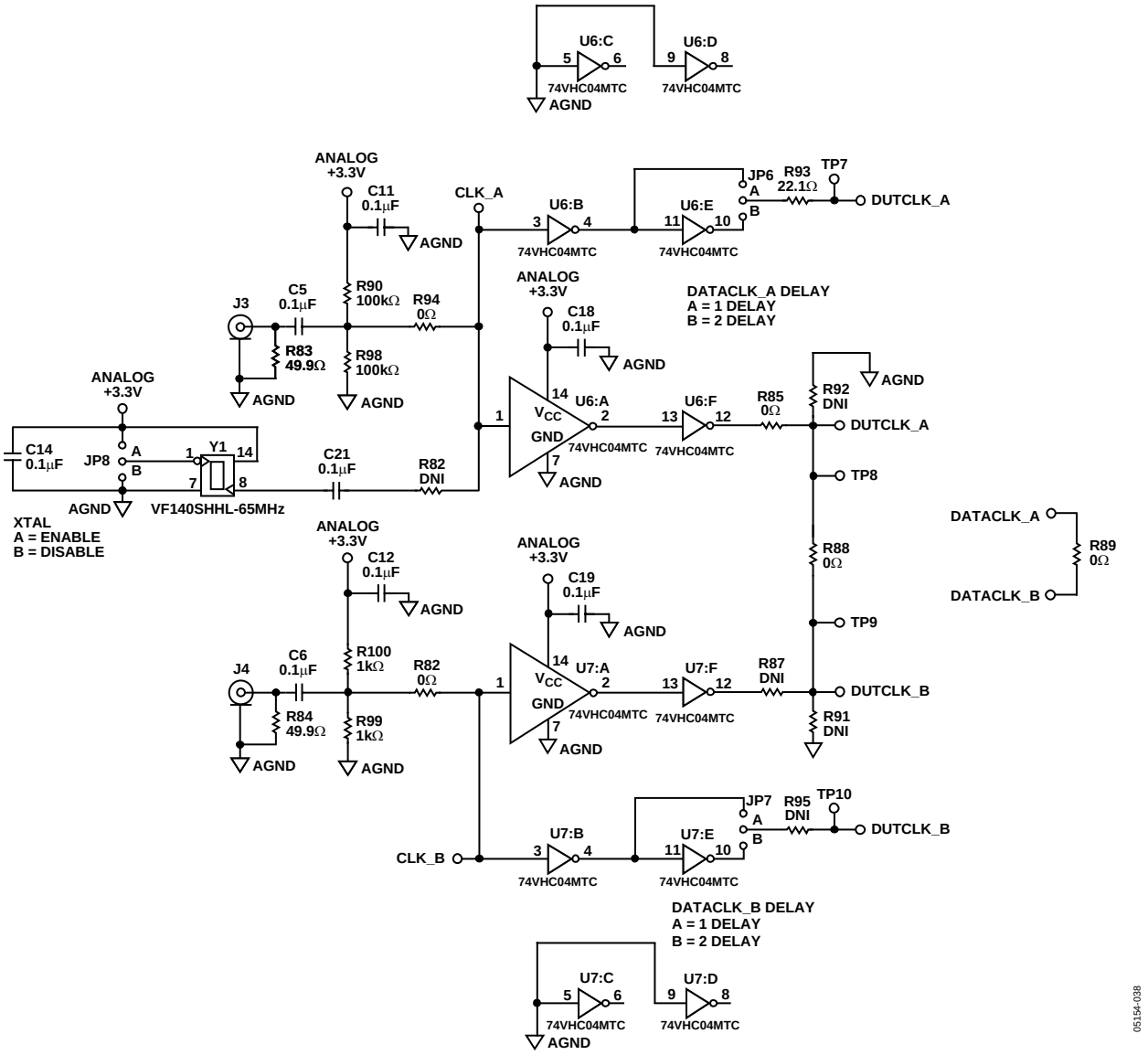

Figure 32. AD15252 Evaluation Board Schematic: Encode

OUTLINE DIMENSIONS

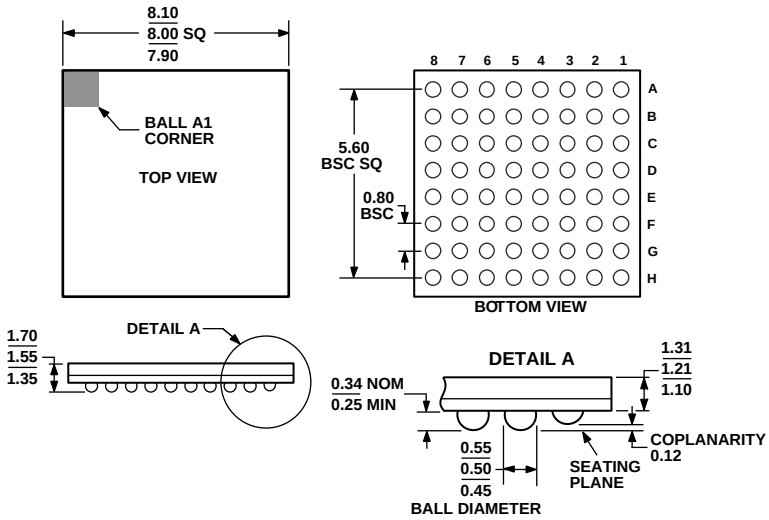

Figure 33. 64-Lead Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD15252BBC	−40°C to +85°C	64-Lead Chip Scale Package Ball Grid Array (CSP_BGA)	BC-64-1
AD15252/PCB		Evaluation Board	

NOTES

D05154–0–8/05(0)