74LVT125

3.3 V quad buffer; 3-state

Rev. 05 — 10 February 2005 Product data sheet

1. General description

The LVT125 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device combines low static and dynamic power dissipation with high speed and high output drive. The 74LVT125 device is a quad buffer that is ideal for driving bus lines. The device features four output enable inputs ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$ and $4\overline{OE}$), each controlling one of the 3-state outputs.

2. Features

- Quad bus interface
- 3-state buffers
- Output capability: +64 mA and –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - Machine model: exceeds 200 V

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay nA to nY	C_L = 50 pF; V_{CC} = 3.3 V	-	2.7	-	ns
t_{PHL}	propagation delay nA to nY	C_L = 50 pF; V_{CC} = 3.3 V	-	2.9	-	ns
C_I	input capacitance	V_I = 0 V or 3.0 V	-	4	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V	-	8	-	pF
I_{CC}	quiescent supply current	outputs disabled; V_{CC} = 3.6 V	-	0.13	-	mA

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4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT125D	–40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT125DB	–40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVT125PW	–40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVT125BQ	–40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 leads terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram

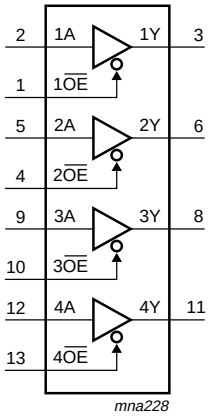

Fig 1. Logic symbol

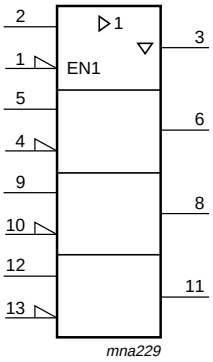

Fig 2. IEC logic symbol

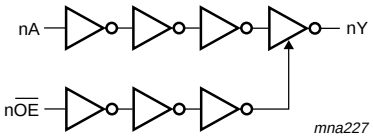

Fig 3. Logic diagram

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6. Pinning information

6.1 Pinning

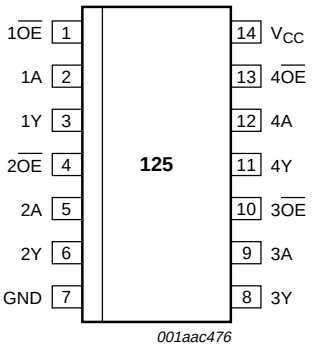
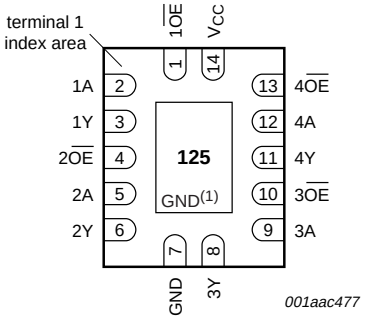


Fig 4. Pin configuration SO14, SSOP14 and TSSOP14



Transparent top view

(1) The die substrate is attached to the exposed die pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN14

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	1 output enable input (active LOW)
1A	2	1 data input
1Y	3	1 data output
$2\overline{OE}$	4	2 output enable input (active LOW)
2A	5	2 data input
2Y	6	2 data output
GND	7	ground (0 V)
3Y	8	3 data output
3A	9	3 data input
$3\overline{OE}$	10	3 output enable input (active LOW)
4Y	11	4 data output
4A	12	4 data input
$4\overline{OE}$	13	4 output enable input (active LOW)
V_{CC}	14	supply voltage

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7. Functional description

7.1 Function table

Table 4: Function table [1]

Input		Output
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
V_I	input voltage		[1]	–0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+7.0	V
I_{IK}	input diode current	$V_I < 0$ V		-	–50	mA
I_{OK}	output diode current	$V_O < 0$ V		-	–50	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-	–64	mA
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature		[2]	-	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

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9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	–32	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
V_{IK}	input diode voltage	I_{IK} = –18 mA; V_{CC} = 2.7 V		-	–0.9	–1.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –100 µA; V_{CC} = 2.7 V to 3.6 V;		V_{CC} – 0.2	V_{CC} – 0.1	-	V
		I_{OH} = –8 mA; V_{CC} = 2.7 V		2.4	2.5	-	V
		I_{OH} = –32 mA; V_{CC} = 3.0 V		2.0	2.2	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V					
		I_{OL} = 100 µA		-	0.1	0.2	V
		I_{OL} = 24 mA		-	0.3	0.5	V
		V_{CC} = 3.0 V					
		I_{OL} = 16 mA		-	0.25	0.4	V
		I_{OL} = 32 mA		-	0.3	0.5	V
		I_{OL} = 64 mA		-	0.4	0.55	V
I_{LI}	input leakage current						
	all input pins	V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		-	1	10	µA
	control pins	V_{CC} = 3.6 V; V_{CC} or GND		-	±0.1	±1	µA
	data pins	V_{CC} = 3.6 V; V_I = V_{CC}	[2]	-	0.1	1	µA
		V_{CC} = 3.6 V; V_I = 0 V	[2]	-	–1	–5	µA
I_{OFF}	power-down output current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		-	1	±100	µA
I_{HOLD}	bus hold current nA input	V_{CC} = 3 V; V_I = 0.8 V	[3]	75	150	-	µA
		V_{CC} = 3 V; V_I = 2.0 V		–75	–150	-	µA
		V_{CC} = 0 V to 3.6 V; V_I = 3.6 V		±500	-	-	µA

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Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{EX}	external current into output	output in HIGH-state when $V_O > V_{CC}$; V_O = 5.5 V and V_{CC} = 3.0 V		-	60	125	µA
I_{PU}, I_{PD}	power-up or power-down 3-state output current	$V_{CC} \leq 1.2$ V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ = don't care	[4]	-	±1	±100	µA
I_{OZ}	3-state output current	V_{CC} = 3.6 V; $V_I = V_{IH}$ or V_{IL}					
		output HIGH: V_O = 3.0 V		-	1	5	µA
		output LOW: V_O = 0.5 V		-	–1	–5	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A					
		outputs HIGH		-	0.13	0.19	mA
		outputs LOW		-	2	7	mA
		outputs disabled	[5]	-	0.13	0.19	mA
ΔI_{CC}	additional supply current per input pin	V_{CC} = 3 V to 3.6 V; one input at V_{CC} – 0.6 V and other inputs at V_{CC} or GND;	[6]	-	0.1	0.2	mA
C_I	input capacitance	V_I = 0 V or 3.0 V		-	4	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V		-	8	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
t_{PLH}	propagation delay nA to nY	V_{CC} = 2.7 V	-	-	4.5	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.7	4.0	ns
t_{PHL}	propagation delay nA to nY	V_{CC} = 2.7 V	-	-	4.9	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.9	3.9	ns
t_{PZH}	output enable time $n\overline{OE}$ to nY	V_{CC} = 2.7 V	-	-	6.0	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.4	4.7	ns
t_{PZL}	output enable time $n\overline{OE}$ to nY	V_{CC} = 2.7 V	-	-	6.5	ns
		V_{CC} = 3.3 V ± 0.3 V	1.1	3.4	4.7	ns

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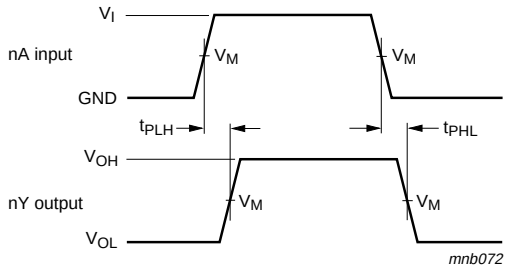
Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}	output disable time $n\overline{OE}$ to nY	V_{CC} = 2.7 V	-	-	5.7	ns
		V_{CC} = 3.3 V ± 0.3 V	1.8	3.7	5.1	ns
t_{PLZ}	output disable time $n\overline{OE}$ to nY	V_{CC} = 2.7 V	-	-	4.0	ns
		V_{CC} = 3.3 V ± 0.3 V	1.3	2.6	4.5	ns

[1] Typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

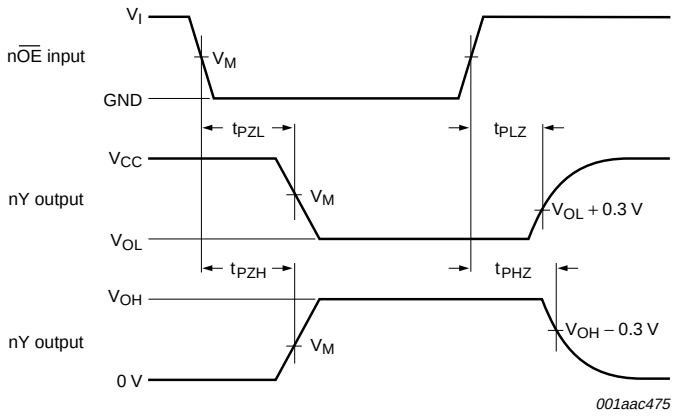
12. Waveforms



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 6. Propagation delay input (nA) to output (nY)



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 7. Enable and disable times of 3-state outputs

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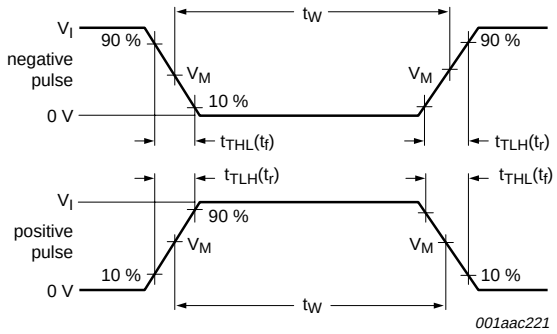
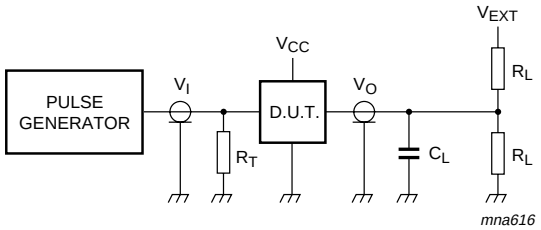


V_M = 1.5 V.

a. Input pulse definition



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

b. Test circuit

Fig 8. Load circuitry for switching times

Table 9: Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

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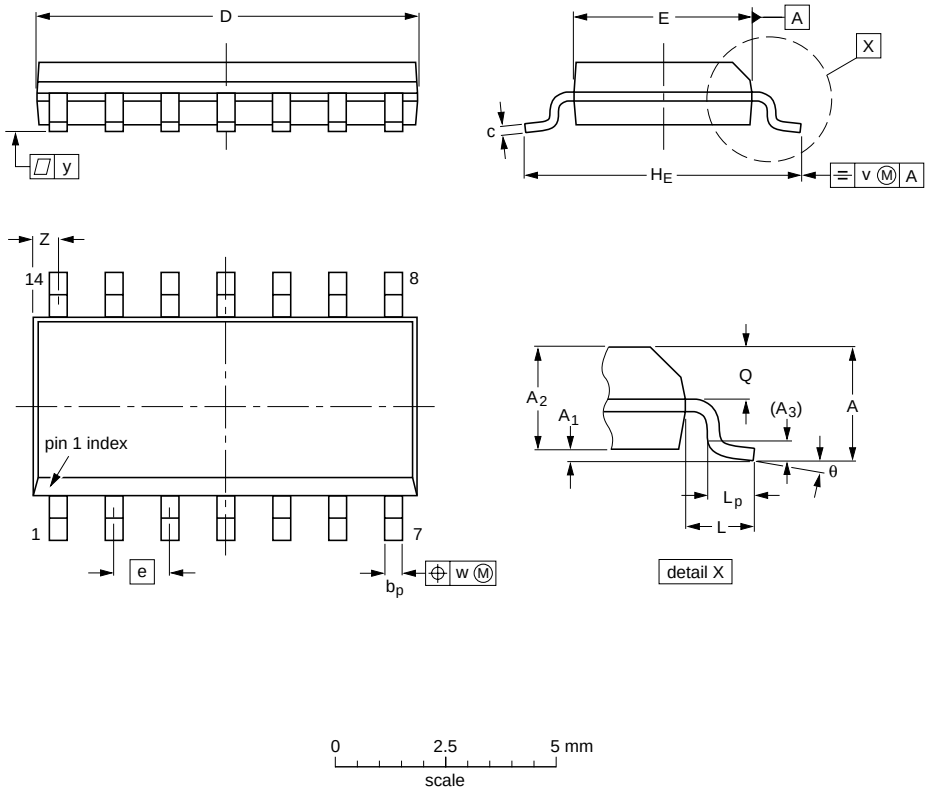
13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SO14 (SOT108-1)

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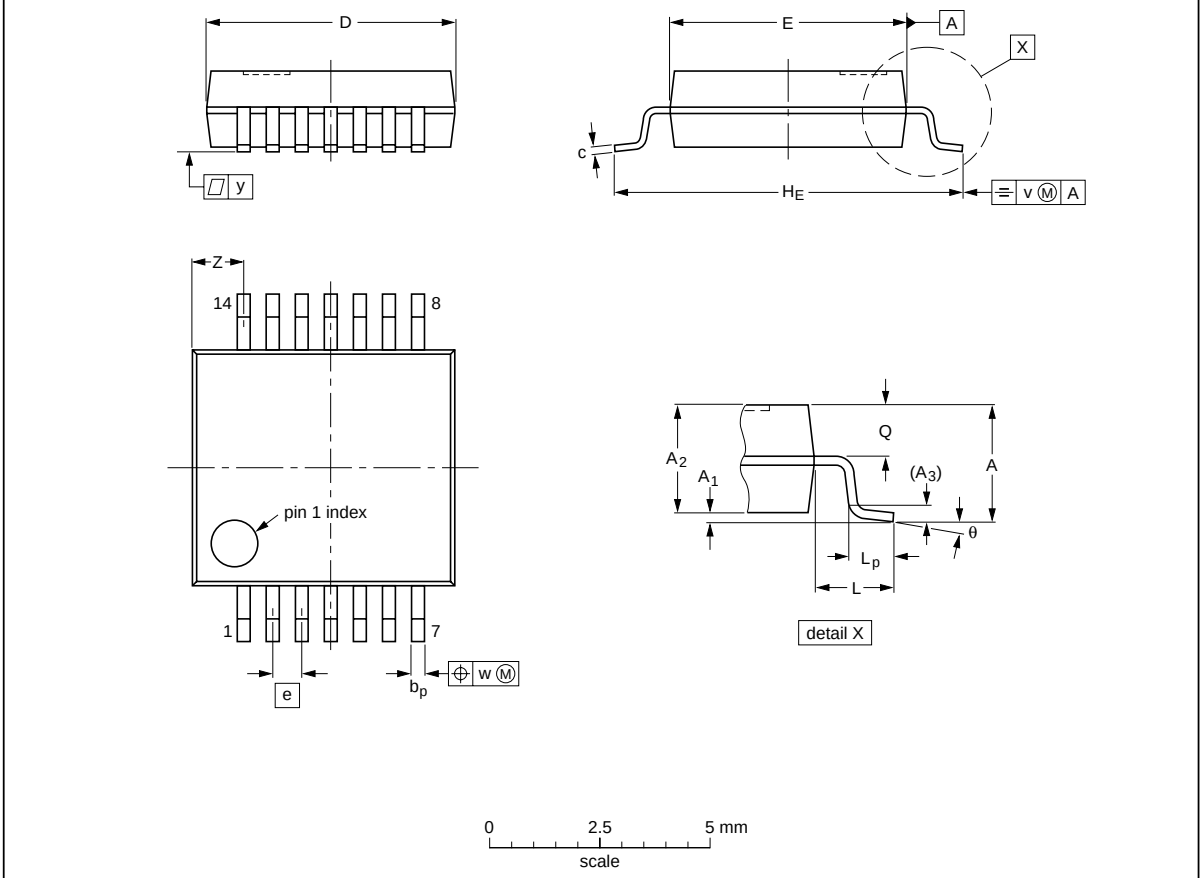
SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SSOP14 (SOT337-1)

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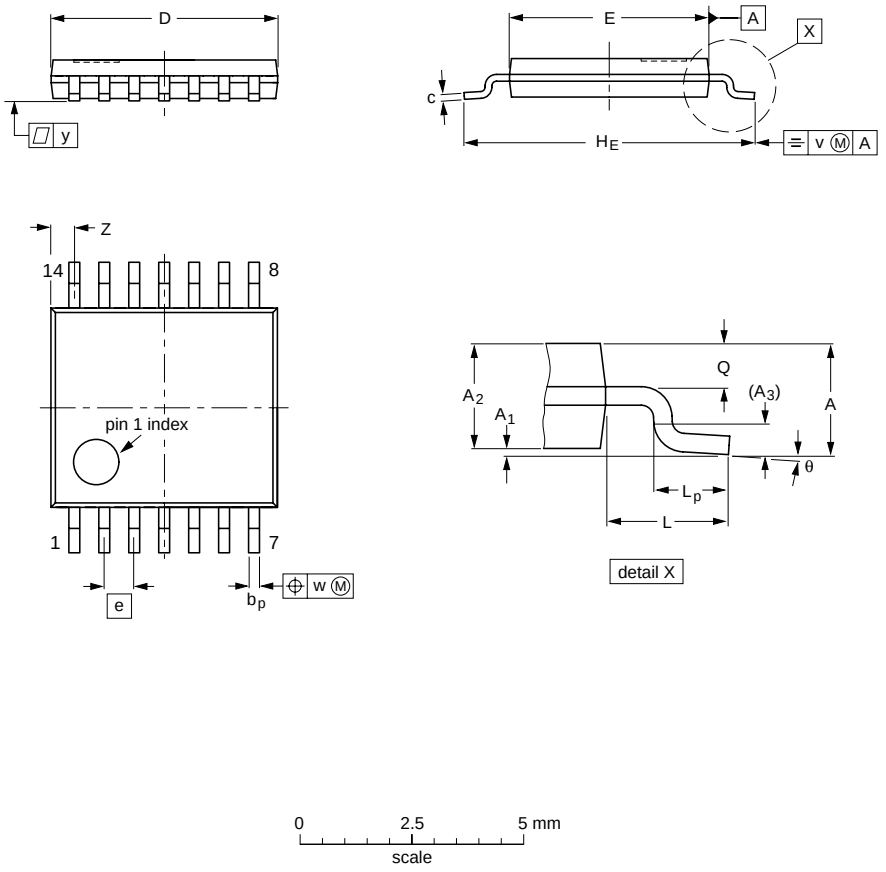
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline TSSOP14 (SOT402-1)

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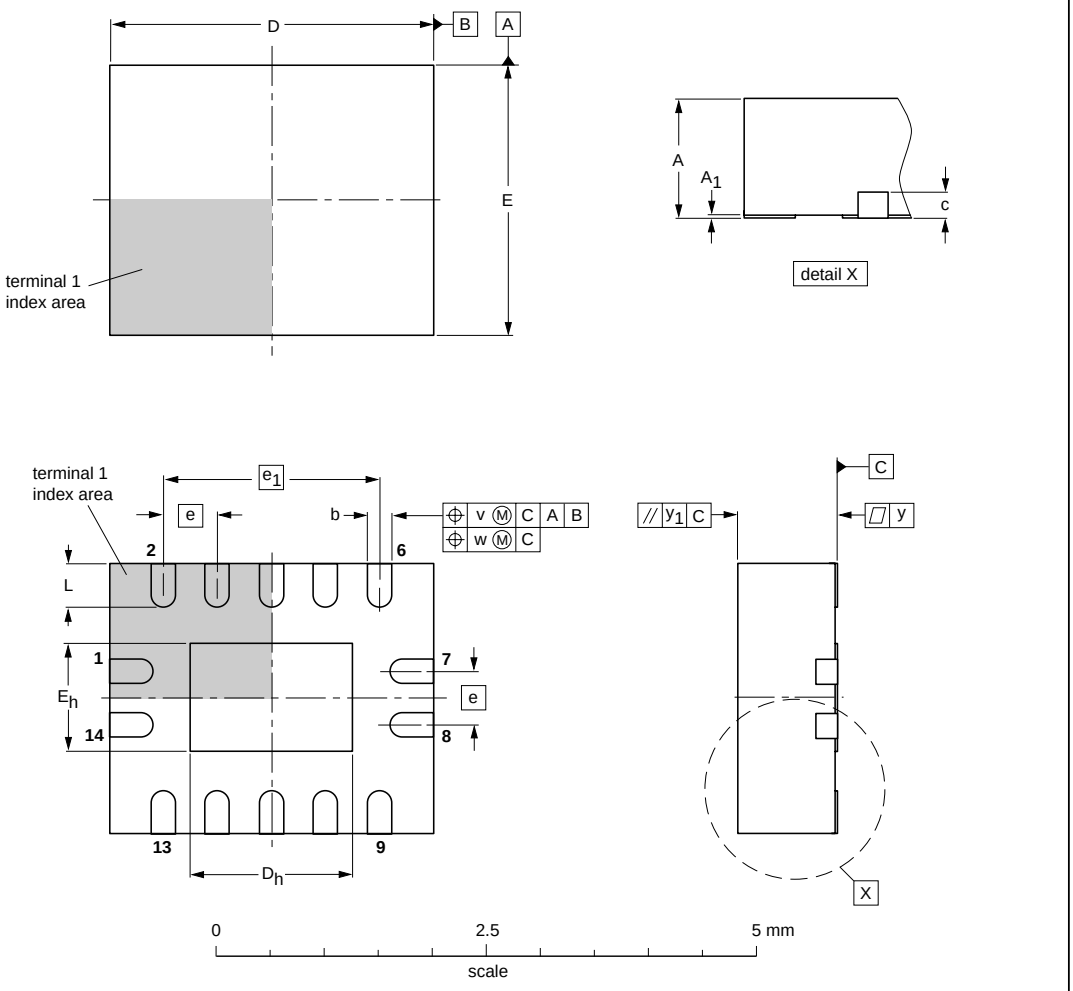
DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 12. Package outline DHVQFN14 (SOT762-1)

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14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVT125_5	20050210	Product data sheet	-	9397 750 14703	74LVT125_4
Modifications:	• Table 2: Corrected type number				
74LVT125_4	20050207	Product data sheet	-	9397 750 14552	74LVT125_3
74LVT125_3	20040624	Product data sheet	-	9397 750 13535	74LVT125_2
74LVT125_2	19980219	Product specification	-	9397 750 03514	74LVT125_1
74LVT125_1	-	-	-	-	-

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15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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18. Contact information

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Date of release: 10 February 2005
Document number: 9397 750 14703

Published in The Netherlands

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