MP3/USB 2.0 High Speed Switch with Negative Signal Handling

ISL54206A

The Intersil ISL54206A dual SPDT (Single Pole/Double Throw) switches combine low distortion audio and accurate USB 2.0 high speed data (480Mbps) signal switching in the same low voltage device. When operated with a 2.7V to 3.6V single supply, these analog switches allow audio signal swings below-ground, allowing the use of a common USB and audio headphone connector in Personal Media Players and other portable battery powered devices.

The ISL54206A logic control pins are 1.8V compatible, which allows for control via a standard µcontroller. With a V_{DD} voltage in the range of 2.7V to 3.6V, the IN pin voltage can exceed the V_{DD} rail allowing for the USB 5V V_{BUS} voltage from a computer to directly drive the IN pin to switch between the audio and USB signal sources in the portable device. The part has an audio enable control pin to open all the switches and put the part in a low power state.

The ISL54206A is available in a small 10 Ld 2.1mmx1.6mm ultra-thin µTQFN package and a 10 Ld 3mmx3mm TDFN package. It operates over a temperature range of -40°C to +85°C.

Features

- High Speed (480Mbps) and Full Speed (12Mbps) Signaling Capability per USB 2.0
- Low Distortion Negative Signal Capability
- Control Pin to Open all Switches and Enter Low Power State
- Low Distortion Headphone Audio Signals
  - THD+N at 20mW into 32Ω Load. . . . . <0.1%
- Cross-talk Audio Channels (20Hz to 20kHz) . . -110dB
- Single Supply Operation (V_{DD}) . . . . . 2.5V to 5.5V
- -3dB Bandwidth USB Switches. 630MHz
- Available in µTQFN and TDFN Packages
- Pb-Free (RoHS Compliant)
- Compliant with USB 2.0 Short Circuit Requirements Without Additional External Components

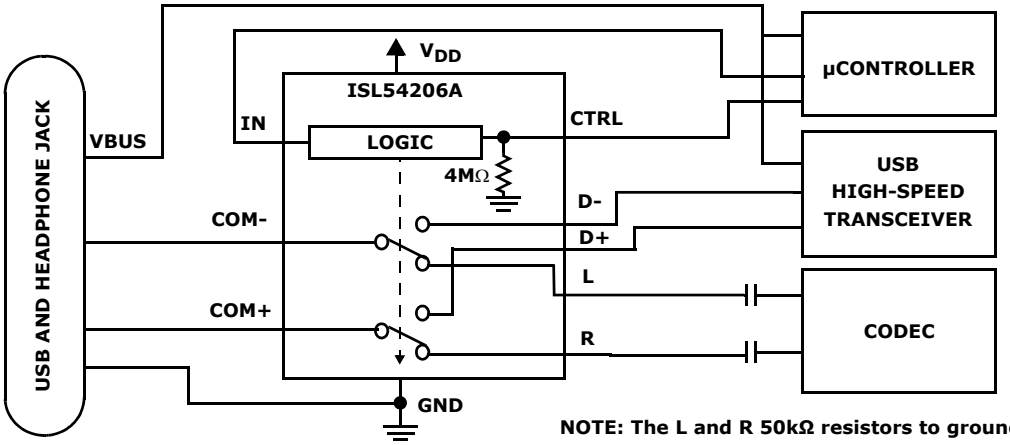
Applications* (see page 18)

- MP3 and Other Personal Media Players
- Cellular/Mobile Phones
- PDA's
- Audio/USB Switching

Related Literature* (see page 18)

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)".
- Application Note AN1337 "ISL54206AEVAL1Z Evaluation Board User's Manual".

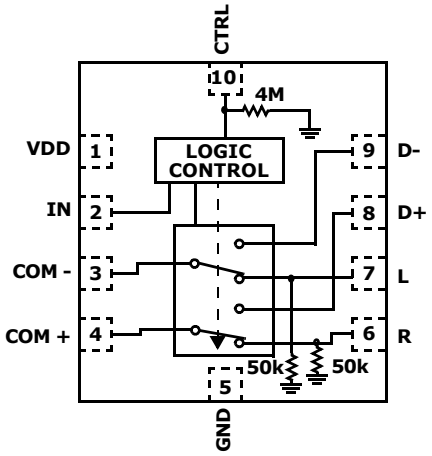
Application Block Diagram



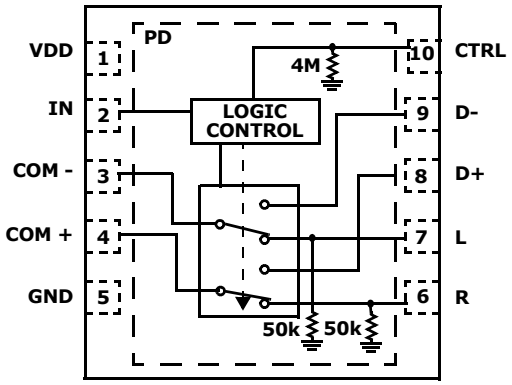
NOTE: The L and R 50kΩ resistors to ground are not shown.

Pin Configurations (Note 1)

ISL54206A
(10 LD µTQFN)
TOP VIEW



ISL54206A
(10 LD TDFN)
TOP VIEW



NOTE:

1. ISL54206A Switches shown for IN = Logic "0" and CTRL = Logic "1".

Truth Table

ISL54206A			
IN	**CTRL**	**L, R**	**D+, D-**
0	0	OFF	OFF
0	1	ON	OFF
1	X	OFF	ON

IN: Logic "0" when ≤0.5V, Logic "1" when ≥1.4V with 2.7V to 3.6V supply.
CTRL: Logic "0" when ≤0.5V or Floating, Logic "1" when ≥1.4V with 2.7V to 3.6V supply.

Pin Descriptions

ISL54206A		
PIN NO.	**NAME**	**FUNCTION**
1	VDD	Power Supply
2	IN	Digital Control Input
3	COM-	Voice and Data Common Pin
4	COM+	Voice and Data Common Pin
5	GND	Ground Connection
6	R	Audio Right Input
7	L	Audio Left Input
8	D+	USB Differential Input
9	D-	USB Differential Input
10	CTRL	Digital Control Input (Audio Enable)
-	PD	Thermal Pad. Tie to Ground or Float (TDFN package only)

Ordering Information

PART NUMBER (Note 5)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54206AIRTZ (Note 3)	06AZ	-40 to +85	10 Ld 3mmx3mm TDFN	L10.3x3A
ISL54206AIRTZ-T (Notes 2, 3)	06AZ	-40 to +85	10 Ld 3mmx3mm TDFN (Tape and Reel)	L10.3x3A
ISL54206AIRUZ-T (Notes 2, 4)	FU	-40 to +85	10 Ld 2.1mmx1.6mm µTQFN (Tape and Reel)	L10.2.1x1.6A
ISL54206AEVAL1Z	Evaluation Board			

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL54206A. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

VDD to GND . . . . . -0.3 to 6.0V
Input Voltages
D+, D-, L, R (Note 6). . . . . - 2V to ((V_{DD}) + 0.3V)
IN (Note 6). . . . . -2V to 5.5V
CTRL (Note 6). . . . . -0.3 to ((V_{DD}) + 0.3V)
Output Voltages
COM-, COM+ (Note 6) . . . . . -2V to ((V_{DD}) + 0.3V)
Continuous Current (Audio Switches) . . . . . ±150mA
Peak Current (Audio Switches)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±300mA
Continuous Current (USB Switches) . . . . . ±40mA
Peak Current (USB Switches)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating:
Human Body Model . . . . . >7kV
Machine Model . . . . . >400V
Charged Device Model . . . . . >1.4kV
Latch-up Tested per JEDEC; Class II Level A . . . . . at 85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld µTQFN (Notes 7, 8)	145	90
10 Ld TDFN (Notes 9, 10)	55	16

Maximum Junction Temperature (Plastic Package). . +150°C
Maximum Storage Temperature Range . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Signals on D+, D-, L, R, COM-, COM+, CTRL, IN exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
8. For θ_{JC}, the "case temp" location is taken at the package top center.
9. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
10. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Note 11), unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 15)	TYP	MAX (Notes 12, 15)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Audio Switches (L, R)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 3.0V, IN = 0.5V, CTRL = 1.4V	Full	**-1.5**	-	**1.5**	V
ON-Resistance, r_{ON}	V_{DD} = 5.0V, IN = 0V, CTRL = V_{DD}, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (See Figure 3)	25	-	2.47	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 4.2V, IN = 0V, CTRL = V_{DD}, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (See Figure 3)	25	-	2.50	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 2.85V, IN = 0V, CTRL = V_{DD}, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (See Figure 3)	25	-	2.87	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.0V, IN = 0.5V, CTRL = 1.4V, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (See Figure 3)	25	-	2.65	4.0	Ω
		Full	-	-	**5.5**	Ω
R_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.0V, IN = 0.5V, CTRL = 1.4V, I_{COMx} = 40mA, V_L or V_R = Voltage at max r_{ON} over signal range of -0.85V to 0.85V, (Note 14)	25	-	0.02	0.13	Ω
		Full	-	-	**0.16**	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V_{DD} = 3.0V, IN = 0.5V, CTRL = 1.4V, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (Note 13)	25	-	0.03	0.05	Ω
		Full	-	-	**0.07**	Ω

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Note 11), unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 15)	TYP	MAX (Notes 12, 15)	UNITS
Discharge Pull-Down Resistance, R_L, R_R	V_{DD} = 3.6V, IN = 0V, CTRL = 3.6V, V_{COM-} or V_{COM+} = -0.85V, 0.85V, V_L or V_R = -0.85V, 0.85V, V_{D+} and V_{D-} = floating, Measure current through the discharge pull-down resistor and calculate resistance value.	25	-	50	-	kΩ
USB Switches (D+, D-)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 3.6V, IN = 1.4V, CTRL = 1.4V	Full	**0**	-	**V_{DD}**	V
ON-Resistance, r_{ON}	V_{DD} = 5.0V, IN = V_{DD}, CTRL = V_{DD}, I_{COMx} = 1mA, V_{D+} or V_{D-} = 5V (See Figure 4)	+25	-	17.7	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 4.2V, IN = V_{DD}, CTRL = V_{DD}, I_{COMx} = 1mA, V_{D+} or V_{D-} = 4.2V (See Figure 4)	+25	-	19.5	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 2.85V, IN = V_{DD}, CTRL = V_{DD}, I_{COMx} = 1mA, V_{D+} or V_{D-} = 2.85V (See Figure 4)	+25	-	26	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.3V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 1mA, V_{D+} or V_{D-} = 3.3V (See Figure 4)	+25	-	23.5	30	Ω
		Full	-	-	**35**	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.6V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 40mA, V_{D+} or V_{D-} = 0V to 400mV (See Figure 4)	25	-	4.6	5	Ω
		Full	-	-	**6.5**	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.6V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 40mA, V_{D+} or V_{D-} = Voltage at max R_{ON} over signal range of 0V to 400mV, (Note 14)	25	-	0.06	0.5	Ω
		Full	-	-	**0.55**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V_{DD} = 3.6V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 40mA, V_{D+} or V_{D-} = 0V to 400mV, (Note 13)	25	-	0.4	0.6	Ω
		Full	-	-	**1.0**	Ω
OFF Leakage Current, $I_{D+(OFF)}$ or $I_{D-(OFF)}$	V_{DD} = 3.6V, IN = 0V, CTRL = 3.6V, V_{COM-} or V_{COM+} = 0.5V, 0V, V_{D+} or V_{D-} = 0V, 0.5V, V_L and V_R = float	25	-10	-	10	nA
		Full	**-70**	-	**70**	nA
ON Leakage Current, I_{Dx}	V_{DD} = 3.3V, IN = 3.3V, CTRL = 0V or 3.3V, V_{D+} or V_{D-} = 2.0V, V_{COM-},V_{COM+}, V_L and V_R = float	25	-30	8	30	nA
		Full	**-300**	-	**300**	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF, (See Figure 1)	25	-	67	-	ns
Turn-OFF Time, t_{OFF}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF, (See Figure 1)	25	-	48	-	ns
Break-Before-Make Time Delay, t_D	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF, (See Figure 2)	25	-	18	-	ns
Skew, t_{SKEW}	V_{DD} = 3.3V, IN = 3.3V, CTRL = 0V or 3.3V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 750ps at 480Mbps, (Duty Cycle = 50%) (See Figure 7)	25	-	50	-	ps
Total Jitter, t_J	V_{DD} = 3.3V, IN = 3.3V, CTRL = 0V or 3.3V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 750ps at 480Mbps	25	-	210	-	ps
Propagation Delay, t_{PD}	V_{DD} = 3.3V, IN = 3.3V, CTRL = 0V or 3.3V, R_L = 45Ω, C_L = 10pF, (See Figure 7)	25	-	250	-	ps
Crosstalk (Channel-to-Channel), R to COM-, L to COM+	V_{DD} = 3.3V, IN = 0V, CTRL = 3.3V, R_L = 32Ω, f = 20Hz to 20kHz, V_R or V_L = 0.707V_{RMS} ($2V_{P-P}$), (See Figure 6)	25	-	-110	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{DD} = 3.0V, IN = 0V, CTRL = 3V, V_L or V_R = 0.707V_{RMS} ($2V_{P-P}$), R_L = 32Ω	25	-	0.06	-	%
USB Switch -3dB Bandwidth	Signal = 0dBm, 0.2V_{DC} offset, R_L = 50Ω, C_L = 5pF	25	-	630	-	MHz
D+/D- OFF Capacitance, $C_{D+(OFF)}$, $C_{D-(OFF)}$	f = 1MHz, V_{DD} = 3.3V, IN = 0V, CTRL = 3.3V, V_{D-} or V_{D+} = V_{COMx} = 0V, (See Figure 5)	25	-	6	-	pF

Electrical Specifications - 2.7V to 3.6V Supply

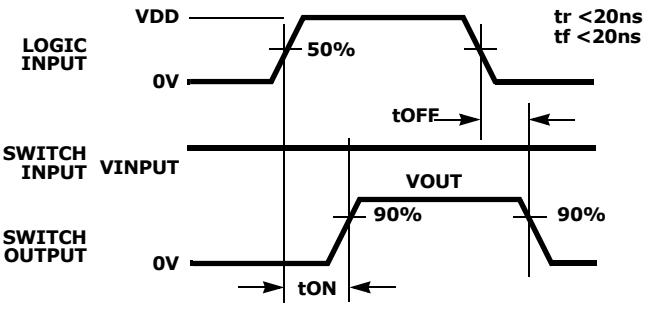
Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Note 11), unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 15)	TYP	MAX (Notes 12, 15)	UNITS
L/R OFF Capacitance, C_{LOFF}, C_{ROFF}	f = 1MHz, V_{DD} = 3.3V, IN = 0V, CTRL = 0V or 3.3V, V_L or V_R = V_{COMx} = 0V, (See Figure 5)	25	-	9	-	pF
COM ON Capacitance, $C_{COM-(ON)}$, $C_{COM+(ON)}$	f = 1MHz, V_{DD} = 3.3V, IN = 3.0V, CTRL = 0V or 3.3V, V_{D-} or V_{D+} = V_{COMx} = 0V, (See Figure 5)	25	-	10	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	**2.5**	-	**5.5**	V
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, IN = 0V or 3.6V, CTRL = 3.6V	25	-	6	8	µA
		Full	-	-	**10**	µA
Positive Supply Current, I_{DD}	V_{DD} = 4.2V, IN = 0V or 4.2V, CTRL = 4.2V	25	-	6	-	µA
Positive Supply Current, I_{DD}	V_{DD} = 5.0V, IN = 0V or 5.0V, CTRL = 5.0V	25	-	8	-	µA
Positive Supply Current, I_{DD} (Low Power State)	V_{DD} = 3.6V, IN = 0V, CTRL = 0V or float	25	-	4	25	nA
		Full	-	150	-	nA
DIGITAL INPUT CHARACTERISTICS						
Voltage Low, V_{INL}, V_{CTRLL}	V_{DD} = 2.7V to 3.6V	Full	-	-	**0.5**	V
Voltage High, V_{INH}, V_{CTRLH}	V_{DD} = 2.7V to 3.6V	Full	**1.4**	-	-	V
Input Current, I_{INL}, I_{CTRLL}	V_{DD} = 3.6V, IN = 0V, CTRL = 0V	Full	**-50**	20	**50**	nA
Input Current, I_{INH}	V_{DD} = 3.6V, IN = 3.6V, CTRL = 0V	Full	**-50**	20	**50**	nA
Input Current, I_{CTRLH}	V_{DD} = 3.6V, IN = 0V, CTRL = 3.6V	Full	**-2**	1.1	**2**	µA
CTRL Pull-Down Resistor, R_{CTRL}	V_{DD} = 3.6V, IN = 0V, CTRL = 3.6V	Full	-	4	-	MΩ

NOTES:

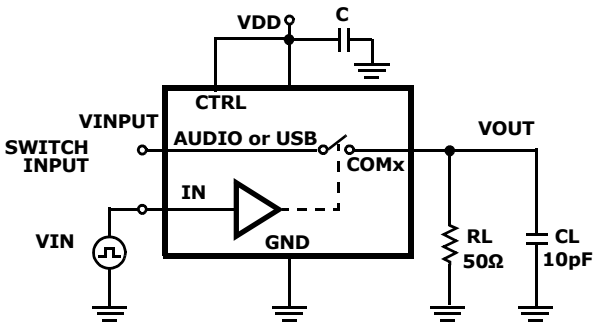
11. V_{LOGIC} = Input voltage to perform proper function.
12. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
13. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
14. R_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max R_{ON} value, between L and R or between D+ and D-.
15. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

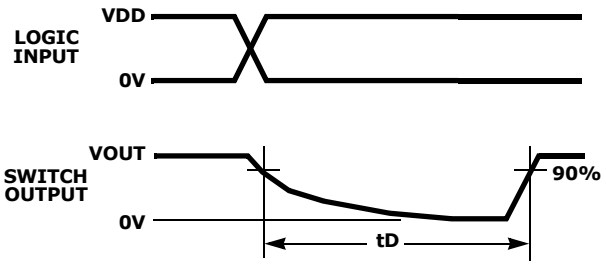
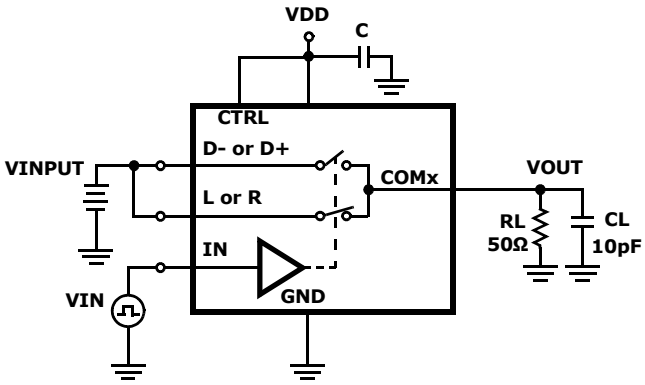


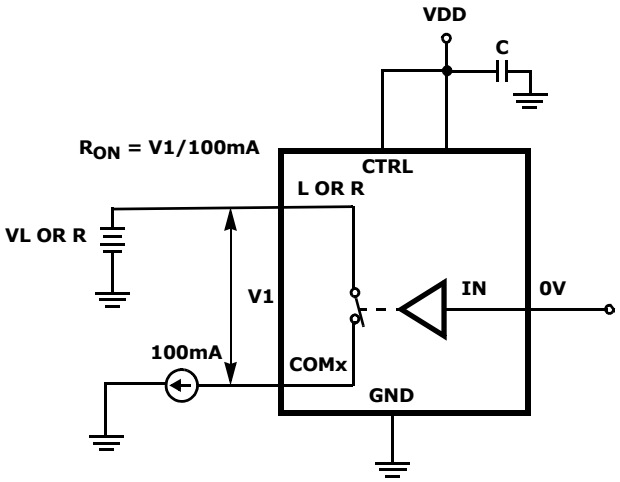
FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

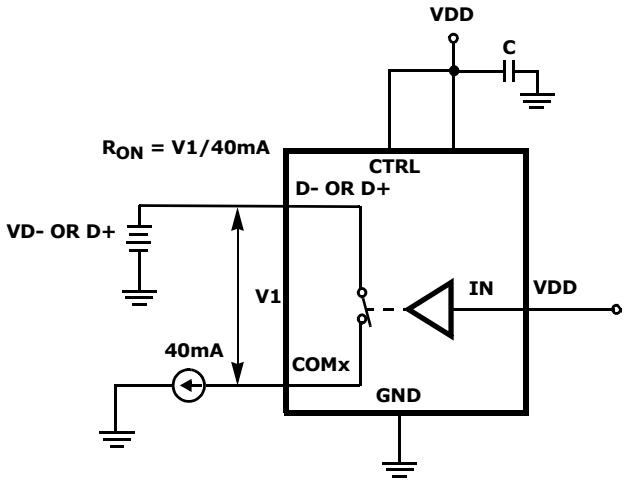
FIGURE 2B. TEST CIRCUIT

FIGURE 2. BREAK-BEFORE-MAKE TIME



Repeat test for all switches.

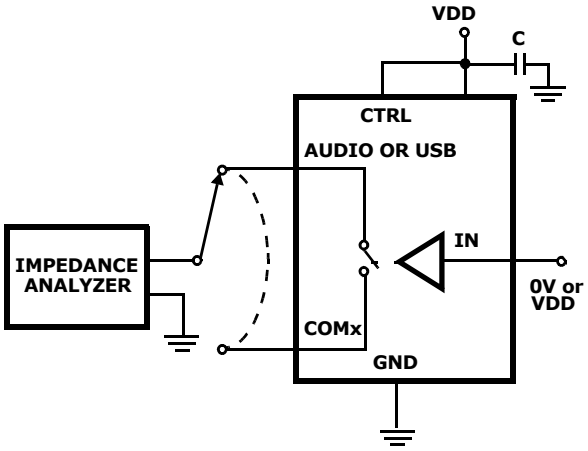
FIGURE 3. AUDIO R_{ON} TEST CIRCUIT



Repeat test for all switches.

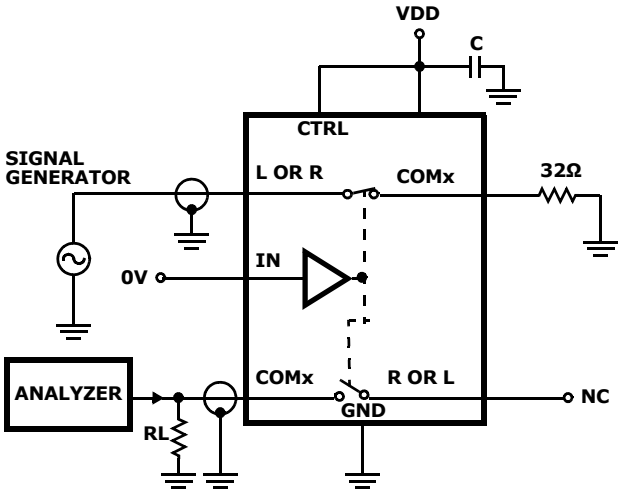
FIGURE 4. USB R_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Repeat test for all switches.

FIGURE 5. CAPACITANCE TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 6. AUDIO CROSSTALK TEST CIRCUIT

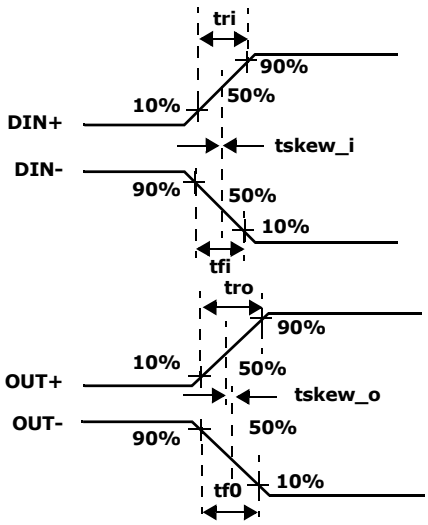
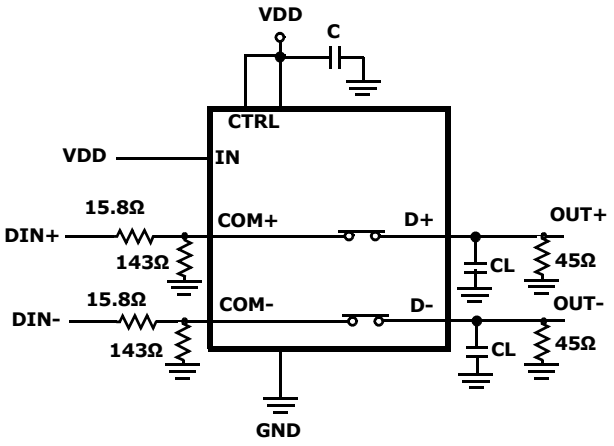


FIGURE 7A. MEASUREMENT POINTS

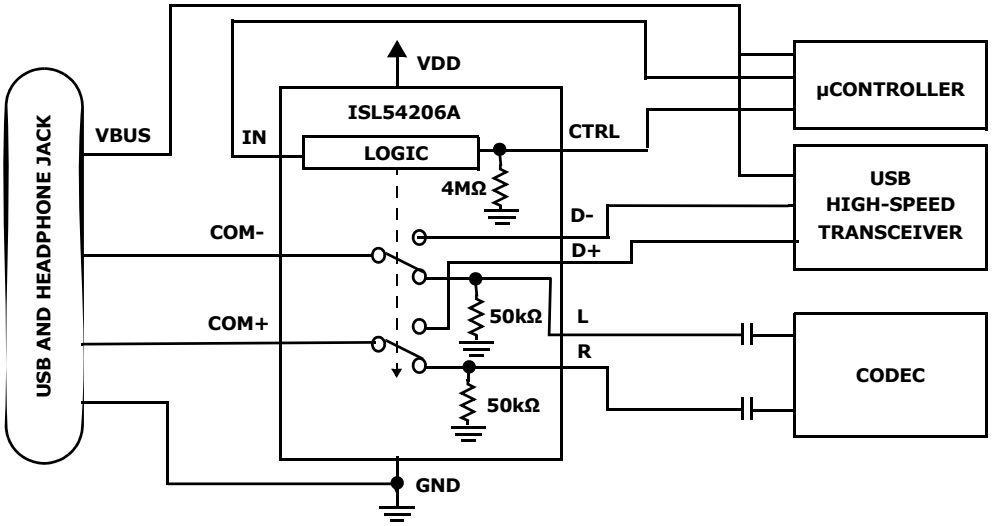


|tro - tri| Delay Due to Switch for Rising Input and Rising Outpu
|tfo - tfi| Delay Due to Switch for Falling Input and Falling Outp
|tskew_0| Change in Skew through the Switch for Output Signa
|tskew_i| Change in Skew through the Switch for Input Signals

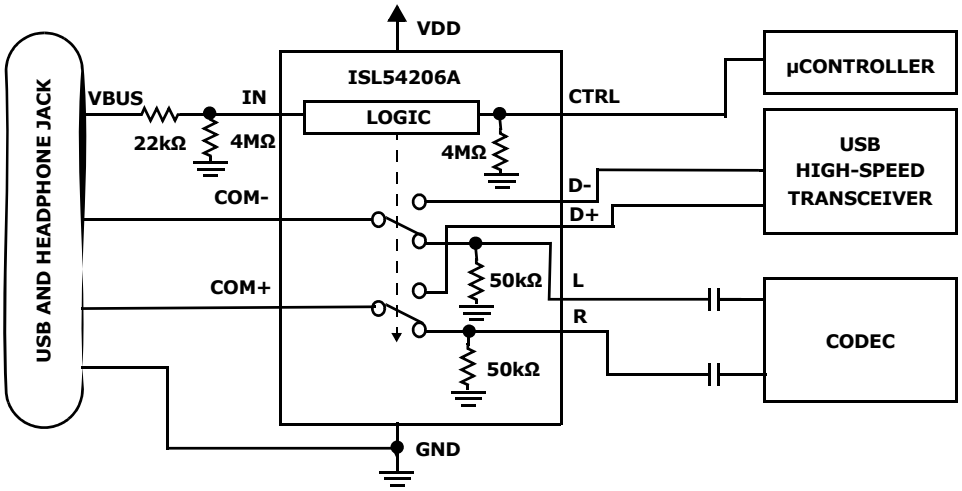
FIGURE 7B. TEST CIRCUIT

FIGURE 7. SKEW TEST

Application Block Diagrams



LOGIC CONTROL VIA MICRO-PROCESSOR



LOGIC CONTROL VIA VBUS VOLTAGE FROM COMPUTER OR USB HUB

Detailed Description

The ISL54206A device is a dual single pole/double throw (SPDT) analog switch device that can operate from a single DC power supply in the range of 2.5V to 5.5V. It was designed to function as a dual 2 to 1 multiplexer to select between USB differential data signals and audio L and R stereo signals. It comes in tiny µTQFN and TDFN packages for use in MP3 players, PDAs, cell phones, and other personal media players.

The part consists of two 3Ω audio switches and two 5Ω USB switches. The audio switches can accept signals that swing below ground. They were designed to pass audio left and right stereo signals, that are ground referenced, with minimal distortion. The USB switches were designed to pass high-speed USB differential data signals with minimal edge and phase distortion.

The ISL54206A was specifically designed for MP3 players, cell phones and other personal media player applications that need to combine the audio headphone jack and the USB data connector into a single shared connector, thereby saving space and component cost. Typical application block diagrams of this functionality is shown above.

The ISL54206A has a single logic control pin (IN) that selects between the audio switches and the USB switches. This pin can be driven Low or High to switch between the audio CODEC drivers and USB transceiver of the MP3 player or cellphone. The ISL54206A also contains a logic control pin (CTRL) that when driven Low while IN is Low, opens all switches and puts the part into a low power state, drawing typically 1nA of I_{DD} current.

A detailed description of the two types of switches is provided in the following sections. The USB transmission and audio playback are intended to be mutually exclusive operations.

Audio Switches

The two audio switches (L, R) are 3Ω switches that can pass signals that swing below ground by as much as 1.5V. They were designed to pass ground reference stereo signals with minimal insertion loss and very low distortion. Crosstalk between the audio switches over the audio band is < -110dB.

Over a signal range of ±1V (0.707V_{RMS}) with V_{DD} >2.7V, these switches have an extremely low R_{ON} resistance variation. They can pass ground referenced audio signals with very low distortion (<0.06% THD+N) when delivering 15.6mW into a 32Ω headphone speaker load. See Figures 8, Figures 9, Figures 10, and Figures 11 THD+N performance curves.

These switches are uni-directional switches. The audio drivers should be connected at the L and R side of the switch (pin 7 and pin 8) and the speaker loads should be connected at the COM side of the switch (pin 3 and pin 4).

The audio switches are active (turned ON) whenever the IN voltage is ≤0.5V and the CTRL voltage to ≥1.4V.

Note: Whenever the audio switches are ON, the USB transceivers need to be in the high impedance state or static high or low state.

USB Switches

The two USB switches (D+, D-) are bidirectional switches that can pass rail-to-rail signals. When powered with a 3.6V supply, these switches have a nominal r_{ON} of 4.6Ω over the signal range of 0V to 400mV with a r_{ON} flatness of 0.4Ω. The r_{ON} matching between the D+ and D- switches over this signal range is only 0.06Ω ensuring minimal impact by the switches to USB high speed signal transitions. As the signal level increases, the r_{ON} resistance increases. At signal level of 3.3V the switch resistance is nominally 23Ω.

The USB switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals typically in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high speed signal quality specifications. See high-speed eye diagram Figure 15.

The USB switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling. See the full-speed eye diagrams, Figures 12 thru 14.

The maximum signal range for the USB switches is from -1.5V to V_{DD}. The signal voltage at D- and D+ should not be allowed to exceed the V_{DD} voltage rail or go below ground by more than -1.5V.

The USB switches are active (turned ON) whenever the IN voltage is ≥1.4V.

Note: Whenever the USB switches are ON, the audio drivers of the CODEC need to be at AC or DC ground or floating to keep from interfering with the data transmission.

USB Switch Cell Off-Isolation

Due to the unique internal architecture of the ISL54206A part, the USB switch cell has limited off-isolation to a negative signal at the COM side of the part.

When driving an audio signal into the L and R inputs a small negative voltage will appear at the D- and D+ lines as the audio signal transitions below ground. With a USB transceiver connected at the D-/D+ pins and with a 32Ω headphone connected at the COM pins Table 1 shows the negative voltage generated at the D-/D+ lines as you increase the audio amplitude across the headphone load.

TABLE 1.

AUDIO SIGNAL AMPLITUDE	D-/D+ VOLTAGE (V)	
	+25°C	+85°C
800mV_{P-P}	-0.22	-0.27
880mV_{P-P}	-0.24	-0.3
1.08V_{P-P}	-0.3	-0.34
2V_{P-P}	-0.41	-0.44
2.25V_{P-P}	-0.47	-0.5
4V_{P-P}	-0.83	-0.85

The USB specification (USB Specification Rev 2.0, Chapter 7, Section 7.1.1) states that a USB transceiver must be able to tolerate a -1V signal at its D-/D+ differential inputs. The data in the table shows that the -1V level is never exceeded during audio operation and should have no impact on the long-term reliability of the USB transceiver.

ISL54206A Operation

The following discussion discusses using the ISL54206A in the typical application shown in the block diagrams on page 9.

V_{DD} SUPPLY

The DC power supply connected at VDD (pin 1) provides the required bias voltage for proper switch operation. The part can operate with a supply voltage in the range of 2.5V to 5.5V.

In a typical USB/Audio application for portable battery powered devices, the V_{DD} voltage will come from a battery or an LDO and be in the range of 2.7V to 3.6V. For best possible USB full-speed operation (12Mbps), it is recommended that the V_{DD} voltage be ≥2.5V in order to get a USB data signal level above 2.5V.

LOGIC CONTROL

The state of the ISL54206A device is determined by the voltage at the IN pin (pin 2) and the CTRL pin (pin 10). Refer to "Truth Table" on page 2. These logic pins are 1.8V logic compatible when V_{DD} is in the range of 2.7V to 3.6V and can be controlled by a standard µprocessor.

The CTRL pin is internally pulled low through a 4MΩ resistor to ground and can be left floating or tri-stated by

the µprocessor. The CTRL control pin is only active when IN is logic "0".

The IN pin does not have an internal pull-down resistor and must not be allowed to float. It must be driven High or Low.

The voltage at the IN pin can exceed the V_{DD} voltage by as much as 2.55V. This allows the V_{BUS} voltage from a computer or USB hub (4.4V to 5.25V) to drive the IN pin while the V_{DD} voltage is in the range of 2.7V to 3.6V. An external pull-down resistor is required from the IN pin to ground when directly driving the IN pin with the computer VBUS voltage. See "USING THE COMPUTER VBUS VOLTAGE TO DRIVE THE "IN" PIN" on page 11.

Logic Control Voltage Levels

IN = Logic "0" (Low) when IN $\leq$0.5V
IN = Logic "1" (High) when IN $\geq$1.4V
CTRL = Logic "0" (Low) when $\leq$0.5V or floating.
CTRL = Logic "1" (High) when $\geq$1.4V

Audio Mode

If the IN pin = Logic "0" and CTRL pin = Logic "1," the part will be in the Audio mode. In Audio mode, the L (left) and R (right) 3Ω audio switches are ON and the D- and D+ 5Ω USB switches are OFF (high impedance).

When nothing is plugged into the common connector or a headphone is plugged into the common connector, the µprocessor will sense that there is no voltage at the VBUS pin of the connector and will drive and hold the IN control pin of the ISL54206A low. As long as the CTRL = Logic "1," the ISL54206A part will be in the audio mode and the audio drivers of the media player can drive the headphones and play music.

USB Mode

If the IN pin = Logic "1" and CTRL pin = Logic "0" or Logic "1" the part will go into USB mode. In USB mode, the D- and D+ 5Ω switches are ON and the L and R 3Ω audio switches are OFF (high impedance).

When a USB cable from a computer or USB hub is connected at the common connector, the µprocessor will sense the presence of the 5V VBUS and drive the IN pin voltage high. The ISL54206A part will go into the USB mode. In USB mode, the computer or USB hub transceiver and the MP3 player or cell phone USB transceiver are connected and digital data will be able to be transmitted back and forth.

When the USB cable is disconnected, the µprocessor will sense that the 5V VBUS voltage is no longer connected and will drive the IN pin low and put the part back into the Audio or Low Power Mode.

Low Power Mode

If the IN pin = Logic "0" and CTRL pin = Logic "0," the part will be in the Low Power mode. In the Low Power mode, the audio switches and the USB switches are OFF (high impedance). In this state, the device draws typically 1nA of current.

USING THE COMPUTER V_{BUS} VOLTAGE TO DRIVE THE "IN" PIN

External IN Pull-Down Resistor

Rather than using a microprocessor to control the IN logic pin you can directly drive the IN pin using the V_{BUS} voltage from the computer or USB hub. In order to do this, you must connect an external resistor from the IN pin to ground.

When a headphone or nothing is connected at the common connector, the external pull-down will pull the IN pin low putting the ISL54206A in the Audio mode or Low Power mode depending on the condition of the CTRL pin.

When a USB cable is connected at the common connector, the voltage at the IN pin will be driven to 5V and the part will automatically go into the USB mode.

When the USB cable is disconnected from the common connector, the voltage at the IN pin will be pulled low by the pull-down resistor and return to the Audio Mode or Low Power Mode depending on the condition of the CTRL pin.

Note: The voltage at the IN pin can exceed the V_{DD} voltage by as much as 2.55V. This allows the V_{BUS} voltage from a computer or USB hub (4.4V to 5.25V) to drive the IN pin while the V_{DD} voltage is in the range of 2.7V to 3.6V.

External IN Series Resistor

The ISL54206A contains a clamp circuit between IN and VDD. Whenever the IN voltage is greater than the V_{DD} voltage by more than 2.55V, current will flow through this clamp circuitry into the V_{DD} power supply bus.

During normal USB operation, V_{DD} is in the range of 2.7V to 3.6V and IN (V_{BUS} voltage from computer or USB hub) is in the range of 4.4V to 5.25V, the clamp circuit is not active and no current will flow through the clamp into the V_{DD} supply.

In a USB application, the situation can exist where the V_{BUS} voltage from the computer could be applied at the IN pin before the V_{DD} voltage is up to its normal operating voltage range and current will flow through the clamp into the V_{DD} power supply bus. This current could be quite high when V_{DD} is OFF or at 0V and could potentially damage other components connected in the circuit. In the application circuit, a 22kΩ resistor has been put in series with the IN pin to limit the current to a safe level during this situation.

It is recommended that a current limiting resistor in the range of 10kΩ to 50kΩ be connected in series with the IN pin. It will have minimal impact on the logic level at the IN pin during normal USB operation and protect the circuit during the time V_{BUS} is present before V_{DD} is up to its normal operating voltage.

Note: No external resistor is required in applications where the voltage at the IN pin will not exceed V_{DD} by more than 2.55V.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

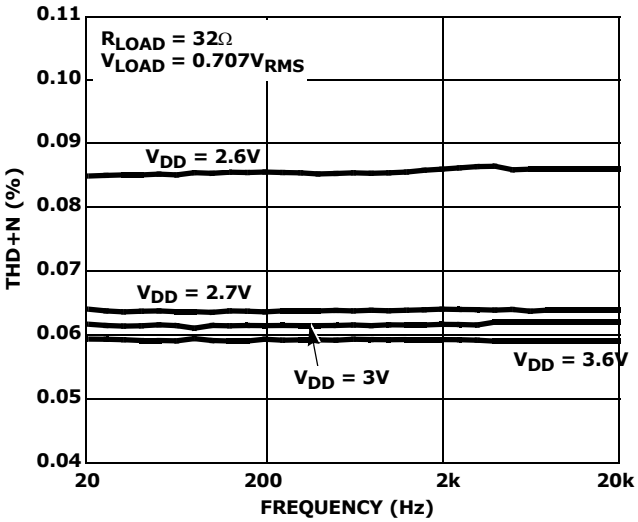


FIGURE 8. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

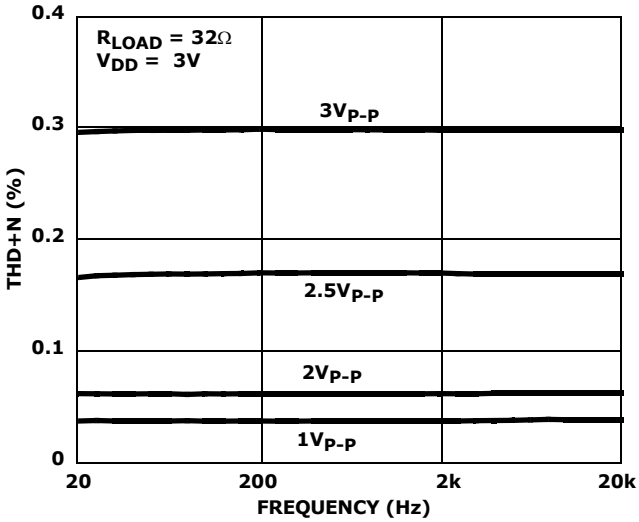


FIGURE 9. THD+N vs SIGNAL LEVELS vs FREQUENCY

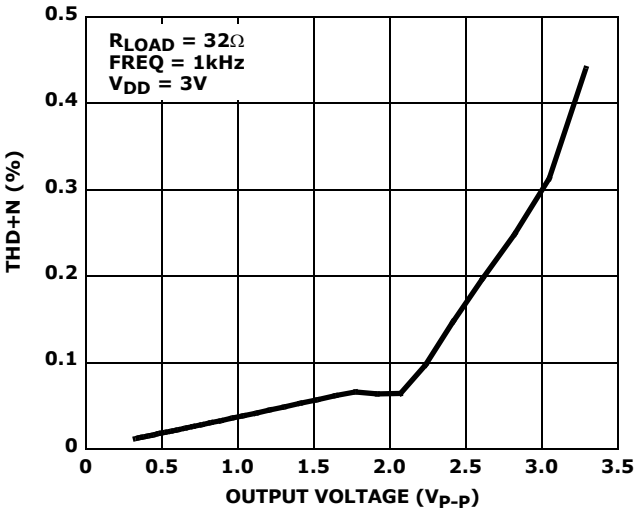


FIGURE 10. THD+N vs OUTPUT VOLTAGE

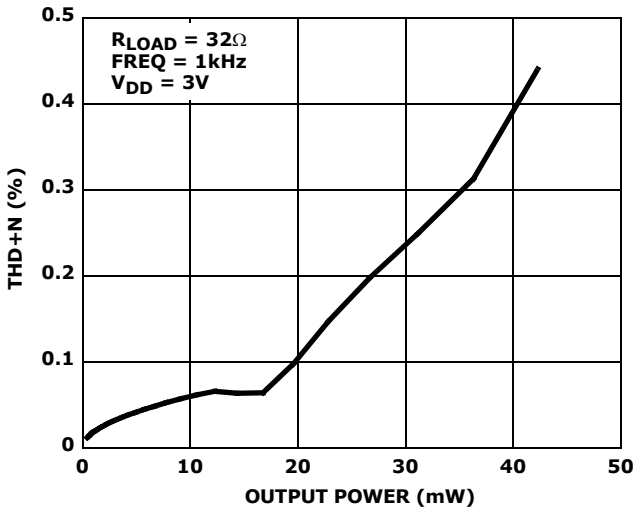


FIGURE 11. THD+N vs OUTPUT POWER

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

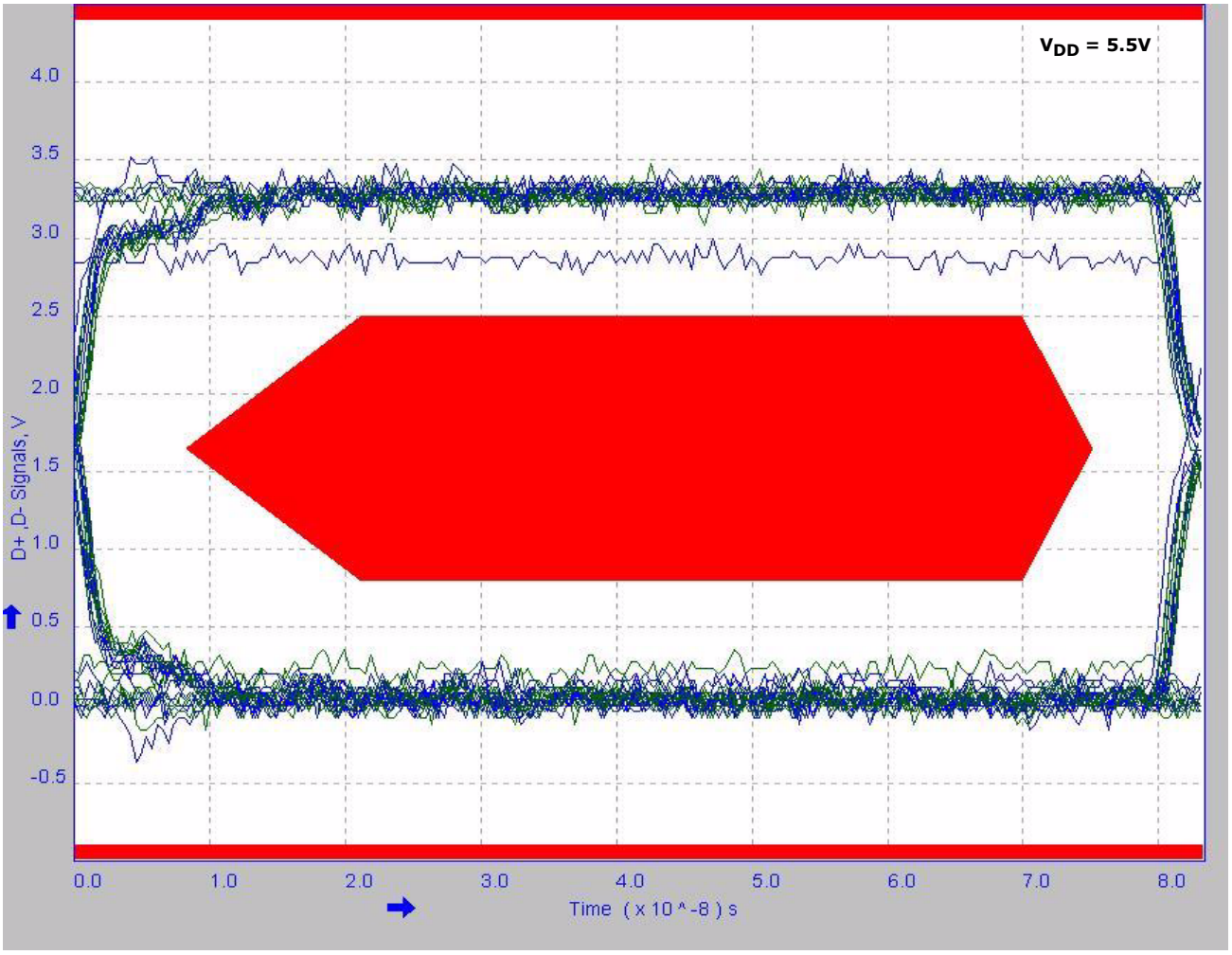


FIGURE 12. EYE PATTERN: 12MBps WITH SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

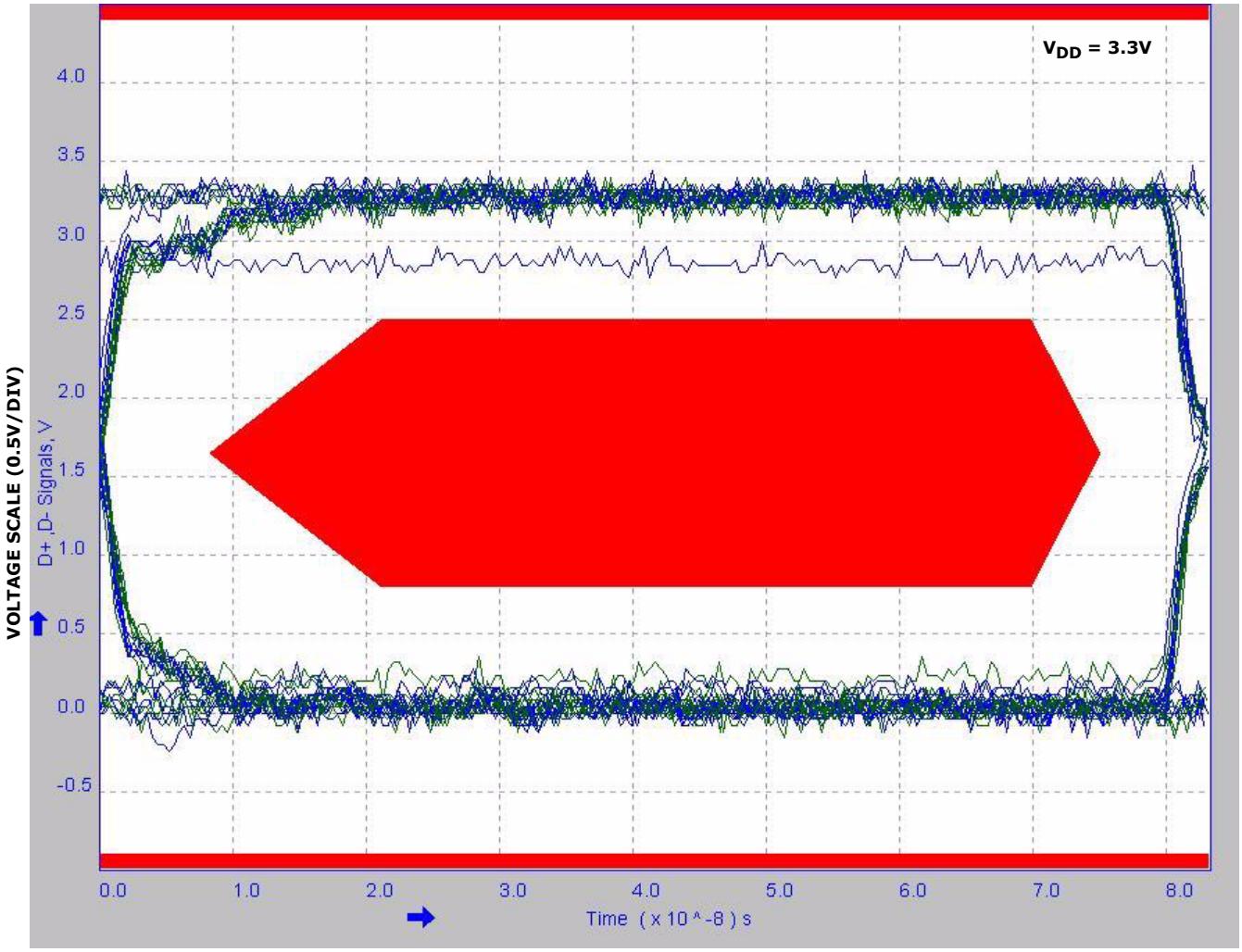


FIGURE 13. EYE PATTERN: 12MBps WITH SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

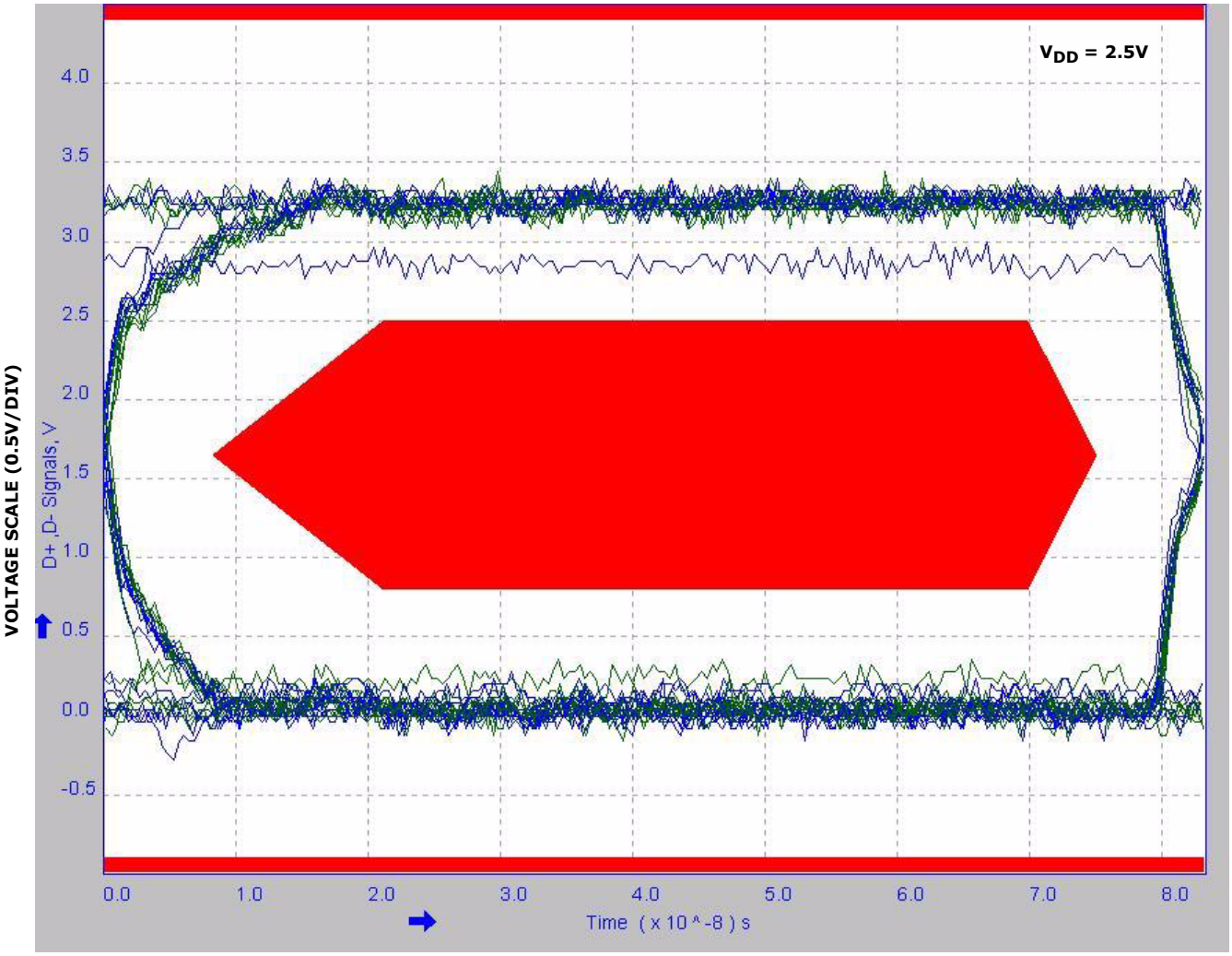
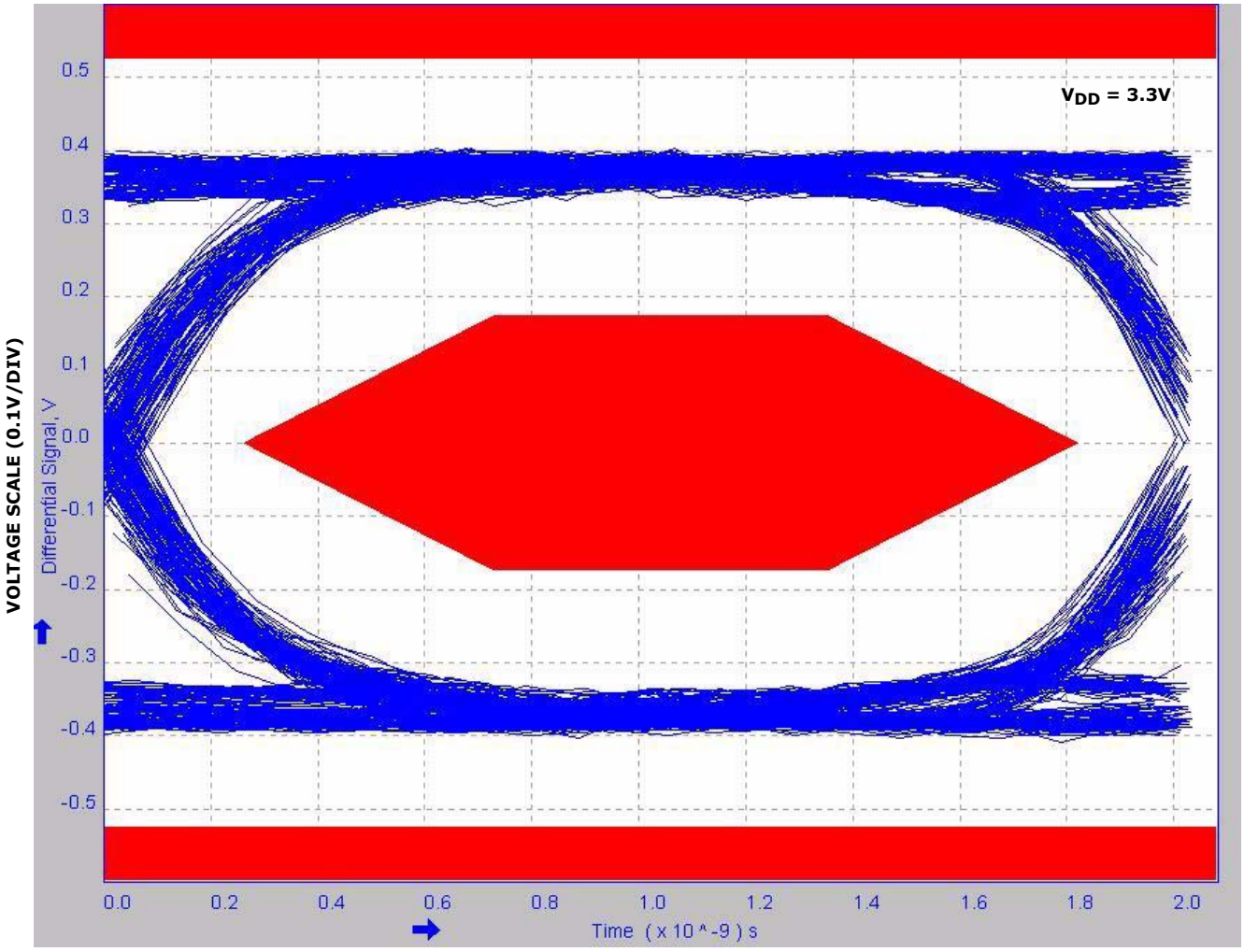


FIGURE 14. EYE PATTERN: 12MBps WITH SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**



TIME SCALE (0.2ns/DIV.)

FIGURE 15. EYE PATTERN: 480MBps USB SIGNAL WITH SWITCHES IN THE SIGNAL PATH

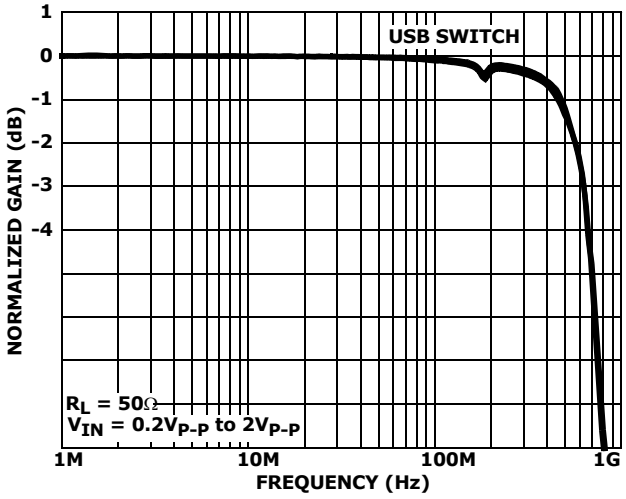


FIGURE 16. FREQUENCY RESPONSE

Die Characteristics

SUBSTRATE AND TDFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

98

PROCESS:

Submicron CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
10/19/10	FN6515.3	In “USB Switch Cell Off-Isolation” on page 10, changed 2nd sentence of 2nd paragraph from "With a USB transceiver connected at the D-/D+ pins and with a 32W headphone.." to "With a USB transceiver connected at the D-/D+ pins and with a 32Ω headphone.."
09/24/2010	FN6515.2	Added section titled “USB Switch Cell Off-Isolation” to page 10.
06/15/2010	FN6515.1	On page 1: Added "The L and R 50kΩ resistors to ground are not shown." to “Application Block Diagram”. Removed (2) 50kΩ resistors, which were tied to L and R next to "CODEC" block Updated Pb-free bullet in “Features” On page 2: Added PD to “Pin Descriptions” table Updated Pb-free notes in “Ordering Information” per new verbiage based on lead finish. Added TB347 link to ordering information for reel specifications. On page 4: Added Latch up to Abs Max Ratings Added Theta JC to “Thermal Information”. Changed 10 Ld µTQFN Theta JA from 130 to 145. Changed 10 Ld TDFN Theta JA from 110 to 55. Added applicable Theta JC notes. Added standard over temp note to common conditions of spec table (Boldface limits apply..) On page 5: Changed “ON Leakage Current, I_{Dx}” room temp and full temp limits from: Room temp MIN/TYP/MAX: from -10/2/10nA to -30/8/30nA Full temp MIN/MAX: from -75/75nA to -300/300nA On page 6: Changed “Positive Supply Current, IDD (Low Power State)” room temp and full temp limits from: Room temp TYP/MAX: from 1/7nA to 4/25nA Full temp: removed MAX of 140nA. Added TYP of 150nA On page 4 to page 6: Updated standard over-temp Note 15 in MIN/MAX columns of the Electrical Specifications table. On page 19: Updated POD L10.2.1X1.6A to most recent revision. Changes were: Convert to new format by moving dimensions from table onto drawing Corrected leadframe thickness in Detail x from 0.2 REF to 0.125 REF Corrected Note 4 to read "...between 0.15mm and 0.30mm...", it previously read "...between .015mm and 0.30mm..." Corrected the word "indentifier" in Note 8 to read "identifier". On page 20: Updated POD L10.3x3A to most recent revision. Changes were to add Typical Recommended Land Pattern & convert to new format by moving dimensions from table onto drawing (no dimension changes)
06/25/2007	FN6515.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL54206A

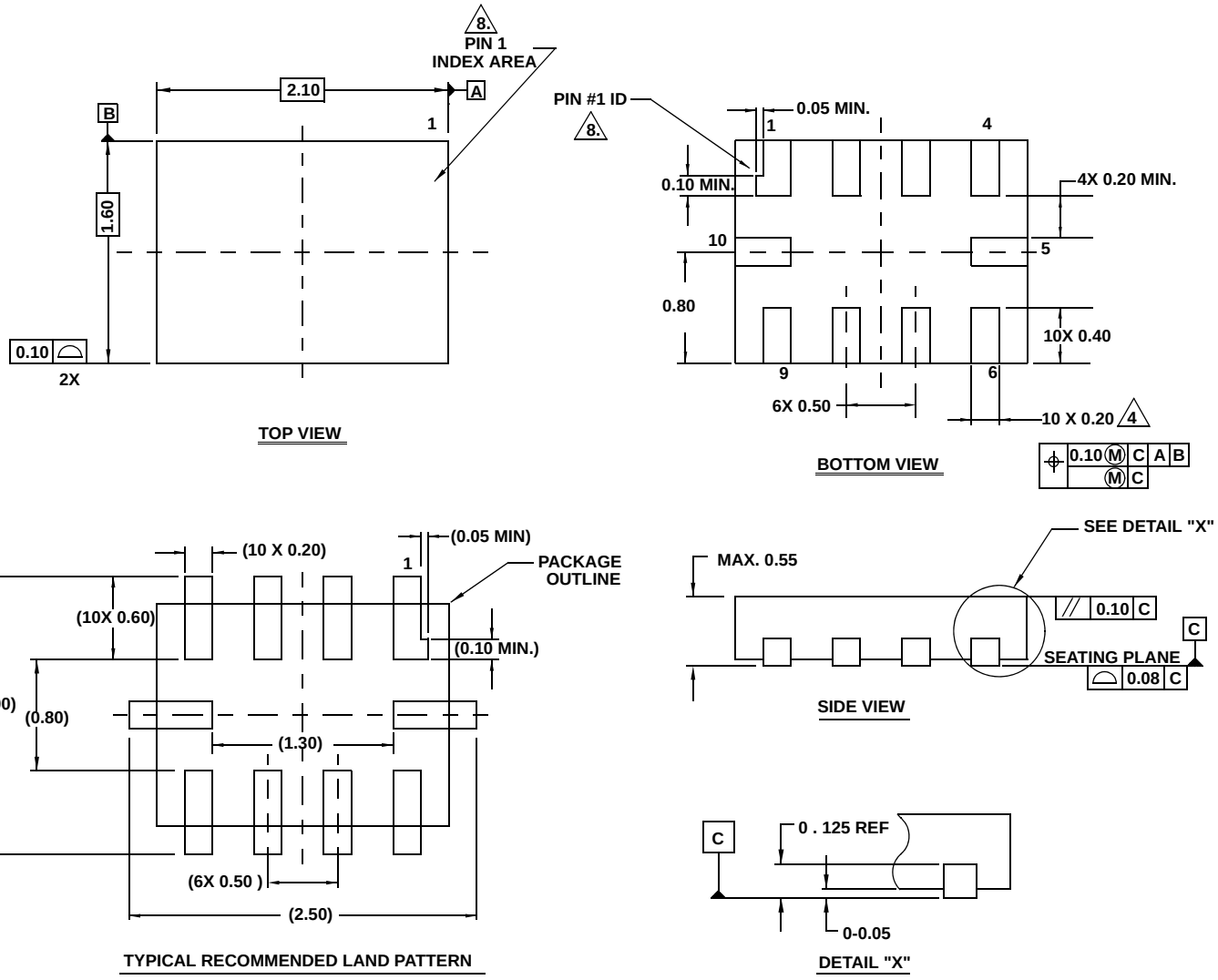
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

Package Outline Drawing

L10.2.1x1.6A

10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



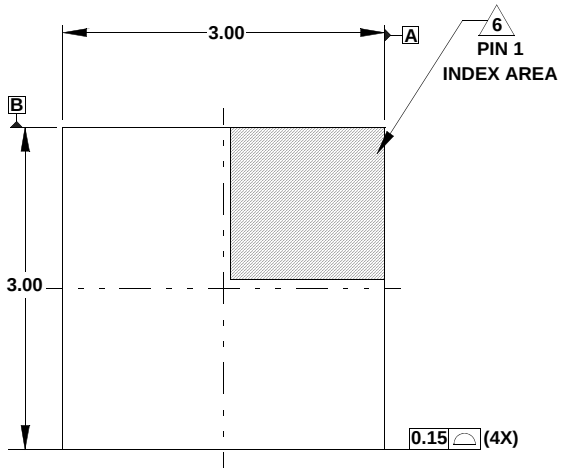
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All Dimensions are in millimeters. Angles are in degrees. Dimensions in ( ) for Reference Only.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Maximum package warpage is 0.05mm.
6. Maximum allowable burrs is 0.076mm in all directions.
7. Same as JEDEC MO-255UABD except:
   No lead-pull-back, MIN. Package thickness = 0.45 not 0.50mm
   Lead Length dim. = 0.45mm max. not 0.42mm.
8. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

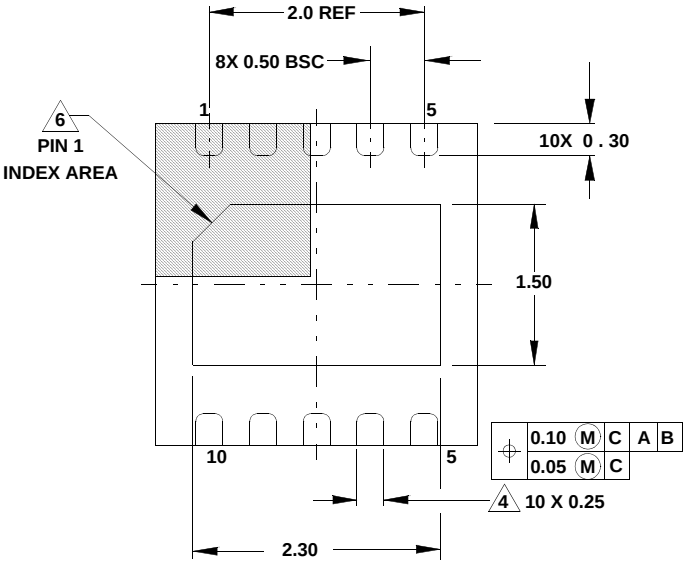
Package Outline Drawing

L10.3x3A

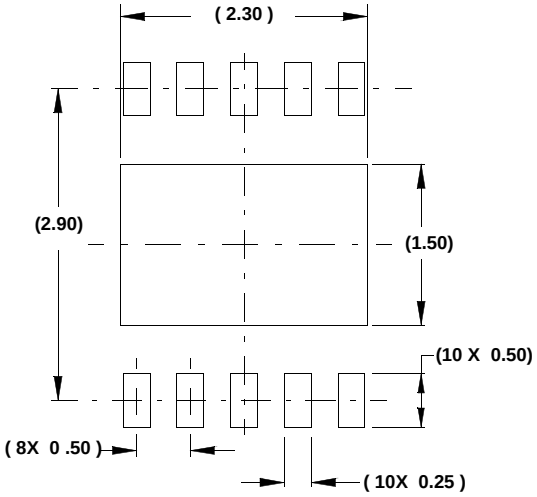
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



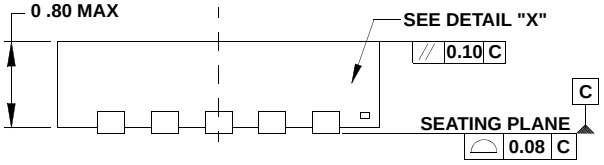
TOP VIEW



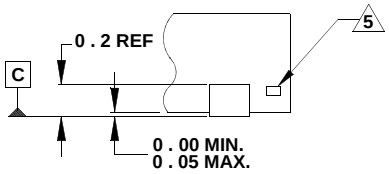
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
   Angular ±2.50°
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229-WEED-3 except exposed pad length (2.30mm).