74LVCH32245A

32-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Rev. 03 — 20 August 2007 Product data sheet

1. General description

The 74LVCH32245A is a 32-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features four output enable ($n\overline{OE}$) inputs for easy cascading and four send/receive (nDIR) inputs for direction control. Pin $n\overline{OE}$ controls the outputs so that the buses are effectively isolated.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

To ensure the high-impedance state during power-up or power-down, pin $n\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when V_{CC} = 0 V
- All data inputs have bus hold
- Complies with JEDEC standard JESD8-B / JESD36
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from −40 °C to +85 °C
- Packaged in plastic fine-pitch ball grid array package

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVCH32245AEC	–40 °C to +85 °C	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

4. Functional diagram

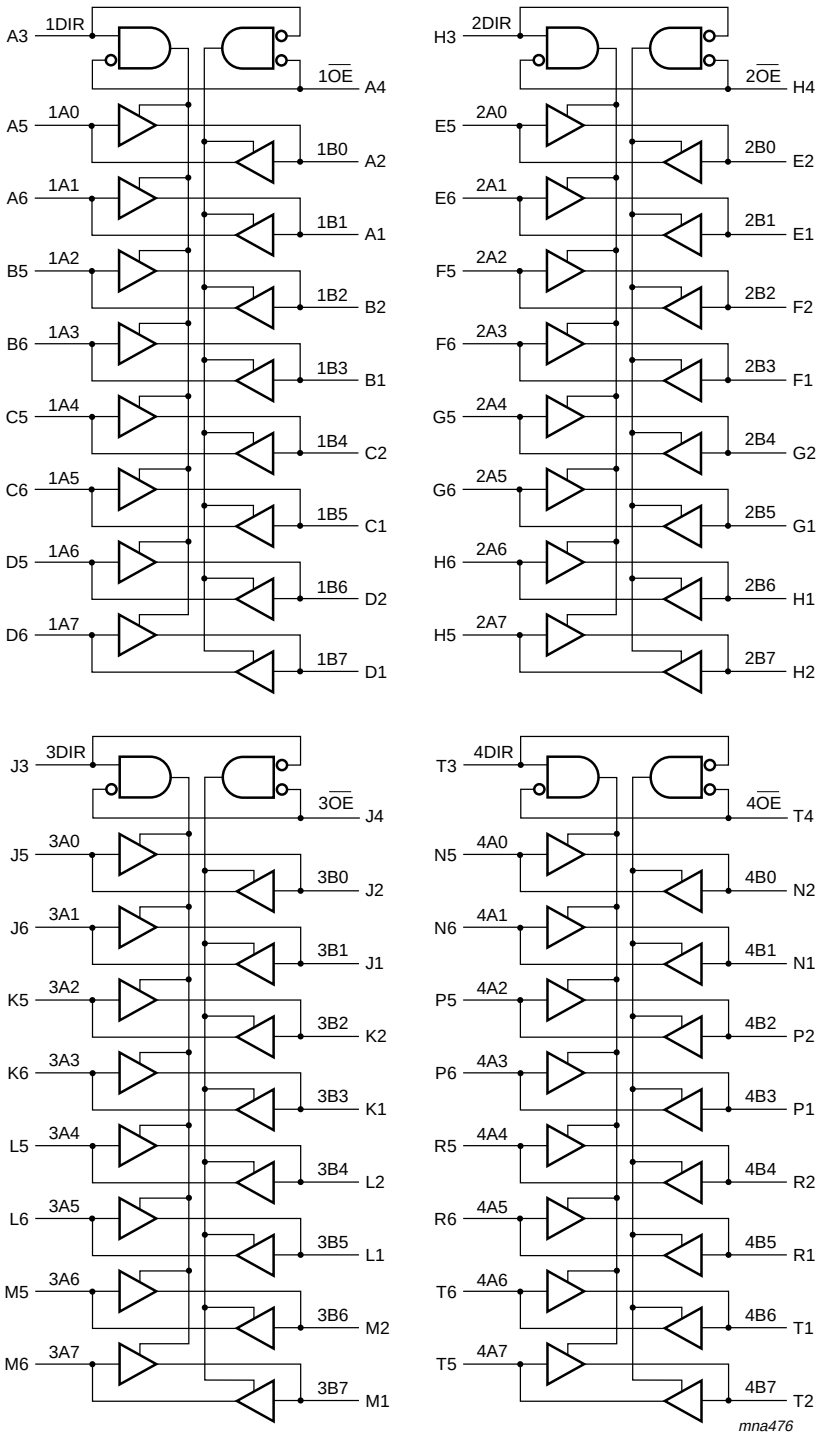


Fig 1. Logic symbol

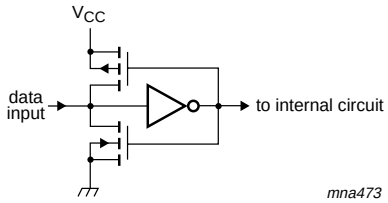


Fig 2. Bus hold circuit

5. Pinning information

5.1 Pinning

mna475

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	1A1	1A3	1A5	1A7	2A1	2A3	2A5	2A6	3A1	3A3	3A5	3A7	4A1	4A3	4A5	4A6
5	1A0	1A2	1A4	1A6	2A0	2A2	2A4	2A7	3A0	3A2	3A4	3A6	4A0	4A2	4A4	4A7
4	1$\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	2$\overline{OE}$	3$\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	4$\overline{OE}$
3	1DIR	GND	V_{CC}	GND	GND	V_{CC}	GND	2DIR	3DIR	GND	V_{CC}	GND	GND	V_{CC}	GND	4DIR
2	1B0	1B2	1B4	1B6	2B0	2B2	2B4	2B7	3B0	3B2	3B4	3B6	4B0	4B2	4B4	4B7
1	1B1	1B3	1B5	1B7	2B1	2B3	2B5	2B6	3B1	3B3	3B5	3B7	4B1	4B3	4B5	4B6

Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Pin name	Ball	Description
nDIR (n = 1 to 4)	A3, H3, J3, T3	direction control
n$\overline{OE}$ (n = 1 to 4)	A4, H4, J4, T4	output enable input (active LOW)
1A[0:7]	A5, A6, B5, B6, C5, C6, D5, D6	input or output
1B[0:7]	A2, A1, B2, B1, C2, C1, D2, D1	input or output
2A[0:7]	E5, E6, F5, F6, G5, G6, H6, H5	input or output
2B[0:7]	E2, E1, F2, F1, G2, G1, H1, H2	input or output
3A[0:7]	J5, J6, K5, K6, L5, L6, M5, M6	input or output
3B[0:7]	J2, J1, K2, K1, L2, L1, M2, M1	input or output
4A[0:7]	N5, N6, P5, P6, R5, R6, T6, T5	input or output
4B[0:7]	N2, N1, P2, P1, R2, R1, T1, T2	input or output
GND	B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	ground (0 V)
V_{CC}	C3, C4, F3, F4, L3, L4, P3, P4	supply voltage

6. Functional description

Table 3. Function selection[1]

Input		Output	
nOE	**nDIR**	**nAn**	**nBn**
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW state	[2]	–0.5	V_{CC} + 0.5	V
		output 3-state	[2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current		[3]	-	200	mA
I_{GND}	ground current		[3]	–200	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C	[4]	-	1000	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] All supply and ground pins connected externally to one voltage source.

[4] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.2 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	V_{CC} (V)		Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C								
V_{IH}	HIGH-level input voltage		1.2		V_{CC}	-	-	V
			2.7 to 3.6		2.0	-	-	V
V_{IL}	LOW-level input voltage		1.2		-	-	GND	V
			2.7 to 3.6		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = −100 µA	2.7 to 3.6		V_{CC} − 0.2	V_{CC}	-	V
		I_O = −12 mA	2.7		V_{CC} − 0.5	-	-	V
		I_O = −18 mA	3.0		V_{CC} − 0.6	-	-	V
		I_O = −24 mA	3.0		V_{CC} − 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA	2.7 to 3.6		-	GND	0.20	V
		I_O = 12 mA	2.7		-	-	0.40	V
		I_O = 24 mA	3.0		-	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND	3.6	[2]	-	±0.1	±5	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	3.6	[2][3]	-	±0.1	±5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V	0.0		-	±0.1	±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6		-	0.1	40	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} − 0.6 V; I_O = 0 A	2.7 to 3.6		-	5	500	µA
C_I	input capacitance	V_I = GND to V_{CC}	0 to 3.6		-	5.0	-	pF
$C_{I/O}$	input/output capacitance	V_I = GND to V_{CC}	0 to 3.6		-	10	-	pF
I_{BHL}	bus hold LOW current	V_I = 0.8 V	3.0	[4][5]	75	-	-	µA
I_{BHH}	bus hold HIGH current	V_I = 2.0 V	3.0	[4][5]	−75	-	-	µA
I_{BHLO}	bus hold LOW overdrive current		3.6	[4][6]	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current		3.6	[4][6]	−500	-	-	µA

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] The bus hold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input terminal.

[3] For I/O ports the parameter I_{OZ} includes the input leakage current.

[4] Valid for data inputs only. Note that control inputs do not have a bus hold circuit.

[5] The specified sustaining current at the data input holds the input below the specified V_I level.

[6] The specified overdrive current at the data input forces the data input to the opposite input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 6.

Symbol	Parameter	Conditions	V_{CC} (V)		Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C								
t_{pd}	propagation delay	nAn to nBn; nBn to nAn; see Figure 4	1.2	[2]	-	13.0	-	ns
			2.7		1.0	2.7	4.7	ns
			3.0 to 3.6		1.0	2.2	4.5	ns
t_{en}	enable time	$n\overline{OE}$ to nAn, nBn: see Figure 5	1.2	[2]	-	15.0	-	ns
			2.7		1.5	3.6	6.7	ns
			3.0 to 3.6		1.0	2.8	5.5	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn, nBn; see Figure 5	1.2	[2]	-	11.0	-	ns
			2.7		1.5	3.4	6.6	ns
			3.0 to 3.6		1.5	3.2	5.6	ns
$t_{sk(o)}$	output skew time		3.0 to 3.6	[3]	-	-	1.0	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	3.3	[4]	-	30	-	pF

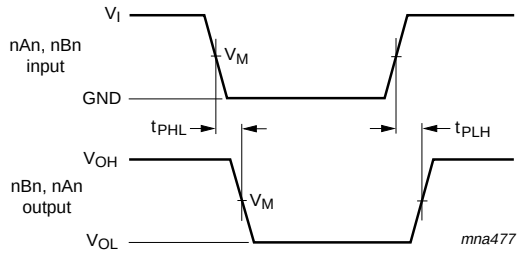
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms

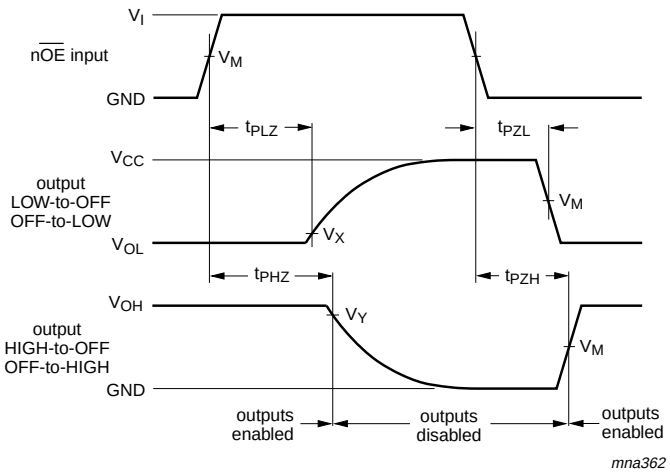


V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.

V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. The input (nAn, nBn) to output (nBn, nAn) propagation delays



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.

V_M = 0.5 $\times V_{CC}$ at V_{CC} < 2.7 V.

$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V;

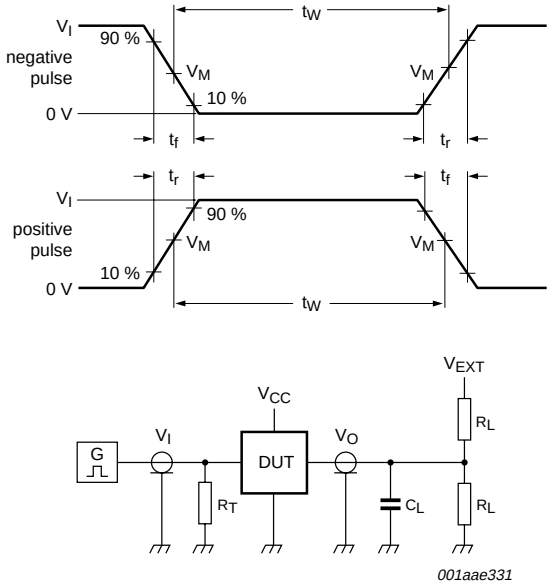
$V_X = V_{OL}$ + 0.15 V at V_{CC} < 2.7 V.

$V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V;

$V_Y = V_{OH}$ − 0.15 V at V_{CC} < 2.7 V.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. 3-state enable and disable times.



Test data is given in Table 8.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

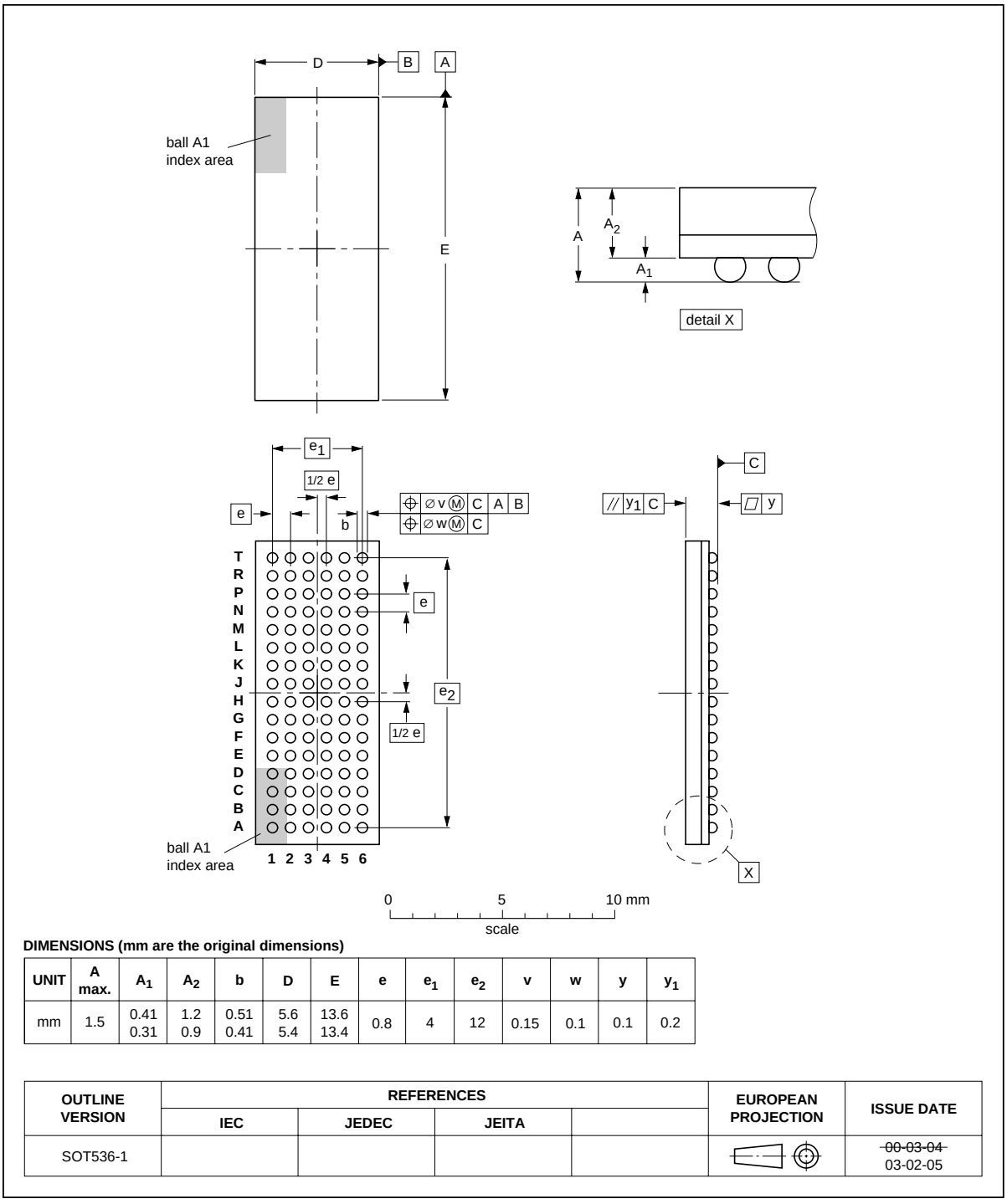
Fig 6. Load circuitry for switching times

Table 8. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						~~00-03-04~~ 03-02-05

Fig 7. Package outline SOT536-1 (LFBGA96)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCH32245A_3	20070820	Product data sheet	-	74LVCH32245A_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Error in Table 2 “Pin description” corrected. • Quick Reference Data section deleted. Information (C_{PD}, C_I, $C_{I/O}$) moved from it to Table 6 and Table 7. • Some parameter symbols and descriptions have been updated to comply with NXP guidelines.			
74LVCH32245A_2	20040511	Product specification	-	74LVC_LVCH32245A_1
74LVC_LVCH32245A_1	19990901	-	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

17. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 20 August 2007
Document identifier: 74LVCH32245A_3