

## DS3245 Quad MOS Clock Driver

### General Description

The DS3245 is a quad bipolar-to-MOS clock driver with TTL compatible inputs. It is designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

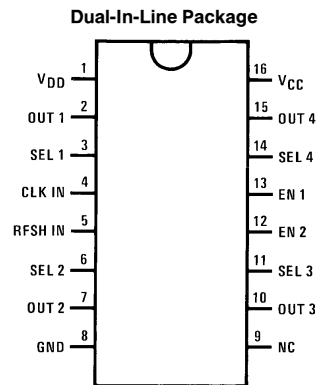
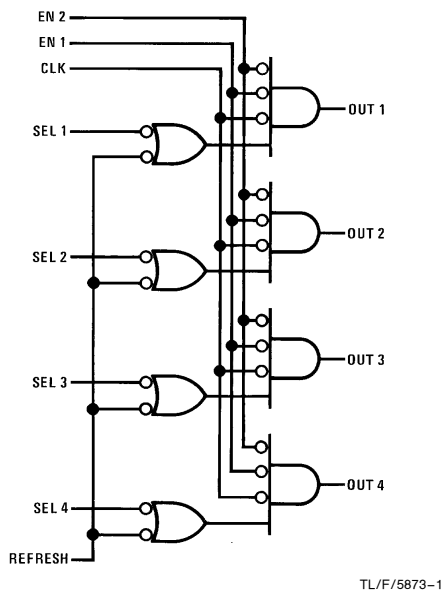
Only 2 supplies,  $5 V_{DC}$  and  $12 V_{DC}$ , are required without compromising the usual high  $V_{OH}$  specification obtained by circuits using a third supply.

The device features 2 common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

### Features

- TTL compatible inputs
- Operates from 2 standard supplies:  $5 V_{DC}$ ,  $12 V_{DC}$
- Internal bootstrap circuit eliminates need for external PNP's
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function equivalent to Intel 3245

### Logic and Connection Diagrams



Top View

Order Number DS3245J or DS3245N  
See NS Package Number J16A or N16A

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	-10°C to +85°C
Storage Temperature	-65°C to +150°C
Supply Voltage, $V_{CC}$	-0.5V to +7V
Supply Voltage, $V_{DD}$	-0.5V to +14V
All Input Voltages	-1.0V to $V_{DD}$
Outputs for Clock Driver	-1.0V to $V_{DD} + 1V$
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

\*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

## Operating Conditions

	Min	Max	Units
Supply Voltage, $V_{CC}$	4.75	5.25	V
Supply Voltage, $V_{DD}$	11.4	12.6	V
Operating Temperature $\theta T_A$	0	75	°C

## Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{FD}$	Select Input Load Current	$V_F = 0.45V$			-0.25	mA
$I_{FE}$	Enable Input Load Current	$V_F = 0.45V$			-1.0	mA
$I_{RD}$	Select Input Leakage Current	$V_R = 5V$			10	$\mu A$
$I_{RE}$	Enable Input Leakage Current	$V_R = 5V$			40	$\mu A$
$V_{OL}$	Output Low Voltage	$I_{OL} = 5\text{ mA}, V_{IH} = 2V$			0.45	V
		$I_{OL} = -5\text{ mA}$	-1.0			V
$V_{OH}$	Output High Voltage	$I_{OH} = -1\text{ mA}, V_{IL} = 0.8V$	$V_{DD} - 0.50$			V
		$I_{OH} = 5\text{ mA}$			$V_{DD} + 1.0$	V
$V_{IL}$	Input Low Voltage, All Inputs				0.8	V
$V_{IH}$	Input High Voltage, All Inputs		2			V
$V_{CLAMP}$	Input Clamp Voltage	$V_{CC} = \text{Min}, I_{IN} = -12\text{ mA}$		-1.0	-1.5	V

## Power Supply Current Drain

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{CC}$	Current from $V_{CC}$ Output in High State	$V_{CC} = 5.25V,$ $V_{DD} = 12.6V$		26	34	mA
$I_{DD}$	Current from $V_{DD}$ Output in High State	$V_{CC} = 5.25V,$ $V_{DD} = 12.6V$		23	30	mA
$I_{CC}$	Current from $V_{CC}$ Output in Low State	$V_{CC} = 5.25V,$ $V_{DD} = 12.6V$		29	39	mA
$I_{DD}$	Current from $V_{DD}$ Output in Low State	$V_{CC} = 5.25V,$ $V_{DD} = 12.6V$		13	19	mA

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Unless otherwise specified min/max limits apply across the 0°C to +°C range. All typical values are for  $T_A = 25^\circ C$  and  $V_{CC} = 5V$  and  $V_{DD} = 12V$ .

**Note 3:** All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

## Switching Characteristics $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$ , $V_{CC} = 5\text{V} \pm 5\%$ , $V_{DD} = 12\text{V} \pm 5\%$

Symbol	Parameter	Conditions	Min(1)	Typ(2,4)	Max(3)	Units
$t_{-+}$	Input to Output Delay	$R_{\text{SERIES}} = 0$	5	11		ns
$t_{\text{DR}}$	Delay Plus Rise Time	$R_{\text{SERIES}} = 0$		20	32	ns
$t_{+ -}$	Input to Output Delay	$R_{\text{SERIES}} = 0$	3	7		ns
$t_{\text{DF}}$	Delay Plus Fall Time	$R_{\text{SERIES}} = 0$		18	32	ns
$t_{\text{T}}$	Output Transition Time	$R_{\text{SERIES}} = 20\Omega$	10	17	25	ns
$t_{\text{DR}}$	Delay Plus Rise Time	$R_{\text{SERIES}} = 20\Omega$		27	38	ns
$t_{\text{DF}}$	Delay Plus Fall Time	$R_{\text{SERIES}} = 20\Omega$		25	38	ns

## Capacitance $T_A = 25^\circ\text{C}$ (5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{\text{IN}}$	Input Capacitance, $\bar{I}_1, \bar{I}_2, \bar{I}_3, \bar{I}_4$			5	8	pF
$C_{\text{IN}}$	Input Capacitance, $\bar{R}, \bar{C}, \bar{E}1, \bar{E}2$			8	12	pF

Note 1:  $C_L = 150\text{ pF}$

Note 2:  $C_L = 200\text{ pF}$

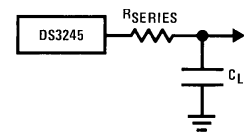
Note 3:  $C_L = 250\text{ pF}$

} These values represent a range of total stray plus clock capacitance for nine 4k RAMs.

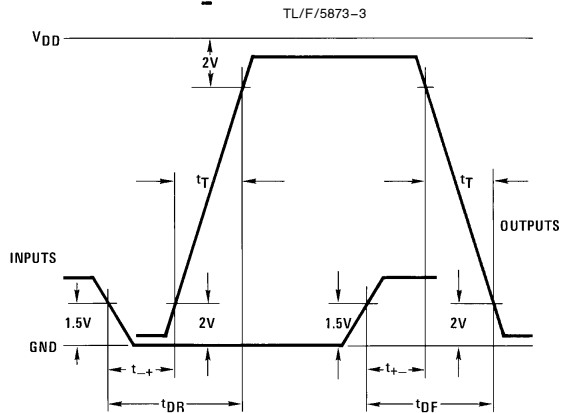
Note 4: Typical values are measured at  $25^\circ\text{C}$ .

Note 5: This parameter is periodically sampled and is not 100% tested. Condition of measurement is  $f = 1\text{ MHz}$ ,  $V_{\text{BIAS}} = 2\text{V}$ ,  $V_{\text{CC}} = 0\text{V}$ , and  $T_A = 25^\circ\text{C}$ .

## AC Test Circuit and Switching Time Waveforms

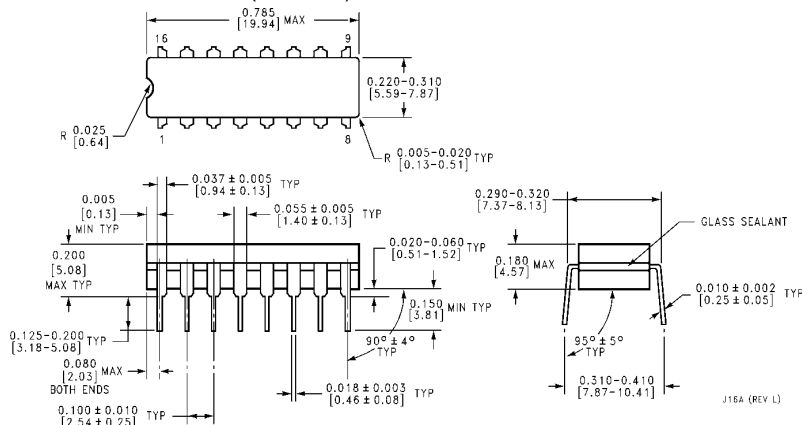


Input pulse amplitudes: 3V  
 Input pulse rise and fall times:  
 5 ns between 1V and 2V  
 Measurements points: see waveforms

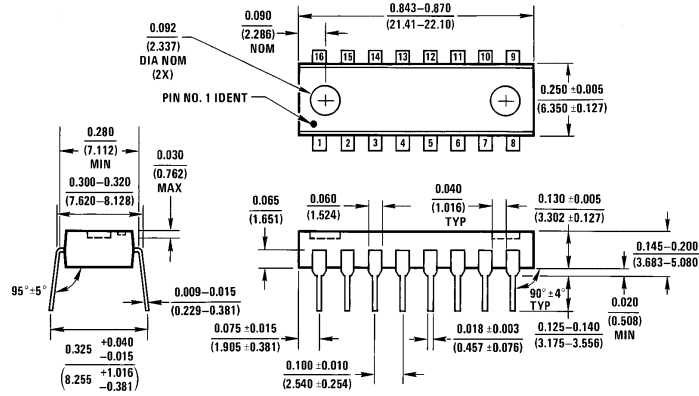


TL/F/5873-4

**Physical Dimensions** inches (millimeters)



**Ceramic Dual-in-Line Package (J)**  
**Order Number DS3245J**  
**NS Package Number J16A**



**Molded Dual-in-Line Package (N)**  
**Order Number DS3245N**  
**NS Package Number N16A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 <p><b>National Semiconductor Corporation</b>          1111 West Bardin Road          Arlington, TX 76017          Tel: 1(800) 272-9959          Fax: 1(800) 737-7018</p>	<p><b>National Semiconductor Europe</b>          Fax: (+49) 0-180-530 85 86          Email: cnjwge@tevm2.nsc.com          Deutsch Tel: (+49) 0-180-530 85 85          English Tel: (+49) 0-180-532 78 32          Français Tel: (+49) 0-180-532 93 58          Italiano Tel: (+49) 0-180-534 16 80</p>	<p><b>National Semiconductor Hong Kong Ltd.</b>          19th Floor, Straight Block,          Ocean Centre, 5 Canton Rd.          Tsimshatsui, Kowloon          Hong Kong          Tel: (852) 2737-1600          Fax: (852) 2736-9960</p>	<p><b>National Semiconductor Japan Ltd.</b>          Tel: 81-043-299-2309          Fax: 81-043-299-2408</p>
--	--	---	---

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.