



M41T315Y* M41T315V/W

Serial Access Phantom RTC Supervisor

FEATURES SUMMARY

- 3.0V, 3.3V, OR 5V OPERATING VOLTAGE
- REAL TIME CLOCK KEEPS TRACK OF TENTHS/HUNDREDTHS OF SECONDS, SECONDS, MINUTES, HOURS, DAYS, DATE OF THE MONTH, MONTHS, AND YEARS
- AUTOMATIC LEAP YEAR CORRECTION VALID UP TO 2100
- AUTOMATIC SWITCH-OVER AND DESELECT CIRCUITRY
- CHOICE OF POWER-FAIL DESELECT VOLTAGES:
(V_{PFD} = Power-fail Deselect Voltage)
 - M41T315Y: $V_{CC} = 4.5$ to $5.5V$
 $4.25V \leq V_{PFD} \leq 4.50V$
 - M41T315V: $V_{CC} = 3.0$ to $3.6V$
 $2.80V \leq V_{PFD} \leq 2.97V$
 - M41T315W: $V_{CC} = 2.7$ to $3.3V$
 $2.60V \leq V_{PFD} \leq 2.70V$
- NO ADDRESS SPACE REQUIRED TO COMMUNICATE WITH RTC
- PROVIDES NONVOLATILE SUPERVISOR FUNCTIONS FOR BATTERY BACKUP OF SRAM
- FULL $\pm 10\%$ V_{CC} OPERATING RANGE
- INDUSTRIAL OPERATING TEMPERATURE RANGE (-40 to $+85^{\circ}C$)
- ULTRA-LOW BATTERY SUPPLY CURRENT OF $500nA$ (max)
- OPTIONAL PACKAGING INCLUDES A 28-LEAD SOIC and SNAPHAT[®] TOP (to be ordered separately)
- SNAPHAT PACKAGE PROVIDES DIRECT CONNECTION FOR A SNAPHAT TOP, WHICH CONTAINS THE BATTERY AND CRYSTAL

Figure 1. 16-pin SOIC Package

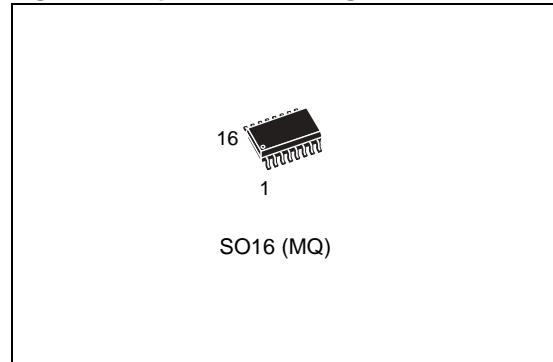
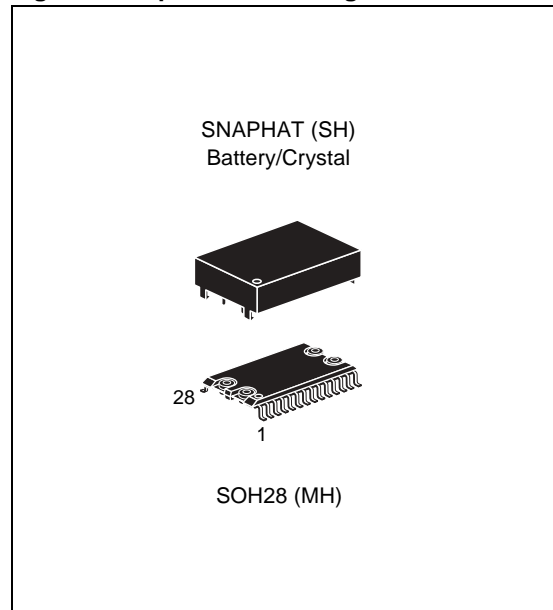


Figure 2. 28-pin SOIC Package



* Contact Local Sales Office

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SUMMARY DESCRIPTION

The M41T315Y/V/W RTC Supervisor is a combination of a CMOS TIMEKEEPER® and a nonvolatile memory supervisor. Power is constantly monitored by the memory supervisor. In the event of power instability or absence, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM by switching on and invoking write protection to prevent data corruption in the memory and RTC.

The clock keeps track of tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including leap year correction.

The clock operates in one of two formats:

- a 12-hour mode with an AM/PM indicator; or
- a 24-hour mode

The nonvolatile supervisor supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The M41T315Y/V/W can be interfaced with RAM without leaving gaps in memory.

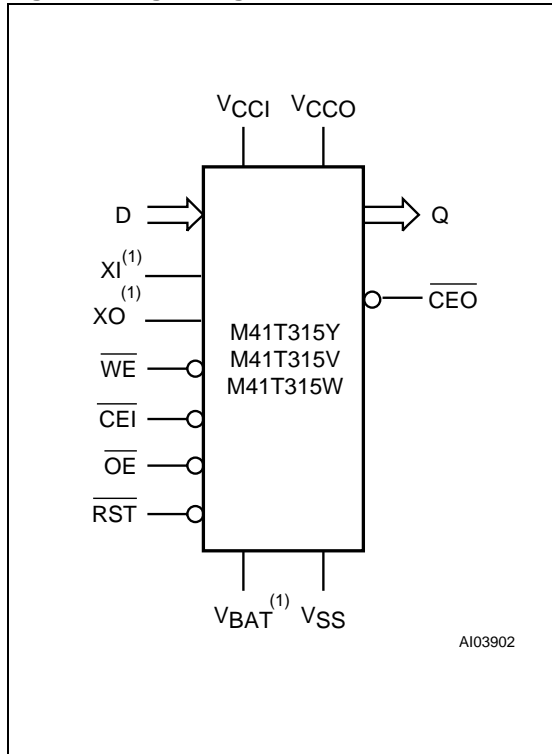
The M41T315Y/V/W is supplied in a 28-lead SOIC SNAPHAT® package (which integrates both crystal and battery in a single SNAPHAT top) or a 16-pin SOIC. The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery and crystal. The unique design allows the SNAPHAT battery/crystal package to be mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is also keyed to prevent reverse insertion.

The 28-pin SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is "M4TXX-BR12SH" (see [Table 17.](#), page 22).

Caution: Do not place the SNAPHAT battery/crystal top in conductive foam, as this will drain the lithium button-cell battery.

Figure 3. Logic Diagram



Note: 1. For 16-pin SOIC only

Table 1. Signal Names

| | |
|-------|--------------------------------|
| XI-XO | 32.768 kHz Crystal Connection |
| D | Data Input |
| Q | Data Output |
| RST | Reset Input |
| CEO | Chip Enable Output |
| CEI | Chip Enable Input |
| VBAT | Battery Input |
| OE | Output Enable Input |
| WE | WRITE Enable Input |
| VCCO | Switched Supply Voltage Output |
| VCCI | Supply Voltage Input |
| VSS | Ground |
| NC | Not Connected Internally |
| DU | Don't Use |

Figure 4. 16-pin SOIC Connections

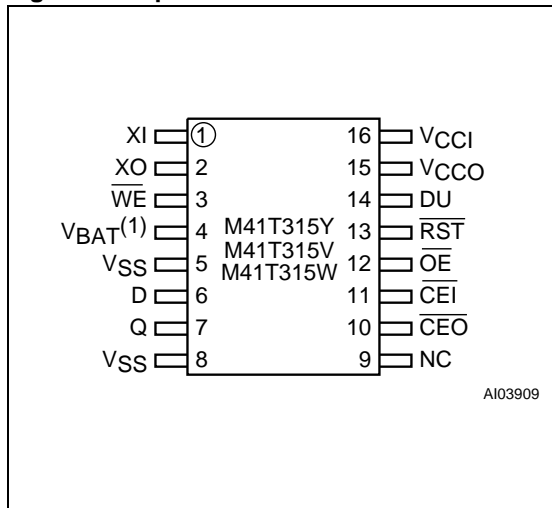
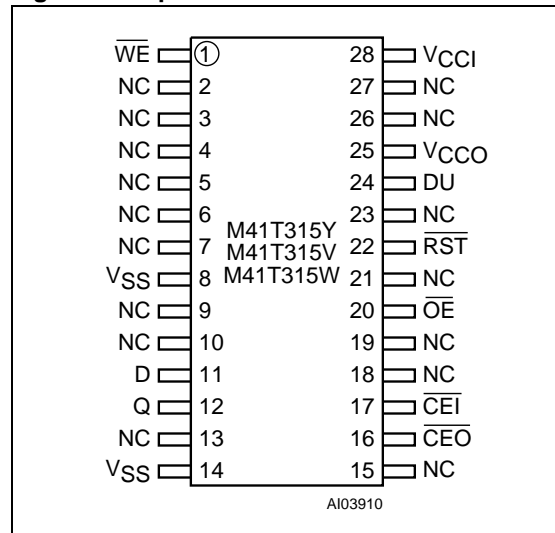


Figure 5. 28-pin SOIC Connections



Note: 1. Should be tied to VSS if not used.

Figure 6. Block Diagram

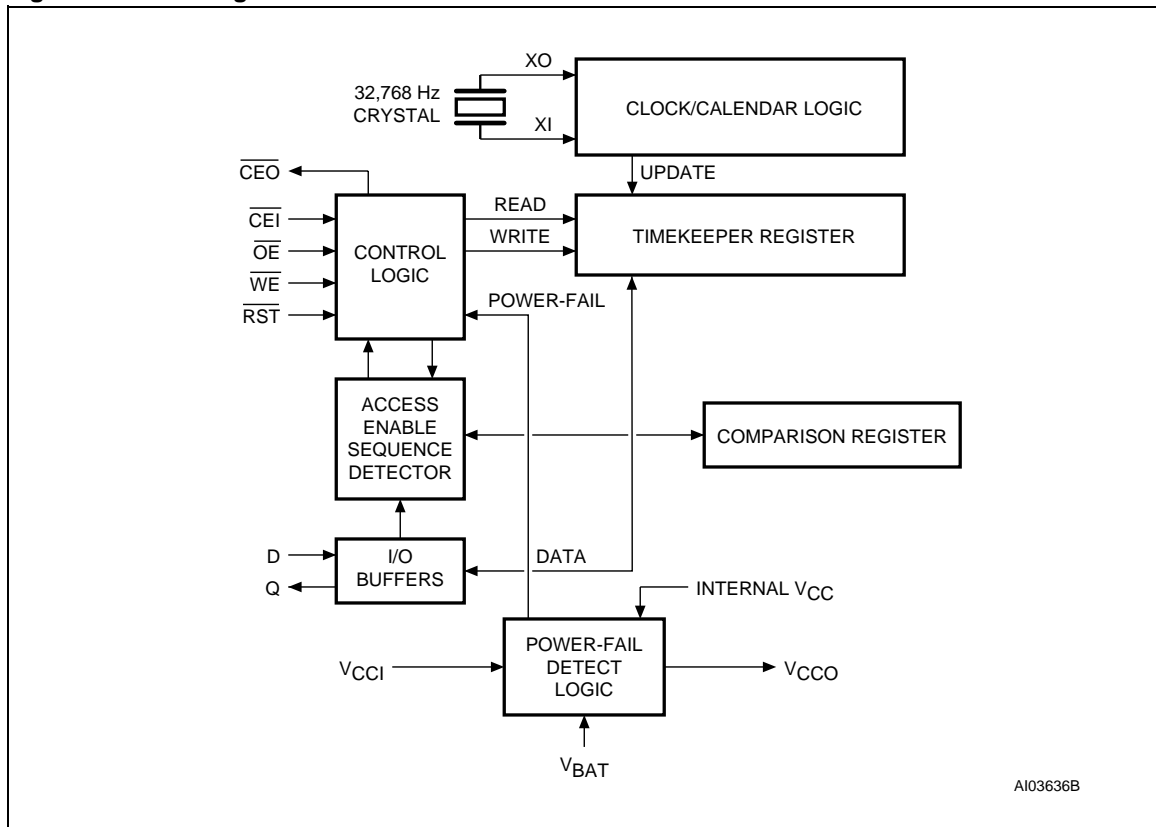
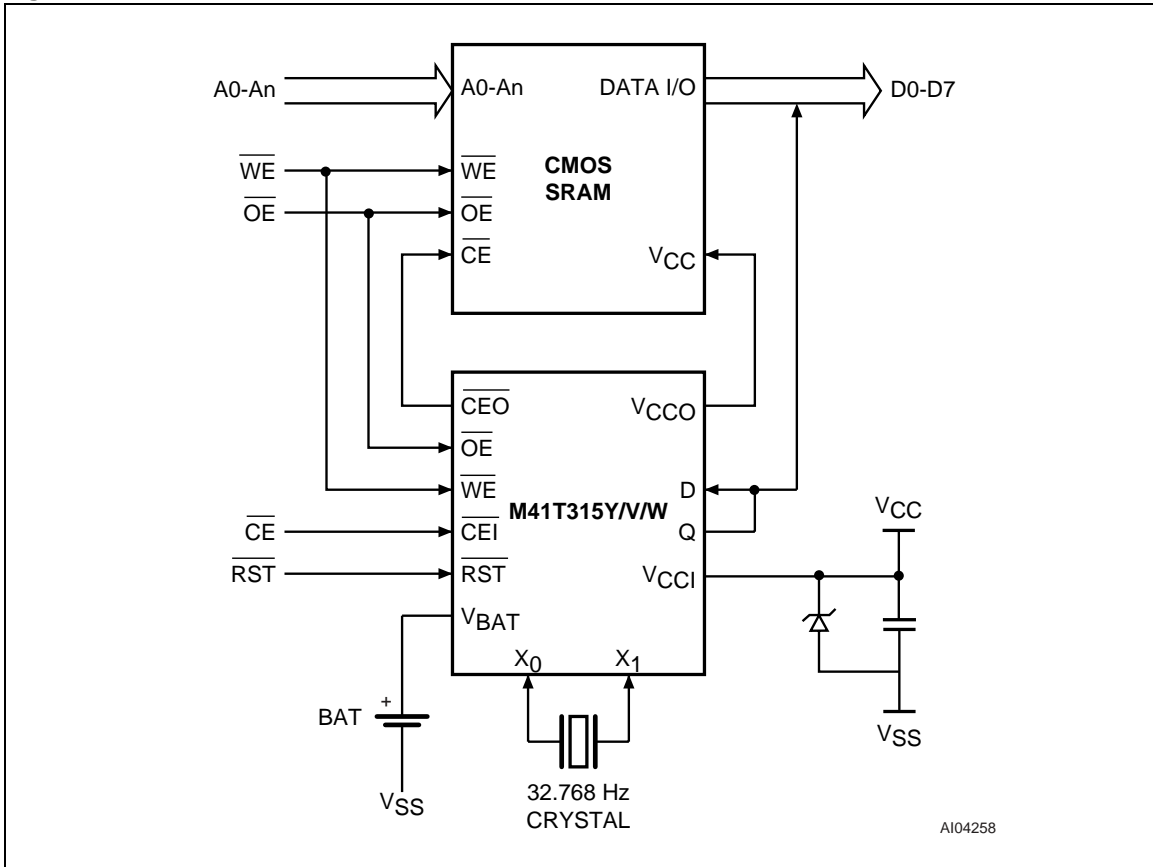


Figure 7. M41T315Y/V/W to RAM/Clock Interface



OPERATION

Figure 6., page 5 illustrates the main elements of the device. The following paragraphs describe the signals and functions.

Communication with the clock is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive WRITE cycles containing the proper data on data in (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the chip enable output pin ($\overline{\text{CEO}}$).

After recognition is established, the next 64 READ or WRITE Cycles either extract or update data in the clock and $\overline{\text{CEO}}$ remains high during this time, disabling the connected memory (see Table 2., page 7).

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable input ($\overline{\text{CEI}}$), output enable ($\overline{\text{OE}}$), and WRITE enable ($\overline{\text{WE}}$). Initially, a READ cycle using the $\overline{\text{CEI}}$ and $\overline{\text{OE}}$ control of the clock starts the pattern recognition sequence by moving the pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive WRITE cycles are executed using the $\overline{\text{CEI}}$ and $\overline{\text{WE}}$ control of the clock. These 64 WRITE cycles are used only to gain access to the clock.

When the first WRITE cycle is executed, it is compared to the first bit of the 64-bit comparison reg-

ister. If a match is found, the pointer increments to the next location of the comparison register and awaits the next WRITE cycle.

If a match is not found, the pointer does not advance and all subsequent WRITE cycles are ignored. If a READ cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 WRITE cycles as described above until all the bits in the comparison register have been matched (see Figure 10., page 11.)

With a correct match for 64 bits, access to the registers is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the device to either receive data on D, or transmit data on Q, depending on the level of $\overline{\text{OE}}$ pin or the $\overline{\text{WE}}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{\text{CEI}}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the device.

For a SO16 pin package, a standard 32.768 kHz quartz crystal can be directly connected to the M41T315Y/V/W via pins 1 and 2 (XI, XO). The crystal selected for use should have a specified load capacitance (C_L) of 12.5 pF (see Table 10., page 17).

Table 2. Operating Modes

| Mode | V _{CC} | $\overline{\text{CEI}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | D | Q | Power |
|----------|--|-------------------------|------------------------|------------------------|-----------------|------------------|----------------------|
| Deselect | 4.5 to 5.5V or 3.0 to 3.6V or 2.7 to 3.3V | V _{IH} | X | X | Hi-Z | Hi-Z | Standby |
| WRITE | | V _{IL} | X | V _{IL} | D _{IN} | Hi-Z | Active |
| READ | | V _{IL} | V _{IL} | V _{IH} | Hi-Z | D _{OUT} | Active |
| READ | | V _{IL} | V _{IH} | V _{IH} | Hi-Z | Hi-Z | Active |
| Deselect | V _{SO} to V _{PFD} (min) ⁽¹⁾ | X | X | X | Hi-Z | Hi-Z | CMOS Standby |
| Deselect | ≤ V _{SO} ⁽¹⁾ | X | X | X | Hi-Z | Hi-Z | Battery Back-up Mode |

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.

Note: 1. See Table 11., page 17 for details.

Non-volatile Supervisor Operation

A switch is provided to direct power from the battery input or V_{CC1} to V_{CC0} with a maximum voltage drop of 0.3 Volts. The V_{CC0} output pin is used to supply uninterrupted power to CMOS SRAM. The M41T315Y/V/W safeguards the clock and RAM data by power-fail detection and write protection.

Power-fail detection occurs when V_{CC1} falls below V_{PFD} which is set by an internal bandgap reference. The M41T315Y/V/W constantly monitors the V_{CC1} supply pin. When V_{CC1} is less than V_{PFD} ,

power-fail circuitry forces the chip enable output ($\overline{CE0}$) to V_{CC1} or $V_{BAT}-0.2$ volts for external RAM write protection. During nominal supply conditions, $\overline{CE0}$ will track $\overline{CE1}$ with a propagation delay. Internally, the M41T315Y/V/W aborts any data transfer in progress without changing any of the device registers and prevents future access until V_{CC1} exceeds V_{PFD} . Figure 7., page 6 illustrates a typical RAM/clock interface.

Figure 8. READ Mode Waveforms

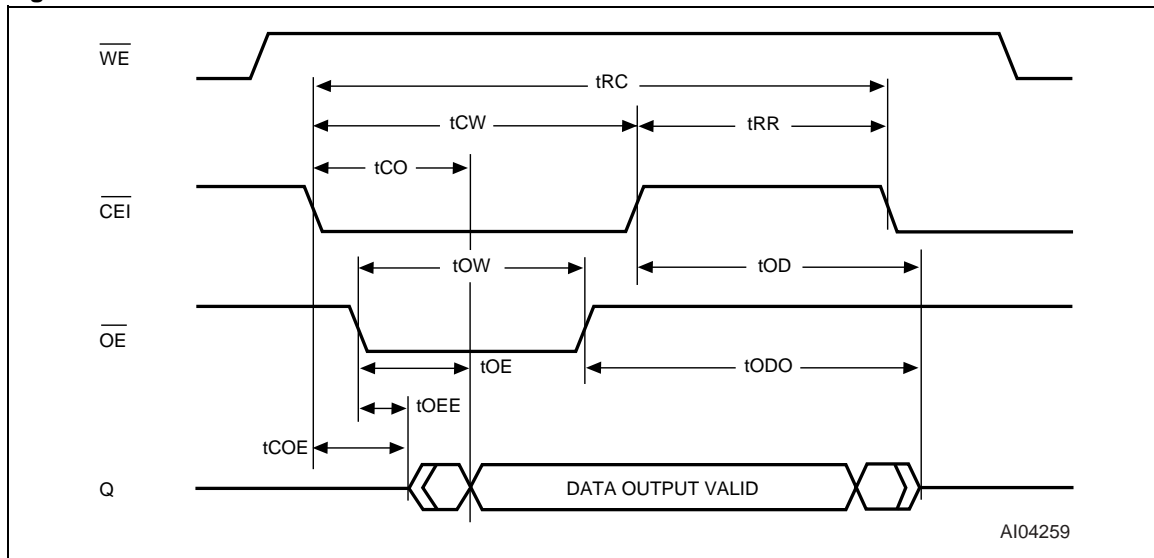


Figure 9. WRITE Mode Waveforms

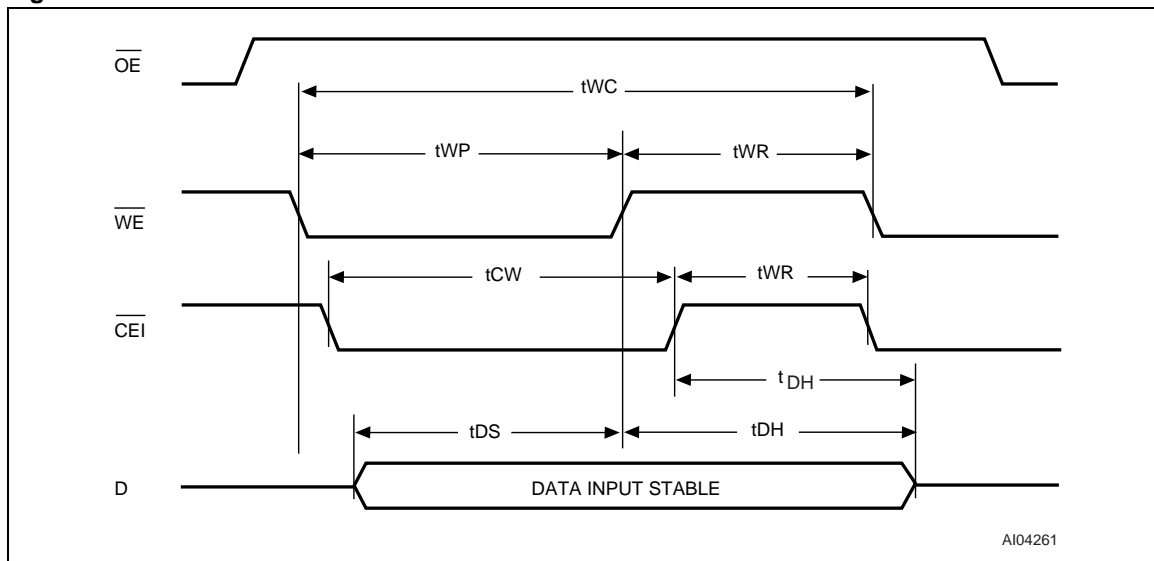


Table 3. AC Electrical Characteristics (M41T315Y)

| Symbol | | Parameter ⁽¹⁾ | Min | Typ | Max | Units |
|--|--------------------------------|--|-----|-----|-----|-------|
| t _{AVAV} | t _{RC} | READ Cycle Time | 65 | | | ns |
| t _{ELQV} | t _{CO} | $\overline{\text{CEI}}$ Access Time | | | 55 | ns |
| t _{GLQV} | t _{OE} | $\overline{\text{OE}}$ Access Time | | | 55 | ns |
| t _{ELQX} | t _{COE} | $\overline{\text{CEI}}$ to Output Low Z | 5 | | | ns |
| t _{GLQX} | t _{OEE} | $\overline{\text{OE}}$ to Output Low Z | 5 | | | ns |
| t _{EHQZ} | t _{OD} | $\overline{\text{CEI}}$ to Output High Z | | | 25 | ns |
| t _{GHQZ} | t _{ODO} | $\overline{\text{OE}}$ to Output High Z | | | 25 | ns |
| | t _{RR} | READ Recovery | 10 | | | ns |
| t _{ELEH} | t _{CW} | $\overline{\text{CEI}}$ Pulse Width | 55 | | | ns |
| t _{GLGH} | t _{OW} | $\overline{\text{OE}}$ Pulse Width | 55 | | | ns |
| t _{AVAV} | t _{WC} | WRITE Cycle | 65 | | | ns |
| t _{WLWH} | t _{WP} | WRITE Pulse Width | 55 | | | ns |
| t _{EHAX} t _{WHAX} | t _{WR} ⁽²⁾ | WRITE Recovery | 10 | | | ns |
| t _{DVEH} t _{DVWH} | t _{DS} ⁽³⁾ | Data Setup | 30 | | | ns |
| t _{EHDX} t _{WHDX} | t _{DH} ⁽³⁾ | Data Hold Time | 0 | | | ns |
| | t _{RST} | $\overline{\text{RST}}$ Pulse Width | 65 | | | ns |

Note: 1. Valid for Ambient Operating Temperature: T_A = -40 to 85°C; V_{CC} = 4.5 to 5.5V (except where noted).

2. t_{WR} is a function of the latter occurring edge of WE or CEI.

3. t_{DH} and t_{DS} are functions of the first occurring edge of WE or CEI in RAM mode.

M41T315Y*, M41T315V, M41T315W

Table 4. AC Electrical Characteristics (M41T315V/W)

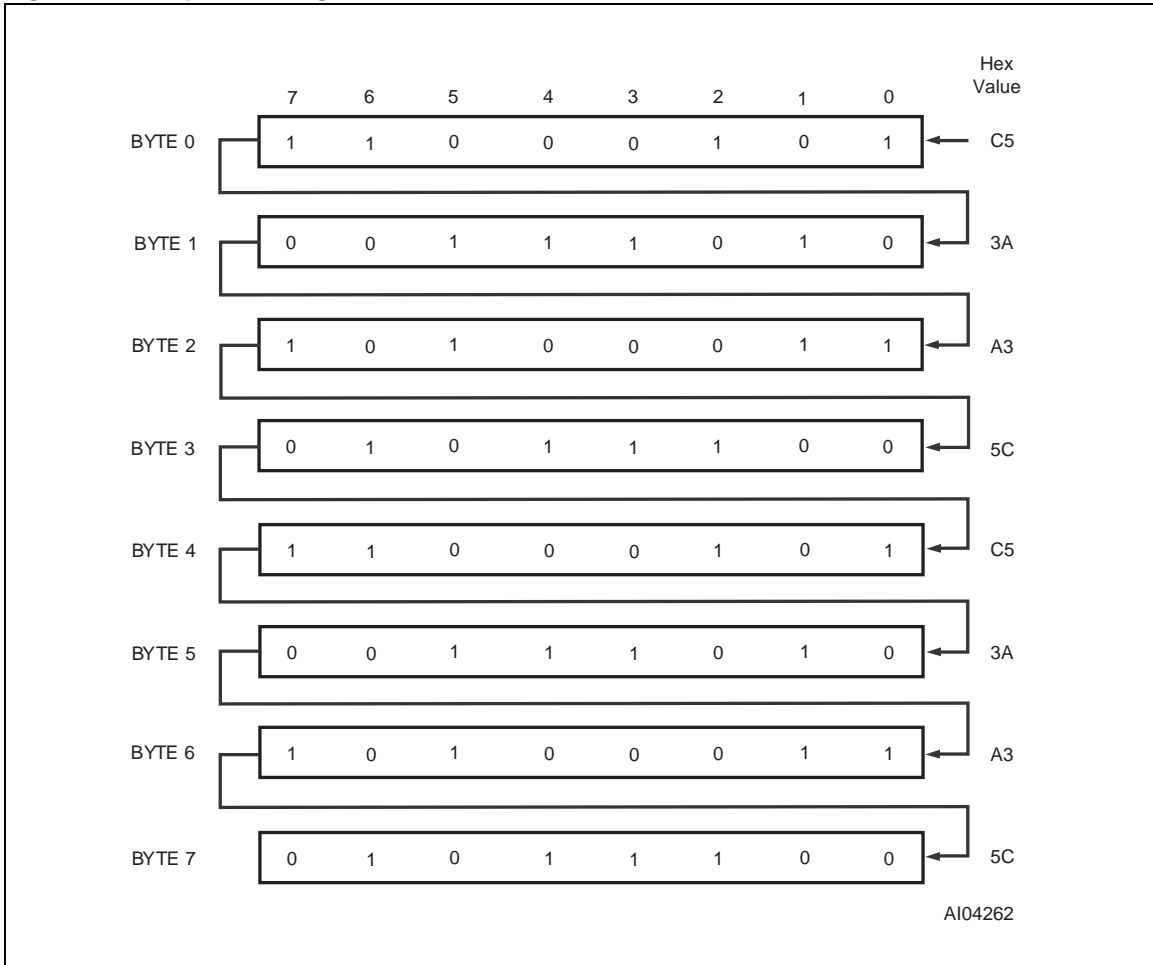
| Symbol | | Parameter ⁽¹⁾ | Min | Typ | Max | Units |
|--|--------------------------------|--|-----|-----|-----|-------|
| t _{AVAV} | t _{RC} | READ Cycle Time | 85 | | | ns |
| t _{ELQV} | t _{CO} | $\overline{\text{CEI}}$ Access Time | | | 85 | ns |
| t _{GLQV} | t _{OE} | $\overline{\text{OE}}$ Access Time | | | 85 | ns |
| t _{ELQX} | t _{COE} | $\overline{\text{CEI}}$ to Output Low Z | 5 | | | ns |
| t _{GLQX} | t _{OEE} | $\overline{\text{OE}}$ to Output Low Z | 5 | | | ns |
| t _{EHQZ} | t _{OD} | $\overline{\text{CEI}}$ to Output High Z | | | 30 | ns |
| t _{GHQZ} | t _{ODO} | $\overline{\text{OE}}$ to Output High Z | | | 30 | ns |
| | t _{RR} | READ Recovery | 20 | | | ns |
| t _{ELEH} | t _{CW} | $\overline{\text{CEI}}$ Pulse Width | 65 | | | ns |
| t _{GLGH} | t _{OW} | $\overline{\text{OE}}$ Pulse Width | 60 | | | ns |
| t _{AVAV} | t _{WC} | WRITE Cycle | 85 | | | ns |
| t _{WLWH} | t _{WP} | WRITE Pulse Width | 60 | | | ns |
| t _{EHAX} t _{WHAX} | t _{WR} ⁽²⁾ | WRITE Recovery | 25 | | | ns |
| t _{DVEH} t _{DVWH} | t _{DS} ⁽³⁾ | Data Setup | 35 | | | ns |
| t _{EHDX} t _{WHDX} | t _{DH} ⁽³⁾ | Data Hold Time | 5 | | | ns |
| | t _{RST} | $\overline{\text{RST}}$ Pulse Width | 85 | | | ns |

Note: 1. Valid for Ambient Operating Temperature: T_A = -40 to 85°C; VCC = 2.7 to 3.6V (except where noted).

2. t_{WR} is a function of the latter occurring edge of WE or CEI.

3. t_{DH} and t_{DS} are functions of the first occurring edge of WE or CEI in RAM mode.

Figure 10. Comparison Register Definition



Note: Pattern recognition in "hex" is C5, 3A, A3, 5C, C5, 3A, A3, and 5C. The odds of this pattern being accidentally duplicated and sending aberrant entries to the RTC is less than 1 in 10^{19} . This pattern is sent to the clock LSB to MSB.

Data Retention

Most low power SRAMs on the market today can be used with the M41T315Y/V/W. There are, however some criteria which should be used in making the final choice of an SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M41T315Y/V/W and SRAMs to be Don't Care once V_{CCI} falls below $V_{PFD}(\min)$. The SRAM should also guarantee data retention down to $V_{CC}=2.0$ volts. The chip enable access time must be sufficient to meet the system needs with the chip enable output propagation delays included. If the SRAM includes a second chip enable pin (E2), this pin should be tied to V_{OUT} .

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular

SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0 volts. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the I_{BAT} value of the M41T315Y/V/W to determine the total current requirements for data retention. The available battery capacity for the SNAPHAT[®] of your choice can then be divided by this current to determine the amount of data retention available (see [Table 17.](#), [page 22](#)).

For a further more detailed review of lifetime calculations, please see Application Note AN1012.

CLOCK OPERATION

Clock Register Information

Clock information is contained in eight registers of 8 bits, each of which is sequentially accessed 1 bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the clock registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These READ/WRITE registers are defined in [Table 5., page 13.](#)

Data contained in the clock registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with Bit 0 of Register 0 and ending with Bit 7 of Register 7.

AM-PM/12/24 Mode

Bit 7 of the hours register is defined as the 12-hour or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, Bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, Bit 5 is the second 10-hour bit (20-23 hours).

Oscillator and Reset Bits

Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin input. When the Reset Bit is set to logic '1,' the reset input pin is ignored. When the Reset Bit is set to logic '0,' a low input on the reset pin will cause the device to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to logic '0,' the oscillator turns on and the real time clock/calendar begins to increment.

Zero Bits

Registers 1, 2, 3, 4, 5, and 6 contain one (1) or more bits that will always read logic '0.' When writing to these locations, either a logic '1' or '0' is acceptable.

Table 5. RTC Register Map

| Register | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function/Range BCD Format | |
|----------|-------------|------------|-------------------------|-------------------------|------------------------|-----------------|---------|---------|------------------------------|------|
| | | | | | | | | | | |
| 0 | 0.1 Seconds | | | 0.01 Seconds | | | Seconds | 00-99 | | |
| 1 | 0 | 10 Seconds | | | Seconds | | | Seconds | 00-59 | |
| 2 | 0 | 10 Minutes | | | Minutes | | | Minutes | 00-59 | |
| 3 | 12/24 | 0 | 10 / A/P | Hrs | Hours (24 Hour Format) | | | Hours | 01-12/ 00-23 | |
| 4 | 0 | 0 | $\overline{\text{OSC}}$ | $\overline{\text{RST}}$ | 0 | Day of the Week | | | Day | 01-7 |
| 5 | 0 | 0 | 10 date | | Date: Day of the Month | | | Date | 01-31 | |
| 6 | 0 | 0 | 0 | 10M | Month | | | Month | 01-12 | |
| 7 | 10 Years | | | Year | | | Year | 00-99 | | |

Keys:

A/P = AM/PM Bit

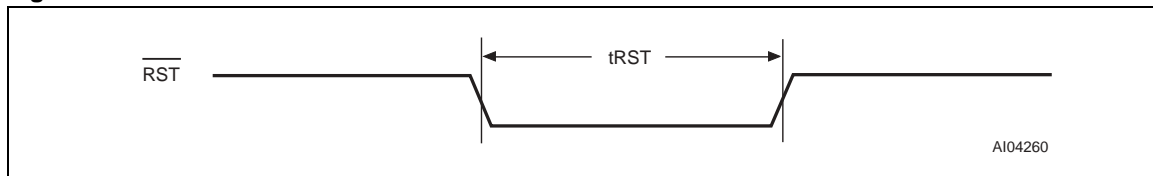
12/24 = 12 or 24-hour mode Bit

$\overline{\text{OSC}}$ = Oscillator Bit

$\overline{\text{RST}}$ = Reset Bit

0 = Must be set to '0'

Figure 11. Reset Pulse Waveform



MAXIMUM RATING

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is

not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

| Symbol | Parameter | | Value | Unit |
|---------------------------------|--|------------|-------------------------------|------|
| T _A | Operating Temperature | | -40 to +85 | °C |
| T _{STG} | Storage Temperature (V _{CC} , Oscillator Off) | SNAPHAT® | -40 to +85 | °C |
| | | SOIC | -55 to +125 | °C |
| T _{SLD} ⁽¹⁾ | Lead Solder Temperature for 10 seconds | | 260 | °C |
| V _{CCI} | Supply Voltage (on any pin relative to Ground) | M41T315Y | -0.3 to +7.0 | V |
| | | M41T315V/W | -0.3 to +4.6 | V |
| V _{IO} | Input or Output Voltages | | -0.3 to V _{CC} + 0.3 | V |
| I _O | Output Current | | 20 | mA |
| P _D | Power Dissipation | | 1 | W |

Note: 1. For SO package, standard (SnPb) lead finish: Reflow at peak temperature of 225°C (total thermal budget not to exceed 180°C for between 90 to 150 seconds).
 2. For SO package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

CAUTION: Negative undershoots below -0.3V are not allowed on any pin while in the Battery Back-up mode.
CAUTION: Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

DC AND AC PARAMETERS

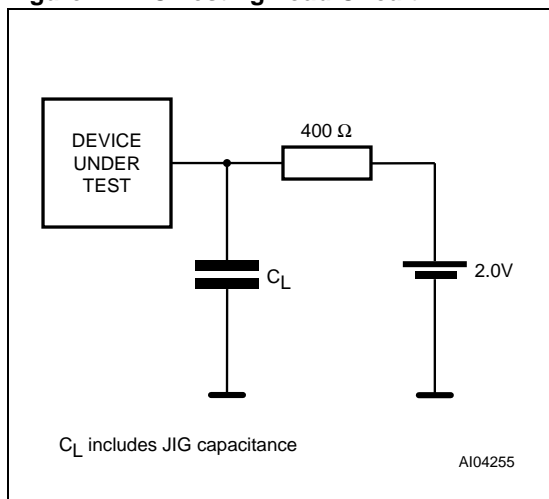
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7. DC and AC Measurement Conditions

| Parameter | M41T315Y | M41T315V/W |
|---------------------------------------|-------------|-------------|
| V _{CC} Supply Voltage | 4.5 to 5.5V | 2.7 to 3.6V |
| Ambient Operating Temperature | -40 to 85°C | -40 to 85°C |
| Load Capacitance (C _L) | 100pF | 50pF |
| Input Rise and Fall Times | ≤ 5ns | ≤ 5ns |
| Input Pulse Voltages | 0 to 3V | 0 to 3V |
| Input and Output Timing Ref. Voltages | 1.5V | 1.5V |

Figure 12. AC Testing Load Circuit



Note: 50pF for M41T315V.

Table 8. Capacitance

| Symbol | Parameter ^(1,2) | Min | Max | Unit |
|--------------------------------|----------------------------|-----|-----|------|
| C _{IN} | Input Capacitance | | 10 | pF |
| C _{IO} ⁽³⁾ | Input / Output Capacitance | | 10 | pF |

Note: 1. Effective capacitance measured with power supply at 5V; sampled only; not 100% tested.
 2. At 25°C, f = 1MHz.
 3. Outputs were deselected.

Table 9. DC Characteristics

| Sym | Parameter | Test Condition ⁽¹⁾ | M41T315Y | | | M41T315V/W | | | Unit |
|------------------|---------------------------------|---|--|-----------|----------------|--|-----|----------------------|------|
| | | | -65 | | | -85 | | | |
| | | | Min | Typ | Max | Min | Typ | Max | |
| $I_{IL}^{(2)}$ | Input Leakage Current | $0V \leq V_{IN} \leq V_{CC}$ | | | ±1 | | | ±1 | µA |
| I_{OL} | Output Leakage Current | $0V \leq V_{OUT} \leq V_{CC}$ | | | ±1 | | | ±1 | µA |
| $I_{CC1}^{(3)}$ | Supply Current | | | | 10 | | | 6 | mA |
| $I_{CCO1}^{(4)}$ | V_{CC} Power Supply Current | $V_{CC0} = V_{CC1} - 0.3$ | | | 150 | | | 100 | mA |
| $I_{CC2}^{(3)}$ | Supply Current (TTL Standby) | $\overline{CEI} = V_{IH}$ | | | 3 | | | 2 | mA |
| $I_{CC3}^{(3)}$ | V_{CC} Power Supply Current | $\overline{CEI} = V_{CC1} - 0.2$ | | | 1 | | | 1 | mA |
| $V_{IL}^{(5)}$ | Input Low Voltage | | -0.3 | | 0.8 | -0.3 | | 0.6 | V |
| $V_{IH}^{(5)}$ | Input High Voltage | | 2.2 | | $V_{CC} + 0.3$ | 2.0 | | $V_{CC} + 0.3$ | V |
| $V_{OL}^{(6)}$ | Output Low Voltage | $I_{OL} = 4.0 \text{ mA}$ | | | 0.4 | | | 0.4 | V |
| $V_{OH}^{(6)}$ | Output High Voltage | $I_{OH} = -1.0 \text{ mA}$ | 2.4 | | | 2.4 | | | V |
| V_{PFD} | Power Fail Deselect | | 4.25 | | 4.50 | 2.80 (V) 2.60 (W) | | 2.97 (V) 2.70 (W) | V |
| V_{SO} | Battery Back-up Switchover | | | V_{BAT} | | | 2.5 | | V |
| V_{BAT} | Battery Voltage | | 2.5 | | 3.7 | 2.5 | | 3.7 | V |
| V_{CEO} | \overline{CEO} Output Voltage | | $V_{CC1} - 0.2$ or $V_{BAT} - 0.2$ | | | $V_{CC1} - 0.2$ or $V_{BAT} - 0.2$ | | | V |
| $I_{BAT}^{(3)}$ | Battery Current | $V_{BAT} = 3.0V$ $T_A = 25^\circ C$ $V_{CC} = 0V$ | | | 0.5 | | | 0.5 | µA |
| $I_{CCO2}^{(7)}$ | Battery Backup Current | $V_{CC0} = V_{BAT} - 0.2V$ | | | 100 | | | 100 | µA |

- Note: 1. Valid for Ambient Operating Temperature: $T_A = -40$ to $85^\circ C$; $V_{CC} = 4.5$ to $5.5V$ or 2.7 to $3.6V$ (except where noted).
 2. Applies to all input pins except RST, which is pulled internally to V_{CC1} .
 3. Measured without RAM connected.
 4. I_{CCO1} is the maximum average load current the device can supply to external memory.
 5. Voltages are referenced to Ground.
 6. Measured with load shown in [Figure 12., page 15.](#)
 7. I_{CCO2} is the maximum average load current that the device can supply to memory in the battery backup mode.

Table 10. Crystal Electrical Characteristics (Externally Supplied)

| Symbol | Parameter ^(1,2) | Min | Typ | Max | Unit |
|----------------|----------------------------|-----|--------|-----|------|
| f _O | Resonant Frequency | | 32.768 | | kHz |
| R _S | Series Resistance | | | 60 | kΩ |
| C _L | Load Capacitance | | 12.5 | | pF |

Note: 1. These values are externally supplied. STMicroelectronics recommends the KDS DT-38: 1TA/1TC252E127, Tuning Fork Type (through-hole) or the DMX-26S: 1TJS125FH2A212, (SMD) quartz crystal for industrial temperature operations. KDS can be contacted at kouhou@kdsj.co.jp or <http://www.kdsj.co.jp> for further information on this crystal type.

Note: 1. Load capacitors are integrated within the M41T315Y/V/W. Circuit board layout considerations for the 32.768kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

Figure 13. Power Down/Up Mode AC Waveforms

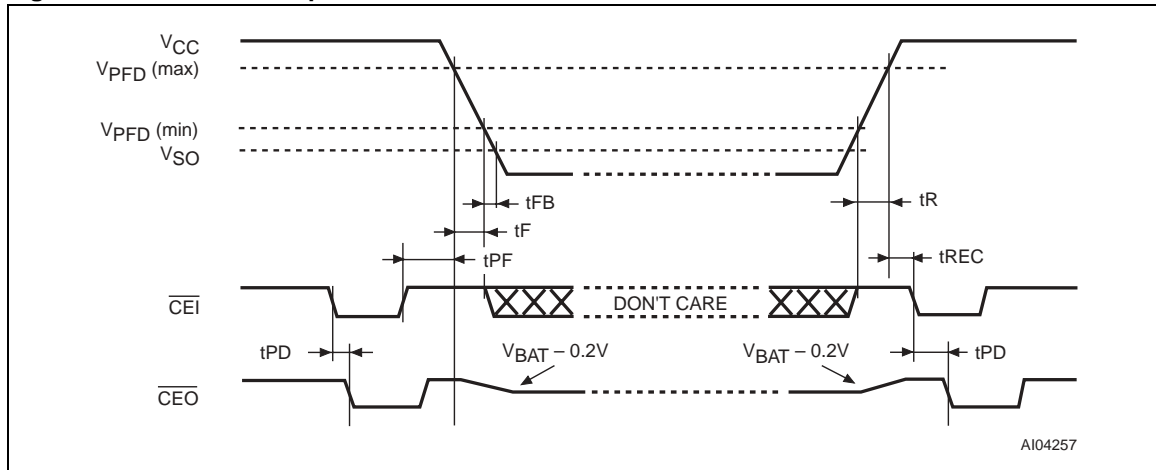


Table 11. Power Down/Up Trip Points DC Characteristics

| Symbol | Parameter ^(1,2) | Min | Max | Unit |
|----------------------------------|--|------------|-----|------|
| t _{REC} | V _{PF D} (max) to $\overline{\text{CEI}}$ low | 1.5 | 2.5 | ms |
| t _F | V _{PF D} (max) to V _{PF D} (min) V _{CC} Fall Time | 300 | | μs |
| t _{FB} | V _{PF D} (min) to V _{SO} V _{CC} Fall Time | 10 | | μs |
| t _R | V _{PF D} (min) to V _{PF D} (max) V _{CC} Rise Time | 0 | | μs |
| t _{PF} | $\overline{\text{CEI}}$ High to Power-Fail | 0 | | μs |
| t _{PD} ^(3,4) | $\overline{\text{CEI}}$ Propagation Delay | M41T315Y | 10 | ns |
| | | M41T315V/W | 15 | ns |

Note: 1. Valid for Ambient Operating Temperature: T_A = -40 to 85°C; V_{CC} = 4.5 to 5.5V or 2.7 to 3.6V (except where noted).

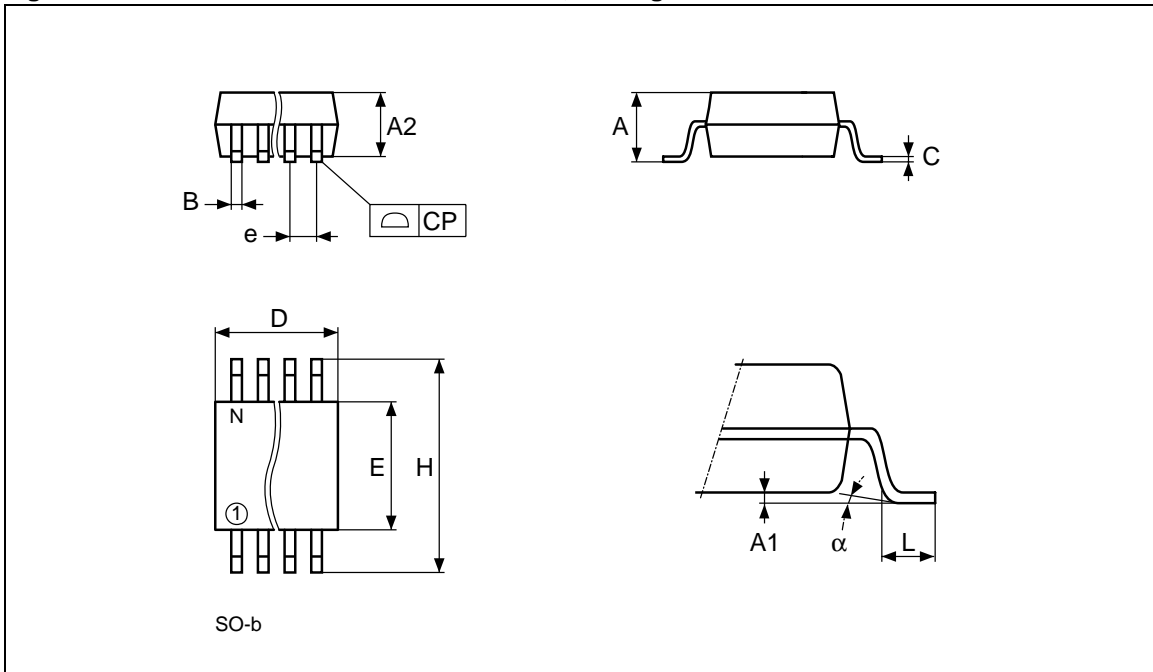
2. Measured at 25°C.

3. Measured with load shown in [Figure 12., page 15.](#)

4. Input pulse rise and fall times equal 10ns

PACKAGE MECHANICAL INFORMATION

Figure 14. SO16 – 16-lead Plastic Small Outline, Package Outline

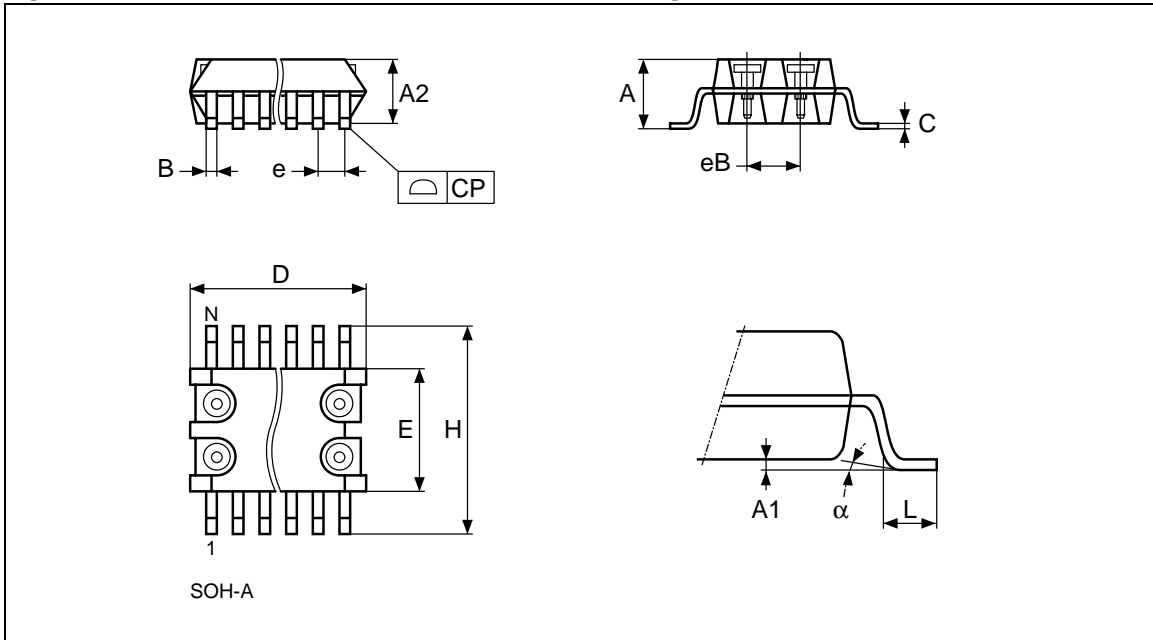


Note: Drawing is not to scale.

Table 12. SO16 – 16-lead Plastic Small Outline (150 mils body width), Package Mech. Data

| Symb | mm | | | inches | | |
|------|------|------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.75 | | | 0.069 |
| A1 | | 0.10 | 0.25 | | 0.004 | 0.010 |
| A2 | | | 1.60 | | | 0.063 |
| B | | 0.35 | 0.46 | | 0.014 | 0.018 |
| C | | 0.19 | 0.25 | | 0.007 | 0.010 |
| D | | 9.80 | 10.00 | | 0.386 | 0.394 |
| E | | 3.30 | 4.00 | | 0.150 | 0.158 |
| e | 1.27 | – | – | 0.050 | – | – |
| H | | 5.80 | 6.20 | | 0.228 | 0.244 |
| L | | 0.40 | 1.27 | | 0.016 | 0.050 |
| a | | 0° | 8° | | 0° | 8° |
| N | 16 | | | 16 | | |
| CP | | | 0.10 | | | 0.004 |

Figure 15. SOH28 – 28-lead Plastic Small Outline, Package Outline



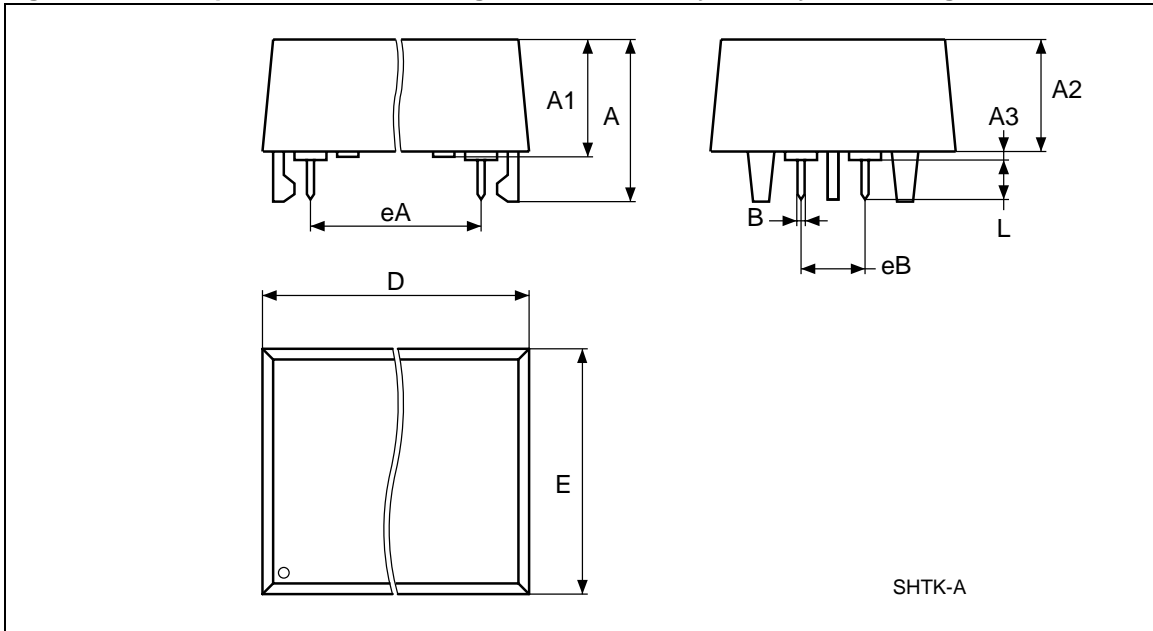
Note: Drawing is not to scale.

Table 13. SOH28 – 28-lead Plastic Small Outline, Package Mechanical Data

| Symb | mm | | | inches | | |
|------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 3.05 | | | 0.120 |
| A1 | | 0.05 | 0.36 | | 0.002 | 0.014 |
| A2 | | 2.34 | 2.69 | | 0.092 | 0.106 |
| B | | 0.36 | 0.51 | | 0.014 | 0.020 |
| C | | 0.15 | 0.32 | | 0.006 | 0.012 |
| D | | 17.71 | 18.49 | | 0.697 | 0.728 |
| E | | 8.23 | 8.89 | | 0.324 | 0.350 |
| e | 1.27 | – | – | 0.050 | – | – |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| H | | 11.51 | 12.70 | | 0.453 | 0.500 |
| L | | 0.41 | 1.27 | | 0.016 | 0.050 |
| a | | 0° | 8° | | 0° | 8° |
| N | | 28 | | | 28 | |
| CP | | | 0.10 | | | 0.004 |

M41T315Y*, M41T315V, M41T315W

Figure 16. SH – 4-pin SNAPHAT Housing for 48mAh Battery and Crystal, Package Outline

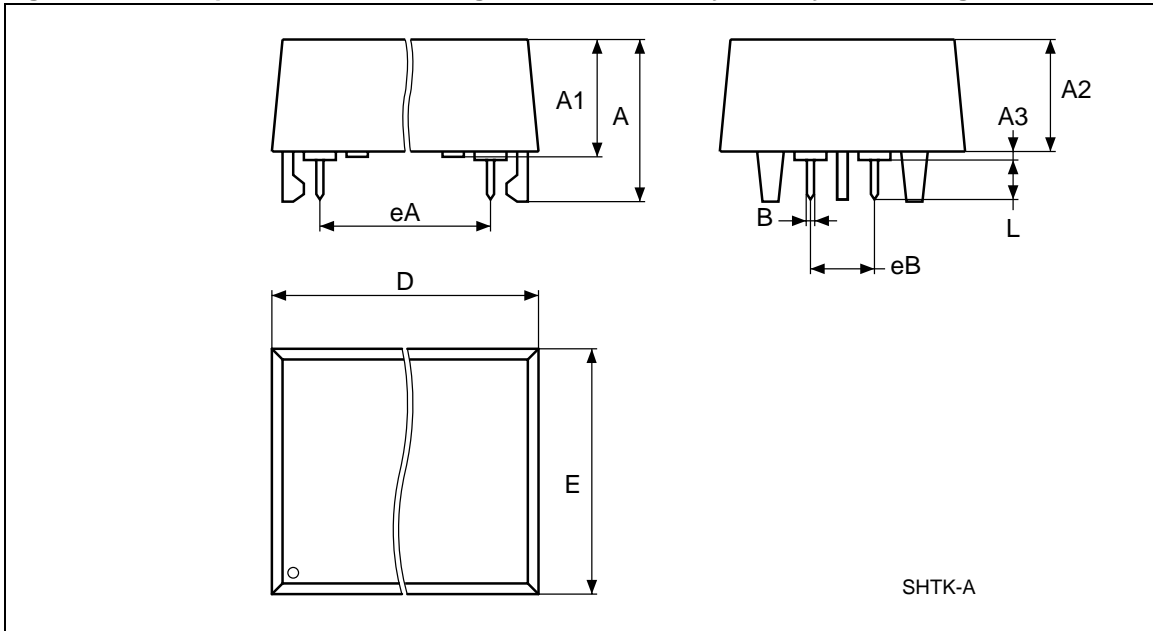


Note: Drawing is not to scale.

Table 14. SH – 4-pin SNAPHAT Housing for 48mAh Battery and Crystal, Package Mech. Data

| Symb | mm | | | inches | | |
|------|-----|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 9.78 | | 0 | 0.385 |
| A1 | | 6.73 | 7.24 | | 0.265 | 0.285 |
| A2 | | 6.48 | 6.99 | | 0.255 | 0.275 |
| A3 | | | 0.38 | | 0 | 0.015 |
| B | | 0.46 | 0.56 | | 0.018 | 0.022 |
| D | | 21.21 | 21.84 | | 0.835 | 0.860 |
| E | | 14.22 | 14.99 | | 0.560 | 0.590 |
| eA | | 15.55 | 15.95 | | .6122 | .6280 |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| L | | 2.03 | 2.29 | | 0.080 | 0.090 |

Figure 17. SH – 4-pin SNAPHAT Housing for 120mAh Battery and Crystal, Package Outline



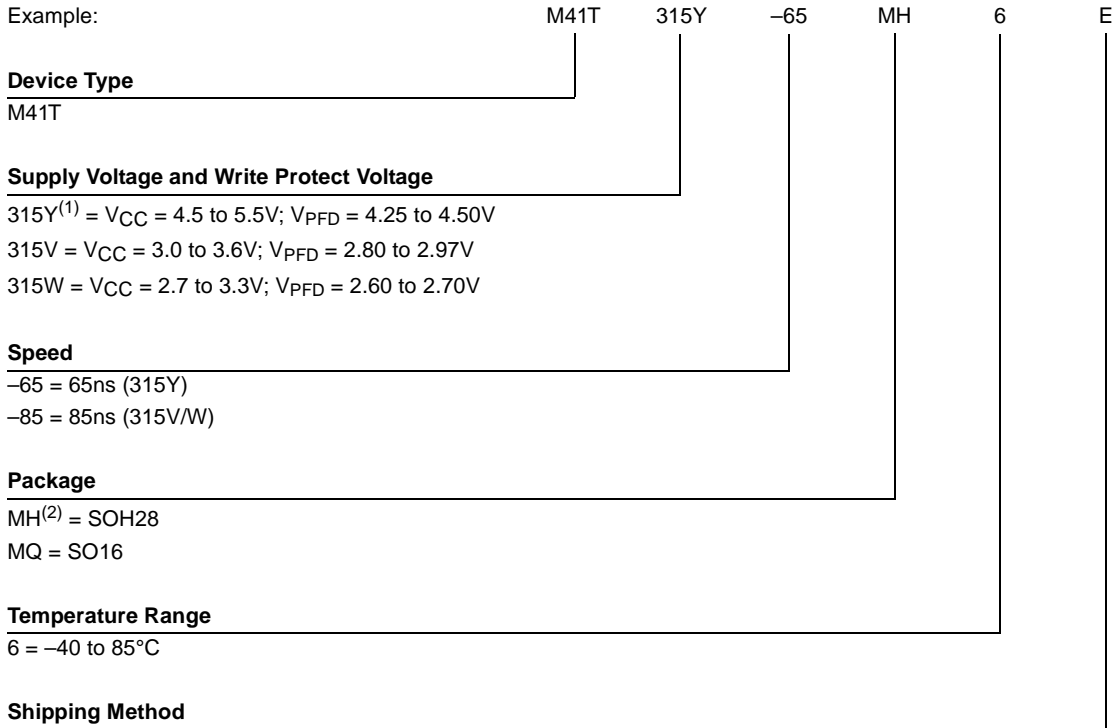
Note: Drawing is not to scale.

Table 15. SH – 4-pin SNAPHAT Housing for 120mAh Battery and Crystal, Package Mech. Data

| Symb | mm | | | inches | | |
|------|-----|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 10.54 | | 0 | 0.415 |
| A1 | | 8.00 | 8.51 | | 0.315 | 0.335 |
| A2 | | 7.24 | 8.00 | | 0.285 | 0.315 |
| A3 | | | 0.38 | | 0 | 0.015 |
| B | | 0.46 | 0.56 | | 0.018 | 0.022 |
| D | | 21.21 | 21.84 | | 0.835 | 0.860 |
| E | | 17.27 | 18.03 | | 0.680 | 0.710 |
| eA | | 15.55 | 15.95 | | .6122 | .6280 |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| L | | 2.03 | 2.29 | | 0.080 | 0.090 |

PART NUMBERING

Table 16. Ordering Information Scheme



Note: 1. Contact Local Sales Office
2. The SOIC package (SOH28) requires the SNAPHAT[®] battery package which is ordered separately under the part number "M4TXX-BR12SHX" in plastic tube or "M4TXX-BR12SHXTR" in Tape & Reel form (see Table 17).

Caution: Do not place the SNAPHAT battery package "M4TXX-BR12SH" in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

Table 17. SNAPHAT Battery Table

| Part Number | Description | Package |
|--------------|----------------------------------|---------|
| M4T28-BR12SH | Lithium Battery (48mAh) SNAPHAT | SH |
| M4T32-BR12SH | Lithium Battery (120mAh) SNAPHAT | SH |



REVISION HISTORY

Table 18. Document Revision History

| Date | Rev. # | Revision Details |
|-----------|--------|---|
| June 2001 | 1.0 | First Issue |
| 17-Jul-01 | 1.1 | Basic formatting changes |
| 18-Sep-01 | 1.2 | Changed pin 8 in 28-pin to V _{SS} |
| 27-Sep-01 | 1.3 | Added ambient temp to DC Characteristics table (Table 9) |
| 01-May-02 | 1.4 | Modify reflow time and temperature footnote (Table 6) |
| 04-Nov-02 | 1.5 | Modify Crystal Electrical Characteristics table footnotes (Table 10); add marketing status (Table 16) |
| 26-Mar-03 | 1.6 | Update test condition (Table 9) |
| 08-Jun-04 | 2.0 | Reformatted; add Lead-free information (Table 6, 16) |

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