# DATA SHEET

## 74LVC2373A
## 74LVCH2373A

Octal D-type transparent latch with 5-volt tolerant inputs/outputs; damping resistor (3-State)

Product specification

1997 Mar 12

IC24 Data Handbook

Philips
Semiconductors

PHILIPS

# Octal D-type transparent latch with 5-volt tolerant inputs/outputs; damping resistor (3-State)

# 74LVC2373A 74LVCH2373A

## FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when $V_{CC}$ = 0V
- Bushold on all data inputs (74LVCH2373A only)
- Integrated 30Ω damping resistor

## DESCRIPTION

The 74LVC2373A/74LVCH2373A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC2373A/74LVCH2373A is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '2373' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

## QUICK REFERENCE DATA

GND = 0V; $T_{amb}$ = 25°C; $t_r = t_f \leq 2.5$ ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>Dn to Qn<br>LE to Qn | $C_L$ = 50pF<br>$V_{CC}$ = 3.3V | <br>4.4<br>5.0 | ns |
| $C_I$ | Input capacitance | | 5.0 | pF |
| $C_{PD}$ | Power dissipation capacitance per latch | Notes 1, 2 | 20 | pF |

**NOTES:**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   $f_i$ = input frequency in MHz; $C_L$ = output load capacity in pF;
   $f_o$ = output frequency in MHz; $V_{CC}$ = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_I$ = GND to $V_{CC}$.

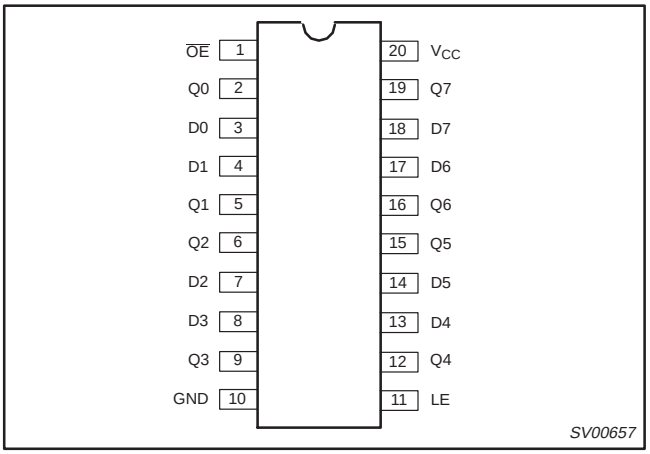
## ORDERING AND PACKAGE INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | PKG. DWG. # |
|---|---|---|---|---|
| 20-Pin Plastic SO | –40°C to +85°C | 74LVC2373A D | 74LVC2373A D | SOT163-1 |
| 20-Pin Plastic SSOP Type II | –40°C to +85°C | 74LVC2373A DB | 74LVC2373A DB | SOT339-1 |
| 20-Pin Plastic TSSOP Type I | –40°C to +85°C | 74LVC2373A PW | LVC2373APW DH | SOT360-1 |
| 20-Pin Plastic SO | –40°C to +85°C | 74LVCH2373A D | 74LVCH2373A D | SOT163-1 |
| 20-Pin Plastic SSOP Type II | –40°C to +85°C | 74LVCH2373A DB | 7LVCH2373A DB | SOT339-1 |
| 20-Pin Plastic TSSOP Type I | –40°C to +85°C | 74LVCH2373A PW | VCH2373APW DH | SOT360-1 |

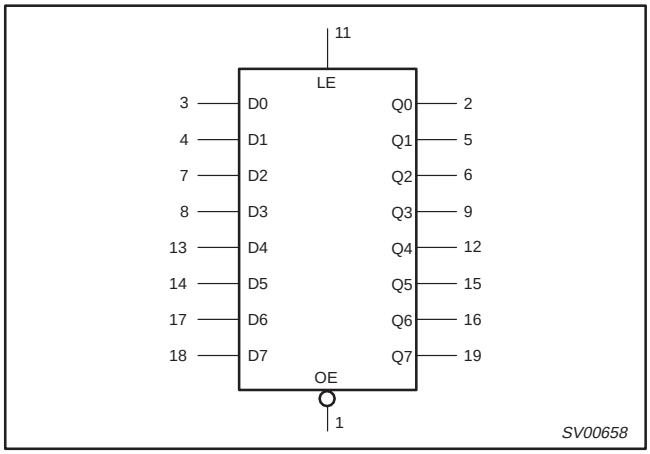
# Octal D-type transparent latch with 5-volt tolerant inputs/outputs; damping resistor (3-State)

74LVC2373A
74LVCH2373A

## PIN CONFIGURATION



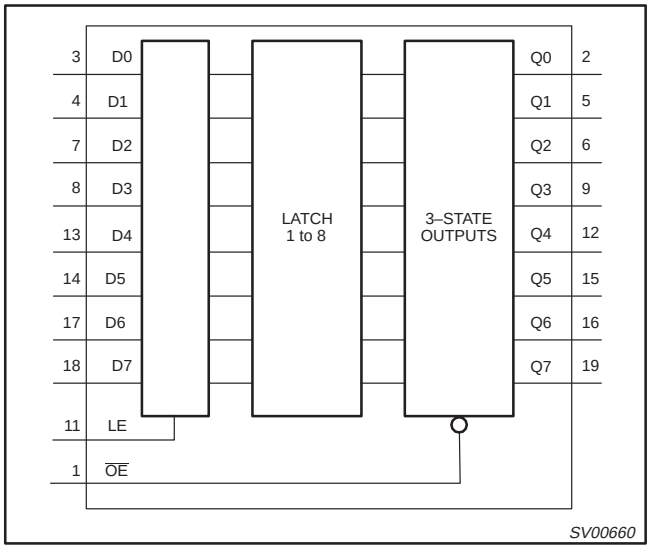

## LOGIC SYMBOL



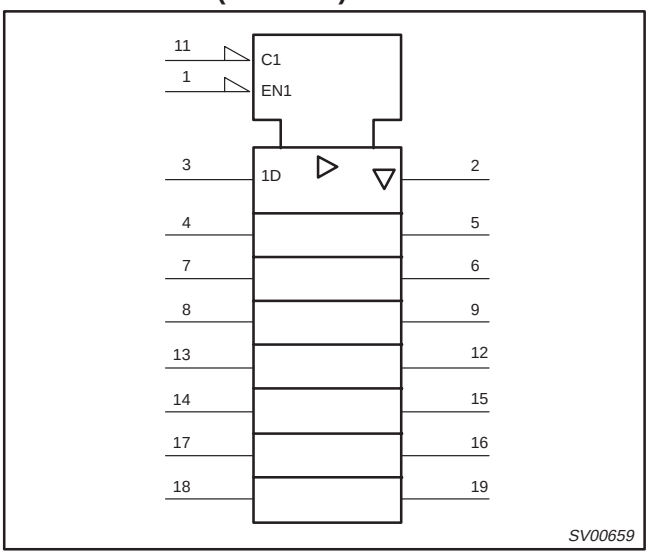

## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|---|---|---|
| 1 | $\overline{OE}$ | Output enable input (active LOW) |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q0–Q7 | 3-State latch outputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0–D7 | Data inputs |
| 10 | GND | Ground (0V) |
| 11 | LE | Latch enable input (active HIGH) |
| 20 | $V_{CC}$ | Positive supply voltage |

## FUNCTIONAL DIAGRAM




## LOGIC SYMBOL (IEEE/IEC)

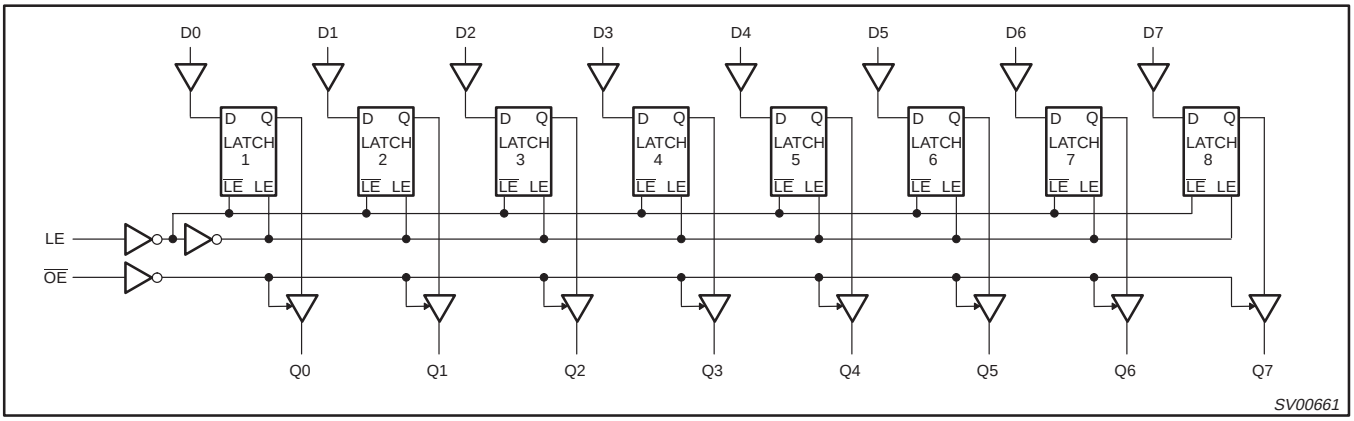



## FUNCTION TABLE

| OPERATING MODES | INPUTS | | | INTERNAL LATCHES | OUTPUTS |
|---|---|---|---|---|---|
| | $\overline{OE}$ | LE | Dn | | Q0 to Q7 |
| Enable and read register (transparent mode) | L<br>L | H<br>H | L<br>H | L<br>H | L<br>H |
| Latch and read register | L<br>L | L<br>L | l<br>h | L<br>H | L<br>H |
| Latch register and disable outputs | H<br>H | L<br>L | l<br>h | L<br>H | Z<br>Z |

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

## LOGIC DIAGRAM




## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | DC supply voltage (for max. speed performance) | | 2.7 | 3.6 | V |
| $V_{CC}$ | DC supply voltage (for low-voltage applications) | | 1.2 | 3.6 | V |
| $V_I$ | DC input voltage range | | 0 | 5.5 | V |
| $V_{I/O}$ | DC input voltage range for I/Os | | 0 | $V_{CC}$ | V |
| $V_O$ | DC output voltage range | | 0 | $V_{CC}$ | V |
| $T_{amb}$ | Operating free-air temperature range | | –40 | +85 | °C |
| $t_r$, $t_f$ | Input rise and fall times | $V_{CC}$ = 1.2 to 2.7V<br>$V_{CC}$ = 2.7 to 3.6V | 0<br>0 | 20<br>10 | ns/V |

## ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +6.5 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | –50 | mA |
| $V_I$ | DC input voltage | Note 2 | –0.5 to +5.5 | V |
| $V_{I/O}$ | DC input voltage range for I/Os | | –0.5 to $V_{CC}$ +0.5 | V |
| $I_{OK}$ | DC output diode current | $V_O > V_{CC}$ or $V_O < 0$ | ±50 | mA |
| $V_{OUT}$ | DC output voltage; output HIGH or LOW | Note 2 | –0.5 to $V_{CC}$ +0.5 | V |
| $V_{OUT}$ | DC output voltage; output 3-State | Note 2 | –0.5 to +6.5 | V |
| $I_{OUT}$ | DC output source or sink current | $V_O$ = 0 to $V_{CC}$ | ±50 | mA |
| $I_{GND}$, $I_{CC}$ | DC $V_{CC}$ or GND current | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –60 to +150 | °C |
| $P_{TOT}$ | Power dissipation per package<br>– plastic mini-pack (SO)<br>– plastic shrink mini-pack (SSOP and TSSOP) | <br>above +70°C derate linearly with 8 mW/K<br>above +60°C derate linearly with 5.5 mW/K | <br>500<br>500 | mW |

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP[1] | MAX | |
| $V_{IH}$ | HIGH level Input voltage | $V_{CC}$ = 1.2V | $V_{CC}$ | | | V |
| | | $V_{CC}$ = 2.7 to 3.6V | 2.0 | | | |
| $V_{IL}$ | LOW level Input voltage | $V_{CC}$ = 1.2V | | | GND | V |
| | | $V_{CC}$ = 2.7 to 3.6V | | | 0.8 | |
| $V_{OH}$ | HIGH level output voltage | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –100µA | $V_{CC}$ – 0.2 | $V_{CC}$ | | V |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –12mA | $V_{CC}$ – 0.6 | | | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –24mA | $V_{CC}$ – 1.0 | | | |
| $V_{OH}$ | HIGH level output voltage | $V_{CC}$ = 2.7V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –6mA[7] | $V_{CC}$ – 0.5 | | | V |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –100µA[7] | $V_{CC}$ – 0.2 | $V_{CC}$ | | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –12mA[7] | $V_{CC}$ – 0.8 | | | |
| $V_{OL}$ | LOW level output voltage | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 100µA | | GND | 0.20 | V |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 24mA | | | 0.55 | |
| $V_{OL}$ | LOW level output voltage | $V_{CC}$ = 2.7V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 6mA[7] | | | 0.40 | V |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 100µA[7] | | GND | 0.20 | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 12mA[7] | | | 0.55 | |
| $I_I$ | Input leakage current | $V_{CC}$ = 3.6V; $V_I$ = 5.5V or GND; Not for I/O pins | | ±0.1 | ±5 | µA |
| $I_{IHZ}/I_{ILZ}$ | Input current for common I/O pins | $V_{CC}$ = 3.6V; $V_I = V_{CC}$ or GND | | ±0.1 | ±15 | µA |
| $I_{OZ}$ | 3-State output OFF-state current | $V_{CC}$ = 3.6V; $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND | | 0.1 | ±10 | µA |
| $I_{CC}$ | Quiescent supply current | $V_{CC}$ = 3.6V; $V_I = V_{CC}$ or GND; $I_O$ = 0 | | 0.1 | 20 | µA |
| $\Delta I_{CC}$ | Additional quiescent supply current per input pin | $V_{CC}$ = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; $I_O$ = 0 | | 5 | 500 | µA |
| $I_{BHL}$ | Bushold LOW sustaining current[2, 3, 4] | $V_{CC}$ = 3.0V; $V_I$ =0.8V | 75 | – | – | µA |
| $I_{BHH}$ | Bushold HIGH sustaining current[2, 3, 4] | $V_{CC}$ = 3.0V; $V_I$ =2.0V | –75 | – | – | µA |
| $I_{BHLO}$ | Bushold LOW overdrive current[2, 3, 5] | $V_{CC}$ = 3.6V | 500 | – | – | µA |
| $I_{BHHO}$ | Bushold HIGH overdrive current[2, 3, 5] | $V_{CC}$ = 3.6V | –500 | – | – | µA |

**NOTES:**

1. All typical values are at $V_{CC}$ = 3.3V and $T_{amb}$ = 25°C.
2. Valid for data inputs of bushold parts (LVCH-A) only.
3. For data inputs only, control inputs do not have a bushold circuit.
4. The specified sustaining current at the data inputs do not have a bushold circuit.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bushold parts, the bushold circuit is switched off when $V_I$ exceeds $V_{CC}$ allowing 5.5V on the input terminal.
7. For data outputs of damping resistor parts only.

## AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3V ±0.3V | | | $V_{CC}$ = 2.7V | | $V_{CC}$ = 1.2V | |
| | | | MIN | TYP[1] | MAX | MIN | MAX | TYP | |
| $t_{PHL}/t_{PLH}$ | Propagation delay Dn to Qn | Figures 1, 5 | 1.5 | – | 8.5 | 1.5 | 9.5 | – | ns |
| $t_{PHL}/t_{PLH}$ | Propagation delay LE to Qn | Figures 2, 5 | 1.5 | – | 9.5 | 1.5 | 11 | – | ns |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time $\overline{OE}$ to Qn | Figures 3, 5 | 1.5 | – | 9.0 | 1.5 | 11 | – | ns |
| $t_{PHZ}/t_{PLZ}$ | 3-State output disble time $\overline{OE}$ to Qn | Figures 3, 5 | 1.5 | – | 6.0 | 1.5 | 6.5 | – | ns |
| $t_W$ | LE pulse width HIGH | Figure 2 | 4.0 | – | – | 4.0 | – | – | ns |
| $t_{su}$ | Set-up time Dn to LE | Figure 4 | 2.0 | – | – | 3.0 | – | – | ns |
| $t_h$ | Hold time Dn to LE | Figure 4 | 2.0 | – | – | 3.0 | – | – | ns |

**NOTE:**
1. These typical values are at $V_{CC}$ = 3.3V and $T_{amb}$ = 25°C.

## AC WAVEFORMS

$V_M$ = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M$ = 0.5 • $V_{CC}$ at $V_{CC}$ < 2.7 V
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 · $V_{CC}$ at $V_{CC}$ < 2.7 V
$V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ – 0.1 · $V_{CC}$ at $V_{CC}$ < 2.7 V

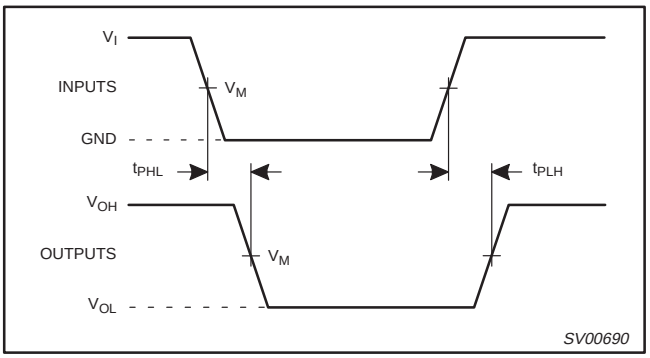



**Figure 1. nput (Dn) to output (Qn) propagation delays**

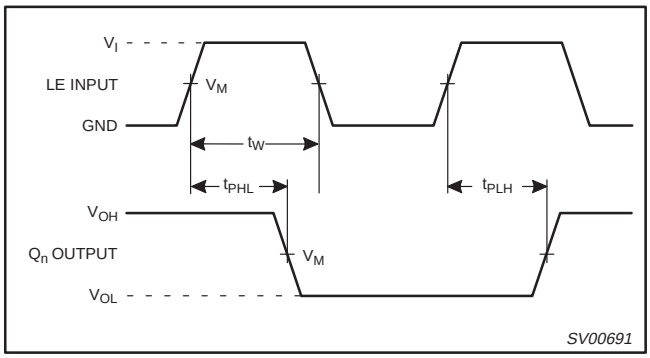



**Figure 2. Latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays**

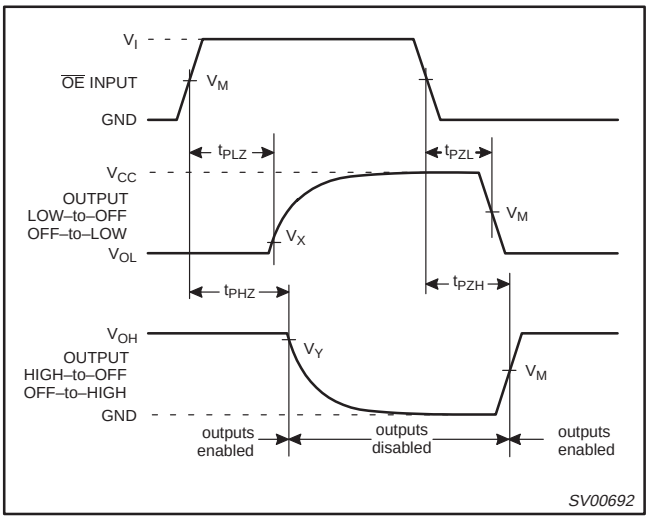



**Figure 3. 3-State enable and disable times**

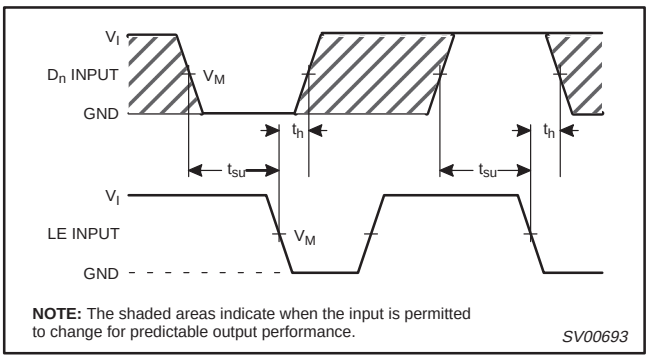
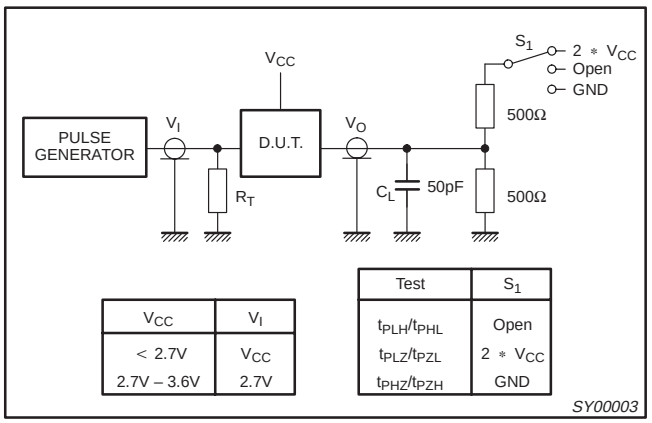



**Figure 4. Data set-up and hold times for the Dn input to the LE input**

## TEST CIRCUIT

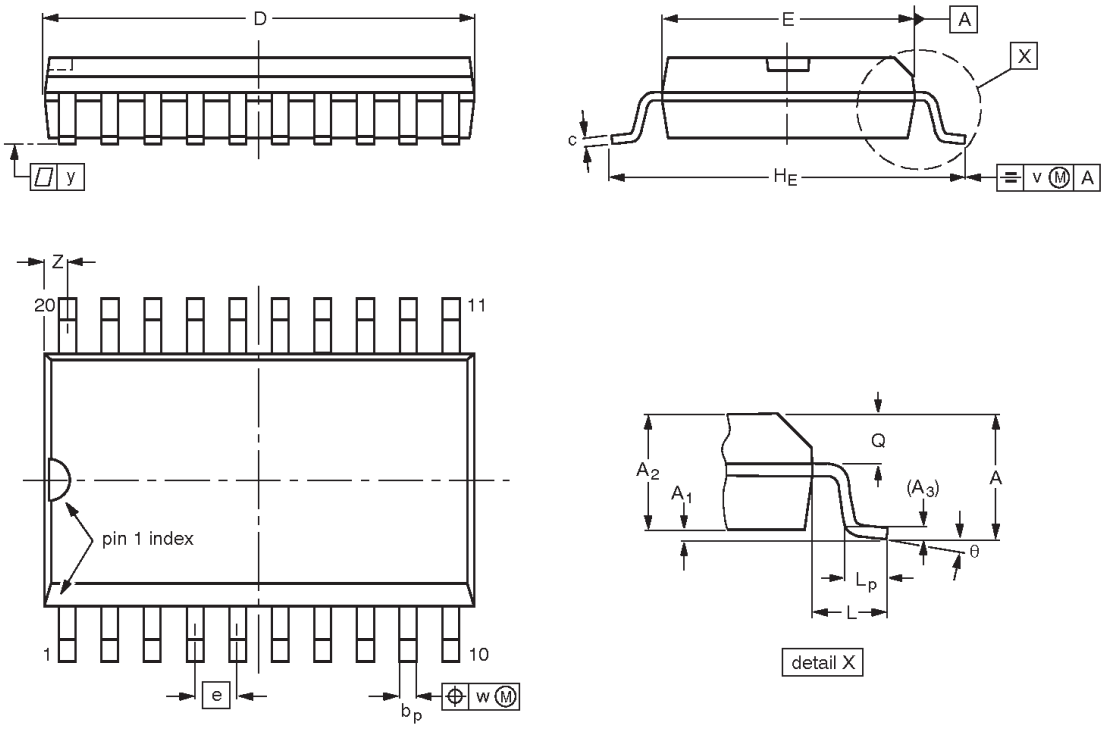


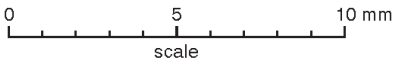

| VCC | VI |
|---|---|
| < 2.7V | VCC |
| 2.7V – 3.6V | 2.7V |

| Test | S1 |
|---|---|
| tPLH/tPHL | Open |
| tPLZ/tPZL | 2 * VCC |
| tPHZ/tPZH | GND |

**Figure 5. Load circuitry for switching times**

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

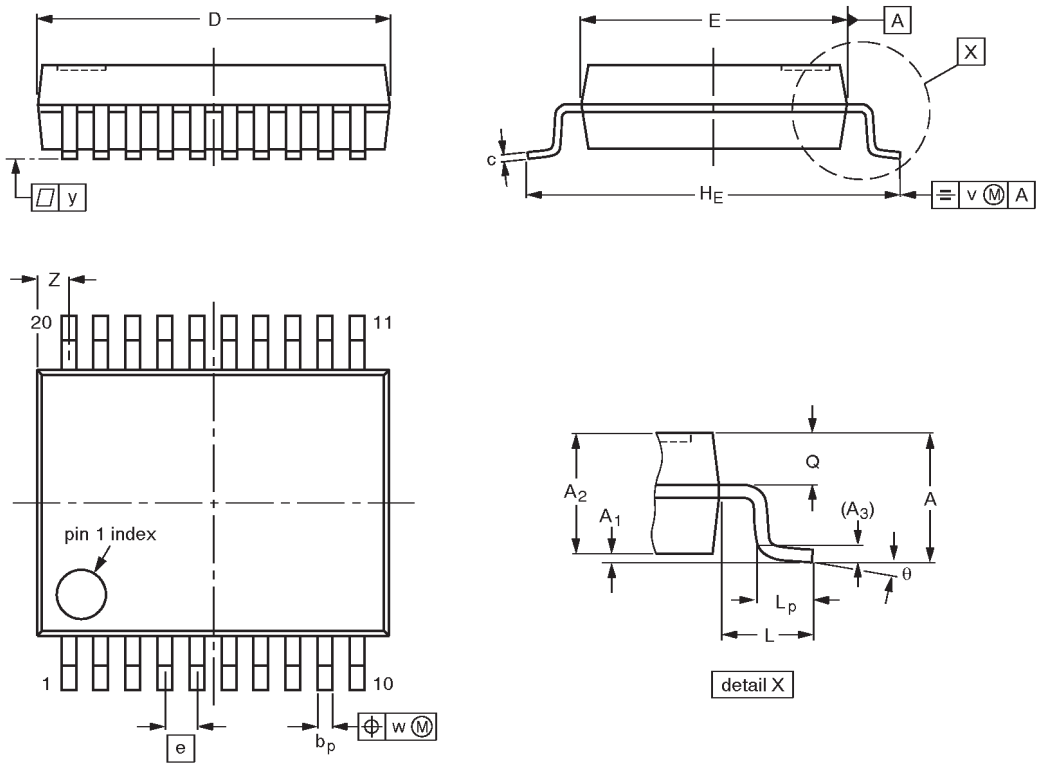
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.30<br>0.10 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.10 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.050 | 0.42<br>0.39 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT163-1 | 075E04 | MS-013AC | | | | ~~92-11-17~~<br>95-01-24 |

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm** **SOT339-1**




**DIMENSIONS (mm are the original dimensions)**

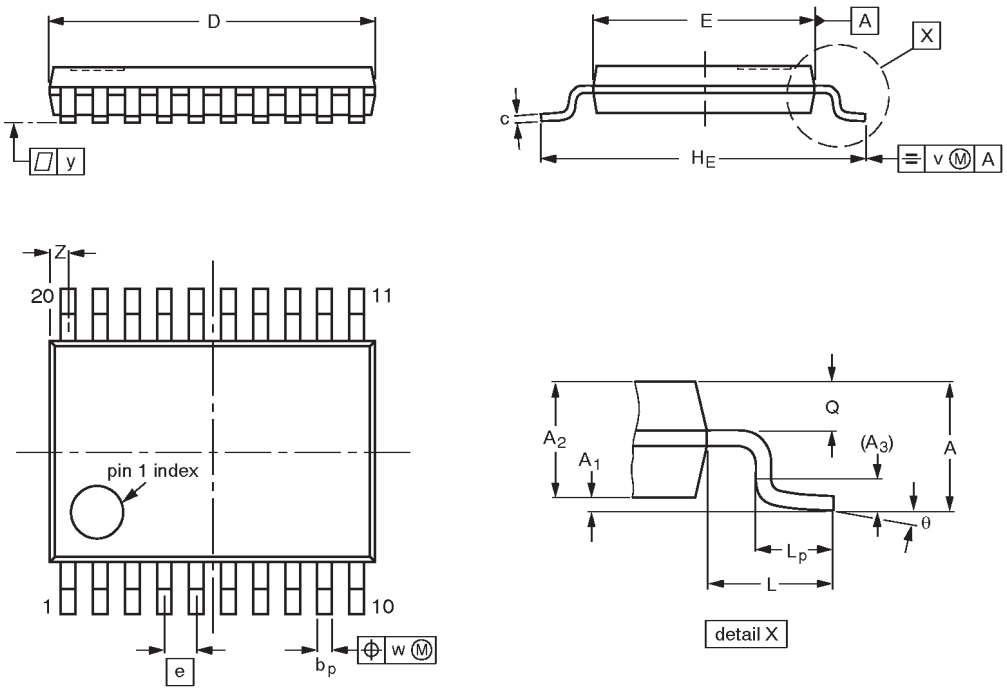
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.0 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 7.4<br>7.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 0.9<br>0.5 | 8°<br>0° |

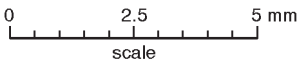
**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT339-1 | | MO-150AE | | | | ~~93-09-08~~<br>95-02-04 |

**TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm** **SOT360-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.10 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1.0 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT360-1 | | MO-153AC | | | | ~~93-06-16~~<br>95-02-04 |

**NOTES**

# Octal D-type transparent latch with 5-volt tolerant inputs/outputs; damping resistor (3-State)

74LVC2373A
74LVCH2373A

## DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| *Objective Specification* | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| *Preliminary Specification* | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| *Product Specification* | Full Production | This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product. |



**Philips Semiconductors**
**811 East Arques Avenue**
**P.O. Box 3409**
**Sunnyvale, California 94088–3409**
**Telephone 800-234-7381**



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