

DATA SHEET

PCF8833 STN RGB - 132 × 132 × 3 driver

Objective specification

2003 Feb 14

STN RGB - 132 × 132 × 3 driver**PCF8833**

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1 FEATURES

- Single chip LCD controller and driver
- 132 rows and 396 column outputs (132 × RGB)
- Low cross talk by Frame Rate Control (FRC)
- 4 kbyte colours (RGB) = 4 : 4 : 4 mode
- 256 colours (RGB) = 3 : 3 : 2 mode using the 209 kbit RAM and a Look-Up Table (LUT)
- 65 kbyte colours (RGB) = 5 : 6 : 5 mode using the 209 kbit RAM with dithering
- 8 colours Power-save mode
- Display data RAM 132 × 132 (RGB) (4 kbyte colour)
- Interfaces:
 - 3-line serial interface
 - 8-bit 8080 Intel CPU interface.
- Display features:
 - Area scrolling
 - 32-line partial Display mode
 - Software programmable colour depth mode
 - N-line inversion for low cross talk.
- On-chip:
 - Oscillator for display system, requires no external components (external clock also possible)
 - Generation of V_{LCD}
 - Segmented temperature compensation of V_{LCD} and frame frequency.
- Logic supply voltage range V_{DD1} to V_{SS1} :
 - 1.5 to 3.3 V.
- Analog supply voltage range for V_{LCD} generation V_{DD2} to V_{SS2} :
 - 2.4 to 4.5 V.
- Analog supply voltage range for reference voltage generation V_{DD3} to V_{SS1} :
 - 2.4 to 3.5 V.
- Display supply voltage range V_{LCD} to V_{SS1} :
 - 3.8 to 20 V.
- Low power consumption; suitable for battery operated systems
- CMOS compatible inputs
- Manufactured in silicon gate CMOS process
- Optimized layout for COF, Chip On Glass (COG) and Transformer Coupled Plasma (TCP) assembly.

2 GENERAL DESCRIPTION

The PCF8833 is a single chip low power CMOS LCD controller driver, designed to drive colour Super-Twisted Nematic (STN) displays of 132 rows and 132 RGB columns. All necessary functions for the display are provided in a single chip, including display RAM which has a capacity of 209 kbit (132 × 12-bit × 132). The PCF8833 uses the Multiple Row Addressing (MRA) driving technique in order to achieve the best optical performance at the lowest power consumption. The PCF8833 offers 2 types of microcontroller interfaces namely the 8080 system interface and the 3-line serial interface.

3 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|----------------|---------|-------------------------|---------|
| | NAME | DESCRIPTION | VERSION |
| PCF8833U/2DA/1 | – | chip with bumps in tray | – |

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4 BLOCK DIAGRAM

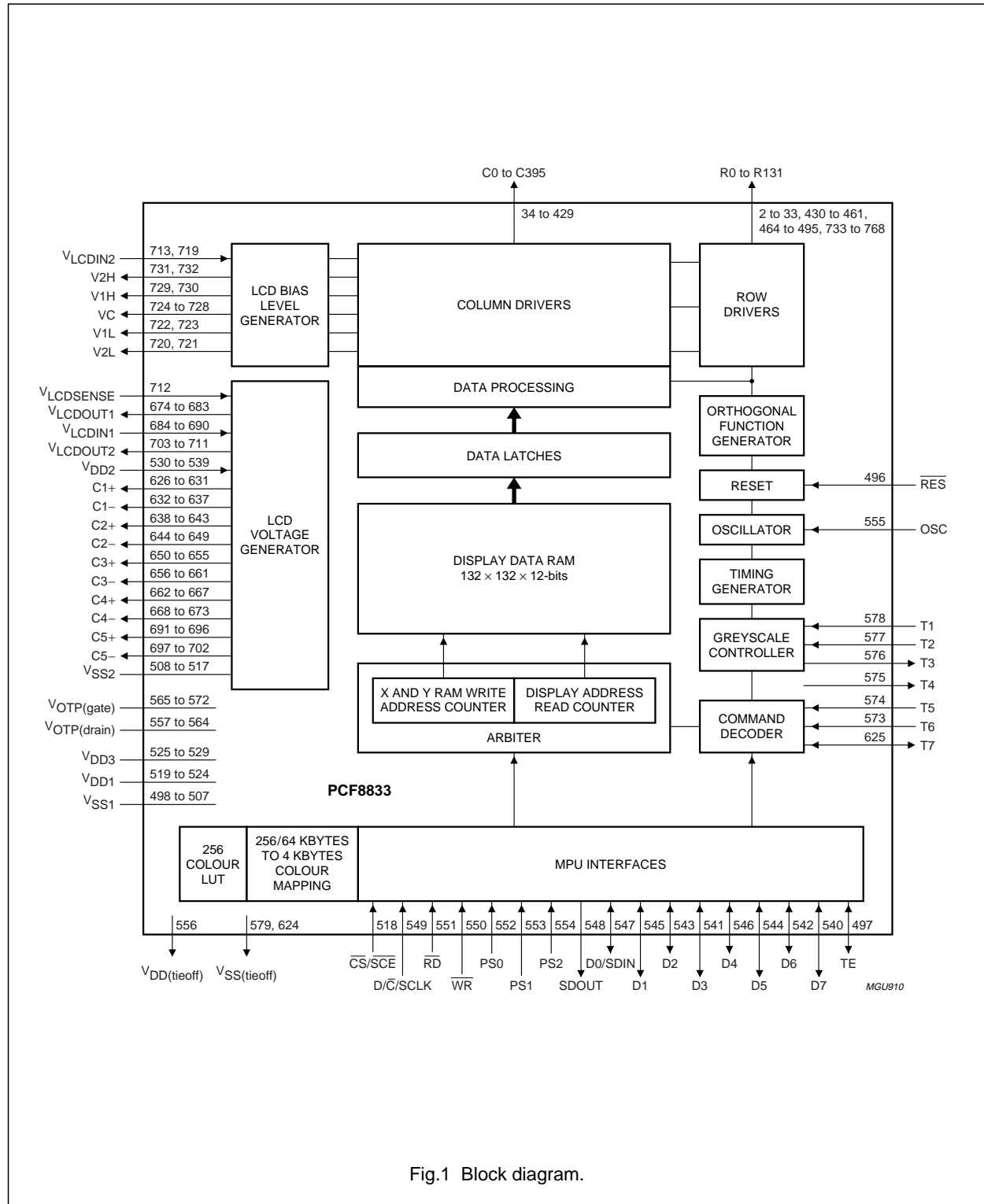


Fig.1 Block diagram.

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5 PINNING

| SYMBOL | PAD | TYPE | DESCRIPTION |
|------------------|------------|------|---|
| R95 to R64 | 2 to 33 | O | LCD row driver outputs |
| C0 to C395 | 34 to 429 | O | LCD column driver outputs |
| R0 to R31 | 430 to 461 | O | LCD row driver outputs |
| R63 to R32 | 464 to 495 | O | LCD row driver outputs |
| RES | 496 | I | external reset; this signal will reset the device and must be applied to properly initialize the chip (active LOW) |
| TE | 497 | O/I | tearing line (in Normal mode it is always an output) |
| V _{SS1} | 498 to 507 | PS | system ground |
| V _{SS2} | 508 to 517 | PS | system ground |
| CS/SCE | 518 | I | chip select parallel interface or serial chip enable (active LOW) |
| V _{DD1} | 519 to 524 | PS | logic supply voltage |
| V _{DD3} | 525 to 529 | PS | V _{DD2} and V _{DD3} are the supply voltage pins for the internal voltage generator including the temperature compensation circuits; V _{DD2} and V _{DD3} can be connected together but in this case care must be taken to respect the supply voltage range (see Chapter 13); V _{DD1} is used as the supply for the rest of the chip. V _{DD1} can be connected together with V _{DD2} and V _{DD3} but in this case care must also be taken to respect the supply voltage range; see Chapter 13. V _{DD2} and V _{DD3} must not be applied before V _{DD1} . If the internal voltage generator is not used, pins V _{DD2} and V _{DD3} must be connected to V _{DD1} . |
| V _{DD2} | 530 to 539 | PS | |
| D7 | 540 | I/O | 8-bit parallel data; in Serial mode tie to V _{SS1} or V _{DD1} |
| D3 | 541 | I/O | 8-bit parallel data; in Serial mode tie to V _{SS1} or V _{DD1} |
| D6 | 542 | I/O | 8-bit parallel data; in Serial mode tie to V _{SS1} or V _{DD1} |
| D2 | 543 | I/O | 8-bit parallel data; in Serial mode tie to V _{SS1} or V _{DD1} |
| D5 | 544 | I/O | 8-bit parallel data; in Serial mode tie to V _{SS1} or V _{DD1} |
| D1 | 545 | I/O | 8-bit parallel data; in Serial mode tie to V _{SS1} or V _{DD1} |
| D4 | 546 | I/O | 8-bit parallel data; in Serial mode tie to V _{SS1} or V _{DD1} |
| D0/SDIN | 547 | I/O | 8-bit parallel data or serial data input |
| SDOUT | 548 | O | serial data output; in Parallel mode tie to V _{DD1} , V _{SS1} or D0 |
| D/C/SCLK | 549 | I | data/command indicator parallel interface or serial clock |
| WR | 550 | I | write clock parallel interface; in Serial mode tie to V _{DD1} (active LOW) |
| RD | 551 | I | read clock parallel interface; in Serial mode tie to V _{DD1} (active LOW) |
| PS0 | 552 | I | set serial or parallel interface mode PS1 and PS2 must tied to either V _{SS1} or V _{DD1} |
| PS1 | 553 | I | set serial or parallel interface mode PS1 and PS2 must tied to either V _{SS1} or V _{DD1} |
| PS2 | 554 | I | set serial or parallel interface mode PS1 and PS2 must tied to either V _{SS1} or V _{DD1} |

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| SYMBOL | PAD | TYPE | DESCRIPTION |
|-------------------------|------------|------|--|
| OSC | 555 | I | oscillator input or external oscillator resistor connection; when the on-chip oscillator is used this input must be connected to V_{DD1} ; an external clock signal, if used, is connected to this input and the internal oscillator must be switched off with a software command; if the oscillator and external clock are all inhibited by connecting pin OSC to V_{SS1} , the display is not clocked and may be left in a DC state; to avoid this the chip should always be put into Power-down mode before stopping the clock. |
| $V_{DD}(\text{tieoff})$ | 556 | O | can be used to tie inputs to V_{DD1} |
| $V_{OTP}(\text{drain})$ | 557 to 564 | PS | supply voltage for OTP programming (write voltage), in Application mode must be tied to V_{SS1} or left open-circuit |
| $V_{OTP}(\text{gate})$ | 565 to 572 | PS | supply voltage for OTP programming, in Application mode must be tied to V_{SS1} or left open-circuit |
| T6 | 573 | I | test pin; not accessible to user; must be connected to V_{SS1} |
| T5 | 574 | I | test pin; not accessible to user; must be connected to V_{SS1} |
| T4 | 575 | O | test pin; not accessible to user; must be left open-circuit |
| T3 | 576 | O | test pin; not accessible to user; must be left open-circuit |
| T2 | 577 | I/O | test pin; not accessible to user; must be also connected to V_{SS1} |
| T1 | 578 | I/O | test pin; not accessible to user; must be also connected to V_{SS1} |
| $V_{SS}(\text{tieoff})$ | 579 | O | can be used to tie inputs to V_{SS1} |
| $V_{SS}(\text{tieoff})$ | 624 | O | can be used to tie inputs to V_{SS1} |
| T7 | 625 | I/O | test pin; not accessible to user; must be connected to V_{SS1} |
| C1+ | 626 to 631 | I | positive input pump capacitor voltage multiplier 1 |
| C1- | 632 to 637 | I | negative input pump capacitor voltage multiplier 1 |
| C2+ | 638 to 643 | I | positive input pump capacitor voltage multiplier 1 |
| C2- | 644 to 649 | I | negative input pump capacitor voltage multiplier 1 |
| C3+ | 650 to 655 | I | positive input pump capacitor voltage multiplier 1 |
| C3- | 656 to 661 | I | negative input pump capacitor voltage multiplier 1 |
| C4+ | 662 to 667 | I | positive input pump capacitor voltage multiplier 1 |
| C4- | 668 to 673 | I | negative input pump capacitor voltage multiplier 1 |
| $V_{LCDOUT1}$ | 674 to 683 | O | output voltage multiplier 1 |
| V_{LCDIN1} | 684 to 690 | PS | LCD supply input voltage 1 |
| C5+ | 691 to 696 | I | positive input pump capacitor voltage multiplier 2 |
| C5- | 697 to 702 | I | negative input pump capacitor voltage multiplier 2 |
| $V_{LCDOUT2}$ | 703 to 711 | O | output voltage multiplier 2 |
| $V_{LCDSENSE}$ | 712 | I | voltage multiplier regulation input; must be connected to $V_{LCDOUT2}$ |
| V_{LCDIN2} | 713 to 719 | PS | LCD supply input voltage 2 |
| V2L | 720, 721 | O | LCD bias level |
| V1L | 722, 723 | O | LCD bias level |
| VC | 724 to 728 | O | LCD bias level |
| V1H | 729, 730 | O | LCD bias level |

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| SYMBOL | PAD | TYPE | DESCRIPTION |
|-------------|------------------------------------|------|------------------------|
| V2H | 731, 732 | O | LCD bias level |
| R96 to R131 | 733 to 768 | O | LCD row driver outputs |
| Dummy | 1, 462, 463, 580 to 623, 769 | | |

6 INSTRUCTIONS

The PCF8833 communicates with the host using an 8-bit parallel interface or a 3-line serial interface. Processing of instructions and data sent to the interface do not require the display clock. The display clock and interface clock are independent from each other. The display clock is derived from the built-in oscillator.

The PCF8833 has 2 types of accesses; those defining the operating mode of the device (instructions) and those filling the display RAM. Since writing to the RAM occurs more frequently, efficient data transfer is achieved by autoincrementing the RAM address pointers.

There are 3 types of instructions:

1. For defining display configuration
2. For setting X and Y addresses
3. Miscellaneous.

Commands in the range of 00H to AFH not defined in Table 1 and command DDH have the same effect as no operation (NOP).

All commands in range B0H to B9H and DEH to FFH are forbidden.

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Table 1 Command table; note 1

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT | OTP | DESCRIPTION | SECTION |
|-----|-------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|---------|-----|---------------------------------------|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | – | no operation (NOP) | 6.2.1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01H | – | software reset (SWRESET) | 6.2.3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02H | – | booster voltage off (BSTROFF) | 6.2.4 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03H | – | booster voltage on (BSTRON) | 6.2.5 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04H | – | read display identification (RDDIDIF) | 6.2.6 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09H | – | read display status (RDDST) | 6.2.7 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10H | – | Sleep_IN | 6.2.8 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11H | – | Sleep_OUT | 6.2.9 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12H | – | Partial mode on (PTLON) | 6.2.10 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13H | – | normal Display mode on (NORON) | 6.2.11 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20H | – | display inversion off (INVOFF) | 6.2.12 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21H | – | display inversion on (INVON) | 6.2.13 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22H | – | all pixel off (DALO) | 6.2.14 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23H | – | all pixel on (DAL) | 6.2.15 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 25H | – | set contrast (SETCON) | 6.2.16 |
| 1 | X | VCON ₆ | VCON ₅ | VCON ₄ | VCON ₃ | VCON ₂ | VCON ₁ | VCON ₀ | 00H | – | set contrast | 6.2.16 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28H | – | display off (DISPOFF) | 6.2.17 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29H | – | display on (DISPON) | 6.2.18 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2AH | – | column address set (CASET) | 6.2.19 |
| 1 | xs[7] | xs[6] | xs[5] | xs[4] | xs[3] | xs[2] | xs[1] | xs[0] | 02H | – | X address start; 0 ≤ xs ≤ 83H | 6.2.19 |
| 1 | xe[7] | xe[6] | xe[5] | xe[4] | xe[3] | xe[2] | xe[1] | xe[0] | 81H | – | X address end; xs ≤ xe ≤ 83H | 6.2.19 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2BH | – | page address set (PASET) | 6.2.20 |
| 1 | ys[7] | ys[6] | ys[5] | ys[4] | ys[3] | ys[2] | ys[1] | ys[0] | 02H | – | Y address start; 0 ≤ ys ≤ 83H | 6.2.20 |
| 1 | ye[7] | ye[6] | ye[5] | ye[4] | ye[3] | ye[2] | ye[1] | ye[0] | 81H | – | Y address end; ys ≤ ye ≤ 83H | 6.2.20 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2CH | – | memory write (RAMWR) | 6.2.21 |
| 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXH | – | write data | 6.2.21 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2DH | – | colour set (RGBSET) | 6.2.22 |
| 1 | X | X | X | X | R3 | R2 | R1 | R0 | 00H | – | red tone 000 | 6.2.22 |
| 1 | 6 bytes for 6 red tones | | | | | | | | | – | 6 red tones | 6.2.22 |

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| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT | OTP | DESCRIPTION | SECTION |
|-----|---------------------------|-----------------|-----------------|------------------|------------------|------------------|------------------|------------------|---------|------------------|--------------------------------------|---------|
| 1 | X | X | X | X | R3 | R2 | R1 | R0 | 0FH | – | red tone 111 | 6.2.22 |
| 1 | X | X | X | X | G3 | G2 | G1 | G0 | 00H | – | green tone 000 | 6.2.22 |
| 1 | 6 bytes for 6 green tones | | | | | | | | | – | 6 green tones | 6.2.22 |
| 1 | X | X | X | X | G3 | G2 | G1 | G0 | 0FH | – | green tone 111 | 6.2.22 |
| 1 | X | X | X | X | B3 | B2 | B1 | B0 | 00H | – | blue tone 00 | 6.2.22 |
| 1 | 2 bytes for 2 blue tones | | | | | | | | | – | 2 blue tones | 6.2.22 |
| 1 | X | X | X | X | B3 | B2 | B1 | B0 | 0FH | – | blue tone 11 | 6.2.22 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30H | – | partial area (PTLAR) | 6.2.23 |
| 1 | AA1S7 | AA1S6 | AA1S5 | AA1S4 | AA1S3 | AA1S2 | AA1S1 | AA1S0 | 00H | – | PTLAR active area start address | 6.2.23 |
| 1 | AA1E7 | AA1E6 | AA1E5 | AA1E4 | AA1E3 | AA1E2 | AA1E1 | AA1E0 | 1FH | – | PTLAR active area end address | 6.2.23 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33H | – | vertical scroll definition (VSCRDEF) | 6.2.24 |
| 1 | TF ₇ | TF ₆ | TF ₅ | TF ₄ | TF ₃ | TF ₂ | TF ₁ | TF ₀ | 00H | – | top fixed area | 6.2.24 |
| 1 | SA ₇ | SA ₆ | SA ₅ | SA ₄ | SA ₃ | SA ₂ | SA ₁ | SA ₀ | 82H | – | scroll area | 6.2.24 |
| 1 | BF ₇ | BF ₆ | BF ₅ | BF ₄ | BF ₃ | BF ₂ | BF ₁ | BF ₀ | 00H | – | bottom fixed area | 6.2.24 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34H | – | tearing line off (TEOFF) | 6.2.25 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35H | – | tearing line on (TEON) | 6.2.26 |
| 1 | X | X | X | X | X | X | X | X | 00H | – | | 6.2.26 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36H | – | memory data access control (MADCTL) | 6.2.27 |
| 1 | MY | MX | V | LAO | RGB | X | X | X | 00H | – | RAM data addressing/data control | 6.2.27 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37H | – | set Scroll Entry Point (SEP) | 6.2.24 |
| 1 | SEP7 | SEP6 | SEP5 | SEP4 | SEP3 | SEP2 | SEP1 | SEP0 | 00H | – | scroll entry point | 6.2.24 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38H | – | Idle mode off (IDMOFF) | 6.2.28 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39H | – | Idle mode on (IDMON) | 6.2.29 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3AH | – | interface pixel format (COLMOD) | 6.2.30 |
| 1 | X | X | X | X | X | P2 | P1 | P0 | 03H | – | colour interface format | 6.2.30 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0H | x ⁽²⁾ | set V _{OP} (SETVOP) | 6.2.31 |
| 1 | X | X | X | X | VPR ₈ | VPR ₇ | VPR ₆ | VPR ₅ | 08H | x | V _{OP} | 6.2.31 |
| 1 | X | X | X | VPR ₄ | VPR ₃ | VPR ₂ | VPR ₁ | VPR ₀ | 01H | x | V _{OP} | 6.2.31 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | BRS | B4H | x | Bottom Row Swap (BRS) | 6.2.32 |

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| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT | OTP | DESCRIPTION | SECTION |
|-----|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|---------|-----|---|---------|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | TRS | B6H | x | Top Row Swap (TRS) | 6.2.33 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | FINV | B9H | – | super Frame INVersion (FINV) | 6.2.34 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | DOR | BAH | – | Data ORder (DOR) | 6.2.35 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | TCDFE | BDH | – | enable/disable DF temp comp (TCDFE) | 6.2.36 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | TCVOPE | BFH | – | enable or disable V _{OP} temp comp (TCVOPE) | 6.2.37 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | EC | C0H | – | Internal or external oscillator (EC) | 6.2.38 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2H | x | set multiplication factor (SETMUL) | 6.2.39 |
| 1 | X | X | X | X | X | X | S1 | S0 | 03H | x | multiplication factor | 6.2.39 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C3H | x | set TC _{VOP} slopes A and B (TC _{VOPAB}) | 6.2.40 |
| 1 | X | SLB ₂ | SLB ₁ | SLB ₀ | X | SLA ₂ | SLA ₁ | SLA ₀ | 34H | x | | 6.2.40 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | C4H | x | set TC _{VOP} slopes C and D (TC _{VOPCD}) | 6.2.40 |
| 1 | X | SLD ₂ | SLD ₁ | SLD ₀ | X | SLC ₂ | SLC ₁ | SLC ₀ | 75H | x | | 6.2.40 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | C5H | x | set divider frequency (TCDF) | 6.2.41 |
| 1 | X | DFA ₆ | DFA ₅ | DFA ₄ | DFA ₃ | DFA ₂ | DFA ₁ | DFA ₀ | 56H | x | set divider factor in region A | 6.2.41 |
| 1 | X | DFB ₆ | DFB ₅ | DFB ₄ | DFB ₃ | DFB ₂ | DFB ₁ | DFB ₀ | 35H | x | set divider factor in region B | 6.2.41 |
| 1 | X | DFC ₆ | DFC ₅ | DFC ₄ | DFC ₃ | DFC ₂ | DFC ₁ | DFC ₀ | 30H | x | set divider factor in region C | 6.2.41 |
| 1 | X | DFD ₆ | DFD ₅ | DFD ₄ | DFD ₃ | DFD ₂ | DFD ₁ | DFD ₀ | 25H | x | set divider factor in region D | 6.2.41 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | C6H | x | set divider frequency 8-colour mode (DF8colour) | 6.2.42 |
| 1 | X | DF8 ₆ | DF8 ₅ | DF8 ₄ | DF8 ₃ | DF8 ₂ | DF8 ₁ | DF8 ₀ | 35H | x | set divider factor in 8-colour mode | 6.2.42 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | C7H | x | set bias system (SETBS) | 6.2.43 |
| 1 | X | X | X | X | VB ₃ | VB ₂ | VB ₁ | VB ₀ | 0BH | x | bias systems | 6.2.43 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | C8H | – | temperature read back (RDTEMP) | 6.2.44 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | C9H | – | N-Line Inversion (NLI) | 6.2.45 |
| 1 | NLI ₇ | NLI ₆ | NLI ₅ | NLI ₄ | NLI ₃ | NLI ₂ | NLI ₁ | NLI ₀ | 13H | x | after NLI time slots inversion | 6.2.45 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DAH | x | read ID1 (RDID1) | 6.2.46 |

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| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT | OTP | DESCRIPTION | SECTION |
|-----|-----|-----|------------------|------------------|------------------|-----|-----|-------|---------|-----|---|---------|
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DBH | x | read ID2 (RDID2) | 6.2.46 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DCH | x | read ID3 (RDID3) | 6.2.46 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | SFD | EFH | x | select factory defaults ⁽³⁾ | 6.2.47 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F0H | – | enter Calibration mode | 15.5 |
| 1 | X | X | ORA ₂ | ORA ₁ | ORA ₀ | X | OPE | CALMM | 00H | – | set calibration control settings | 15.5 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | F1H | – | shift data in OTP shift registers (OTPSHTIN) | 15.5 |
| 1 | OS7 | OS6 | OS5 | OS4 | OS3 | OS2 | OS1 | OS0 | XX | – | multiple data byte; any number of bytes allowed | 15.5 |

Notes

1. X = don't care.
2. This function can be set by OTP.
3. If the OTP bit Enable Factory Defaults (EFD) has been programmed to logic 1 (default value is logic 0), then the Set Factory Defaults (SFD) instruction is ignored and the device will always use the OTP default data.

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6.1 Exit commands

Table 2 Command description

| INPUT COMMAND | PARAMETERS | CONDITIONS | EXIT COMMAND |
|--------------------|---|---|---|
| Sleep_IN (SLPIN) | Power-down mode: display off display voltage generation off | power-down has priority over display and booster settings, but the setting is kept | Sleep_OUT |
| Sleep_OUT (SLPOUT) | exit power-down: display → DISPON/DISPOFF display voltage generation → BSTRON/BSTROFF (refresh from OTP cells if CALMM = 0) | after reset; BSTRON and DISPON is set, but become active only with Sleep_OUT | Sleep_IN reset |
| BSTROFF | display voltage generation off | display is switched on or off by DISPON/DISPOFF | BSTRON reset |
| BSTRON | display voltage generation on | display is switched on or off by DISPON/DISPOFF | BSTROFF |
| DISPOFF | display off | rows and columns are tied to V _{SS1} | DISPON reset |
| DISPON | display on | | DISPOFF |
| NORON | Normal mode on | full display is driven by RAM data | PTLON SEP |
| PTLON | Partial mode on | partial display area is driven by RAM data; display area outside partial area is off | NORON SEP reset |
| SEP | Scroll mode on | | NORON PTLON reset |
| PIXON (DAL) | in full Display mode (NORON) all pixels are on; in partial Display mode only partial area pixels are driven on; pixels outside partial area are off | command INVON is not effective when DAL is active | PIXOFF (DALO) NORON PTLON SEP reset |
| PIXOFF (DALO) | all pixel off | command INVON is not effective when DALO is active | PIXON (DAL) NORON PTLON SEP reset |
| IDMOFF | Idle mode off | full colour resolution stored in the RAM is written to the display | IDMON |
| IDMON | Idle mode on | 8-colour mode became active: The MSB of data stored in RAM is evaluated only | IDMOFF reset |
| INVOFF | inverted display off | | INVON |
| INVON | inverted display on | in Partial mode only pixels of partial area are inverted; INVON is not effective; when DAL or DALO are active | INVOFF reset |
| TEOFF | tearing pulse disabled | | TEON |
| TEON | tearing pulse enabled | | TEOFF reset |

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6.2 Function set**6.2.1 NO OPERATION**

No operation (NOP) has no effect on internal data or settings. However, it can be used to terminate data transfer (read and write).

Table 3 No operation command bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H |

6.2.2 RESET

The PCF8833 has a hardware and a software reset. After power-up a hardware reset (pin RES) must be applied; see Fig.50. The hardware and software resets give the same results. After a reset, the chip has the following state:

- All LCD outputs are set to V_{SS} (display off)
- RAM data unchanged
- Power-down mode (Sleep_IN)
- Command register set to default states; see Table 4
- Interface pins are set to inputs.

After a reset, care must be taken with respect to the reset timing constraints (see Fig.50) when the PCF8833 is powered-up. The power-up must be done by sending the Sleep_OUT command.

After a power-up the display RAM content is undefined. Neither a hardware reset nor a software reset changes the data that is stored in the display RAM. Sending display data must stop 160 ns before issuing a hardware reset, otherwise the last word written to the display RAM may be corrupted. The row and column outputs are tied to V_{SS1} with a reset because power-down (Sleep_IN) is in the reset state.

Table 4 Reset state after hardware and software reset

| COMMAND | DESCRIPTION | RESET STATE |
|----------|--|-------------|
| Sleep_IN | PCF8833 is in Sleep_IN mode (booster and display are switched off) | – |
| INVOFF | display inversion is off | – |
| BSTRON | when Sleep_OUT is active; booster is switched on | – |
| DISPON | when Sleep_OUT is active; display is turned on | – |
| TEOFF | tearing effect line pulse is turned off | – |
| IDMOFF | Idle mode is turned off (4 kbyte colour mode, not 8-colour mode) | – |
| NORON | Normal mode is active, not Scroll or Partial mode | – |
| V | RAM write in X direction | 0 |
| MY | no mirror Y | 0 |
| RGB | colour order is RGB | 0 |
| MX | no mirror X | 0 |
| LAO | line address order (top to bottom) | 0 |
| BRS | bottom rows are not mirrored; note 1 | 0 |
| TRS | top rows are not mirrored; note 1 | 0 |
| FINV | super frame inversion is on | 1 |
| DOR | normal data order | 0 |
| TCDFE | DF temperature compensation switched on | 1 |
| TCVOPE | VOP temperature compensation switched on | 1 |
| EC | internal oscillator | 0 |

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| COMMAND | DESCRIPTION | RESET STATE |
|-----------|---|--------------------|
| xs[7:0] | x address start | 2DEC |
| xe[7:0] | x address end | 129DEC |
| ys[7:0] | y address start | 2DEC |
| ye[7:0] | y address end | 129DEC |
| RGBSET | 256 to 4 kbyte colour LUT | see Section 6.2.22 |
| AA1S[7:0] | partial area start address | 0DEC |
| AA1E[7:0] | partial area end address | 31DEC |
| TF[7:0] | top fixed area | 0DEC |
| SA[7:0] | scroll area | 130DEC |
| BF[7:0] | bottom fixed area | 0DEC |
| SEP[7:0] | scroll entry point | 0DEC |
| P[2:0] | interface pixel format is 12-bit/pixel | 011 |
| VPR[8:0] | programming of V_{LCD2} voltage; note 1 | 257DEC |
| S[1:0] | charge pump multiplication factor; note 1 | 11 |
| SLA[2:0] | select slope for segment A; note 1 | 100 |
| SLB[2:0] | select slope for segment B; note 1 | 011 |
| SLC[2:0] | select slope for segment C; note 1 | 101 |
| SLD[2:0] | select slope for segment D; note 1 | 111 |
| DFA[6:0] | frame frequency for segment A is 80 Hz; note 1 | 56DEC |
| DFB[6:0] | frame frequency for segment B is 130 Hz; note 1 | 35DEC |
| DFC[6:0] | frame frequency for segment C is 150 Hz; note 1 | 30DEC |
| DFD[6:0] | frame frequency for segment D is 180 Hz; note 1 | 25DEC |
| DF8[6:0] | frame frequency for 8-colour mode is 130 Hz; note 1 | 35DEC |
| VB[3:0] | bias system is $F/G_{max} = 2.5$; note 1 | 1011 |
| NLI[7:0] | inversion is after 19 time slots (76 rows in Full mode); note 1 | 19DEC |
| VCON[6:0] | no contrast setting is set (twos complement number); note 1 | 0DEC |
| SFD | OTP programmed data is used; note 1 | 1 |
| CALMM | not in Calibration mode | 0 |
| OPE | disable OTP programming voltage; note 2 | 0 |
| ORA[2:0] | OTP row address selection | 000 |

Notes

1. These values can be set by the module maker. If the factory defaults OTP bit EFD have been set, the value cannot be changed via the interface. Otherwise, the OTP data will be used if SFD is set to logic 1, which is the reset state.
2. Calibration mode may not be entered if the SEAL bit has been set. Programming is only possible when in Calibration mode.

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6.2.3 SOFTWARE RESET

The software reset (SWRESET) has exactly the same effect as the hardware reset; see Section 6.2.2.

After sending SWRESET any command can be sent immediately without any additional delay in between, for instance: Sleep_OUT, BSTRON and DISPON, etc.

Table 5 Software reset register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01H |

6.2.4 BOOSTER VOLTAGE OFF

The DC-to-DC converters are turned off and pins V_{LCDOUT1} and V_{LCDOUT2} become 3-state.

In order to avoid any optical effect on the display, the sequence given in Fig.2 must be used before the internal display supply generation circuits are turned off.

The external LCD supply input voltages (V_{LCDIN1} and V_{LCDIN2}) can be applied while the display voltage generation (BSTROFF) is off. When BSTROFF, DISPON and Sleep_OUT are set, the external LCD supply input voltages (V_{LCDIN1} and V_{LCDIN2}) must be applied, otherwise the display outputs will be undefined.

Command Sleep_IN does not effect the setting of BSTRON/BSTROFF or DISPON/DISPOFF, but switches off the DC-to-DC converter (booster) and ties the display outputs to V_{SS1}.

For the effect of possible combinations of commands Sleep_IN/Sleep_OUT and BSTRON/BSTROFF; see Table 17 and Fig.4. Figure 7 shows the effects of the combination of commands BSTRON and BSTROFF with DISPON and DISPOFF.

Table 6 Booster voltage off register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02H |

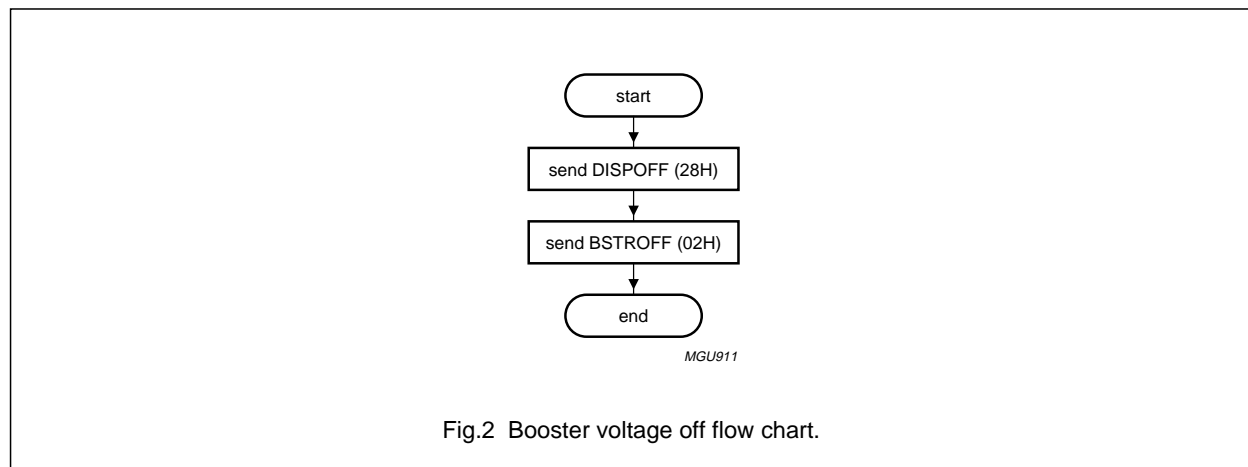


Fig.2 Booster voltage off flow chart.

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6.2.5 BOOSTER VOLTAGE ON

The LCD supply generation circuits will be switched on when the Booster voltage on (BSTRON) command is sent. The BSTRON command has a direct effect only when the PCF8833 is not in Power-down mode (Sleep_OUT is not active).

With a reset DISPON (see Section 6.2.18) and BSTRON are set, the PCF8833 will start-up with Sleep_OUT (see Section 6.2.7) following the built-in start-up sequence which generates the requested voltages and switches on the display, unless DISPOFF and/or BSTROFF was sent. When the LCD supply generation circuits are switched on, it is necessary to wait for a certain time before the power circuits become stable and the display can be switched on. Because this time is dependent on the required V_{LCD} voltage, the external components used, the applied supply voltage and some other parameters, the PCF8833 monitors the LCD supply generation circuit internally and will only switch-on the display when the LCD supply generation circuits are stable.

The status of the LCD supply generation circuits can be monitored with the read display status (RDDST) command; see Section 6.2.7.

Figure 3 shows two sequences for using the BSTRON command, assuming BSTROFF and DISPOFF were set before sending Sleep_OUT. In sequence A the command to switch the display on (DISPON) is sent to the PCF8833 before the BSTRON command is sent. Therefore the display will only be switched on when the LCD supply generation circuit generates a stable V_{LCD}. In sequence B the RDDST command is used to monitor the LCD supply generation circuit and, after the D31 bit of the RDDST is set to logic 1, the DISPON command will be sent; see Section 6.2.7.

For the effect of possible combinations of commands Sleep_IN/Sleep_OUT and BSTRON/BSTROFF; see Table 17 and Fig.4. Figure 7 shows the effects of the combination of commands BSTRON and BSTROFF with DISPON and DISPOFF.

Table 7 Booster voltage on register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03H |

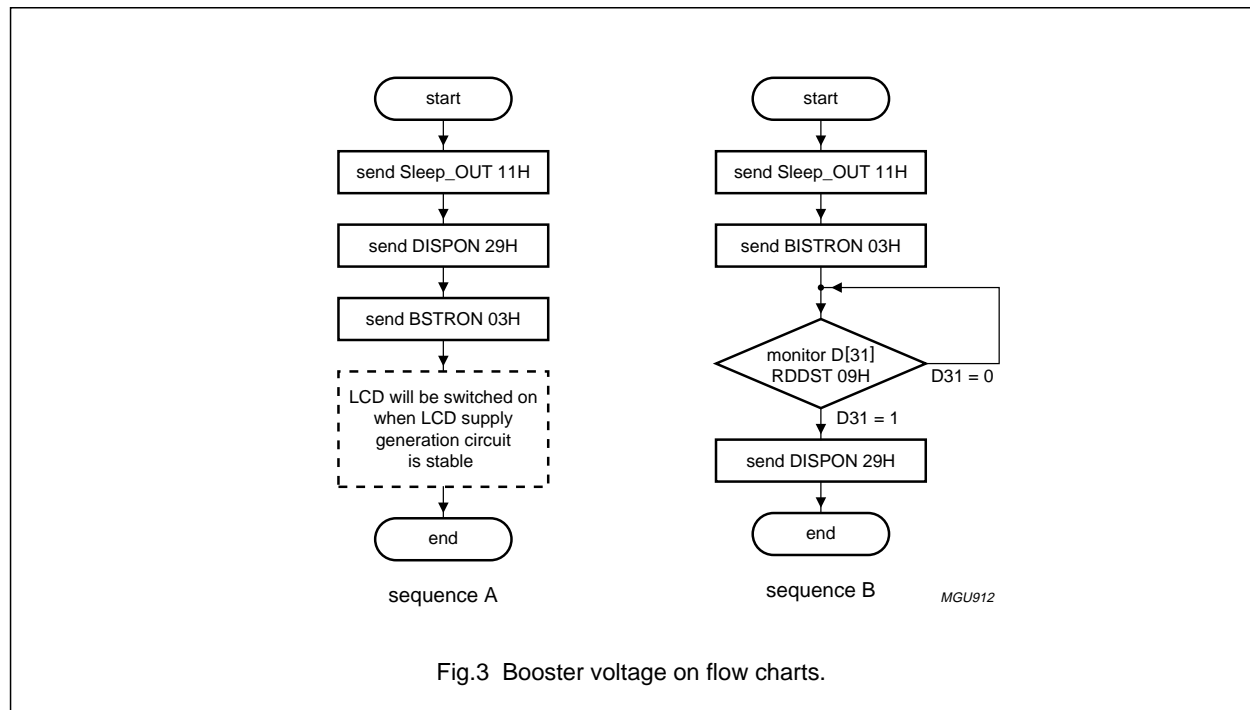


Fig.3 Booster voltage on flow charts.

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6.2.6 READ DISPLAY IDENTIFICATION INFORMATION

The Read Display Identification Information (RDDIDIF) command returns a 24-bit display identification information. The identification information is valid only 5 ms after applying a hardware reset. Therefore the RDDIDIF command should not be sent earlier than 5 ms after a hardware reset.

The input and output data format is given in Table 9. After the command byte 04H is sent, the read starts with one dummy clock cycle followed by the 3 status bytes (see Fig.47).

When less than 25 read clock cycles are sent in Serial mode, the identification information read must be interrupted by a hardware reset or rising edge of \overline{SCE} .

The definition of the display identification bits is given in Table 11.

Table 8 Read display identification information register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04H |

Table 9 RDDIDIF data format for Serial mode

| BIT | D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|---------|-----|---|-----|-----|-----|-----|-----|-----|-----|---------|
| (S)DIN | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04H |
| (S)DOUT | – | X (only one dummy clock cycle, not a full byte) | | | | | | | | X |
| (S)DOUT | – | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | 45H |
| | – | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | XX |
| | – | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XX |

Table 10 RDDIDIF data format for Parallel mode

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04H |
| 1 | X | X | X | X | X | X | X | X | XX |
| 1 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | 45H |
| 1 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | XX |
| 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XX |

Table 11 Description of the display identification bits

| BIT | BIT DESCRIPTION | RD BYTE | REMARK |
|----------|---|----------------------|-----------------------------------|
| D[23:16] | manufacturer ID | RDID1 | hard wired = 45H |
| D15 | driver/module ID (STN B/W = 0 and STN Colour = 1) | RDID2 | OTP programmed; see Chapter 15 |
| D[14:8] | driver/module version ID | | |
| D[7:0] | driver/module code | RDID3 ⁽¹⁾ | OTP programmed; see Chapter 15 |

Note

- RDID3 will be programmed in OTP cells. This ID can be set to 03H by the module maker.

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6.2.7 READ DISPLAY STATUS

The Read Display Status (RDDST) command returns a 32-bit display status information and can be accessed when the PCF8833 is in normal Display mode (see Section 6.2.11), in partial Display mode (see Section 6.2.23) or in Sleep_IN mode; see Section 6.2.8.

The input and output data format is as follows: After the command byte 09H is sent, the read starts with one dummy clock cycle followed by the 4 status bytes (see Fig.48).

When less than 33 read clock cycles are sent in Serial mode the status read must be interrupted by a hardware reset or a rising edge of SCE.

The definition of the display status bits is given in Table 11.

Table 12 Read display status register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09H |

Table 13 RDDST data format for Serial mode

| BIT | D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|---------|-----|---|-----|-----|-----|-----|-----|-----|-----|---------|
| (S)DIN | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09H |
| (S)DOUT | – | X (only one dummy clock cycle, not a full byte) | | | | | | | | XX |
| (S)DOUT | – | D31 | D30 | D29 | D28 | D27 | D26 | 0 | 0 | XX |
| | – | 0 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | XX |
| | – | D15 | 0 | D13 | D12 | D11 | D10 | D9 | 0 | XX |
| | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | XX |

Table 14 RDDST data format for Parallel mode

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09H |
| 1 | X | X | X | X | X | X | X | X | XX |
| 1 | D31 | D30 | D29 | D28 | D27 | D26 | 0 | 0 | XX |
| 1 | 0 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | XX |
| 1 | D15 | 0 | D13 | D12 | D11 | D10 | D9 | 0 | XX |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | XX |

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Table 15 Display identification bits description

| BIT | BIT DESCRIPTION | STATUS |
|----------|-------------------------------------|---|
| D31 | booster voltage status | logic 1 when BSTRON is selected and when the LCD supply generation circuits are ready |
| | | logic 0 when BSTROFF is selected or when the LCD supply generation circuits are not ready |
| D30 | Y address order | logic 1 when MY = 1 |
| | | logic 0 when MY = 0 |
| D29 | X address order | logic 1 when MX = 1 |
| | | logic 0 when MX = 0 |
| D28 | vertical/horizontal addressing mode | logic 1 when V = 1 |
| | | logic 0 when V = 0 |
| D27 | line address order | logic 1 when LAO = 1 |
| | | logic 0 when LAO = 0 |
| D26 | RGB/BGR order | logic 1 when RGB = 1 |
| | | logic 0 when RGB = 0 |
| D[25:23] | no function, but can be read | D[25:23] = 000 |
| D[22:20] | interface pixel format | see Section 6.2.30 |
| | | P2 = D22; P1 = D21 and P0 = D20 |
| D19 | Idle mode | logic 1 when IDMON is selected |
| | | logic 0 when IDMOFF is selected |
| D18 | Partial mode | logic 1 when PTLON is selected |
| | | logic 0 otherwise |
| D17 | Sleep_IN/OUT | logic 1 when Sleep_OUT is selected |
| | | logic 0 when Sleep_IN is selected |
| D16 | normal Display mode | logic 1 when NORON is selected |
| | | logic 0 otherwise |
| D15 | vertical Scroll mode | logic 1 when SEP is selected |
| | | logic 0 otherwise |
| D14 | no function; but can be read | D14 = 0 |
| D13 | display inversion | logic 1 when INVON is selected |
| | | logic 0 when INVOFF is selected |
| D12 | all pixels on | logic 1 when DAL is selected |
| | | logic 0 otherwise |
| D11 | all pixels off | logic 1 when DALO is selected |
| | | logic 0 otherwise |
| D10 | display on/off | logic 1 when DISPON is selected |
| | | logic 0 when DISPOFF is selected |
| D9 | tearing effect line on/off | logic 1 when TEON is selected |
| | | logic 0 when TEOFF is selected |
| D[8:0] | no function; but can be read | D[8:0] = 0:0000:0000 |

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6.2.8 SLEEP_IN

By sending the Sleep_IN command, the PCF8833 immediately enters the Power-down mode, also referred to as the Sleep mode. In the Sleep mode the output voltages of all LCD driver pins (rows and columns) are at V_{SS1} (ground, all pixels are in off state), and the LCD supply generation circuit and the oscillator are switched off. The Sleep_IN command does not change the state of the DISPON/DISPOFF and BSTRON/BSTROFF commands, but has the same effect as DISPOFF and BSTROFF; see Table 17.

While in Sleep_IN mode all commands and data can be sent and will be executed as in the Sleep_OUT state, except some OTP related commands and temperature readout related commands. In the Sleep_IN mode no effect on the display can be seen.

The Sleep_IN mode is exited by command Sleep_OUT; see Section 6.2.9.

Table 16 Sleep_IN register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10H |

Table 17 Sleep_IN/OUT and BSTER_ON/OFF combination

| BSTER_ON/BSTER_OFF | Sleep_IN/Sleep_OUT | Booster ⁽¹⁾ |
|--------------------|--------------------|------------------------|
| ON | ON | ON |
| ON | OFF | OFF |
| OFF | ON | OFF |
| OFF | OFF | OFF |

Note

1. Booster is the built-in DC-to-DC converter also called voltage multiplier or charge pump.

6.2.9 SLEEP_OUT

This command must be sent to allow the PCF8833 to power-up (see Fig.4).

DISPON and BSTRON are set with a reset, the PCF8833 will start-up with Sleep_OUT following the built-in start-up sequence which generates the requested voltages and switches on the display, unless DISPOFF and/or BSTROFF was sent after the last reset.

For the effects of possible combinations of commands Sleep_IN/Sleep_OUT and BSTRON/BSTROFF; see Table 17.

Figure 4 illustrates the flow when sending the Sleep_OUT command. The display is only switched on, when the internally generated voltage V_{LCD2} is high enough.

This time is self adapting and therefore dependent on application conditions:

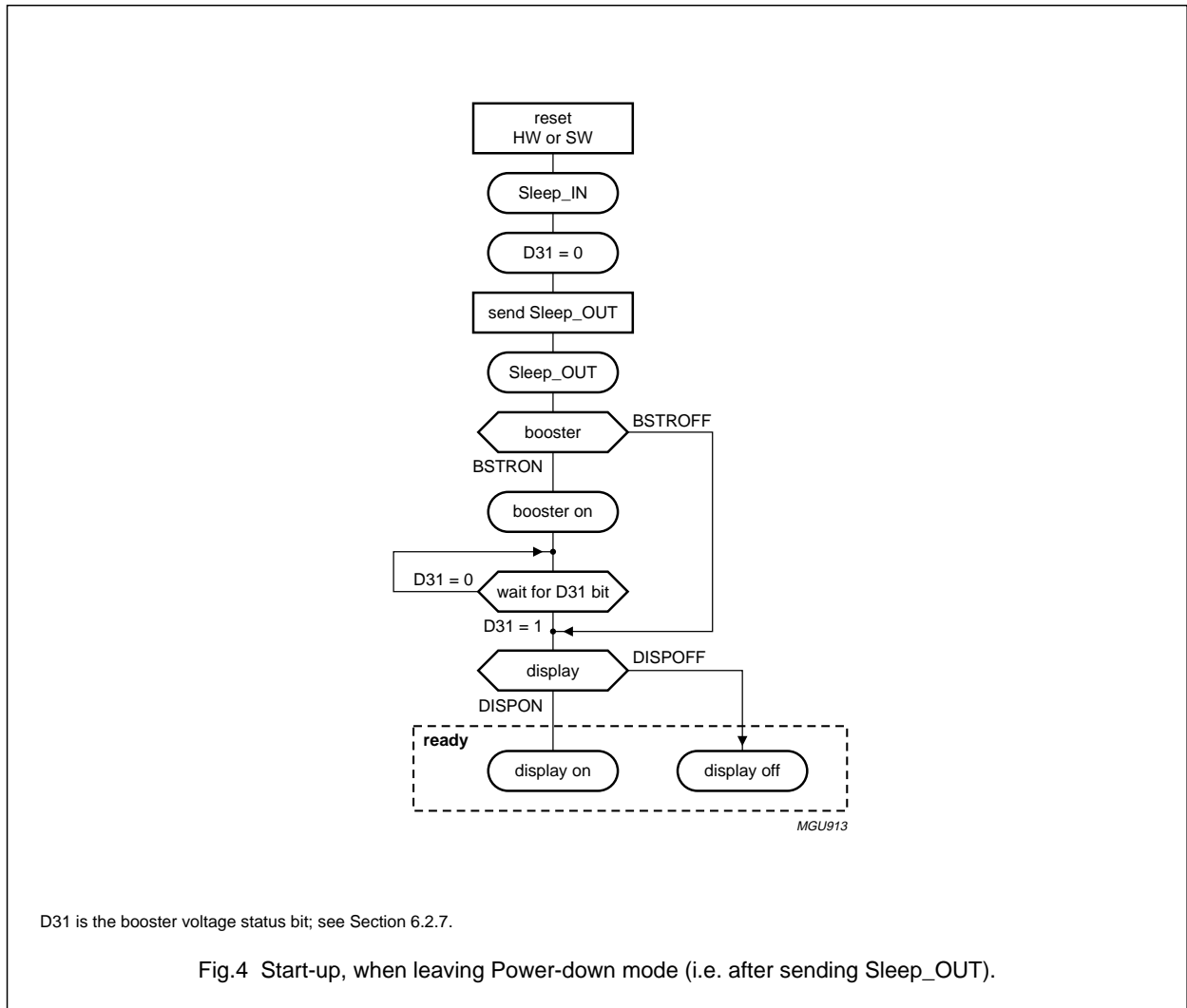
- It is longer for:
 - Low V_{DD2}
 - Higher resistors in supply wires and/or external capacitors
 - Higher external capacitors
 - Higher required V_{LCD2} voltage.
- Some other conditions, which may affect start-up time are:
 - Partial/full mode
 - Selected bias system
 - Temperature
 - Selected temperature coefficients.

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Table 18 Sleep_OUT register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11H |



D31 is the booster voltage status bit; see Section 6.2.7.

Fig.4 Start-up, when leaving Power-down mode (i.e. after sending Sleep_OUT).

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6.2.10 PARTIAL MODE ON

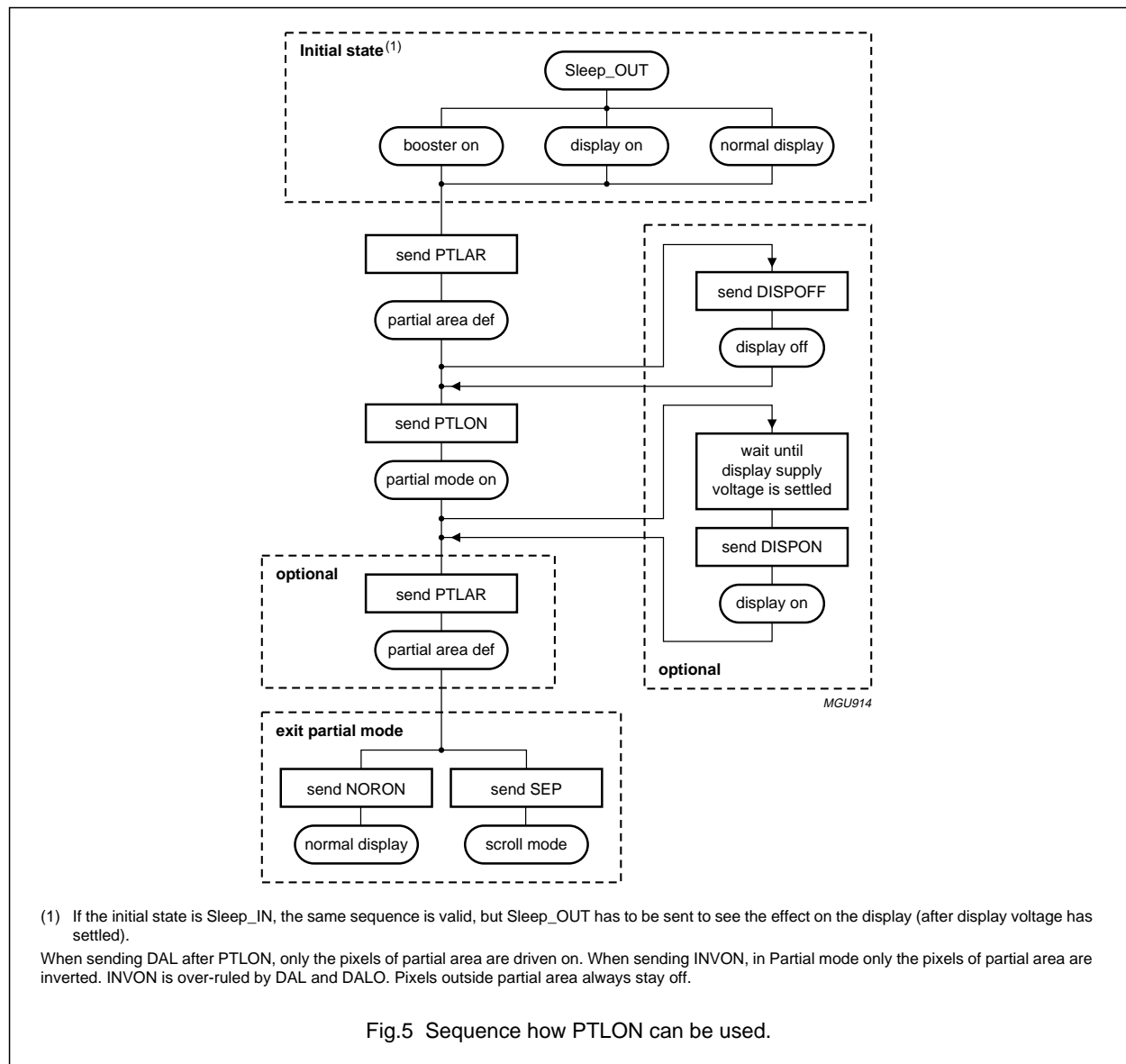
Partial mode on (PTLON) turns on the partial Display mode. Only one partial display size can be chosen. Normal mode, Scroll mode, DALO and DAL are exited with this command. When sending DAL after PTLON, only the pixels of partial area are driven on.

A normal Display mode command is used to exit the Partial mode. How the partial display area can be programmed is given in Section 6.2.23.

A sequence showing how the command PTLON can be used is illustrated in Fig.5.

Table 19 Partial mode on register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12H |



(1) If the initial state is Sleep_IN, the same sequence is valid, but Sleep_OUT has to be sent to see the effect on the display (after display voltage has settled).

When sending DAL after PTLON, only the pixels of partial area are driven on. When sending INVON, in Partial mode only the pixels of partial area are inverted. INVON is over-ruled by DAL and DALO. Pixels outside partial area always stay off.

Fig.5 Sequence how PTLON can be used.

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6.2.11 NORMAL DISPLAY MODE ON

The normal Display mode on command (NORON) turns the display into Normal mode which is also the reset state.

An explanation of how the command NORON can be used is illustrated in Fig.6.

Table 20 Normal Display mode on register bits

| D/C | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DEFAULT |
|-----|----|----|----|----|----|----|----|----|---------|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13H |

6.2.12 DISPLAY INVERSION OFF

The Display inversion off command (INVOFF) turns the display into a non-inverted screen without modifying the display data RAM. Display inversion off is the reset state of the PCF8833.

Table 21 Display inversion off register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20H |

6.2.13 DISPLAY INVERSION ON

The Display inversion on command (INVON) turns the display into an inverted screen without modifying the display data RAM. The RAM data is read out and inverted while writing to the display.

The display Inversion mode can be switched off by sending the INVOFF command; see Section 6.2.12.

When sending INVON, in Partial mode only, the pixels of a partial area are inverted. INVON is overruled by DAL and DALO. In Partial mode the pixels outside of the partial are always off.

Table 22 Display inversion on register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21H |

6.2.14 ALL PIXELS OFF

The All pixels off command (DALO) can be switched off by sending the normal display on command (NORON) (see Section 6.2.11) or by sending the partial Display mode on command (PTLON); see Section 6.2.10. Furthermore DALO is left with the command DAL; see Section 6.2.15. When DALO is active all pixels are driven, as if the display RAM was filled with all zeros (off-state). DALO does not change the data stored in the display RAM. Figure 6 illustrates how DAL (all pixels on) and DALO (all pixels off) can be used.

All pixels will be switched off regardless of the display data RAM.

Table 23 All pixels off register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22H |

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6.2.15 ALL PIXELS ON

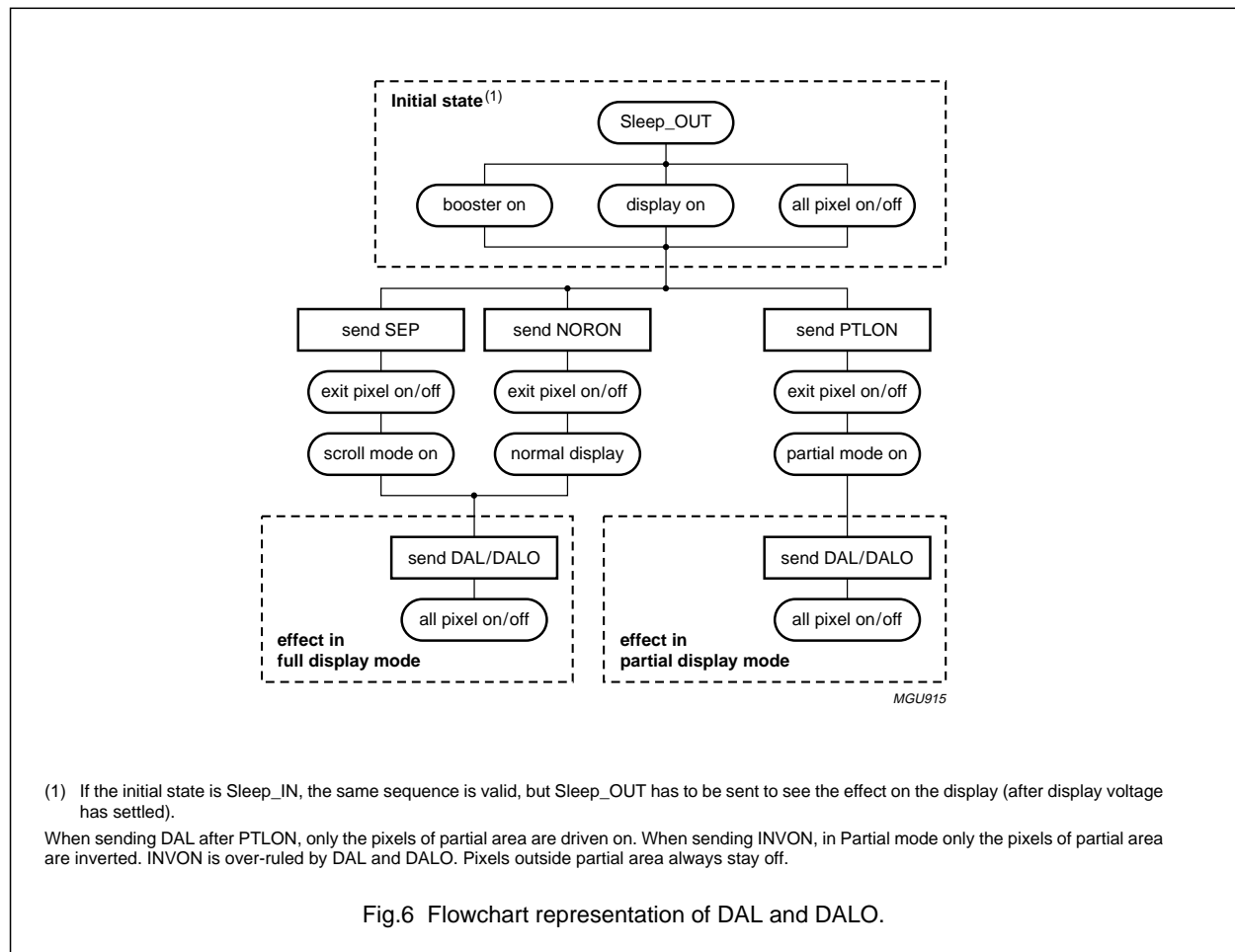
The All pixels on command (DAL) can be switched off by sending the normal display on command (NORON); (see Section 6.2.11) or by sending the partial Display mode on command (PTLON); see Section 6.2.10. Furthermore DAL is left with the command DALO; see Section 6.2.14. When DAL is active all pixels are driven, as if the display RAM was filled with all ones (on-state). DAL does not change the data stored in the display RAM.

When sending DAL after PTLON, only the pixels of the partial area are driven on. When sending INVON in Partial mode only the pixels of the partial area are inverted. INVON is over-ruled by DAL and DALO. Pixels outside the partial area are always off. Figure 6 illustrates how DAL (all pixels on) and DALO (all pixels off) can be used.

All pixels will be switched on regardless of the display data RAM.

Table 24 All pixels on register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23H |



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6.2.16 SET CONTRAST

Using the Set contrast command (SETCON) the V_{LCD} voltage and the contrast of the LCD can be adjusted. The influence of the VCON[6:0] register on the V_{LCD} programming is explained in Section 6.2.31. The VCON[6:0] is a two's complement number; see Table 26. An overview over the complete programming range of V_{LCD} can be found in Section 15.1.

Table 25 Set contrast register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|---------|
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 25H |
| 1 | X | VCON ₆ | VCON ₅ | VCON ₄ | VCON ₃ | VCON ₂ | VCON ₁ | VCON ₀ | 00H |

Table 26 Possible VCON values

| VCON[6:0] | DECIMAL EQUIVALENT | V_{LCD} OFFSET |
|-----------|--------------------|------------------|
| 0111111 | 63 | 2520 mV |
| 0111110 | 62 | 2480 mV |
| 0111101 | 61 | 2440 mV |
| : | : | : |
| 0000010 | 2 | 80 mV |
| 0000001 | 1 | 40 mV |
| 0000000 | 0 | 0 mV |
| 1111111 | -1 | -40 mV |
| 1111110 | -2 | -80 mV |
| : | : | : |
| 1000010 | -62 | -2480 mV |
| 1000001 | -63 | -2520 mV |
| 1000000 | -64 | -2560 mV |

6.2.17 DISPLAY OFF

The Display off command (DISPOFF) connects all rows and columns to V_{SS1} , i.e. all the pixels have a voltage of 0 V. Since the reset state of the PCF8833 is Sleep_IN (see Section 6.2.8) the display will be in the off state after a reset.

The DISPOFF command can be switched off by sending the Display on command (DISPON); see Section 6.2.18. Figure 7 shows the effects of the combination of commands BSTRON and BSTROFF with DISPON and DISPOFF.

Table 27 Display off register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28H |

6.2.18 DISPLAY ON

Using the Display on command (DISPON) the rows and columns are driven according to the current display data RAM content and according to the display timing and settings.

The DISPON command is used to exit the DISPOFF state; see Section 6.2.17.

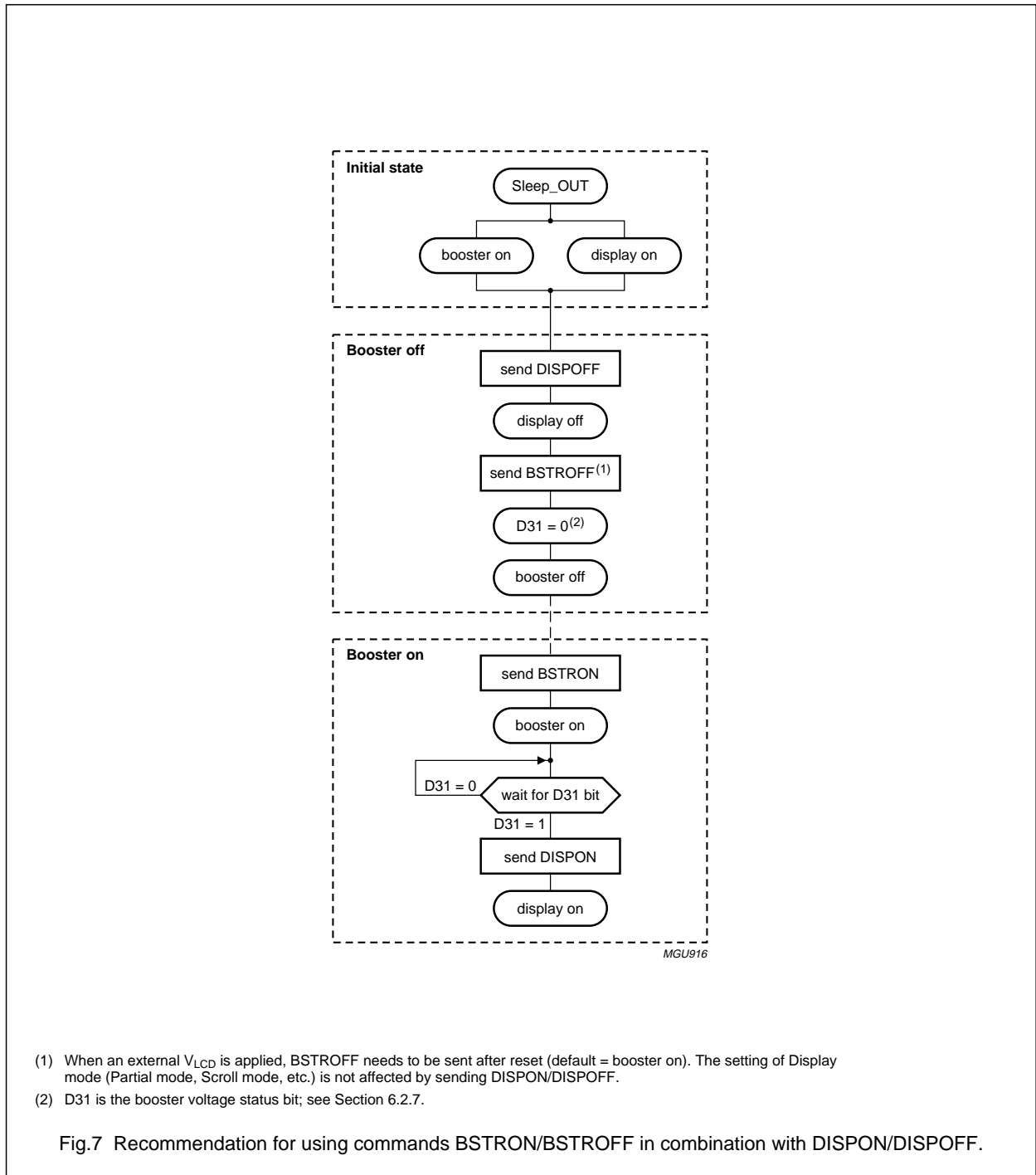
Figure 4 gives additional information on the effect of the DISPON/DISPOFF command. Figure 7 shows the effects of the combination of commands BSTRON and BSTROFF with DISPON and DISPOFF.

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Table 28 Display on register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29H |



- (1) When an external V_{LCD} is applied, BSTROFF needs to be sent after reset (default = booster on). The setting of Display mode (Partial mode, Scroll mode, etc.) is not affected by sending DISPON/DISPOFF.
- (2) D31 is the booster voltage status bit; see Section 6.2.7.

Fig.7 Recommendation for using commands BSTRON/BSTROFF in combination with DISPON/DISPOFF.

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6.2.19 COLUMN ADDRESS SET

The display data RAM parameters *xs* and *xe* define the column address range of the display data RAM for writing data. Parameters *xs* and *xe* are defined between 0 and 131 (83H), and *xs* must be smaller than *xe*.

Table 29 Column address set register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------|
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2AH |
| 1 | <i>xs</i> [7] | <i>xs</i> [6] | <i>xs</i> [5] | <i>xs</i> [4] | <i>xs</i> [3] | <i>xs</i> [3] | <i>xs</i> [3] | <i>xs</i> [0] | 02H |
| 1 | <i>xe</i> [7] | <i>xe</i> [6] | <i>xe</i> [5] | <i>xe</i> [4] | <i>xe</i> [3] | <i>xe</i> [2] | <i>xe</i> [1] | <i>xe</i> [0] | 81H |

6.2.20 PAGE ADDRESS SET

The display data RAM parameters *ys*[7:0] and *ye*[7:0] define the page (row) address range of the display data RAM for writing data. Parameters *ys* and *ye* are defined between 0 and 131 (83H), and *ys* must be smaller than *ye*.

Table 30 Page address set register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------|
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 2BH |
| 1 | <i>ys</i> [7] | <i>ys</i> [6] | <i>ys</i> [5] | <i>ys</i> [4] | <i>ys</i> [3] | <i>ys</i> [3] | <i>ys</i> [3] | <i>ys</i> [0] | 02H |
| 1 | <i>ye</i> [7] | <i>ye</i> [6] | <i>ye</i> [5] | <i>ye</i> [4] | <i>ye</i> [3] | <i>ye</i> [2] | <i>ye</i> [1] | <i>ye</i> [0] | 81H |

6.2.21 MEMORY WRITE

Data written to the display memory (RAM) is validated by the Memory write (RAMWR) command. Entering this command always returns the page address and column address to the start addresses *xs*[7:0] and *ys*[7:0] respectively. Content of the display data RAM is written by the data entered following this command, with the page and/or column address automatically incremented. The data Write mode turned on by this command can be automatically cancelled by entering another command.

After a power-up the display RAM content is undefined. Neither a hardware reset nor a software reset changes the data stored in display RAM. Sending display data must stop 160 ns before issuing a hardware reset, otherwise the last word written to the display RAM may be corrupted.

Table 31 Memory write register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|----|----|----|----|----|----|----|----|---------|
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2CH |
| 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XX |

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6.2.22 COLOUR SET

With the Colour set (RGBSET) command the mapping from the 256-colour interface data is translated to the 4 kbyte colour RAM data of the PCF8833 can be changed. The translation table must be changed, if necessary, before sending 256 colour data. For the red and green pixel 8 from the available 16 grey scales can be selected. For the blue pixel 4 from the 16 grey scales can be selected. The default or reset state of the colour mapping can be found in Table 32.

If the 256-to-4 kbyte colour mapping needs to be changed, the whole table must be sent. The mapping of colours is done when writing data into the RAM, through the application of the Look-Up Table (LUT).

Table 32 Colour set register bits

| D/C | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DEFAULT | DESCRIPTION |
|-----|----|----|----|----|----|----|----|----|---------|----------------|
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2DH | |
| 1 | X | X | X | X | R3 | R2 | R1 | R0 | 00H | red tone 000 |
| 1 | X | X | X | X | R3 | R2 | R1 | R0 | 02H | red tone 001 |
| 1 | X | X | X | X | R3 | R2 | R1 | R0 | 04H | red tone 010 |
| 1 | X | X | X | X | R3 | R2 | R1 | R0 | 06H | red tone 011 |
| 1 | X | X | X | X | R3 | R2 | R1 | R0 | 09H | red tone 100 |
| 1 | X | X | X | X | R3 | R2 | R1 | R0 | 0BH | red tone 101 |
| 1 | X | X | X | X | R3 | R2 | R1 | R0 | 0DH | red tone 110 |
| 1 | X | X | X | X | R3 | R2 | R1 | R0 | 0FH | red tone 111 |
| 1 | X | X | X | X | G3 | G2 | G1 | G0 | 00H | green tone 000 |
| 1 | X | X | X | X | G3 | G2 | G1 | G0 | 02H | green tone 001 |
| 1 | X | X | X | X | G3 | G2 | G1 | G0 | 04H | green tone 010 |
| 1 | X | X | X | X | G3 | G2 | G1 | G0 | 06H | green tone 011 |
| 1 | X | X | X | X | G3 | G2 | G1 | G0 | 09H | green tone 100 |
| 1 | X | X | X | X | G3 | G2 | G1 | G0 | 0BH | green tone 101 |
| 1 | X | X | X | X | G3 | G2 | G1 | G0 | 0DH | green tone 110 |
| 1 | X | X | X | X | G3 | G2 | G1 | G0 | 0FH | green tone 111 |
| 1 | X | X | X | X | B3 | B2 | B1 | B0 | 00H | blue tone 00 |
| 1 | X | X | X | X | B3 | B2 | B1 | B0 | 04H | blue tone 01 |
| 1 | X | X | X | X | B3 | B2 | B1 | B0 | 0BH | blue tone 10 |
| 1 | X | X | X | X | B3 | B2 | B1 | B0 | 0FH | blue tone 11 |

6.2.23 PARTIAL AREA

The Partial area command (PTLAR) sets the partial display area and displays the RAM content of this area. In the partial Display mode the drive voltage can be reduced.

Table 33 Partial area register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|---------|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30H |
| 1 | AA1S ₇ | AA1S ₆ | AA1S ₅ | AA1S ₄ | AA1S ₃ | AA1S ₂ | AA1S ₁ | AA1S ₀ | tbf |
| 1 | AA1E ₇ | AA1E ₆ | AA1E ₅ | AA1E ₄ | AA1E ₃ | AA1E ₂ | AA1E ₁ | AA1E ₀ | tbf |

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The following steps must be followed to enter the Partial mode:

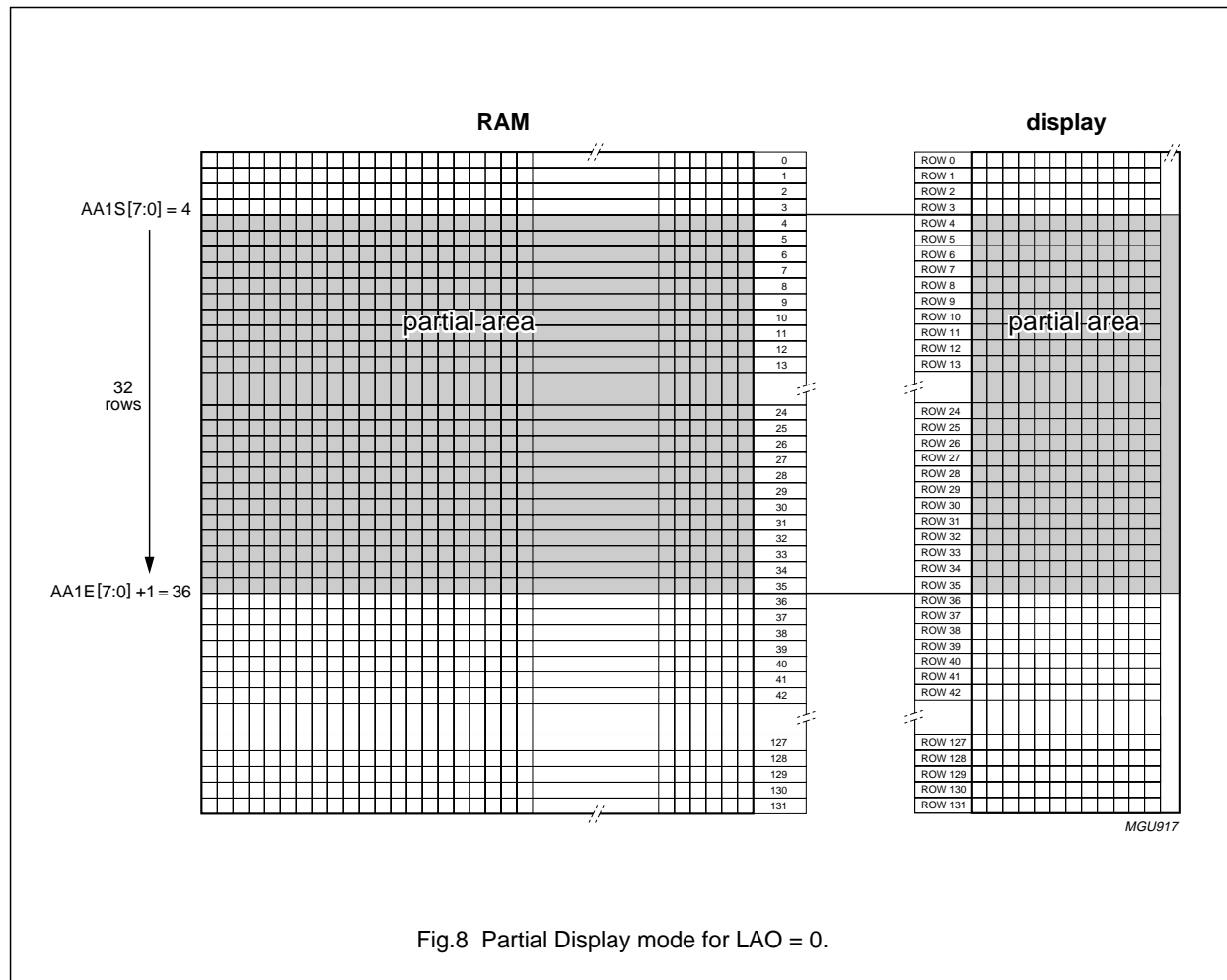
- Set V_{OP} (when the MMOTP cells are used the V_{OP} for the Partial mode is predefined)
- Set bias system (when the MMOTP cells are used the bias system for the Partial mode is predefined)
- Set start address of active area $AA1S[7:0]$; can be set in multiples of 4
- Set end address of active area $AA1E[7:0] + 1$; can be set in multiples of 4
- Enter Partial mode (PTLON).

When setting the addresses the following conditions must be ensured:

- $(AA1E + 1) - AA1S = 32$ (only 1 partial display size setting is possible)
- $AA1 \geq 0$ and $AA1E \leq 131$.

Figure 8 shows how to use the Partial mode with Line Address Order (LAO) set to logic 0. Figure 9 gives an example of Partial mode with LAO set to logic 1, and Fig.10 shows the position of the partial area when the start address of the active area is $AA1S \geq (131 + 1) - 31$, i.e. $AA1S \geq 101$ ($AA1S$ must be set in multiples of 4).

Figure 11 shows how the Partial mode can be used.



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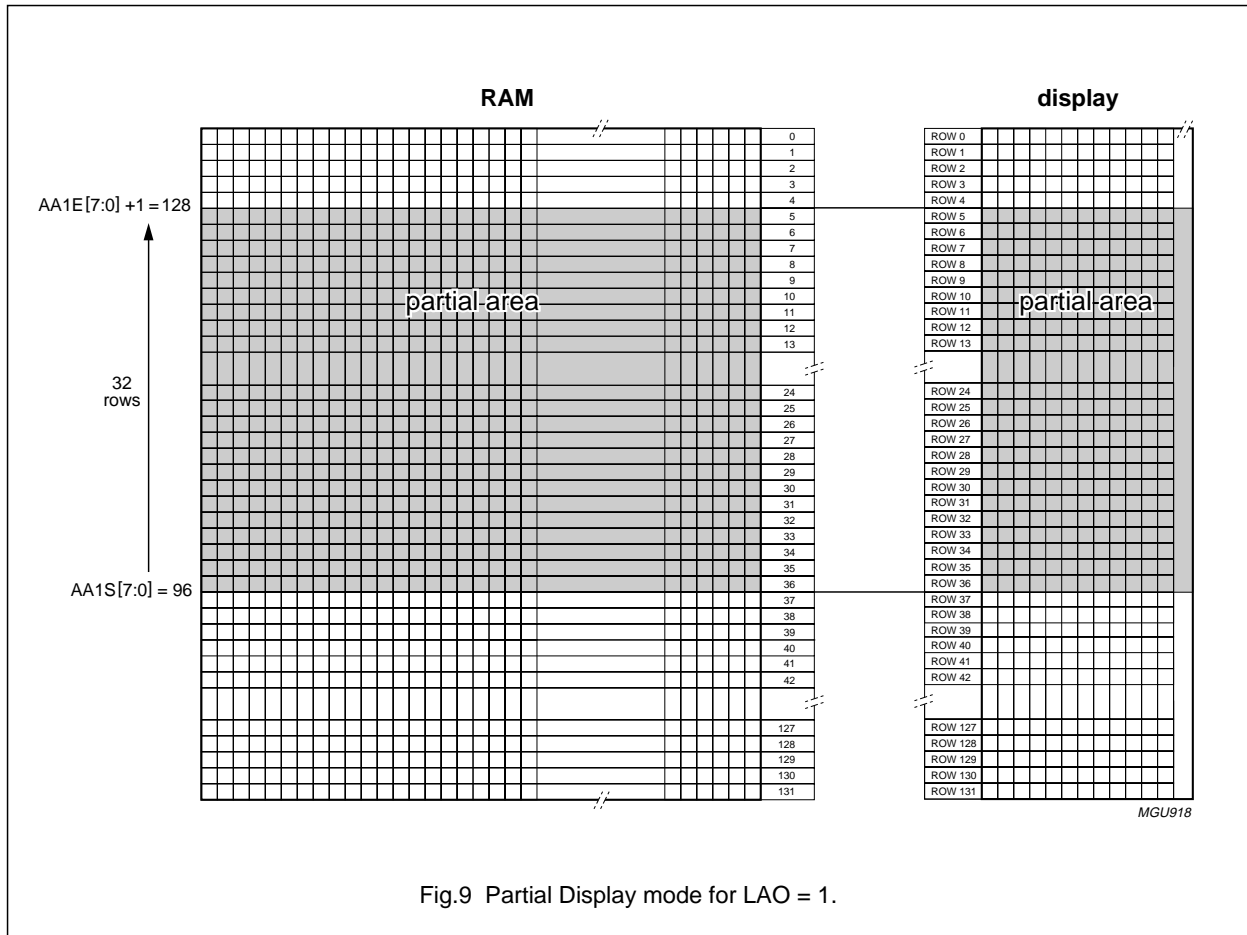


Fig.9 Partial Display mode for LAO = 1.

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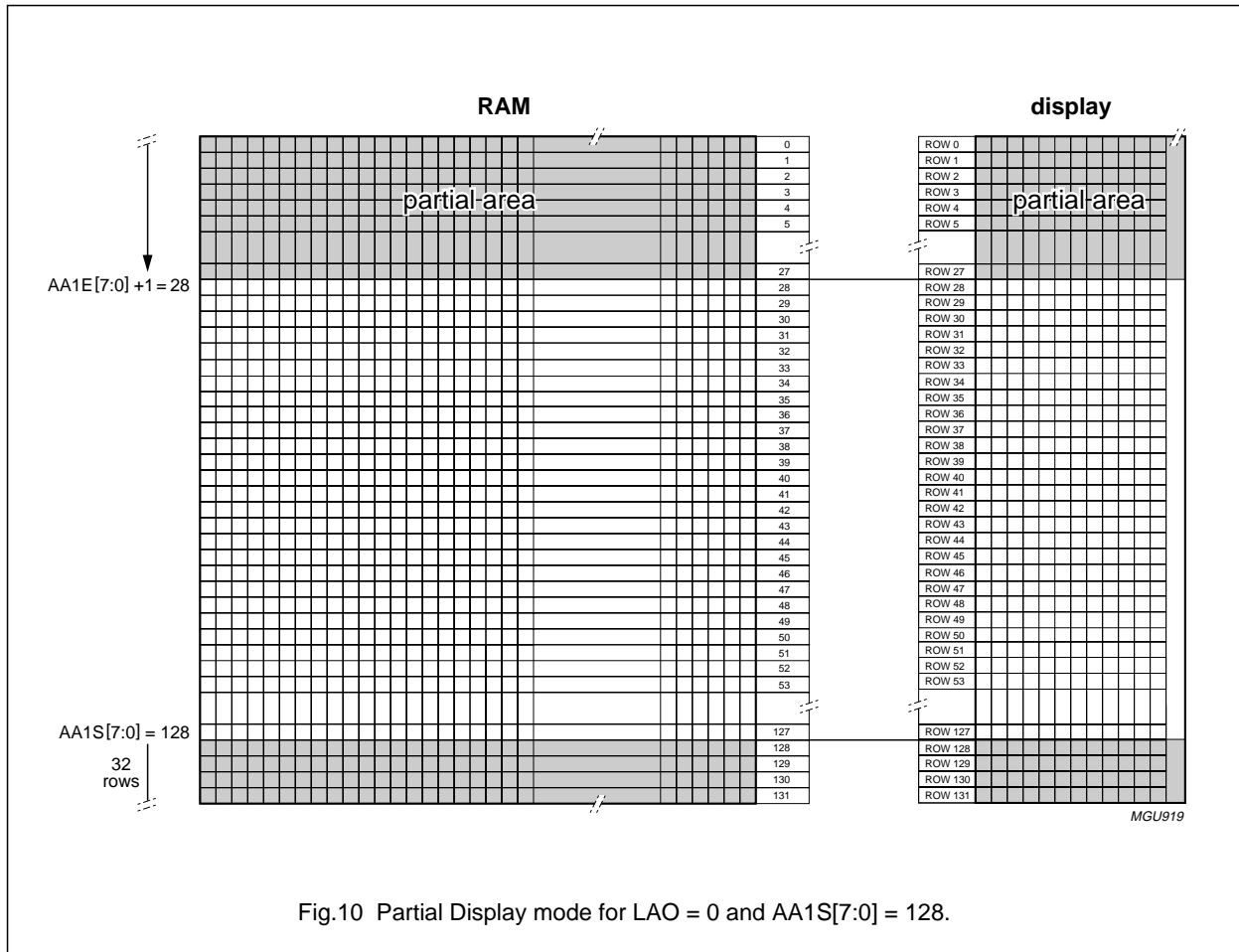
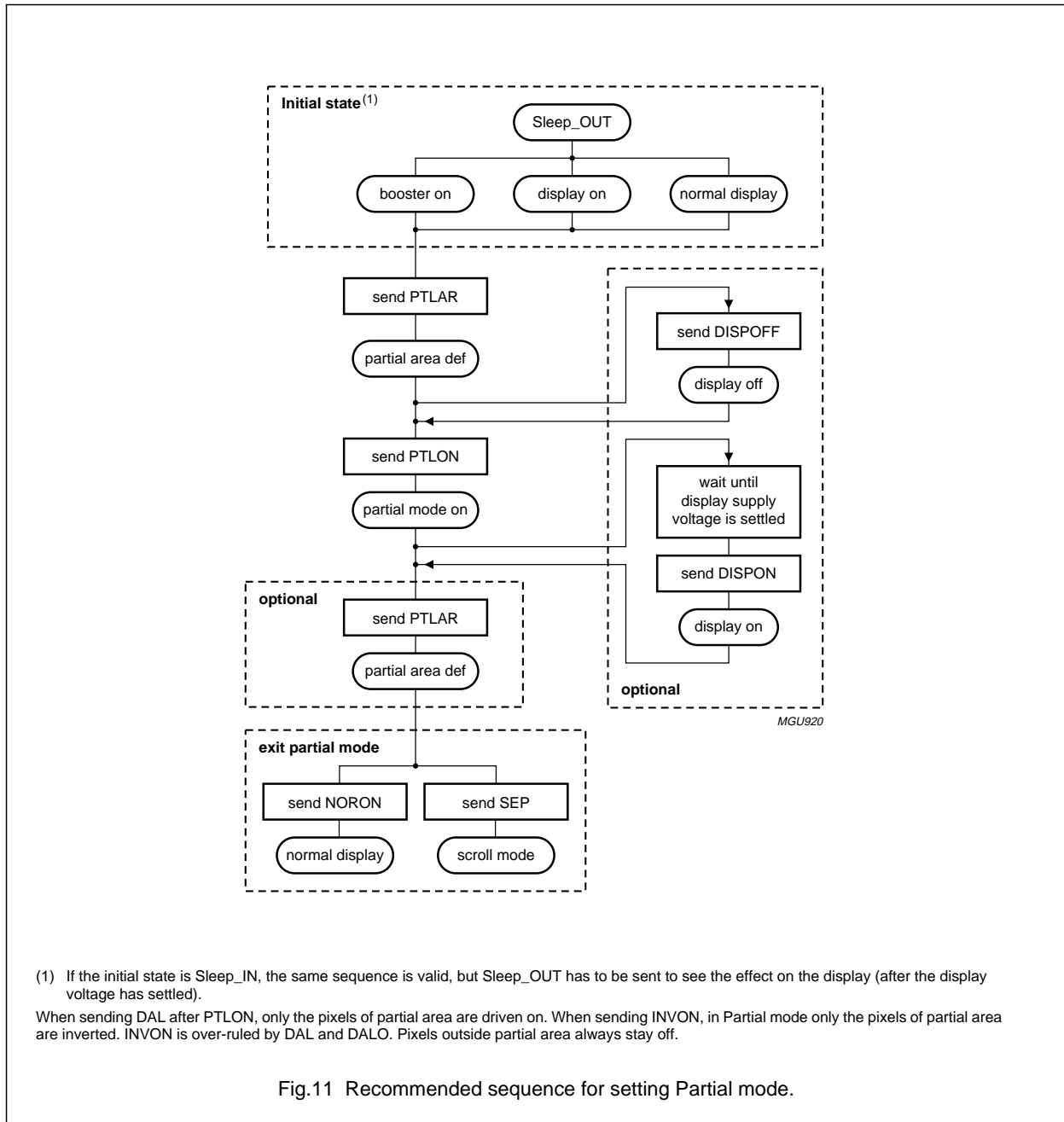


Fig.10 Partial Display mode for LAO = 0 and AA1S[7:0] = 128.

STN RGB - 132 × 132 × 3 driver

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STN RGB - 132 × 132 × 3 driver

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6.2.24 VERTICAL SCROLLING DEFINITION

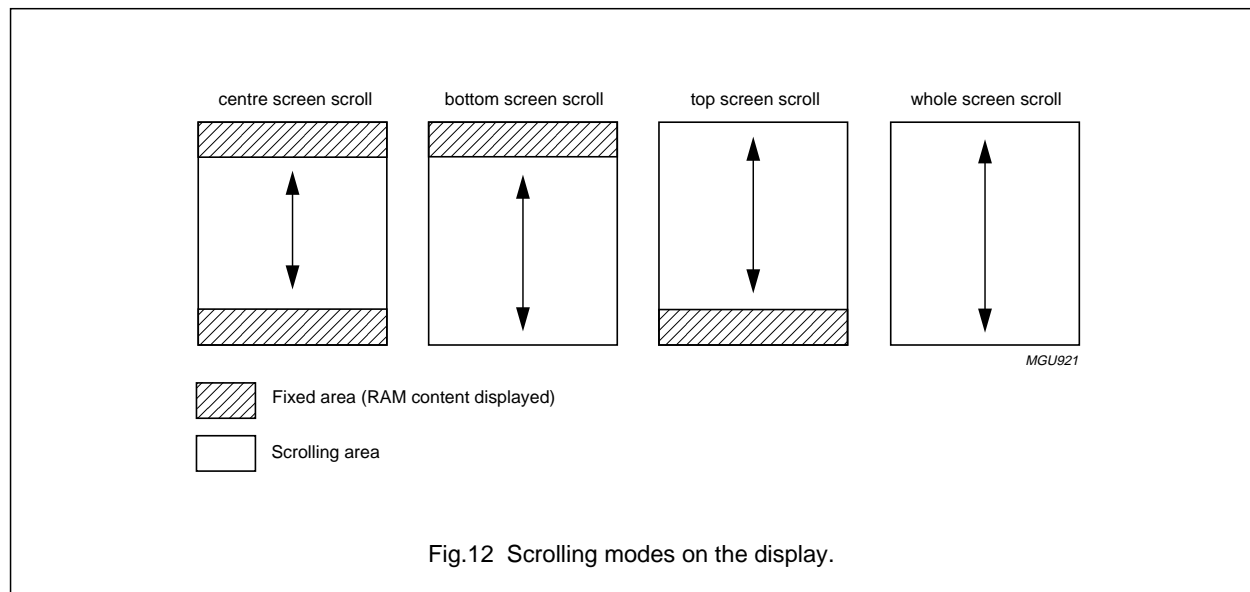
In the PCF8833 three different scrolling modes can be used. These scrolling modes differ from each other in the way the RAM to display mapping is done. The vertical scrolling is defined as follows:

- Vertical scrolling definition (VSCRDEF) command
- TF[7:0] defines the number of lines for the top fixed area on the display, there is no top fixed area when TF[7:0] = 0
- SA[7:0] defines the number of lines for the scrolling area on the display
- BF[7:0] defines the number of lines for the bottom fixed area on the display, there is no bottom fixed area when BF[7:0] = 0.

Figure 12 illustrates the 4 scrolling configurations that can be defined.

Table 34 Vertical scrolling definition register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---------|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33H |
| 1 | TF ₇ | TF ₆ | TF ₅ | TF ₄ | TF ₃ | TF ₂ | TF ₁ | TF ₀ | 00H |
| 1 | SA ₇ | SA ₆ | SA ₅ | SA ₄ | SA ₃ | SA ₂ | SA ₁ | SA ₀ | 82H |
| 1 | BF ₇ | BF ₆ | BF ₅ | BF ₄ | BF ₃ | BF ₂ | BF ₁ | BF ₀ | 00H |



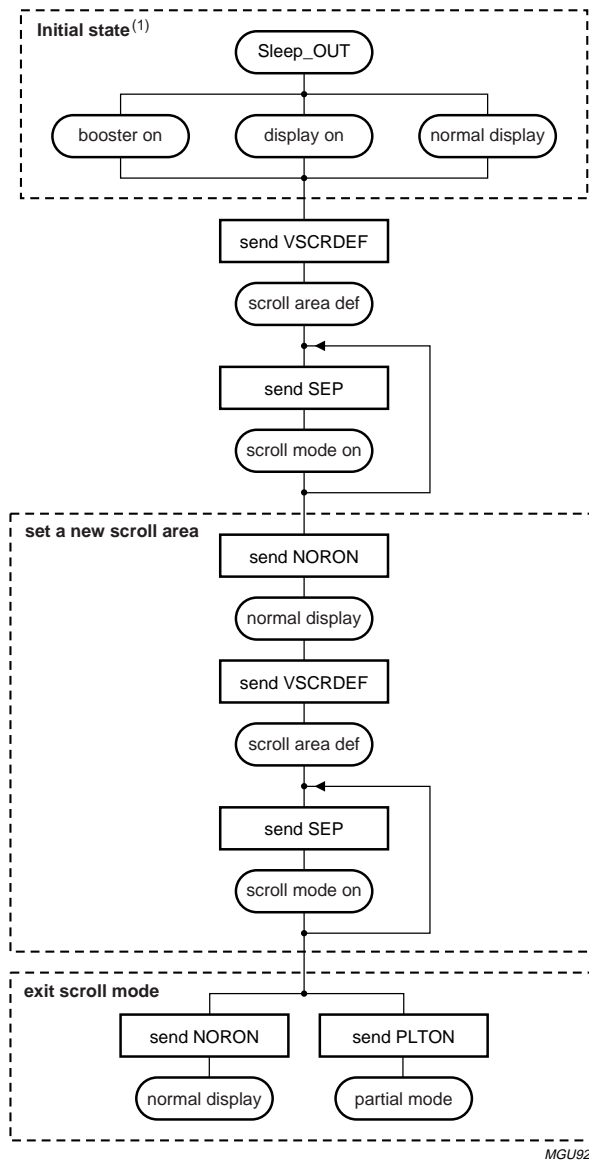
There are 3 different scrolling modes, which are selected as follows:

1. TF + SA + BF = 130 rolling Scroll mode; see Section 6.2.24.1
2. TF + SA + BF = 131 non-rolling Scroll mode; see Section 6.2.24.2
3. TF + SA + BF = 132 non-rolling Scroll mode; see Section 6.2.24.3.

The recommended sequence for setting up the scroll modes is illustrated in Fig.13.

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(1) If the initial state is Sleep_IN, the same sequence is valid, but Sleep_OUT has to be sent to see the effect on the display (after the display voltage has settled).

Fig.13 Recommended sequence for setting up Scroll modes.

STN RGB - 132 × 132 × 3 driver

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6.2.24.1 Rolling Scroll mode

The RAM-to-display mapping for the rolling Scroll mode when a 132 × 130 (columns × rows) display is connected to the PCF8833 is illustrated in Fig.14. In this case rows 0 and 131 must be left open. When a 132 × 132 display is connected, there will be a one-to-one mapping between the RAM and the display, and there will be no unused rows.

The rolling Scroll mode is activated when the Set Entry Scroll Point (SEP) is set; see Table 35.

Figure 15 gives an example for when the PCF8833 is working in the rolling Scroll mode.

When the rolling Scroll mode is used the following sequence can be applied:

- After the desired time interval increment the scroll address to SEP + n for a n-line step
- Keep incrementing the scroll address (SEP) at regular intervals.

The rolling Scroll mode is left when the normal Display mode on (NORON) or the partial Display mode on (PTLON) is selected.

Table 35 Set entry scroll point register bits

| D/C | 7 | D6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|------|------|------|------|------|------|------|------|---------|
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37H |
| 1 | SEP7 | SEP6 | SEP5 | SEP4 | SEP3 | SEP2 | SEP1 | SEP0 | 00H |

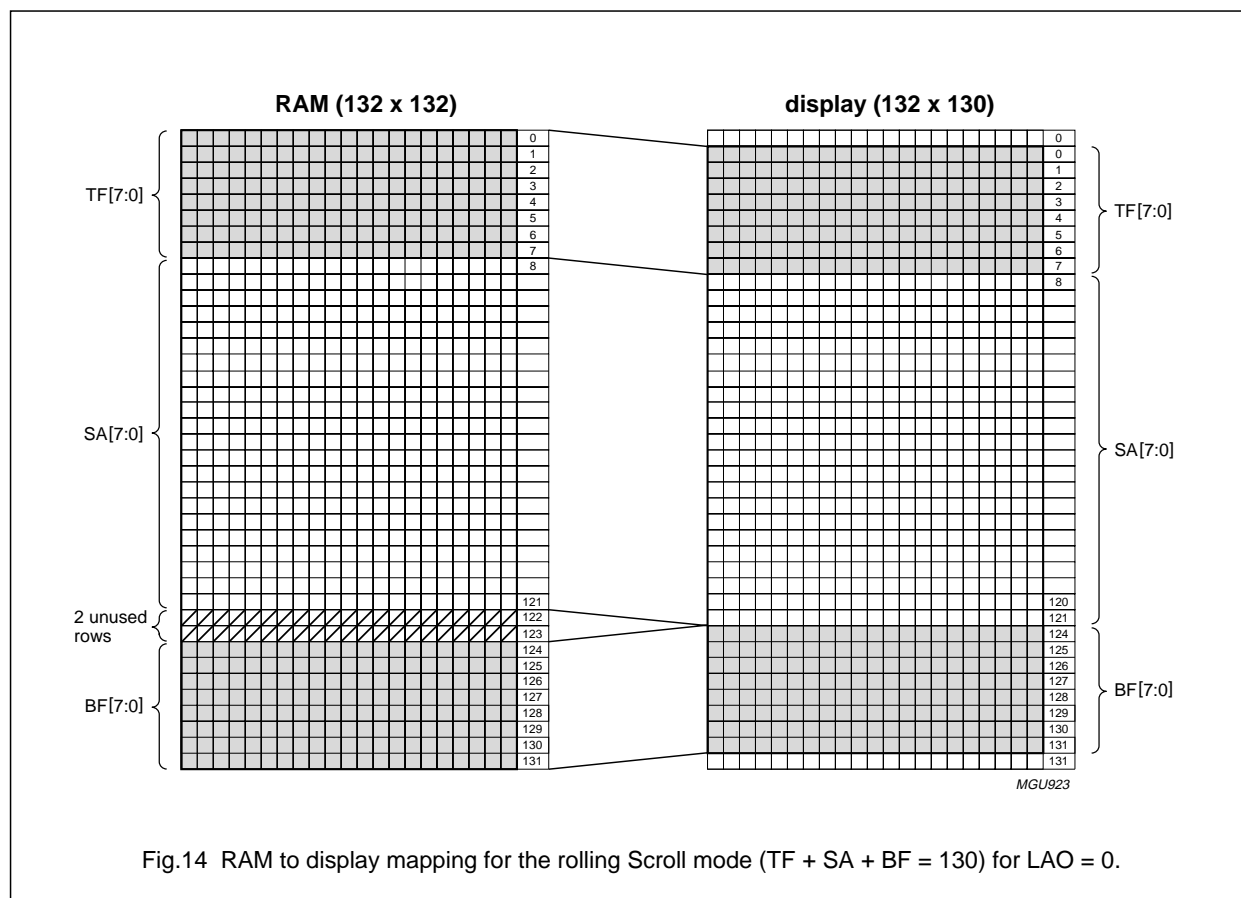


Fig.14 RAM to display mapping for the rolling Scroll mode (TF + SA + BF = 130) for LAO = 0.

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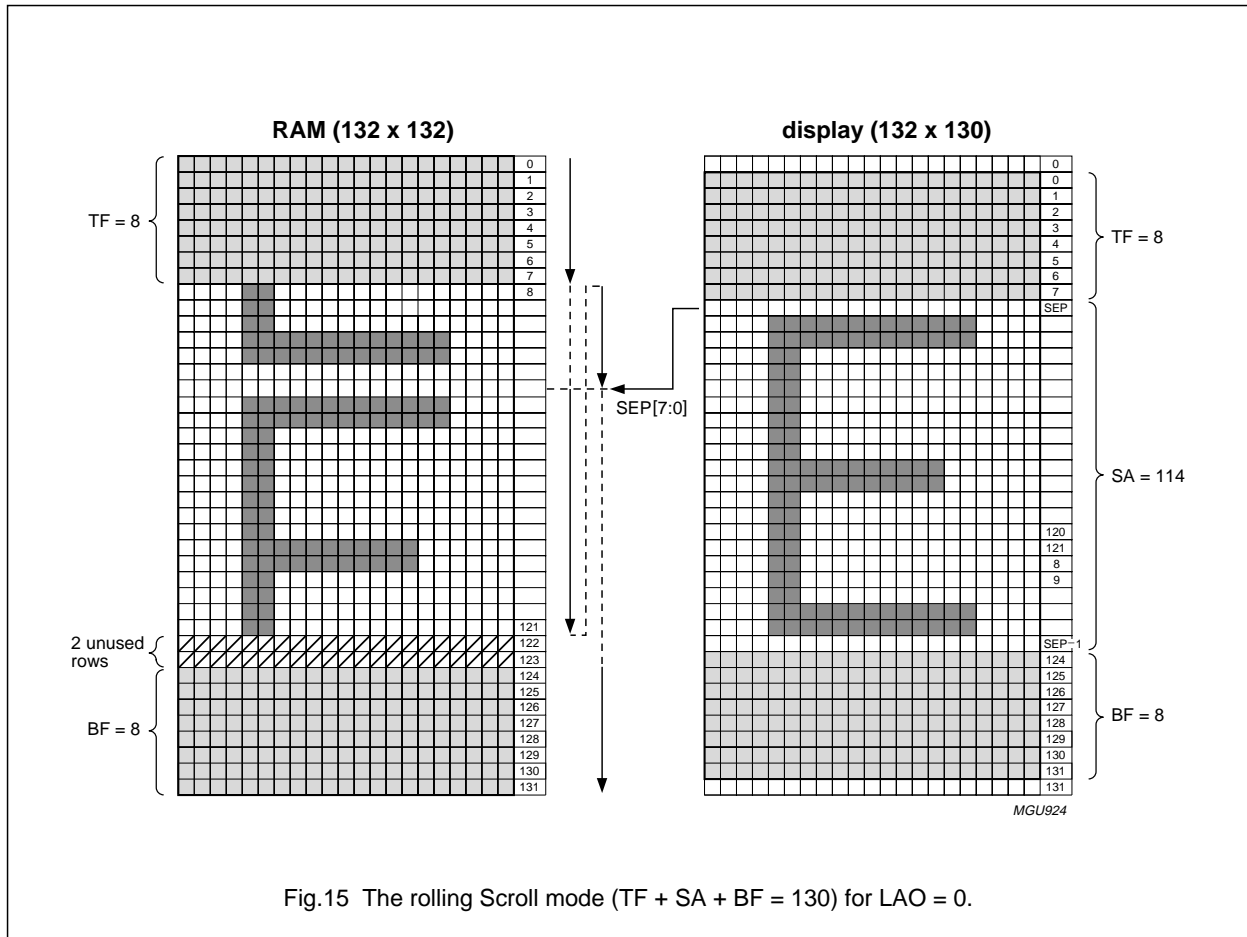


Fig.15 The rolling Scroll mode (TF + SA + BF = 130) for LAO = 0.

STN RGB - 132 × 132 × 3 driver

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6.2.24.2 Non-rolling Scroll mode

The RAM-to-display mapping for the non-rolling Scroll mode when a 132 × 130 (columns × rows) display is connected to the PCF8833 is illustrated in Fig.16. In this case unused rows and columns are to be left open, for instance row 0 and 131. If a 132 × 132 display is connected to the PCF8833 the content of row 0 and 131 will be the same as the content which is displayed in row 1 and 130, respectively. By doing so, the display data RAM will have 1 row in the background, whose content can be updated when it is not displayed.

The non-rolling Scroll mode is activated when the Set Entry Scroll point is set; see Table Fig.36.

An example is given in Figure 17 for the case when the PCF8833 is working in the non-rolling Scroll mode (TF + SA + BF = 131).

When the non-rolling Scroll mode is used the following sequence can be applied:

- Fill the background memory
- After the desired time interval increment the scroll address to SEP + n for a n-line step
- Keep filling the background memory and incrementing scroll address (SEP) at regular intervals to obtain a smooth scrolling.

The non-rolling Scroll mode is left when the normal Display mode on (NORON) or the partial Display mode on (PTLON) is selected.

Table 36 Set entry scroll point register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|------|------|------|------|------|------|------|------|---------|
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37H |
| 1 | SEP7 | SEP6 | SEP5 | SEP4 | SEP3 | SEP2 | SEP1 | SEP0 | 00H |

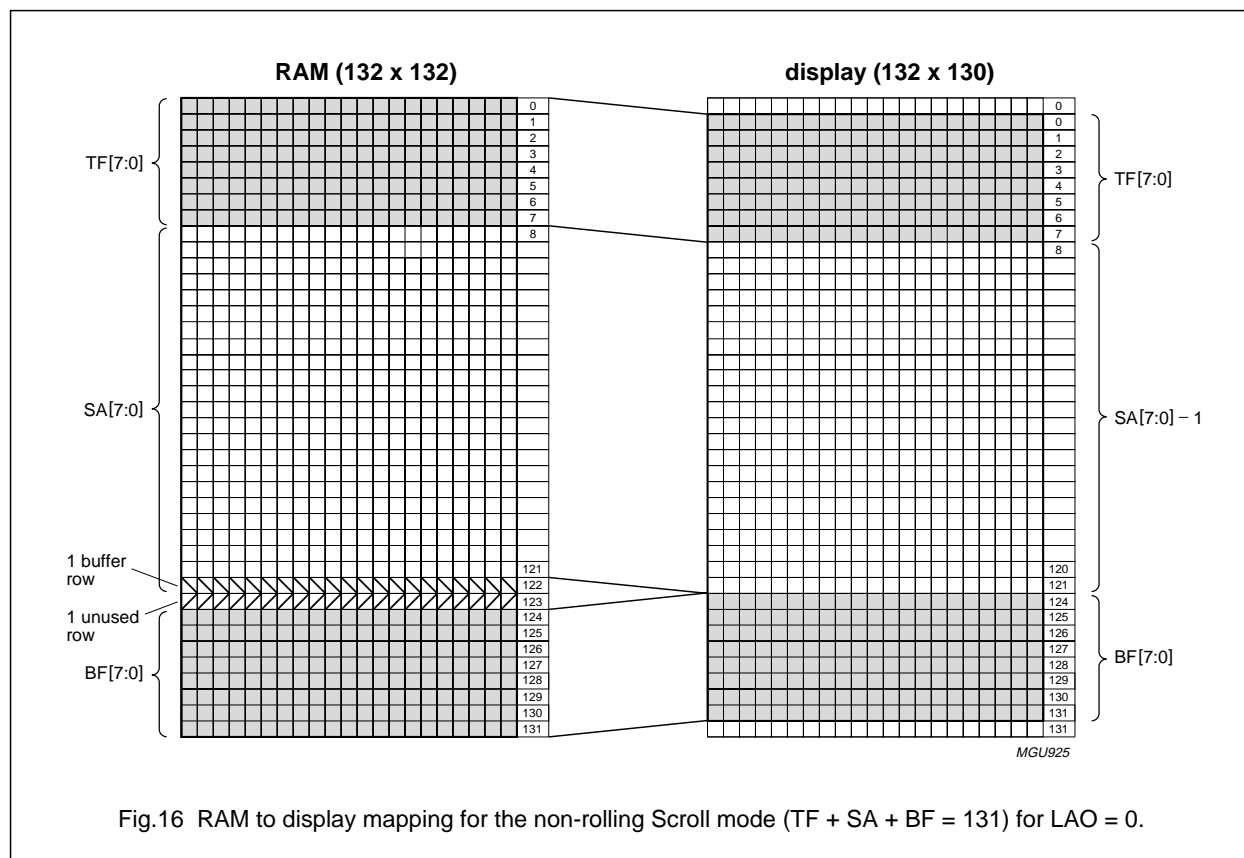
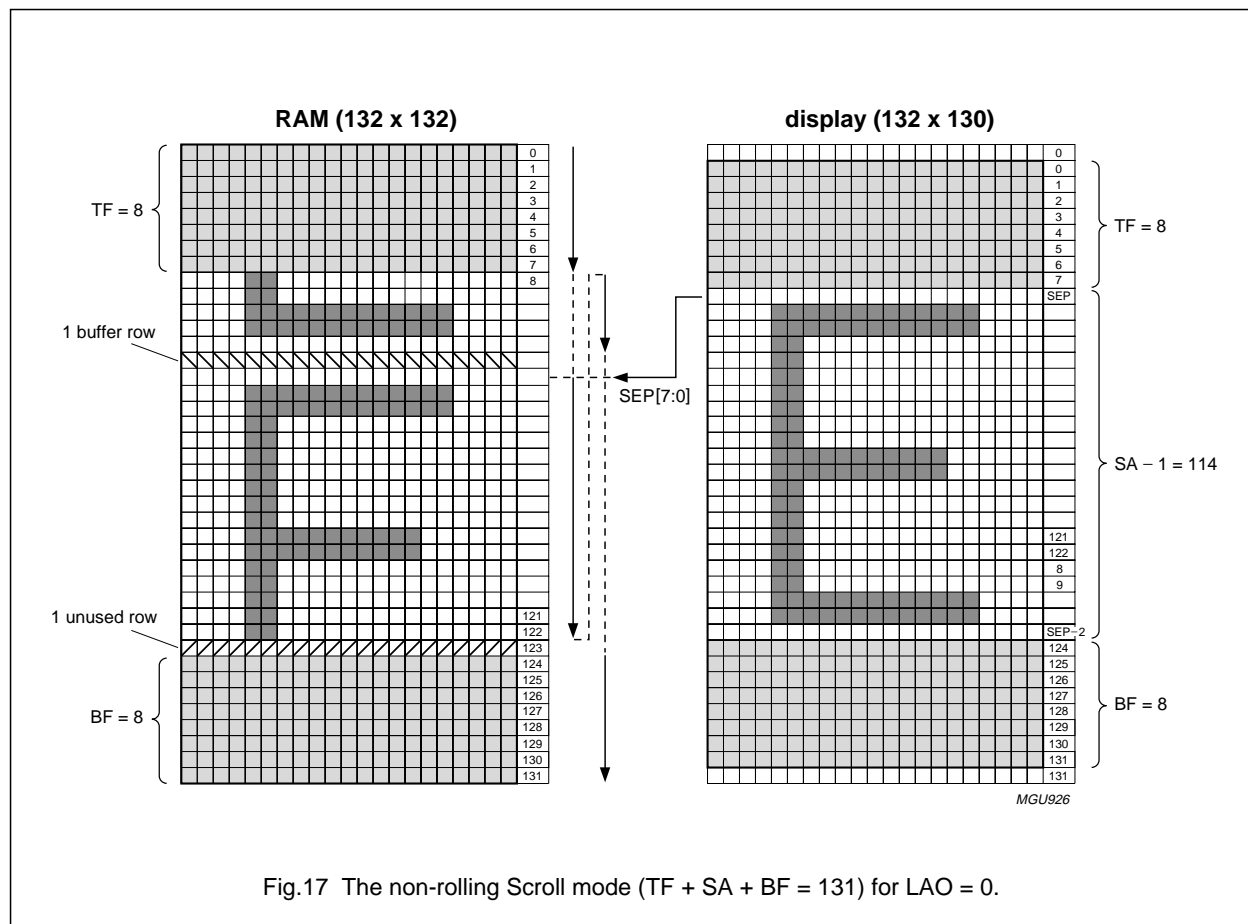


Fig.16 RAM to display mapping for the non-rolling Scroll mode (TF + SA + BF = 131) for LAO = 0.

STN RGB - $132 \times 132 \times 3$ driver

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6.2.24.3 Non-rolling Scroll mode

The RAM-to-display mapping for the non-rolling Scroll mode when a 132×130 (columns \times rows) display is connected to the PCF8833 is illustrated in Fig.18. In this case unused rows and columns are to be left open, for instance row 0 and 131. If a 132×132 display is connected to the PCF8833 the content of row 0 and 131 will be the same as the content which is displayed in row 1 and 130, respectively. By doing so the display data RAM will have 2 rows in the background, whose content can be updated when they are not displayed.

The non-rolling Scroll mode is activated when the Set Entry Scroll Point is set; see Table Fig.37.

Figure 19 shows an example for when the PCF8833 is working in the non-rolling Scroll mode ($TF + SA + BF = 132$).

When the non-rolling Scroll mode is used the following sequence can be applied.

- Fill the background memory
- After the desired time interval increment the scroll address to $SEP + n$ for a n -line step
- Keep filling the background memory and incrementing scroll address (SEP) at regular intervals to obtain a smooth scrolling.

The non-rolling Scroll mode is left when the normal Display mode on (NORON) or the partial Display mode on (PTLON) is selected.

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Table 37 Set entry scroll point register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|------|------|------|------|------|------|------|------|---------|
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37H |
| 1 | SEP7 | SEP6 | SEP5 | SEP4 | SEP3 | SEP2 | SEP1 | SEP0 | 00H |

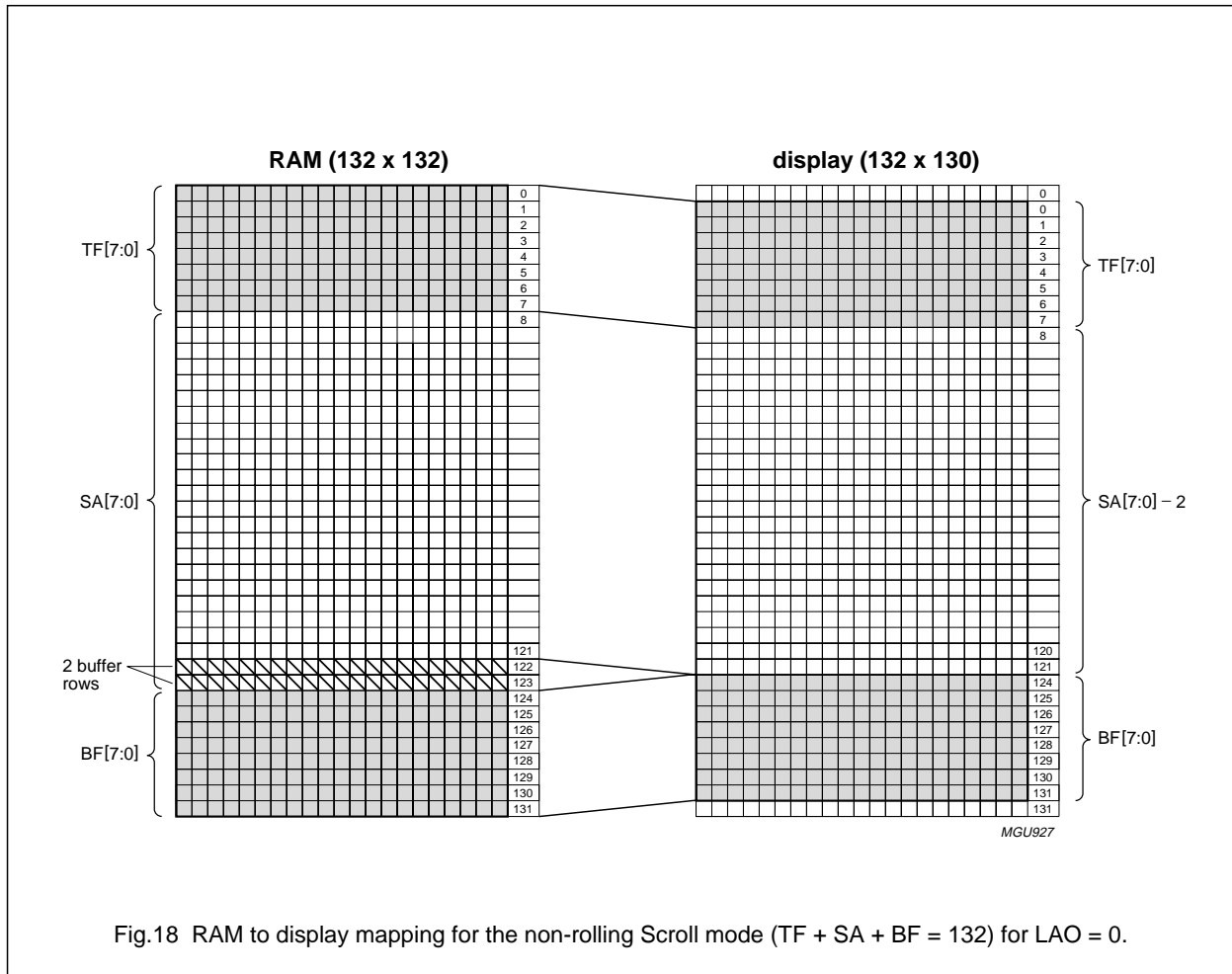


Fig.18 RAM to display mapping for the non-rolling Scroll mode (TF + SA + BF = 132) for LAO = 0.

STN RGB - 132 × 132 × 3 driver

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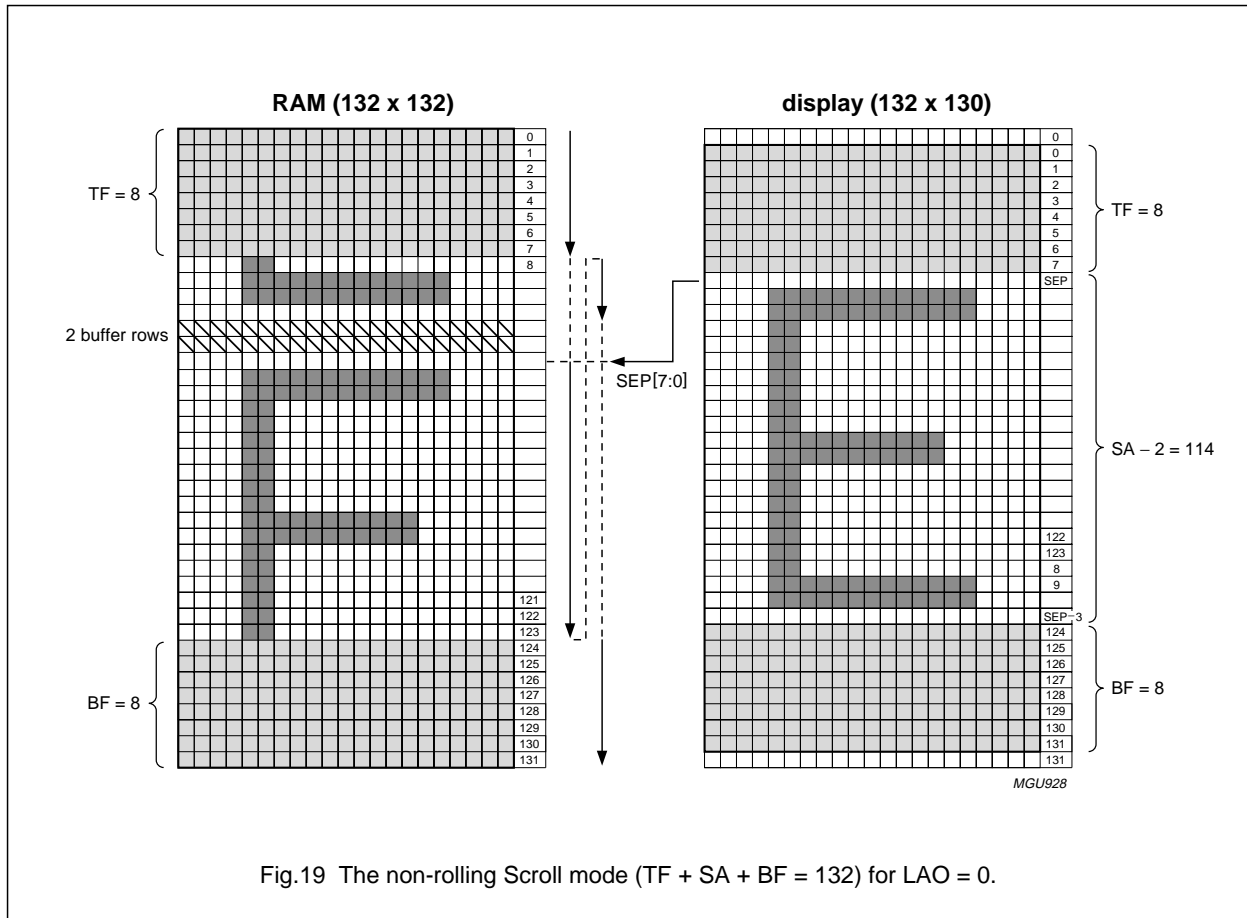


Fig.19 The non-rolling Scroll mode (TF + SA + BF = 132) for LAO = 0.

STN RGB - 132 × 132 × 3 driver

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6.2.24.4 Effect of LAO on scroll modes

An example of when the PCF8833 is working in the non-rolling Scroll mode (TF + SA + BF = 132) with the Line Address Order (LAO) bit set to logic 1, is illustrated in Fig.20. The Scroll modes described in Sections 6.2.24.1 and 6.2.24.2 also work on the same principle when the LAO bit is set to logic 1.

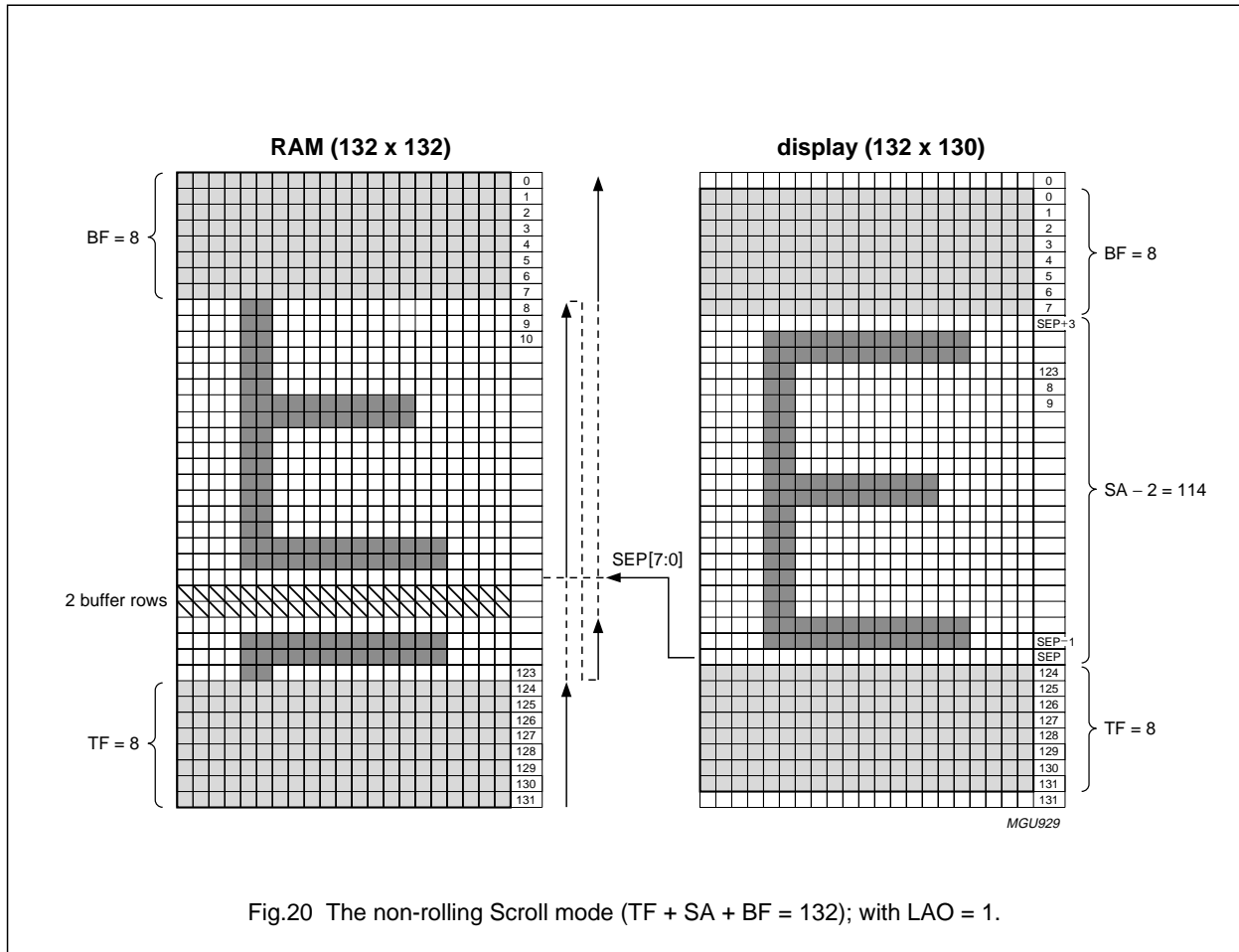


Fig.20 The non-rolling Scroll mode (TF + SA + BF = 132); with LAO = 1.

STN RGB - 132 × 132 × 3 driver

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6.2.25 TEARING EFFECT LINE OFF

The Tearing effect line off (TEOFF) command ties the TE pin LOW.

Table 38 Tearing effect line off register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34H |

6.2.26 TEARING EFFECT LINE ON

The Tearing effect line on (TEON) command turns the TE line of the display on.

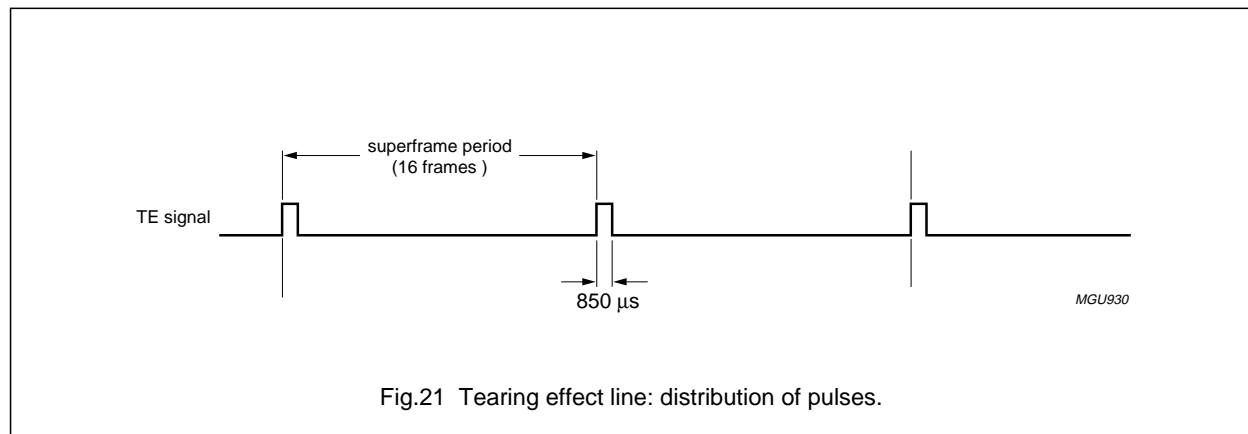
The TE signal indicates the start of a super-frame (equals 16 frames). In 4 kbyte colour mode a whole super-frame is needed to write full colour depth. In 8-colour mode the available colour depth is written in one frame. The tearing signal goes HIGH when the last line of a super-frame is read. The HIGH time is 850 μ s (see Fig.21).

Table 39 Tearing effect line on register bits; note 1

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35H |
| 1 | X | X | X | X | X | X | X | X | 00H |

Note

1. X = don't care.



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6.2.27 MEMORY DATA ACCESS CONTROL

The display data RAM access conditions can be defined by using the Memory data access control (MADCTL) command. The used single control bits together with their reset states are given in Table 41.

Table 40 Memory data access control register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|----|----|---|--------------------|-----|---|---|---|---------|
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36H |
| 1 | MY | MX | V | LAO ⁽¹⁾ | RGB | X | X | X | 00H |

Note

1. Refer to Section 6.2.24.4 for an explanation of LAO on scroll modes and to Section 6.2.23 for an explanation of LAO on Partial mode.

Table 41 Explanation of the memory data access control bits

| BIT | LOGIC 0 (RESET STATE) | LOGIC 1 |
|-----|------------------------------------|------------------------------------|
| MY | no mirror Y | mirror Y |
| MX | no mirror X | mirror X |
| V | RAM write in X direction | vertical RAM write; in Y direction |
| LAO | line address order (top to bottom) | line address order (bottom to top) |
| RGB | RGB | BGR |

The relationship between RAM and display for the MX, MY, RGB and LAO control bits is illustrated Fig.22. Combinations of MX, MY and V are described in more detail in Section 7.2.

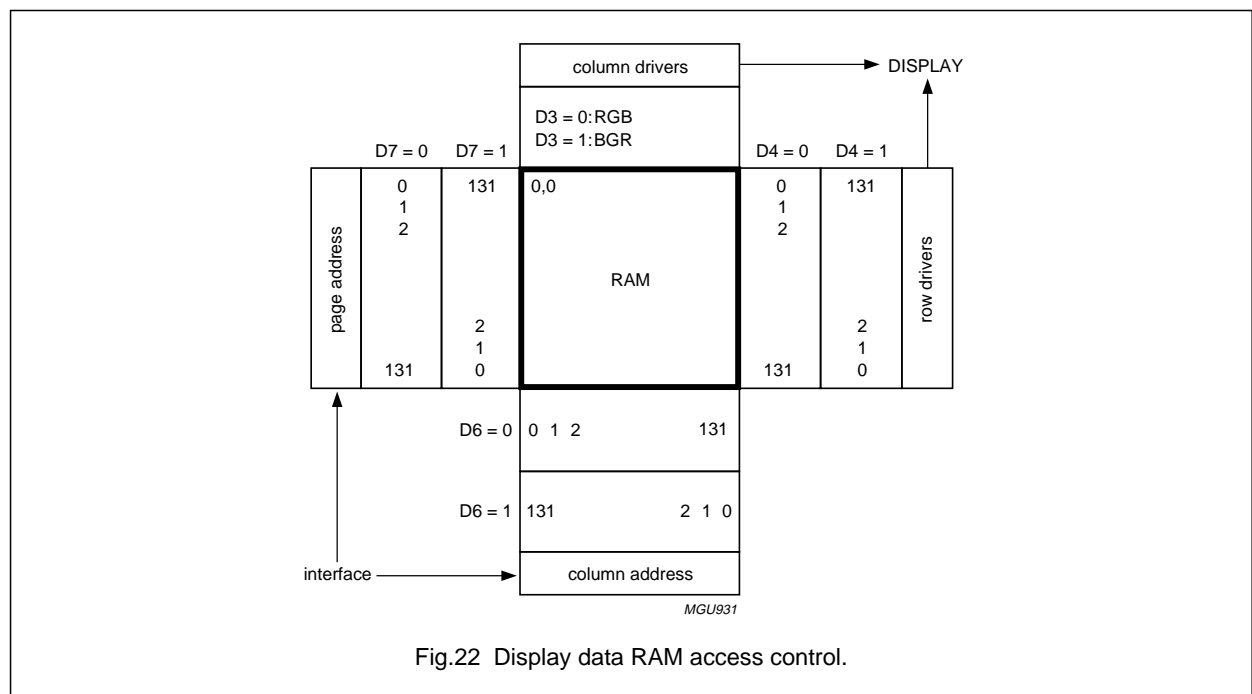


Fig.22 Display data RAM access control.

STN RGB - 132 × 132 × 3 driver

PCF8833

6.2.28 IDLE MODE OFF

The Idle mode off (IDMOFF) command turns off the Idle mode and the PCF8833 is working in the 4 kbyte colour mode. This command is similar to the Idle mode on command (IDMON); see Section 6.2.29.

Table 42 Idle mode off register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38H |

6.2.29 IDLE MODE ON

The Idle mode on (IDMON) command activates the Idle mode of the LCD driver in order to reduce the power consumption. When the Idle mode is switched on, the number of colours is reduced to 8 (only the MSB of data stored in the RAM is used). In addition to the reduction in the number of colours, the frame frequency can also be reduced. The frame frequency for the Idle mode can be programmed separately from the frame frequency in 4 kbyte colour mode; see Section 6.2.41.

Table 43 Idle mode on register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39H |

6.2.30 COLOUR INTERFACE PIXEL FORMAT

By using the Colour interface pixel format command (COLMOD) different interface RGB formats can be chosen. The choice of an RGB format also influences the way display data is transferred to the display data RAM via the interface; see Section 7.1.3.

The different interface RGB formats are given in Table 45.

Table 44 Colour interface pixel format register bits; note 1

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|----|----|----|---------|
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3AH |
| 1 | X | X | X | X | X | P2 | P1 | P0 | 03H |

Note

1. X = don't care.

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Table 45 Interface formats

| P2 | P1 | P0 | INTERFACE FORMATS |
|----|----|----|-----------------------------|
| 0 | 0 | 0 | no action |
| 0 | 0 | 1 | no action |
| 0 | 1 | 0 | 8-bit/pixel ⁽¹⁾ |
| 0 | 1 | 1 | 12-bit/pixel ⁽²⁾ |
| 1 | 0 | 0 | no action |
| 1 | 0 | 1 | 16-bit/pixel ⁽³⁾ |
| 1 | 1 | 0 | no action |
| 1 | 1 | 1 | no action |

Notes

1. PCF8833 is switched into 256 colour mode, 256 colours are mapped to the 4 kbyte RAM with a LUT; see Section 6.2.22.
2. PCF8833 is switched into 4 kbyte colour mode, which is also the reset state.
3. PCF8833 is switched into 64 kbyte colour mode, which is achieved by means of dithering.

6.2.31 SET V_{OP}

The set V_{OP} command (SETVOP) is used to program the optimum LCD supply voltage V_{LCD}.

The reset state of VPR[8:0] is 257DEC (13.88 V).

The optimum LCD supply voltage can be calculated as explained in Section 6.2.43. The V_{OP} value is programmed via the VPR register. Besides the VPR register the V_{OP} value can be calibrated by means of OTP cells or changed with the VCON register (see Fig.23).

Table 46 Set V_{OP} register bits; note 1

| D/C | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DEFAULT |
|-----|----|----|----|------------------|------------------|------------------|------------------|------------------|---------|
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0H |
| 1 | X | X | X | X | VPR ₈ | VPR ₇ | VPR ₆ | VPR ₅ | 08H |
| 1 | X | X | X | VPR ₄ | VPR ₃ | VPR ₂ | VPR ₁ | VPR ₀ | 01H |

Note

1. X = don't care.

The generated V_{LCD} can be calculated with equation (1). Figure 24 is the graphical equivalent to equation (1).

$$V_{LCD} = a + \langle MMVOPCAL[5:0] + VCON[6:0] + V_{PR}[8:0] \rangle \times b \quad (1)$$

Where:

- a is a fixed constant value; see Table 47
- b is a fixed constant value; see Table 47
- V_{PR}[8:0] is the programmed V_{OP} value; the programming range for V_{PR}[8:0] is 5 to 410 (19AH)
- MMVOPCAL[5:0] is the value of the offset stored in the OTP cells in twos complement format; see Section 15.1
- VCON[6:0] is the set contrast value which can be set via the interface and is in twos complement format; see Section 6.2.16.

The VOP[8:0] value must be in the V_{LCD} programming range as shown in Fig.24. Evaluating equation (1), values outside of the programming range indicated in Fig.24 may result. Calculated values below 0 will be mapped to V_{OP} = 0; resulting V_{OP} values higher than 445 will be mapped to V_{OP} = 445. An overview of the complete programming range of V_{LCD} can be found in Section 15.1.

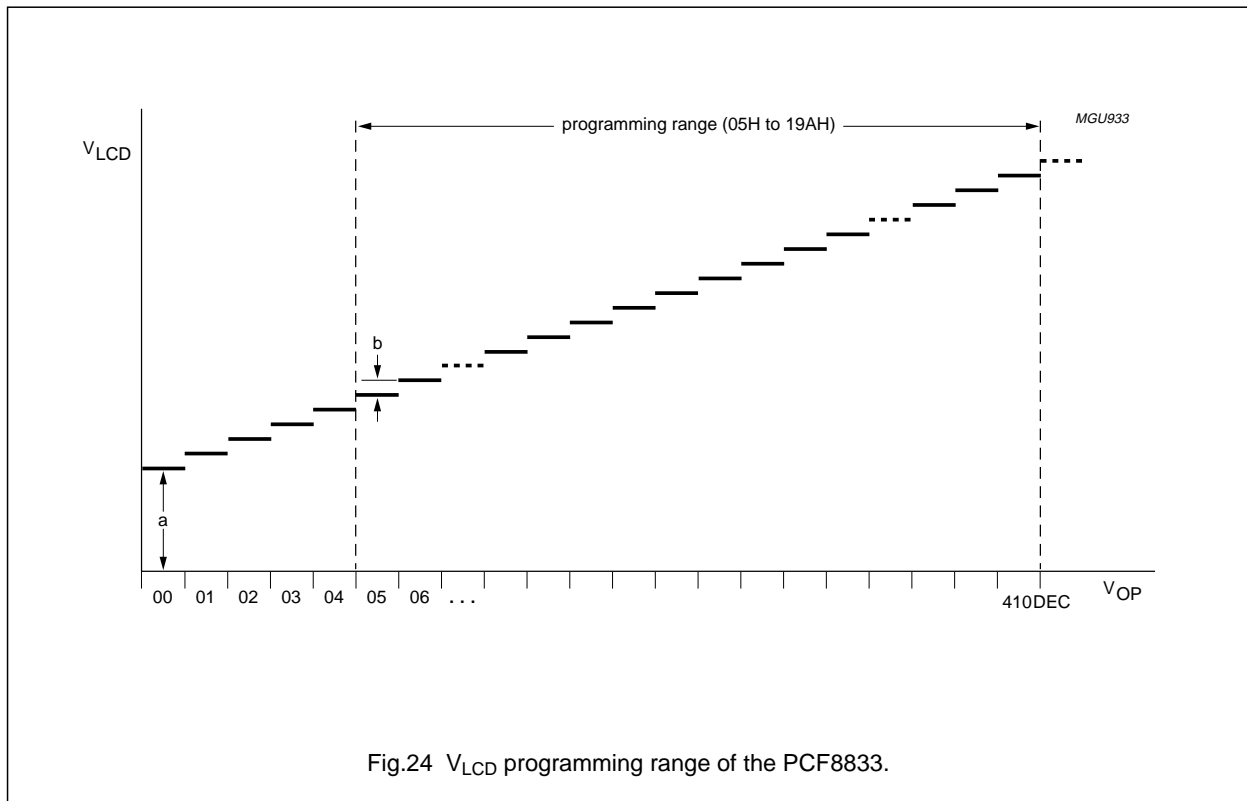
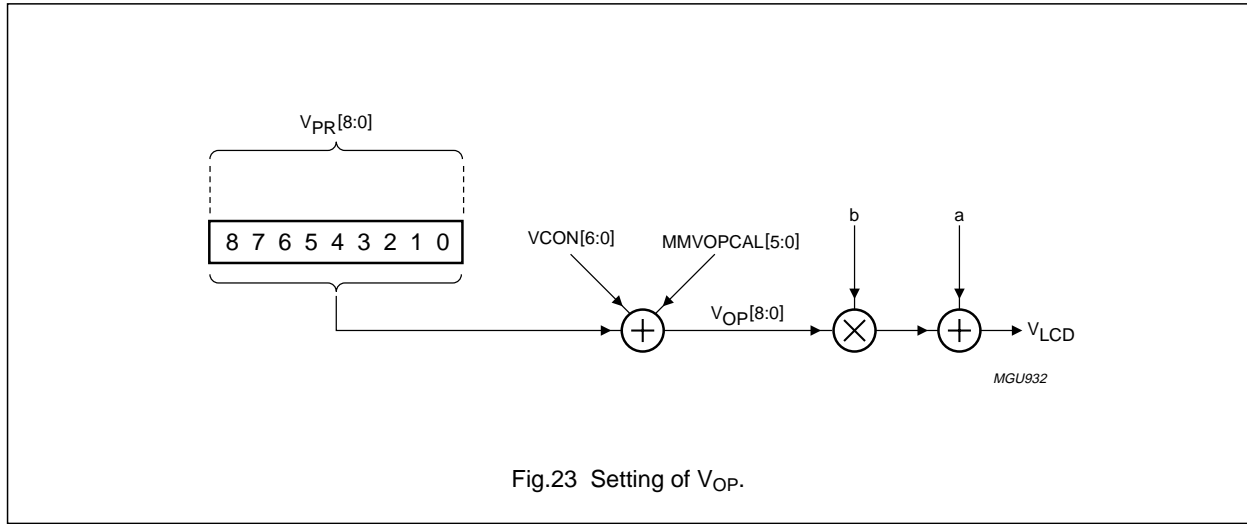
As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD} (20 V) the user has to ensure, while setting the V_{PR} register and selecting the temperature compensation, that under all conditions and including all tolerances the V_{LCD} remains below 20 V.

STN RGB - 132 × 132 × 3 driver

PCF8833

Table 47 Parameters of V_{LCD}

| SYMBOL | VALUE | UNIT |
|--------|-------|------|
| b | 0.04 | V |
| a | 3.6 | V |



STN RGB - 132 × 132 × 3 driver

PCF8833

6.2.32 BOTTOM ROW SWAP

The Bottom Row Swap (BRS) command enables the bottom rows of the PCF8833 to be swapped (mirrored) in order to make an optimum glass layout.

The function of the BRS command in combination with the function of the Top Row Swap (TRS) is illustrated in Figures 25, 26, 27 and 28. A description of the TRS function is given in Section 6.2.33.

The reset state of the BRS command is defined in Table 49.

Table 48 Bottom row swap register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|-----|---------|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | BRS | B4H |

Table 49 Bottom row swap reset state

| BIT | LOGIC 0 (RESET STATE) | LOGIC 1 |
|-----|------------------------------|--------------------------|
| BRS | bottom rows are not mirrored | bottom rows are mirrored |

6.2.33 TOP ROW SWAP

The Top Row Swap (TRS) command enables the top rows of the PCF8833 to be swapped (mirrored) in order to make an optimum glass layout.

The function of the TRS command in combination with BRS is illustrated in Figures 25, 26, 27 and 28. The description of BRS function can be found in Section 6.2.32.

The reset state of the TRS command is given in Table 51.

Table 50 Top row swap register bits

| D/C | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DEFAULT |
|-----|----|----|----|----|----|----|----|-----|---------|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | TRS | B6H |

Table 51 Top row swap reset state

| BIT | LOGIC 0 (RESET STATE) | LOGIC 1 |
|-----|---------------------------|-----------------------|
| TRS | top rows are not mirrored | top rows are mirrored |

STN RGB - 132 × 132 × 3 driver

PCF8833

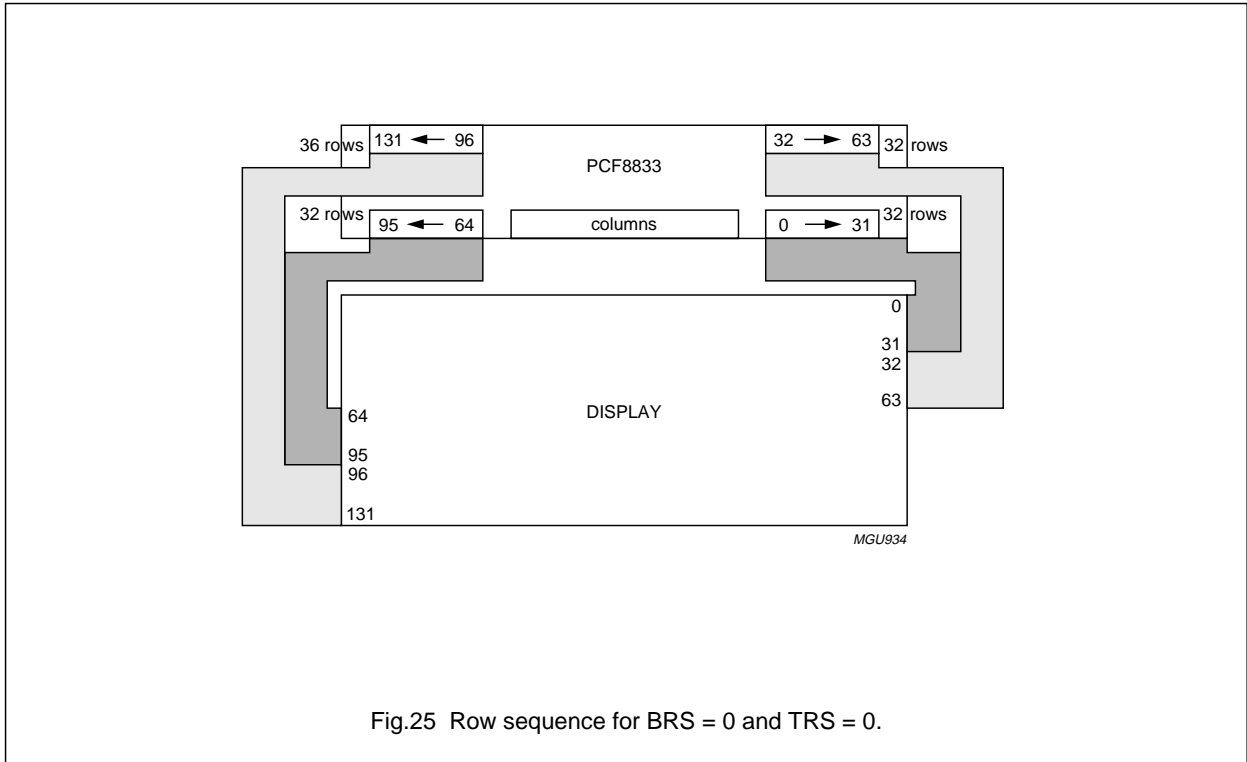


Fig.25 Row sequence for BRS = 0 and TRS = 0.

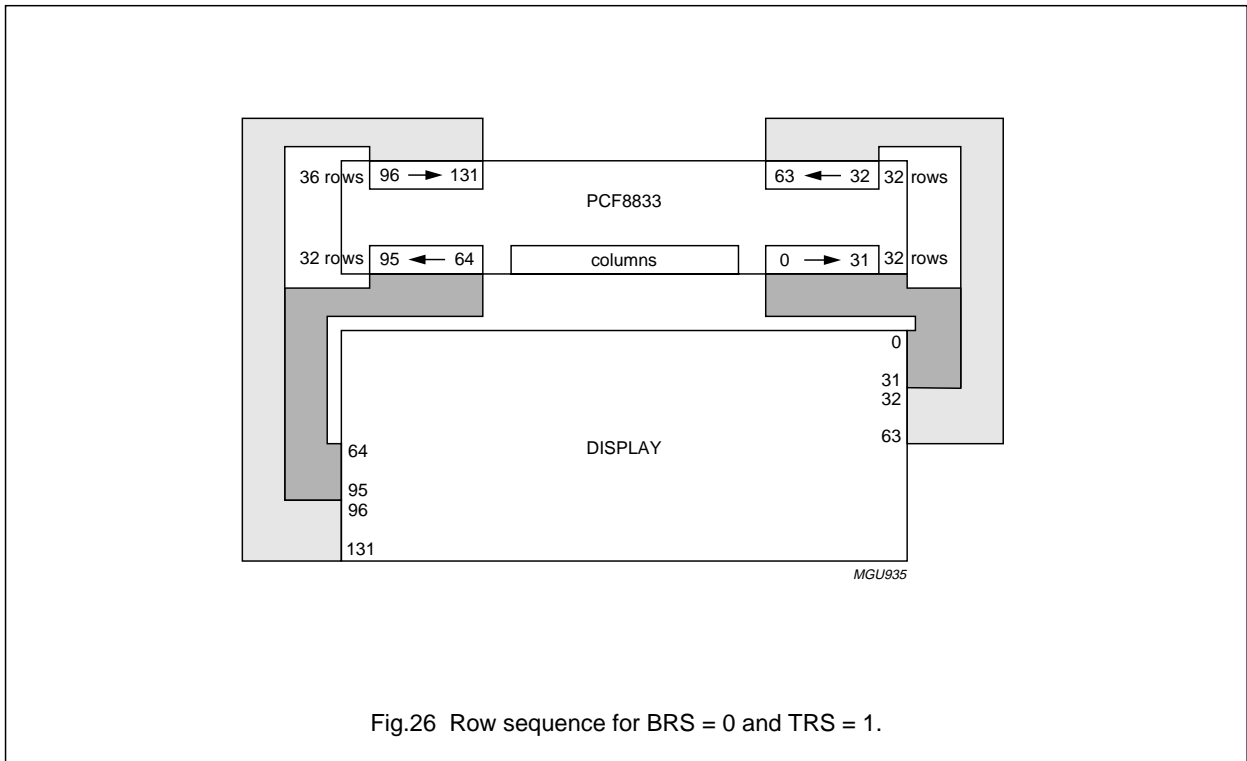


Fig.26 Row sequence for BRS = 0 and TRS = 1.

STN RGB - 132 × 132 × 3 driver

PCF8833

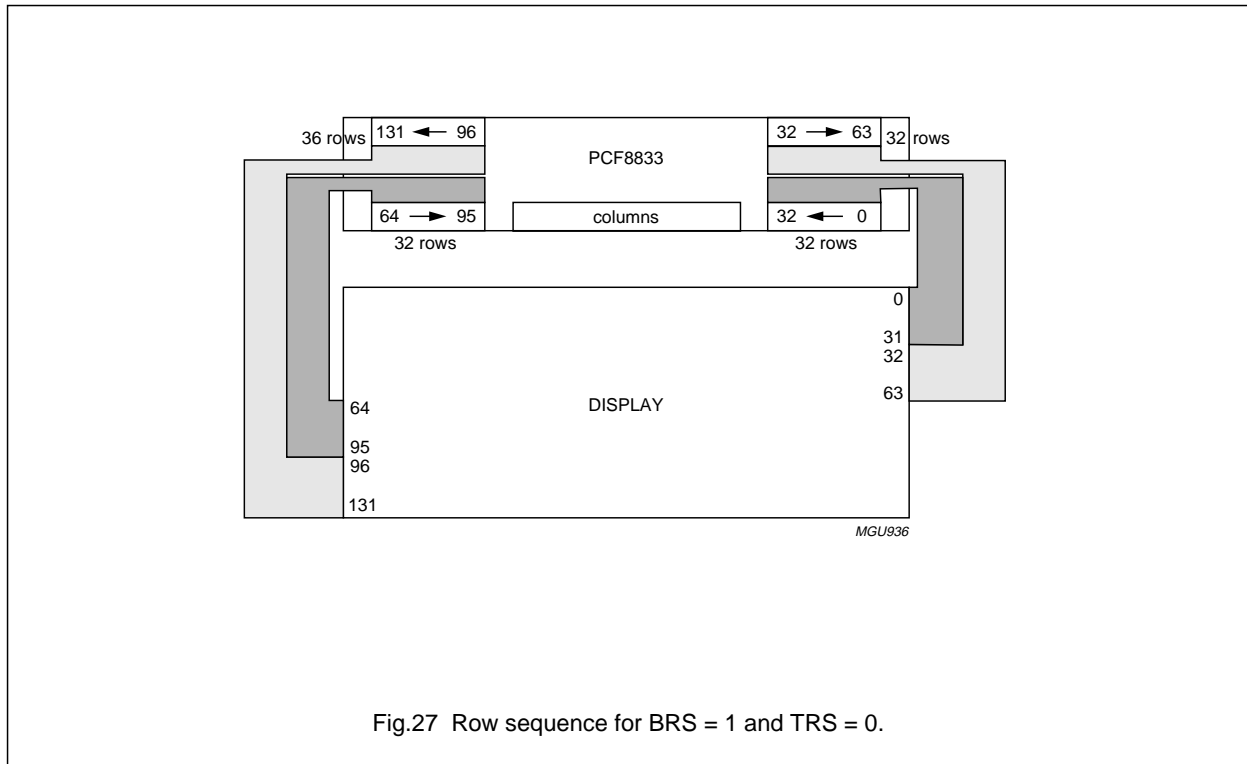


Fig.27 Row sequence for BRS = 1 and TRS = 0.

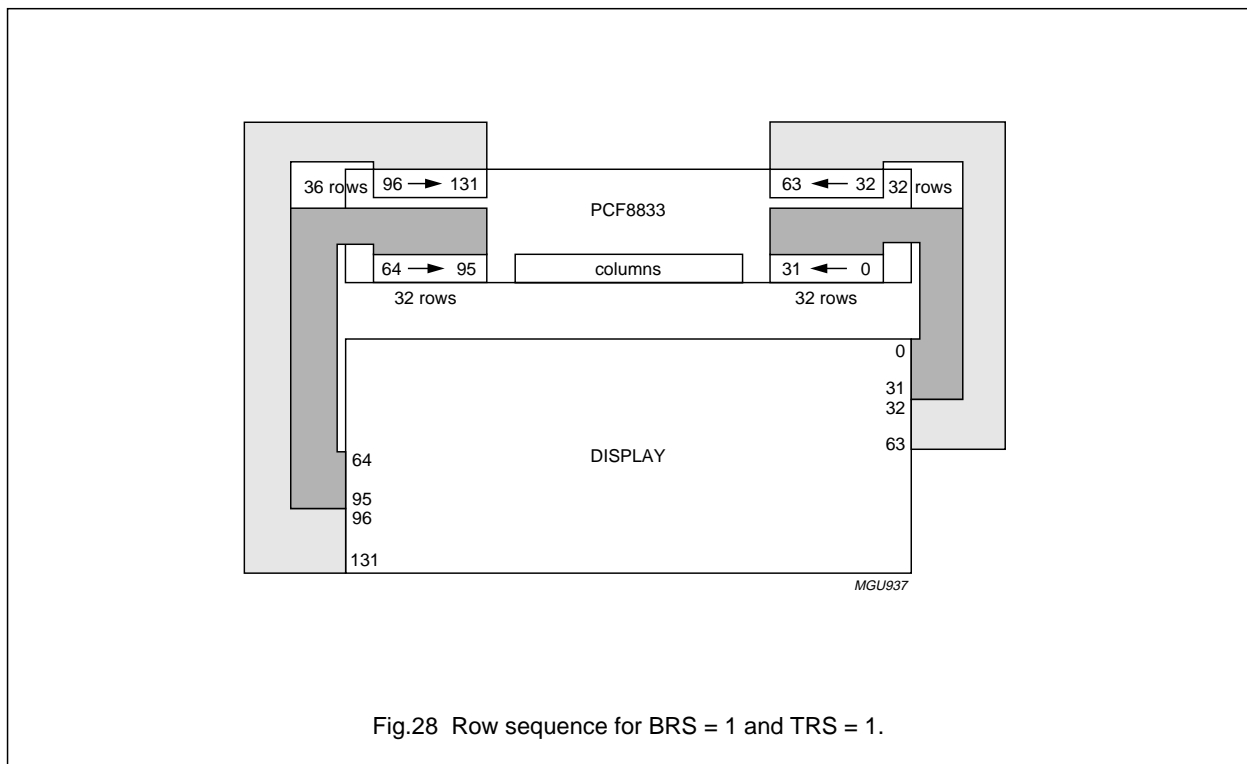


Fig.28 Row sequence for BRS = 1 and TRS = 1.

STN RGB - 132 × 132 × 3 driver

PCF8833

6.2.34 SUPER FRAME INVERSION

The Super frame inversion command (FINV), which is the inversion of the row functions after all rows are written to can be switched off for the PCF8833. When switched off, the inversion of the row functions will then only be done with N-line inversion. Inversion of the row functions is needed so as to avoid a DC component over the LCD display. A detailed description of the N-line inversion is given in Section 6.2.45.

The FINV control bit reset state is defined in Table 52.

Table 52 Super frame inversion register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|------|---------|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | FINV | B9H |

Table 53 Super frame inversion reset state

| BIT | LOGIC 0 | LOGIC 1 (RESET STATE) |
|------|------------------------------|-----------------------------|
| FINV | super frame inversion is off | super frame inversion is on |

6.2.35 DATA ORDER

The data order (DOR) of the data which will be written into the RAM can be changed (swapped).

The DOR command is explained and the reset state defined in Table 55.

Table 54 Data order register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|-----|---------|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | DOR | BAH |

Table 55 Data order reset state

| BIT | LOGIC 0 (RESET STATE) | LOGIC 1 |
|-----|-----------------------|---------------------------------|
| DOR | normal data order | MSB/LSB transposed for RAM data |

6.2.36 TEMPERATURE COMPENSATED FRAME FREQUENCY

The PCF8833 incorporates a temperature segmented frame frequency programming; see Section 6.2.41. This segmented frame frequency can be disabled by using the temperature compensated frame frequency (TCDFE) command.

The TCDFE control bit reset state is defined in Table 57.

When the non-segmented frame frequency is chosen, the frame frequency in segment B (DFB) is valid; see Section 6.2.41.

Table 56 Temperature compensated frame frequency register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|-------|---------|
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | TCDFE | BDH |

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Table 57 Temperature compensated frame frequency reset state

| BIT | LOGIC 0 | LOGIC 1 (RESET STATE) |
|-------|-------------------------------|---------------------------|
| TCDFE | non-segmented frame frequency | segmented frame frequency |

6.2.37 TEMPERATURE COMPENSATED V_{LCD}

The PCF8833 incorporates a temperature segmented V_{OP} programming; see Section 6.2.40. By using the temperature compensated V_{LCD} (TCVOPE) command the temperature segmented V_{LCD} can be disabled.

The TCVOPE control bit reset state is defined in Table 59.

When the non-segmented V_{LCD} programming is chosen the LCD supply voltage is flat, i.e. no compensation over the specified temperature range (offset V_T in Fig.30 is 0).

The TCVOPE command is also used to read back the temperature via the interface; see Section 6.2.44.

Table 58 Temperature segmented V_{LCD} register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|--------|---------|
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | TCVOPE | BFH |

Table 59 Temperature segmented V_{LCD} reset state

| BIT | LOGIC 0 | LOGIC 1 (RESET STATE) |
|--------|--------------------------------------|---|
| TCVOPE | no temperature compensated V_{LCD} | segmented temperature compensated V_{LCD} |

6.2.38 INTERNAL OR EXTERNAL OSCILLATOR

The Internal/external oscillator (EC) command selects the internal or external oscillator. When an external oscillator is used the external clock signal has to be connected to the OSC pad; see Section 7.6.

The EC control bit reset state is defined in Table 61.

Table 60 Internal/external oscillator register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|----|---------|
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | EC | COH |

Table 61 Internal/external oscillator reset state

| BIT | LOGIC 0 (RESET STATE) | LOGIC 1 |
|-----|-----------------------|------------------------|
| EC | internal oscillator | external clock applied |

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6.2.39 SET MULTIPLICATION FACTOR

The Set multiplication factor (SETMUL) command sets the multiplication factor of voltage multiplier 1. A detailed explanation of the LCD voltage supply architecture is given in Section 7.8.

The different multiplication factor settings for voltage multiplier 1 are given in Table 63.

Table 62 Set multiplication factor register bits; note 1

| D/C | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DEFAULT |
|-----|----|----|----|----|----|----|----|----|---------|
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2H |
| 1 | X | X | X | X | X | X | S1 | S0 | 03H |

Note

1. X = don't care.

Table 63 Multiplication factor settings voltage multiplier

| S1 | S0 | MULTIPLICATION FACTOR |
|----|----|----------------------------|
| 0 | 0 | 2 × multiplication |
| 0 | 1 | 3 × multiplication |
| 1 | 0 | 4 × multiplication |
| 1 | 1 | 5 × multiplication; note 1 |

Note

1. Reset state.

6.2.40 SET TCVOP SLOPES A, B, C AND D

The Set TCVOP slopes A, B, C and D (TCVOPAB and TCVOPCD) command splits the temperature range into 4 parts and can be programmed by using the following commands.

Due to the temperature dependency of the liquid crystals viscosity, the LCD controlling voltage V_{LCD} might have to be adjusted at different temperatures to maintain optimum contrast.

There are four equally spaced temperature regions. For each temperature region a different temperature coefficient can be selected. Each coefficient can be selected from a choice of eight different slopes, or multiplication factors (see Table 66) by setting TCVOPAB and TCVOPCD. The controlled V_{LCD} will not be changed linearly, but in 40 mV steps (parameter b in Table 47). Slopes SLA, SLB, SLC and SLD are overwritten by OTP values if these are set.

Table 64 Set TCVOP slopes A and B register bits; note 1

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|------------------|------------------|------------------|---|------------------|------------------|------------------|---------|
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C3H |
| 1 | X | SLB ₂ | SLB ₁ | SLB ₀ | X | SLA ₂ | SLA ₁ | SLA ₀ | 34H |

Note

1. X = don't care.

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Table 65 Set TCVOP slopes C and D register bits; note 1

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|------------------|------------------|------------------|---|------------------|------------------|------------------|---------|
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | C4H |
| 1 | X | SLD ₂ | SLD ₁ | SLD ₀ | X | SLC ₂ | SLC ₁ | SLC ₀ | 75H |

Note

1. X = don't care.

Table 66 Set TCVOP slopes multiplication factors; note 1

| SLA[2:0] SLB[2:0] SLC[2:0] SLD[2:0] | MA MB MC MD | SLOPE |
|--|----------------------|--------------|
| 111 | 1.250 | -53.33 mV/°C |
| 110 | 1.000 | -42.66 mV/°C |
| 101 | 0.875 | -37.33 mV/°C |
| 100 | 0.750 | -32.00 mV/°C |
| 011 | 0.625 | -26.66 mV/°C |
| 010 | 0.500 | -21.33 mV/°C |
| 001 | 0.375 | -16.00 mV/°C |
| 000 | 0.250 | -10.66 mV/°C |

Note

1. For the reset state refer to Table 4. Values overwritten by OTP.

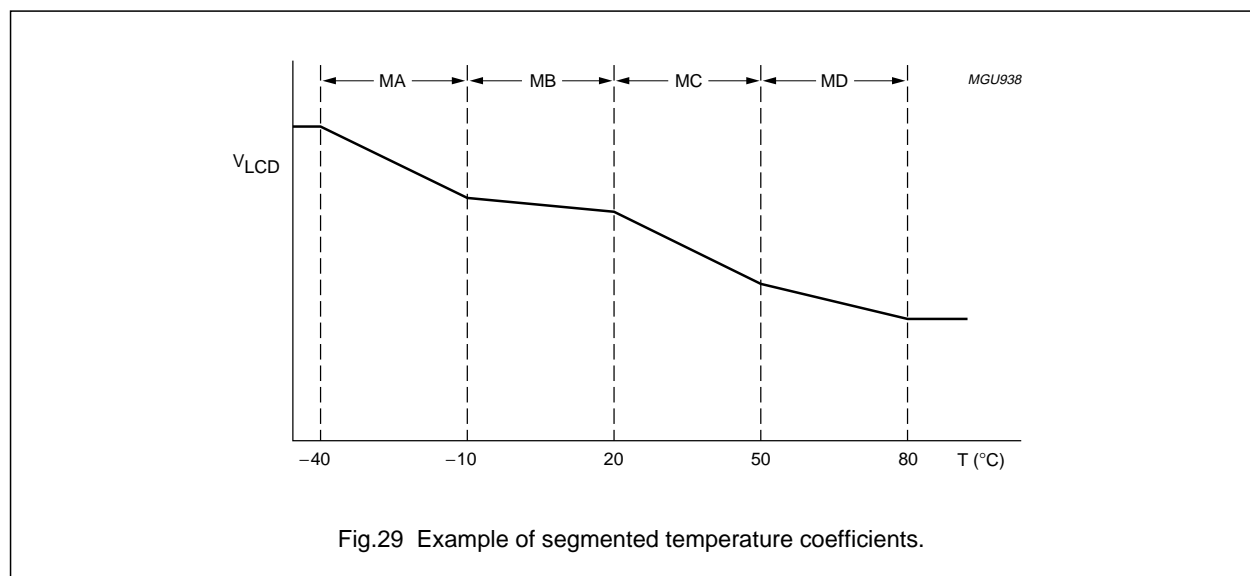


Fig.29 Example of segmented temperature coefficients.

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PCF8833

Temperature compensation is implemented by adding an offset to the V_{OP} value. Previously, in Section 6.2.31, V_{OP} was calculated by adding V_{PR} , V_{CON} and $MMVOPCAL$ settings together. Now, an additional offset V_T is added.

The final result for V_{LCD} calculation is a 9-bit positive number. Care must be taken by the user to ensure that the ranges of V_{PR} , $MMVOPCAL$, V_{CON} and temperature compensation do not cause clipping, and hence undesired results (see Fig.24). The adders will not permit overflow or underflow and will clamp results to either end of the range ($V_{OP} = 0$ or 445). Also, temperatures outside the range -40 to $+79$ °C will be clamped to the last valid offset.

The temperature readout generates an 8-bit result $TD[7:0]$. This temperature readout number is used for temperature compensation.

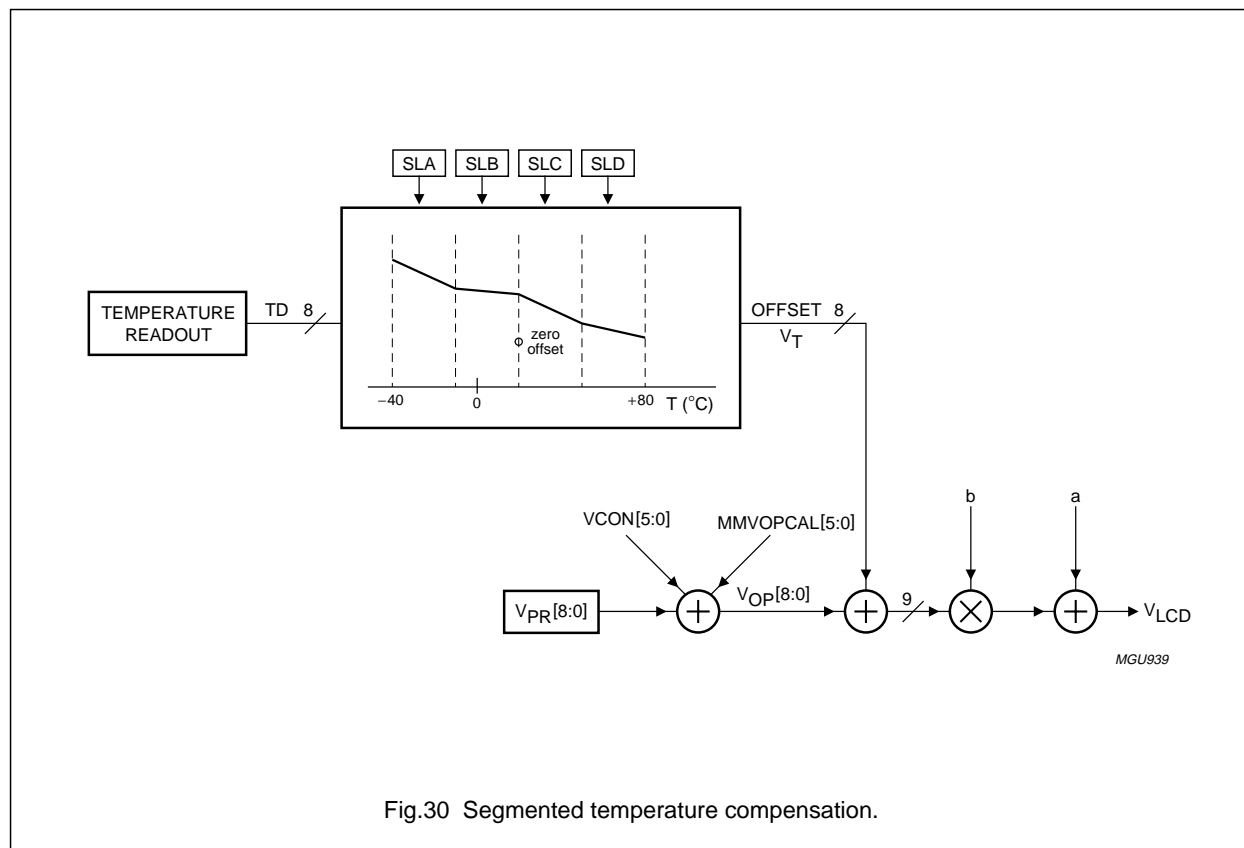
The resolution of the readout is $(-40 \text{ to } +80 \text{ °C})/128 = 0.9375 \text{ °C/LSB}$; where 0 represents -40 °C and 127 represents $+79$ °C; see Section 6.2.44.

The temperature readout function can also be used to read back the temperature value via the interface; see equation (12).

The offset value may be calculated from Table 67. The effect on V_{LCD} can be calculated by multiplying the offset value with the value of b .

For example $T = -8$ °C: $TD = 34$ and $MB = 0.5$:
 $V_{LCD(OS)} = 40 \text{ mV} \times (64 - 34) \times 0.5 = 600 \text{ mV}$.

A complete overview of the programming range of V_{LCD} can be found in Section 15.1.



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Table 67 Offset value

| TEMPERATURE RANGE | TD EQUIVALENT | OFFSET EQUATION VT |
|--------------------|---------------|---|
| <-40 °C | 0 | $32 \times (MB + MA)$ |
| -40 °C to < -10 °C | 0 to 31 | $(32 \times MB) + MA \times (32 - TD)$ |
| -10 to < 20 °C | 32 to 63 | $(64 - TD) \times MB$ |
| 20 °C to < 50 °C | 64 to 95 | $-(TD - 64) \times MC$ |
| 50 to < 80 °C | 96 to 127 | $-((32 \times MC) + MD \times (TD - 96))$ |
| ≥80 °C | >127 | $-(32 \times MC + 31 \times MD)$ |

6.2.41 FRAME FREQUENCY PROGRAMMING

The PCF8833 incorporates temperature segmented Frame frequency programming (TCDF). The temperature range is split into 4 areas as shown in Fig.31.

In each of the segments a Division Factor (DF) can be programmed which determines the Frame Frequency (FF). In equation (2) the frame frequency can be calculated from a given division factor.

$$FF = \frac{1}{DF} \times f_{osc}$$

(2)

Where f_{osc} is the oscillator frequency which is defined in Chapter 13.

The Divider Factor (DF) is a 7-bit number so the upper programming range is limited to 127DEC resulting in a minimum frame frequency of 35.8 Hz. The lower programming range is limited to 20DEC resulting in a maximum frame frequency of 227 Hz. The frame frequency is derived from the built-in oscillator, and thus the tolerance of the frame frequency has the same ratio as that given for the oscillator frequency; see Chapter 13.

When Partial mode is selected (see Sections 6.2.10 and 6.2.23) the same segmented frame frequencies will be used as for the full Display mode.

Table 68 Frame frequency programming register bits; note 1

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|------------------|------------------|------------------|------------------|------------------|------------------|------------------|---------|
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | C5H |
| 1 | X | DFA ₆ | DFA ₅ | DFA ₄ | DFA ₃ | DFA ₂ | DFA ₁ | DFA ₀ | 38H |
| 1 | X | DFB ₆ | DFB ₅ | DFB ₄ | DFB ₃ | DFB ₂ | DFB ₁ | DFB ₀ | 35H |
| 1 | X | DFC ₆ | DFC ₅ | DFC ₄ | DFC ₃ | DFC ₂ | DFC ₁ | DFC ₀ | 30H |
| 1 | X | DFD ₆ | DFD ₅ | DFD ₄ | DFD ₃ | DFD ₂ | DFD ₁ | DFD ₀ | 25H |

Note

1. X = don't care.

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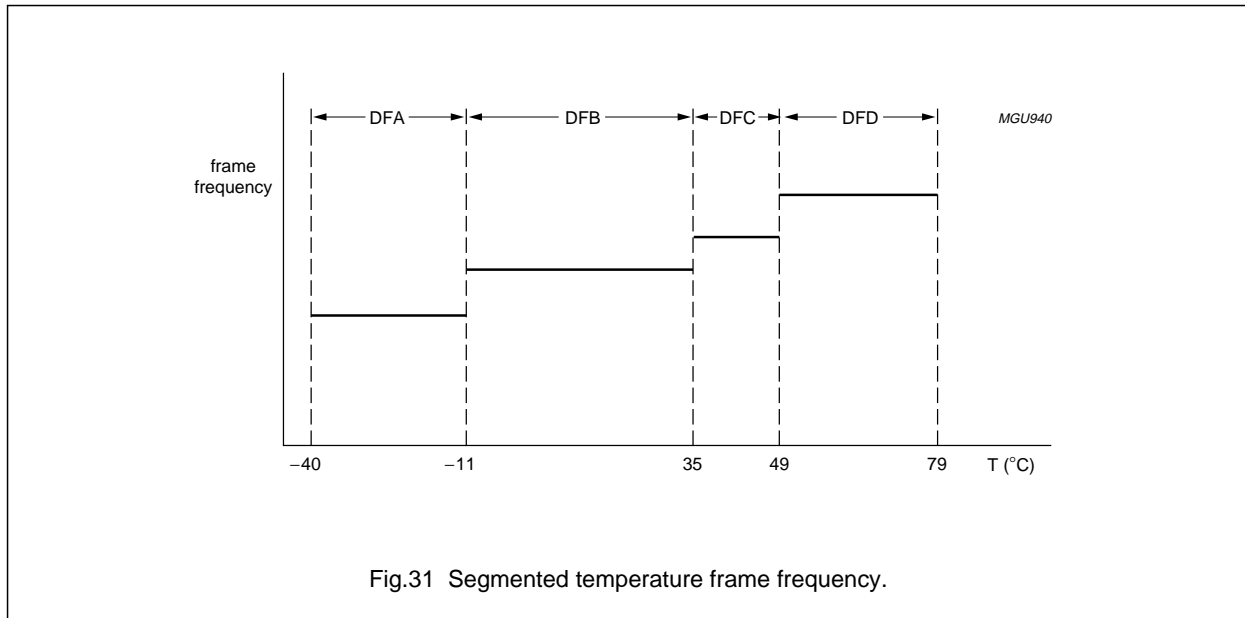


Fig.31 Segmented temperature frame frequency.

6.2.42 FRAME FREQUENCY PROGRAMMING IN 8-COLOUR MODE

When the Idle mode is selected (see Section 6.2.29) the frame frequency is determined from division factor DF8. In the Idle mode the PCF8833 works in 8-colour mode and therefore a lower frame frequency can be chosen which will be the same over the whole temperature range. Calculation of the frame frequency and determining the division factor is the same as explained in Section 6.2.41.

When Partial mode is selected (see Sections 6.2.10 and 6.2.23) the same frame frequency will be used as for the full Display mode in Idle mode.

Table 69 Frame frequency programming in 8-colour mode register bits; note 1

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|------------------|------------------|------------------|------------------|------------------|------------------|------------------|---------|
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | C6H |
| 1 | X | DF8 ₆ | DF8 ₅ | DF8 ₄ | DF8 ₃ | DF8 ₂ | DF8 ₁ | DF8 ₀ | 35H |

Note

1. X = don't care.

6.2.43 SET BIAS SYSTEM

The LCD supply voltage and the bias voltages, which can be chosen, depend on the Liquid Crystal (LC) that is used. In equation (3) the relationship between the V_{ON}/V_{OFF} ratio of LC parameters and the bias system (a) for a given display size (N) is given.

$$\frac{V_{ON}}{V_{OFF}} = \sqrt{\frac{a^2 + N + 2a}{a^2 + N - 2a}} \quad (3)$$

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When the required bias system (a) is defined, the LCD supply voltage for a display size N can be determined; see equation (4).

$$V_{\text{LCD}} = 2a \times V_{\text{ON}} \times \sqrt{\frac{N}{P(a^2 + N + 2a)}} \quad (4)$$

The parameter P in equation (4) is the number of simultaneous selected rows. For the maximum number of rows of 132, P = 4 is chosen. When partial Display mode is selected the P value is set to 1 internally.

The bias voltages needed in a MRA LCD driver depends on the number of simultaneous selected rows (P). The bias voltages of the PCF8833 are given for P = 4 and P = 1; see Fig.32. In the PCF8833 the maximum column voltage (GMAX) is always lower or equal to the row voltage F.

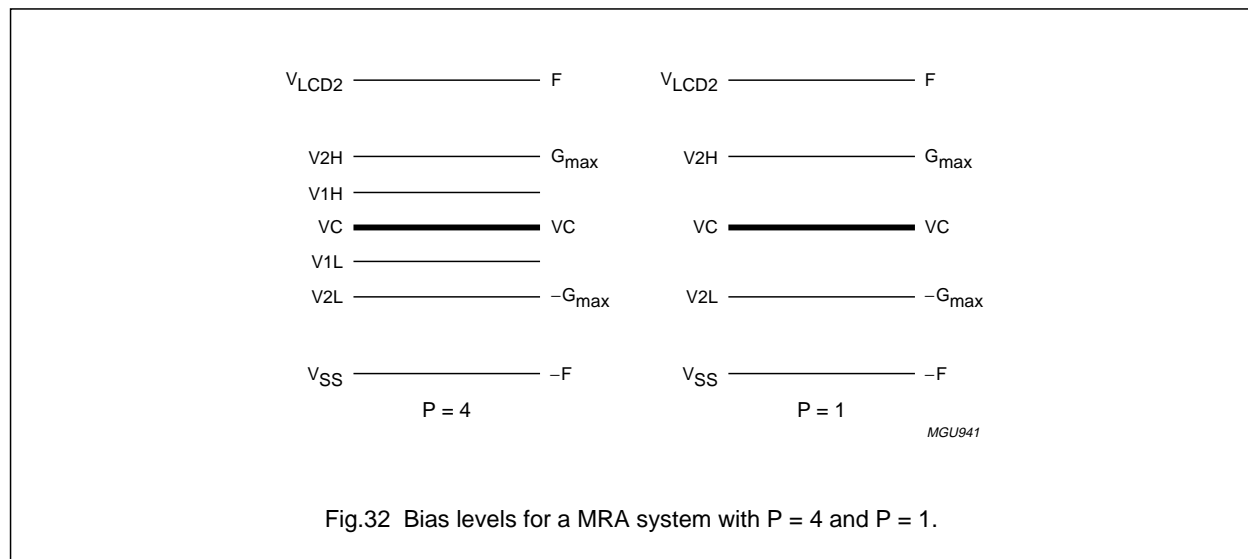


Fig.32 Bias levels for a MRA system with P = 4 and P = 1.

The bias voltage levels are a function of the row voltage F and a:

$$F = \frac{V_{\text{LCD}}}{2} \quad (5)$$

$$F \geq G_{\text{max}} \quad (6)$$

$$F = \frac{G_{\text{max}} \times a}{p} \quad (7)$$

$$\frac{F}{G_{\text{max}}} = \frac{a}{p} \quad (8)$$

Depending on the value of p, the bias levels are set in the ratio of:

$$p = 1: \alpha R - 2R - 2R - \alpha R$$

$$p = 4: \alpha R - R - R - R - \alpha R$$

Where the value of α is in the range from 0 to 4.

The value of F is determined by $(\alpha + 2) \times R$ and the value of G_{max} is determined by $2 \times R$.

The relationship between the ratio F/G_{max} and α :

$$\frac{F}{G_{\text{max}}} = \frac{a}{p} = \frac{(\alpha + 2) \times R}{2 \times R} = \frac{(\alpha + 2)}{2} = 1 + \frac{\alpha}{2} \quad (9)$$

or:

$$\alpha = \left(\frac{F}{G_{\text{max}}} - 1 \right) \times 2 \quad (10)$$

The relation between a and α for a given p is the following:

$$a = \left(\frac{\alpha}{2} + 1 \right) \times p \quad \alpha = \left(\frac{a}{p} - 1 \right) \times 2 \quad (11)$$

This leads to the following bias systems given in Table 70.

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Table 70 Bias system ratios

| VB[3:0] | F/G _{max} | α | a | |
|---------|--------------------|------|-------------------------------|--------------------------------|
| | | | P = 1 (N = 32) ⁽¹⁾ | P = 4 (N = 132) ⁽¹⁾ |
| 0000 | 1.000 | 0.00 | not allowed | not allowed |
| 0001 | 1.250 | 0.50 | | |
| 0010 | 1.375 | 0.75 | | |
| 0011 | 1.500 | 1.00 | | |
| 0100 | 1.625 | 1.25 | 1.500 | |
| 0101 | 1.750 | 1.50 | 1.625 | |
| 0110 | 1.875 | 1.75 | 1.750 | |
| 0111 | 2.000 | 2.00 | 1.875 | 8.0 |
| 1000 | 2.125 | 2.25 | 2.000 | 8.5 |
| 1001 | 2.250 | 2.50 | 2.125 | 9.0 |
| 1010 | 2.375 | 2.75 | 2.250 | 9.5 |
| 1011 | 2.500 | 3.00 | 2.375 | 10.0 ⁽²⁾ |
| 1100 | 2.625 | 3.25 | 2.500 | not allowed |
| 1101 | 2.750 | 3.50 | 2.625 | |
| 1110 | 2.875 | 3.75 | 2.750 | |
| 1111 | 3.000 | 4.00 | 2.875 | |
| | | | 3.000 | |

Notes

- For Partial mode internally P = 1 is set, otherwise P = 4 is selected. Limitations for Partial mode given in Section 6.2.43.2 for respectively for full Display mode given in Section 6.2.43.1 have to be taken into account.
- Reset state.

Table 71 Set bias system register bits; note 1

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|-----------------|-----------------|-----------------|-----------------|---------|
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | C7H |
| 1 | X | X | X | X | VB ₃ | VB ₂ | VB ₁ | VB ₀ | 0BH |

Note

- X = don't care.

6.2.43.1 Limitations on bias voltages in Normal modeV_{DD1}: 1.5 to 3.3 VV_{LCD1}: 5.5 to 11 VV_{LCD2}: 10 to 20 V(V_{LCD2} - V_{LCD1}): 4.5 to 9 V

$$\left(\frac{V_{LCD2}}{2} - V_{LVD1}\right) = 0 \text{ to } 1 \text{ V}$$

but for V_{LCD2}: 10 to 11 V:

$$\left(\frac{V_{LCD2}}{2} - V_{LCD1}\right) = 0 \text{ to } 0.5 \text{ V}$$

6.2.43.2 Limitations on bias voltages in Partial modeV_{DD1}: 1.5 to 3.3 VV_{LCD1}: 2.9 to 12 VV_{LCD2}: 3.8 to 12 V

$$(V_{LCD2} - V_{LCD1})_{\max} = 0.5 \text{ V}$$

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PCF8833

6.2.44 TEMPERATURE READBACK

The PCF8833 has a built-in temperature readback (RDTEMP) measurement device. The measured value is provided as an 8-bit digital value TD[7:0] which can be read back via the interface.

The temperature can be determined from TD[7:0] using the following formula:

$$T = (0.9375 \times TD - 40)^\circ\text{C} \quad (12)$$

Temperature measurements are started automatically every ten seconds when the digital temperature compensation is active (default).

A measurement can be initiated by sending the instruction to set TCVOPE (to either logic 1 or logic 0), irrespective of whether temperature compensation is disabled or not.

After initialization, the measurement will take approximately 5 ms to complete. It is recommended to read the register twice to qualify the returned result, especially if the measurement is triggered automatically.

The input and output data format for the temperature readback is given in Table 73.

Table 72 Temperature readback register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|---|---------|
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | C8H |

Table 73 Temperature readback data format

| SYMBOL | D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|---------|-----|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| (S)DIN | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | C8H |
| (S)DOUT | – | TD[7] | TD[6] | TD[5] | TD[4] | TD[3] | TD[2] | TD[1] | TD[0] | XX |

6.2.45 N-LINE INVERSION

The N-line inversion (NLI) command inverts the row functions after N-line row time slots in order to avoid a DC component on the LCD display. Thus, when N-line is set to 19DEC inversion of the row functions will occur after 76 rows.

With FINV = 1 (see Section 6.2.34) the super-frame inversion is active and the NLI counter always starts at super-frame start.

When FINV = 0 a DC voltage may remain on the display depending on the NLI setting. When FINV = 0 and NLI = 0 there is no inversion, which results in a DC voltage on the display.

Table 74 N-line inversion register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|---------|
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | C9H |
| 1 | NLI ₇ | NLI ₆ | NLI ₅ | NLI ₄ | NLI ₃ | NLI ₂ | NLI ₁ | NLI ₀ | 13H |

Table 75 N-line inversion

| NLI[7:0] | DESCRIPTION |
|-----------|---|
| 0000 0000 | no N-line inversion (super frame inversion) |
| 0000 0001 | inversion after 4 rows in full Display mode or 1 row in Partial mode |
| 0000 0010 | inversion after 8 rows in full Display mode or 2 rows in Partial mode |
| : | : |

STN RGB - 132 × 132 × 3 driver

PCF8833

6.2.46 READBACK

The PCF8833 can be identified when the readback commands (RDID1, RDID2 and RDID3) are sent via the interface. When the readback command is sent, the PCF8833 will send back an 8-bit number.

Depending on the SCLK speed the readback bit D7 might get corrupted. When the speed is reduced to at least half of the specified maximum speed, at least for the D7 bit, the transferred bit is valid.

ID1 is the manufacture ID and is hardwired in the PCF8833.

ID2 is the version ID and is programmed in the module maker OTP cells; see Chapter 15.

ID3 is the module ID and is programmed in the module maker OTP cells; see Chapter 15.

Table 76 RDID1 data format

| SYMBOL | D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|---------|-----|---|---|---|---|---|---|---|---|---------|
| (S)DIN | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DAH |
| (S)DOUT | – | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45H |

Table 77 RDID2 data format; note 1

| SYMBOL | D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|---------|-----|---|---|---|---|---|---|---|---|---------|
| (S)DIN | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DBH |
| (S)DOUT | – | X | X | X | X | X | X | X | X | 80H |

Note

1. X = don't care.

Table 78 RDID3 data format; note 1

| SYMBOL | D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|---------|-----|---|---|---|---|---|---|---|---|---------|
| (S)DIN | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DCH |
| (S)DOUT | – | X | X | X | X | X | X | X | X | 03H |

Note

1. X = don't care.

6.2.47 ENABLE OR DISABLE FACTORY DEFAULTS (SFD)

The Enable or disable factory defaults (SFD) command will enable or disable the factory defaults stored in the MMOTP cells; see Section 15.2. These factory defaults can be set by the module maker. If the OTP bit EFD (enable factory defaults) has been set, these values can not be changed via the interface and the SFD command will have no effect. Otherwise, the data specified by commands will only be used if SFD is set to logic 0.

The reset state of the SFD is defined in Table 80.

Table 79 Enable/disable factory defaults register bits

| D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT |
|-----|---|---|---|---|---|---|---|-----|---------|
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | SFD | EFH |

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Table 80 Enable/disable factory defaults reset state

| BIT | LOGIC 0 | LOGIC 1 (RESET STATE) |
|-----|---|-----------------------------|
| SFD | registers must be set via the interface | OTP programmed data is used |

7 FUNCTIONAL DESCRIPTION**7.1 MPU interfaces**

The PCF8833 can interface to a microcontroller with an 8-bit parallel or a serial interface to transmit both data and commands to the PCF8833.

7.1.1 HARDWIRED INTERFACE SELECTION

The selection of a given interface is done by setting pins PS0, PS1 and PS2 as shown in Table 81. Inputs PS1 and PS2 must be connected to V_{DD1} or V_{SS1} .

Table 81 Interface selection; note 1

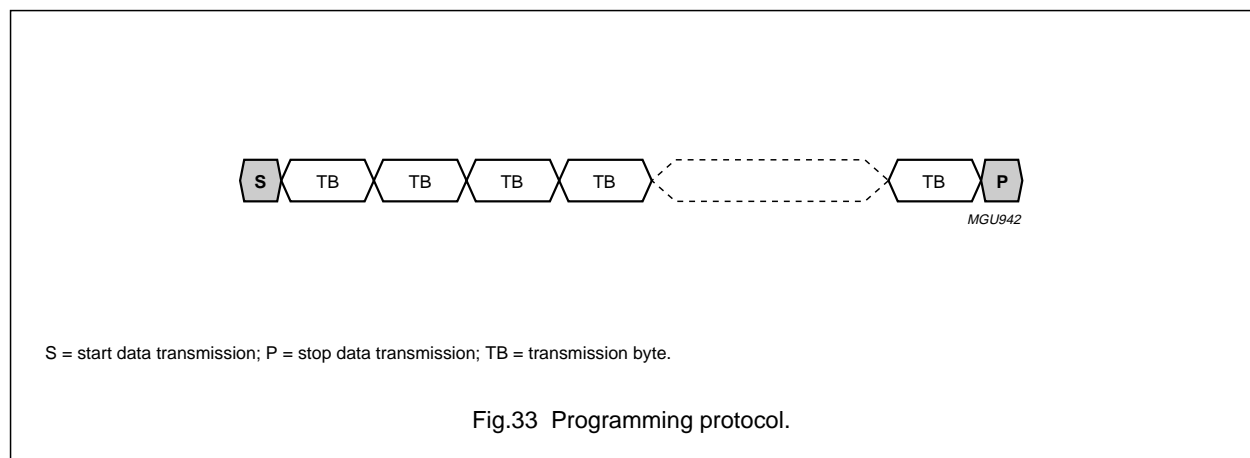
| PS2 | PS1 | PS0 | INTERFACE | READBACK SELECT |
|-----|-----|-----|-----------------|------------------------------|
| X | X | 0 | serial (3-line) | via the read instruction |
| X | X | 1 | 8080 MPU basic | \overline{RD} write strobe |

Note

1. X = don't care.

7.1.2 GENERAL PROTOCOL

The generally supported protocol for programming the LCD driver is shown in Fig.33.



STN RGB - 132 × 132 × 3 driver

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7.1.3 DISPLAY DATA FORMATTING

Different display data formats are available because different colour depths are supported by the PCF8833. The colour depths supported are as follows:

- 4 kbyte colours (12-bit/pixel), RGB 4 : 4 : 4 bits input; see Table 82. The data coming from the interface is directly stored in RAM.
- 65 kbyte colours (16-bit/pixel), RGB 5 : 6 : 5 bits input; see Table 83. The 16-bit data coming from the interface is mapped by means of dithering to 12-bit data. The dithered 12-bit data is then stored in the RAM.
- 256 colours (8-bit/pixel), RGB 3 : 3 : 2 bits input; see Table 84. The 8-bit data coming from the interface is mapped by means of the Look-Up Table (LUT) (see Section 6.2.22) to 12-bit data. The mapped 12-bit data is then stored in the RAM.

There are 3 bytes used to define 2 pixels with the 12-bit colour depth information; see Table 82. The most significant bits are R3, G3 and B3. Data is transferred to the RAM only when all the information i.e. RGB data of that particular pixel is sent.

There are 2 bytes used to transfer 1 pixel with the 16-bit colour depth information; see Table 83. The most significant bits are R4, G5 and B4. When the data transfer is stopped after the first write, the data is not transferred to the display data RAM. The 16-bit data coming from the interface is mapped by means of dithering to 12-bit data. The dithered 12-bit data is then stored in the RAM.

In one byte, 1 pixel is transferred with the 8-bit colour depth information; see Table 84. The most significant bits are R2, G2 and B1. The 8-bit data coming from the interface is mapped by means of a look-up table (see Section 6.2.22) to 12-bit data. The mapped 12-bit data is then stored in the RAM.

Table 82 Write data for RGB 4 : 4 : 4 bits input

| BYTE | D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 1st write | 1 | R ₃ | R ₂ | R ₁ | R ₀ | G ₃ | G ₂ | G ₁ | G ₀ |
| 2nd write | 1 | B ₃ | B ₂ | B ₁ | B ₀ | R ₃ | R ₂ | R ₁ | R ₀ |
| 3rd write | 1 | G ₃ | G ₂ | G ₁ | G ₀ | B ₃ | B ₂ | B ₁ | B ₀ |

Table 83 Write data for RGB 5 : 6 : 5 bits input

| BYTE | D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 1st write | 1 | R ₄ | R ₃ | R ₂ | R ₁ | R ₀ | G ₅ | G ₄ | G ₃ |
| 2nd write | 1 | G ₂ | G ₁ | G ₀ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ |

Table 84 Write data for RGB 3 : 3 : 2 bits input

| BYTE | D/C | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 1st write | 1 | R ₂ | R ₁ | R ₀ | G ₂ | G ₁ | G ₀ | B ₁ | B ₀ |

7.2 Display data RAM and access arbiter

7.2.1 DISPLAY DATA RAM

The PCF8833 has an integrated 132 × 132 × 12-bit single port static RAM. This 209 kbit memory allows a 132 × 132 (RGB) image with a 12-bpp resolution (4 kbyte colour) to be stored on-chip.

STN RGB - 132 × 132 × 3 driver

PCF8833

7.2.2 RAM ACCESS ARBITER

The function of the arbiter is to handle the data flow. If a write access is done on the RAM and a read access is requested at the same time, then the arbiter will ensure that there are no data collisions. Writing data to the RAM has priority. Therefore no handshaking is done at the interface side and the data can be applied to the interface without having data read/write errors on the RAM.

7.2.3 WR ADDRESS COUNTER

The address counter sets the addresses of the display data RAM for writing.

Data is written pixel wise into the RAM of the PCF8833. The data for one pixel is collected (RGB 4 : 4 : 4 bit) before it is written into the display data RAM. The RAM locations are addressed by the address pointers. The address ranges are $X = 0$ to $X = 131$ (83H) and $Y = 0$ to $Y = 131$ (83H). Addresses outside of these ranges are not allowed.

Before writing to the RAM a window must be defined into which data will be written. The window is programmable via the command registers x_s and y_s (designating the start address) and x_e and y_e (designating the end address).

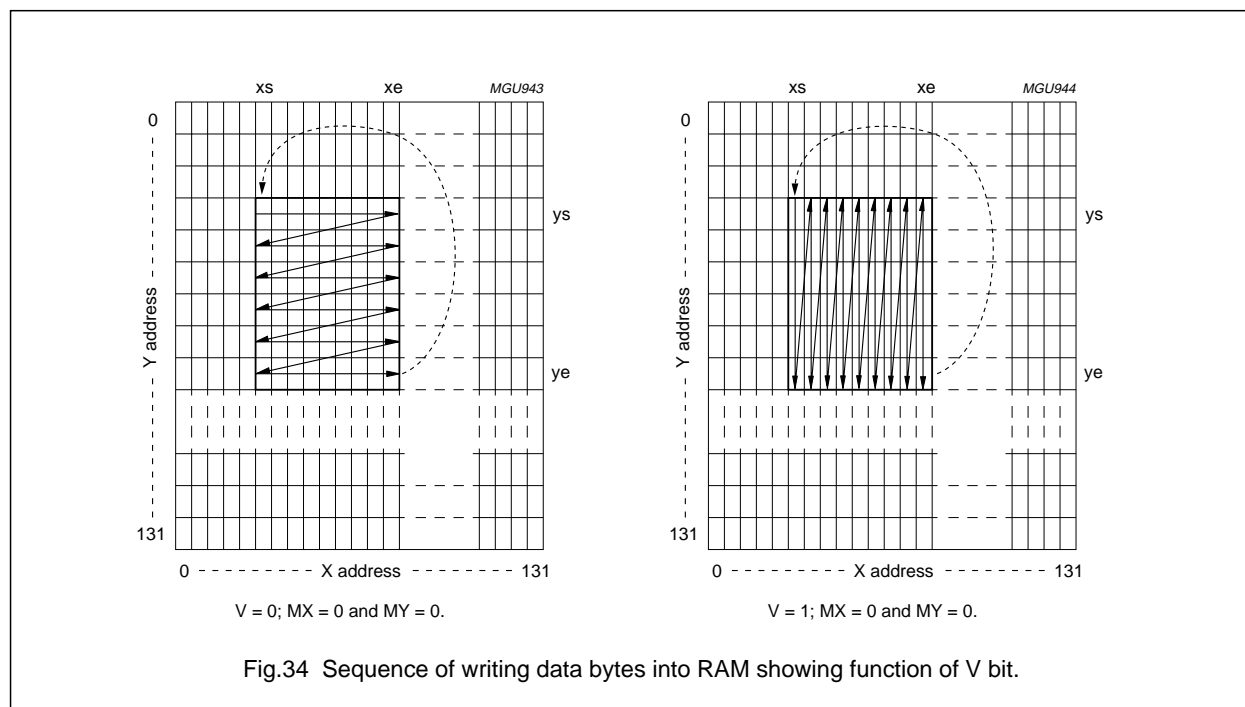
For example, if the whole display content is written, the window will be defined by the following values: $x_s = 0$ (0H), $y_s = 0$ (0H), $x_e = 131$ (83H) and $y_e = 131$ (83H).

In the vertical addressing mode ($V = 1$), the Y address increments after each pixel. After the last Y address ($Y = y_e$), Y wraps around to y_s and X increments to address the next column. In horizontal addressing mode ($V = 0$), the X address increments after each pixel. After the last X address ($X = x_e$), X wraps around to x_s and Y increments to address the next row. After the very last address ($X = x_e$ and $Y = y_e$) the address pointers wrap around to address ($X = x_s$ and $Y = y_s$).

For flexibility in handling a wide variety of display architectures, the command 'Memory Data Access Control (MADCTL)' (see Section 6.2.27) defines flags MX and MY, which allows mirroring of the X and Y addresses. All combinations of flags are allowed. Figures 34, 35 and 36 show the possible combinations of writing to the display RAM. When MX, MY and V is changed, the data must be re-written to the display RAM.

7.2.4 DISPLAY ADDRESS COUNTER

The display address counter generates the addresses for readout of the display data RAM.



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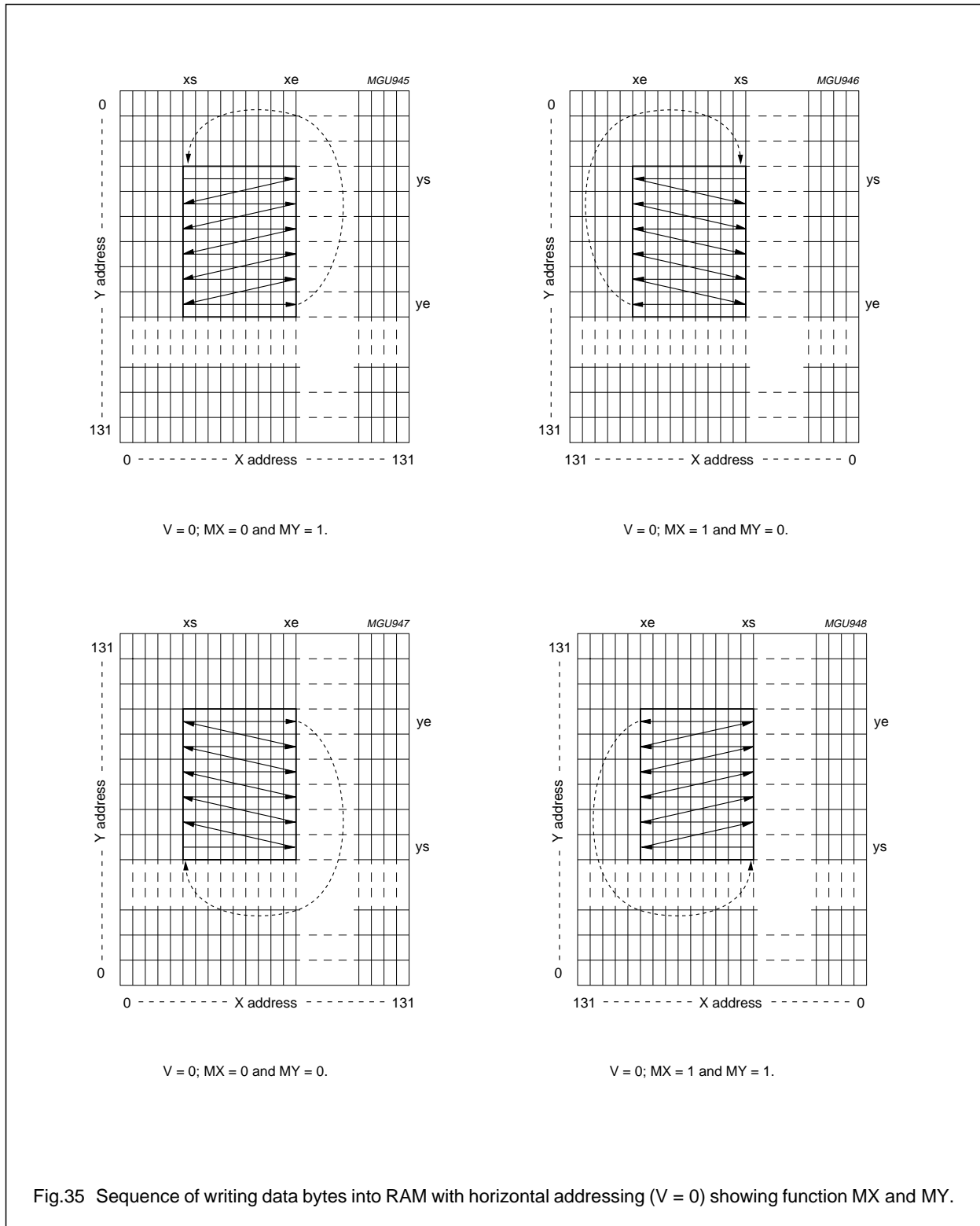


Fig.35 Sequence of writing data bytes into RAM with horizontal addressing ($V = 0$) showing function MX and MY.

STN RGB - 132 × 132 × 3 driver

PCF8833

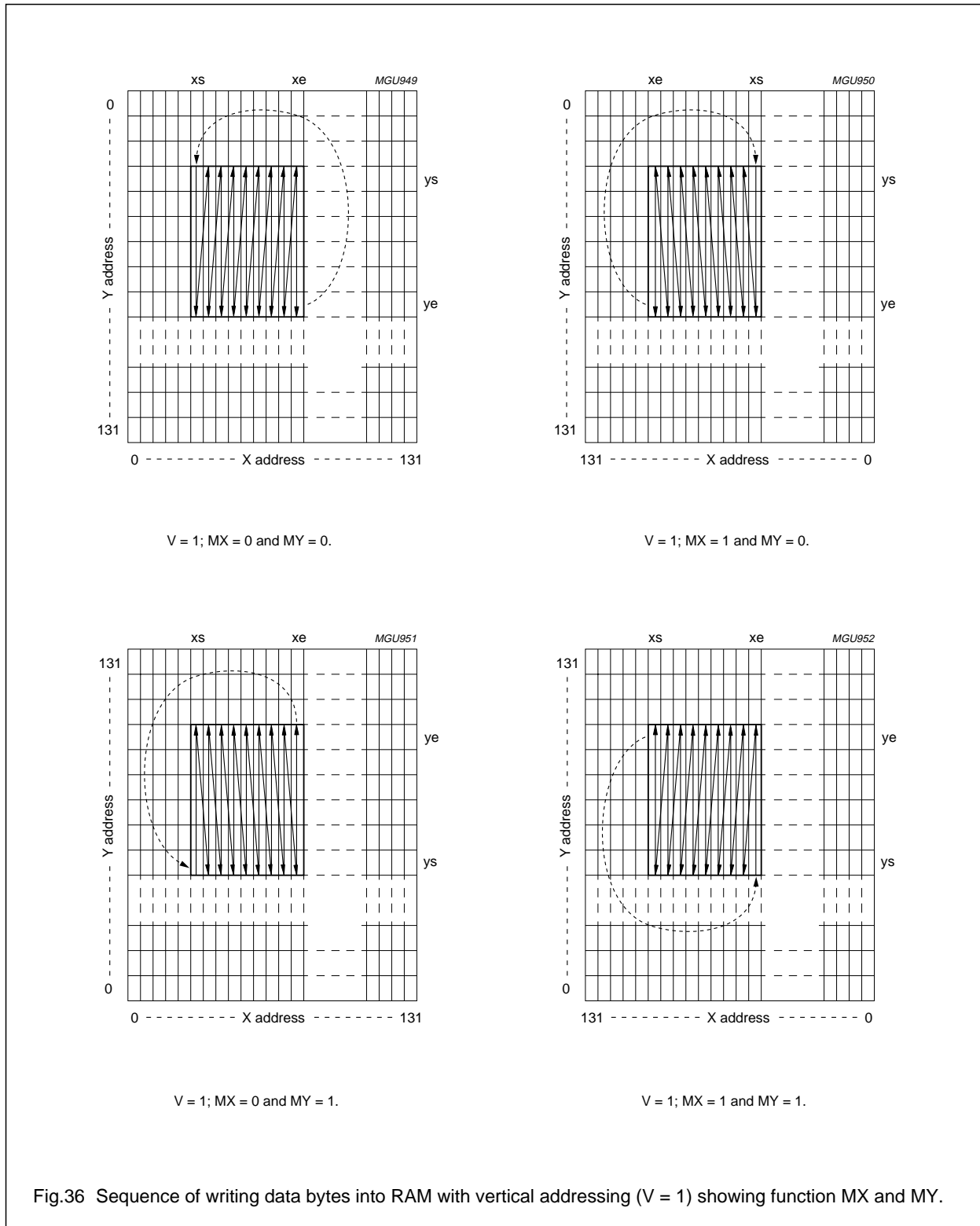


Fig.36 Sequence of writing data bytes into RAM with vertical addressing (V = 1) showing function MX and MY.

STN RGB - 132 × 132 × 3 driver

PCF8833

7.3 Command decoder

The command decoder identifies command words arriving at the interface and routes the following data bytes to their destination. The command set is given in Chapter 6.

7.4 Grey scale controller

For a grey scale driving scheme, Frame Rate Control (FRC) with carefully controlled mixing of the FRC pattern on each pixel is used. The special mixing ensures that the pattern placed on each pixel is different from each of its neighbours. In frame rate control 16 frames form together to produce a super-frame. All 16 frames have the same duration.

7.5 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

7.6 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD1} . An external clock signal, if used, is connected to the OSC input. In this case the internal oscillator must be switched off by a software command; see Section 6.2.38.

7.7 Reset

The chip has a hardware and a software reset. After power-up a hardware reset (pin \overline{RES}) must be applied. The hardware and software reset give the same results. After a reset, the chip has the following state; see Section 6.2.2:

- All column and row outputs are set to V_{SS1} (display off)
- RAM data undefined
- Power-down mode
- Command register set to default states; see Table 4.

7.8 LCD voltage generator and bias level generator

The LCD voltage generator and the bias level generator is illustrated in Fig.37. The V_{LCD} is generated by means of two voltage multipliers, with voltage multiplier 1 being programmable; see Section 6.2.39.

Behaviour of voltage multiplier 2 depends on the mode. In the full Display mode, voltage multiplier 2 behaves as a doubler. In the partial Display mode voltage multiplier 2 feeds the voltage of V_{LCDIN1} directly to $V_{LCDOUT2}$.

The LCD voltage generator requires in total 9 external components (capacitors). The recommended values and voltage ranges for the external components are specified in Table 85. The given values should be referred to as information only. It is recommended to check how patterns with high load are displayed before finalizing the values.

The bias level generator generates the required bias levels according to the programmed bias systems; see Section 6.2.43.

To save power it is recommended to apply capacitors to bias level pads ($V2H$, $V1H$, VC , $V1L$ and $V2L$) of approximately 1 μF . A capacitor at VC pad is expected to be the most effective. Depending on the application of the VC capacitor it might be advantageous or even necessary to set the OPT bit $VCBW = 1$; see Table 97 and Section 15.8.

Table 85 External components

| ITEM | CAPACITOR VALUE | VOLTAGE RANGE |
|--------------------------|------------------|---------------|
| C1 to C4; $C_{V_{LCD1}}$ | 1 to 4.7 μF | 16 V |
| C5; $C_{V_{LCD2}}$ | 1 to 4.7 μF | 25 V |
| $C_{V_{DD2}}$ | 1 to 4.7 μF | 4.5 V |
| $C_{V_{DD1}}$ | 1 μF | 3.3 V |

STN RGB - 132 × 132 × 3 driver

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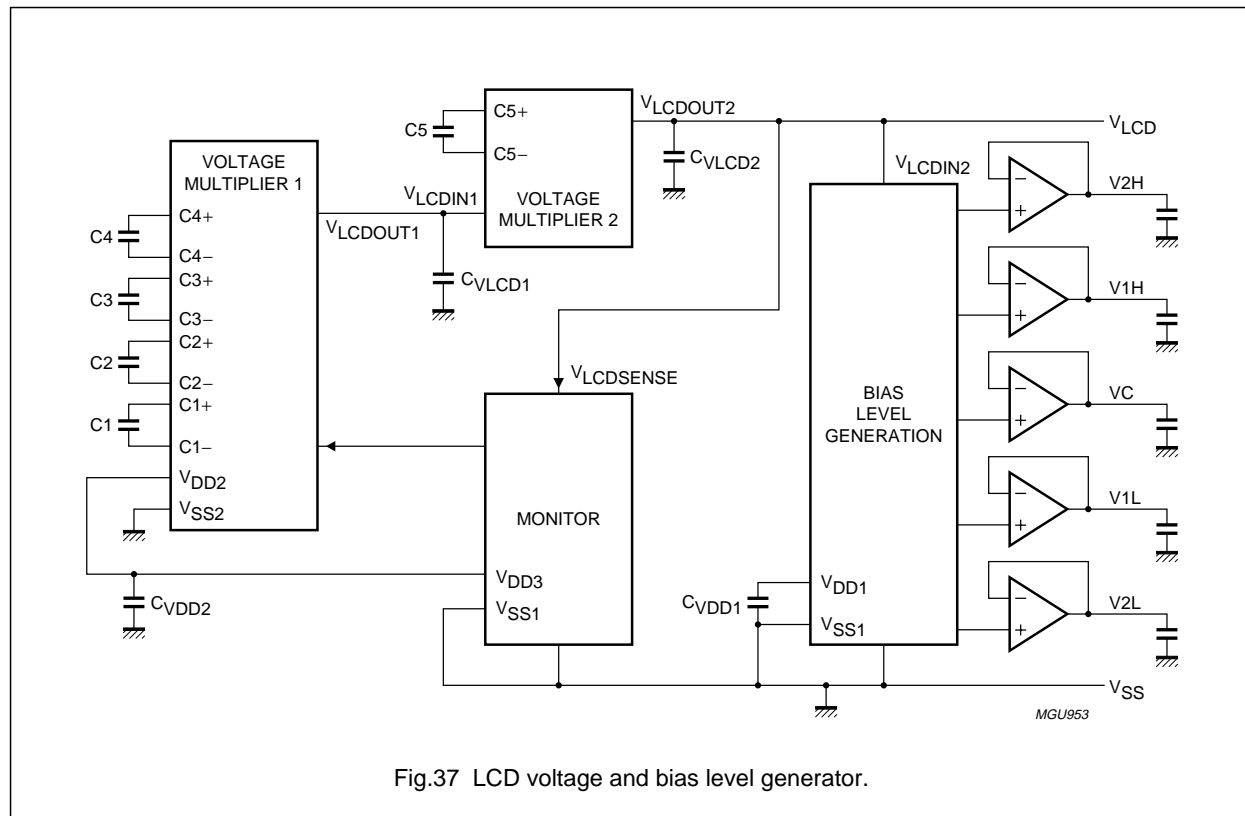


Fig.37 LCD voltage and bias level generator.

7.9 Column drivers, data processing and data latches

The column drivers section includes 132 × 3 column outputs (C0 to C395) which should be connected directly to the LCD. When less than 396 columns are required, the unused column outputs must be left open-circuit.

The column output signals are generated in the data processing block by reading out data from the display RAM and processing with the appropriate orthogonal function which represents the simultaneously selected rows.

7.10 Row drivers

The row drivers section includes 132 row outputs which should be connected directly to the LCD. When less than 132 rows are required the unused column outputs must be left open-circuit.

When the PCF8833 is operating in full Display mode, 4 rows are always selected simultaneously. In partial Display mode the active row output signals are selected one after the other.

8 PARALLEL INTERFACE

The 8080-series 8-bit bidirectional interface can be used for communication between the microcontroller and the PCF8833. The selection of this interfaces is done with pins PS2, PS1 and PS0; see Section 7.1.1.

The interface functions of the 8080-series parallel interface are given in Table 86.

Table 86 8080-series parallel interface function; note 1.

| D/C | RD | WR | OPERATION |
|-----|----|----|----------------------|
| 0 | 1 | R | command write |
| 1 | 1 | R | command data write |
| 1 | 1 | R | display data write |
| 0 | R | 1 | read status register |
| 1 | R | 1 | none |
| 1 | R | R | forbidden |

Note

1. R = rising edge.

STN RGB - 132 × 132 × 3 driver

PCF8833

When sending commands to the PCF8833 the $\overline{D/\overline{C}}$ line must be pulled HIGH when the command data is transferred (see Fig.38). The same is valid when RAM data is sent to the PCF8833 (see Fig.39).

The PCF8833 can send data back to the microcontroller in 2 different ways. The protocol for the RDID1, RDID2, RDID3 and RDTEMP commands is illustrated in Fig.40. Descriptions of these commands is given in Chapter 6. When reading out RDTEMP it is recommended to read this data several times to validate the readout number.

When using the RDDIDIF (see Section 6.2.6) or RDDST (see Section 6.2.7) commands the PCF8833 sends 24 or 32 data bits respectively back to the microcontroller. The protocol for the RDDIDIF and RDDST commands is illustrated in Fig.41.

The parallel interface timing diagram is illustrated in Fig.52. For the dummy read cycle the time t_{ACC} is referenced to the rising edge of the \overline{RD} signal.

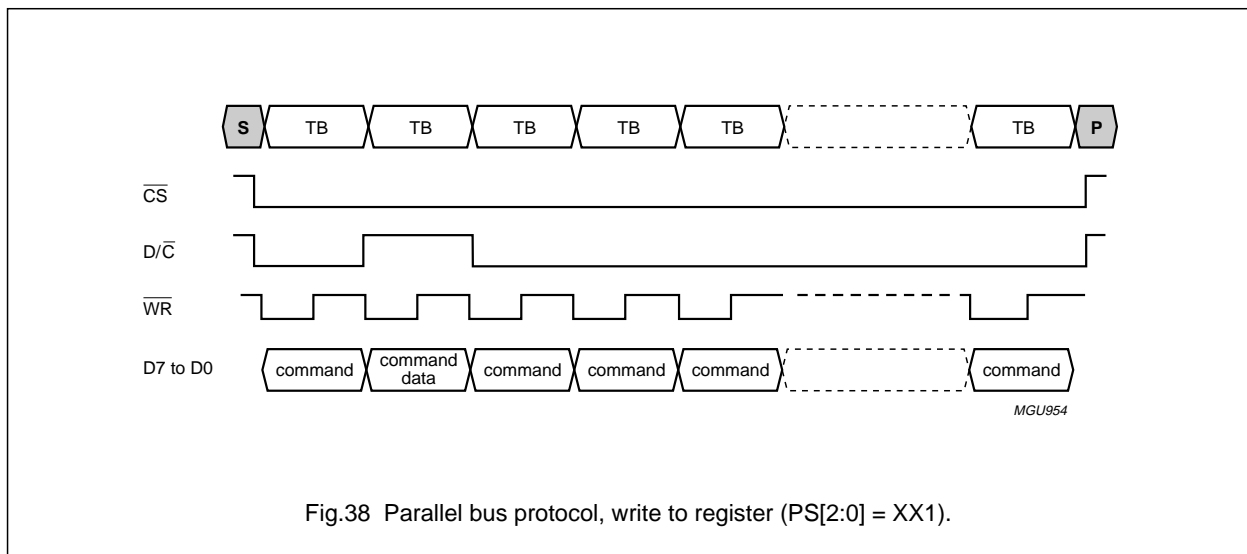


Fig.38 Parallel bus protocol, write to register (PS[2:0] = XX1).

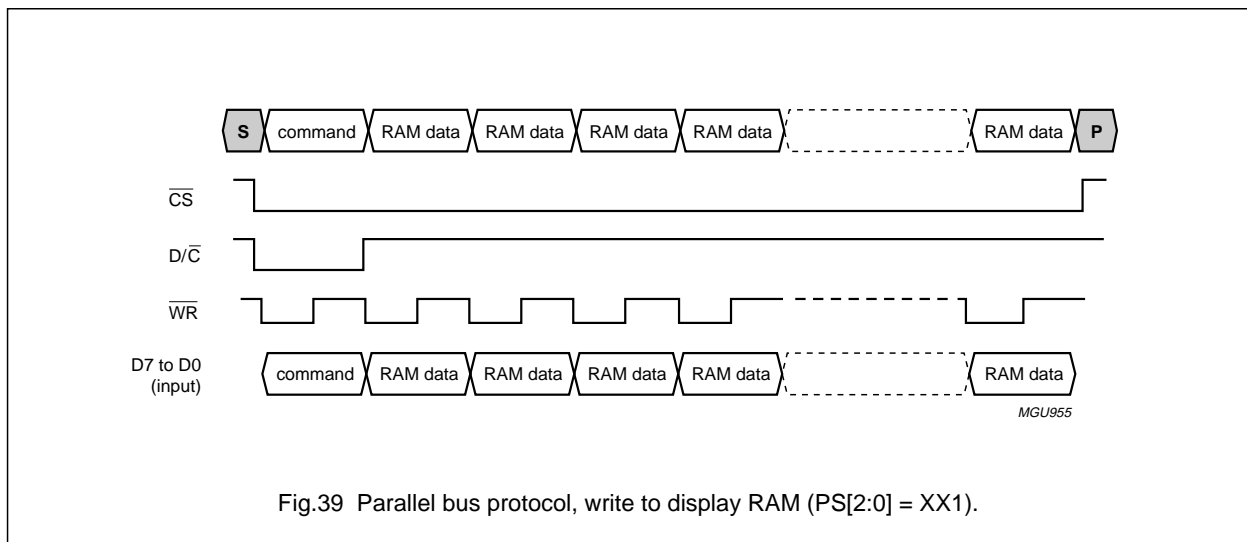
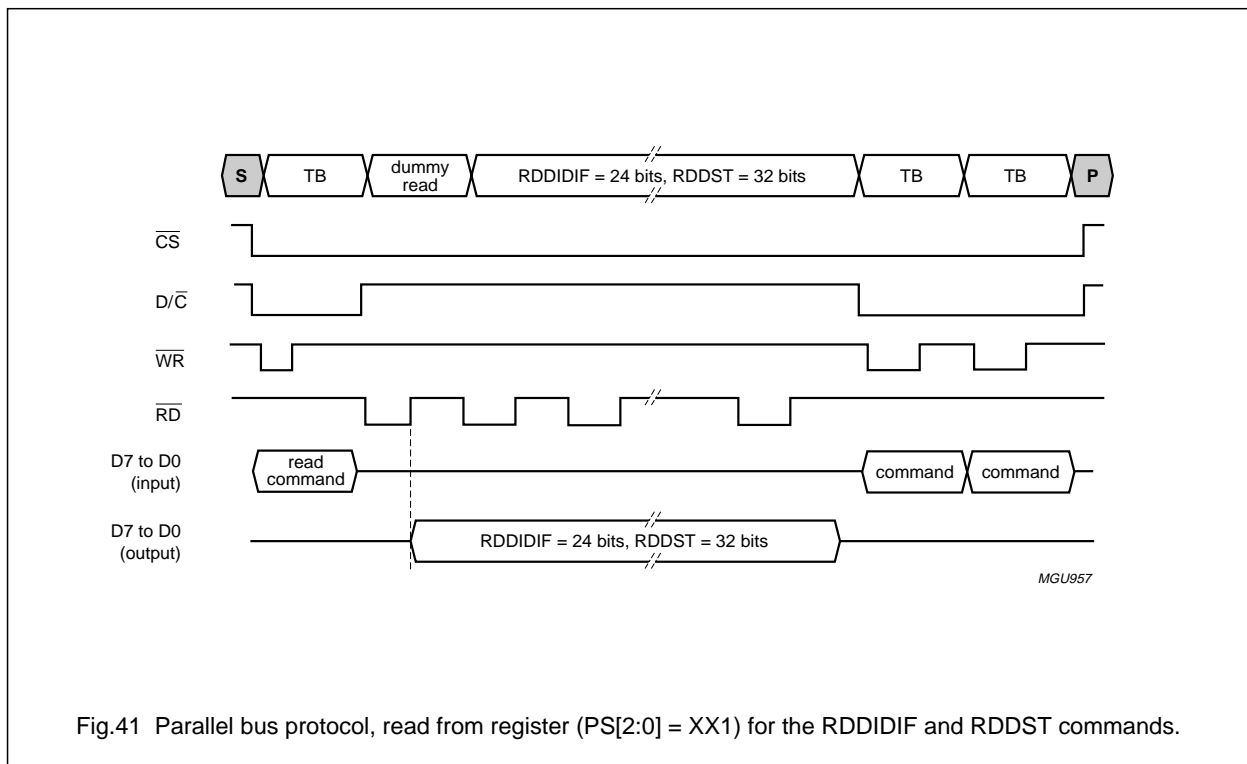
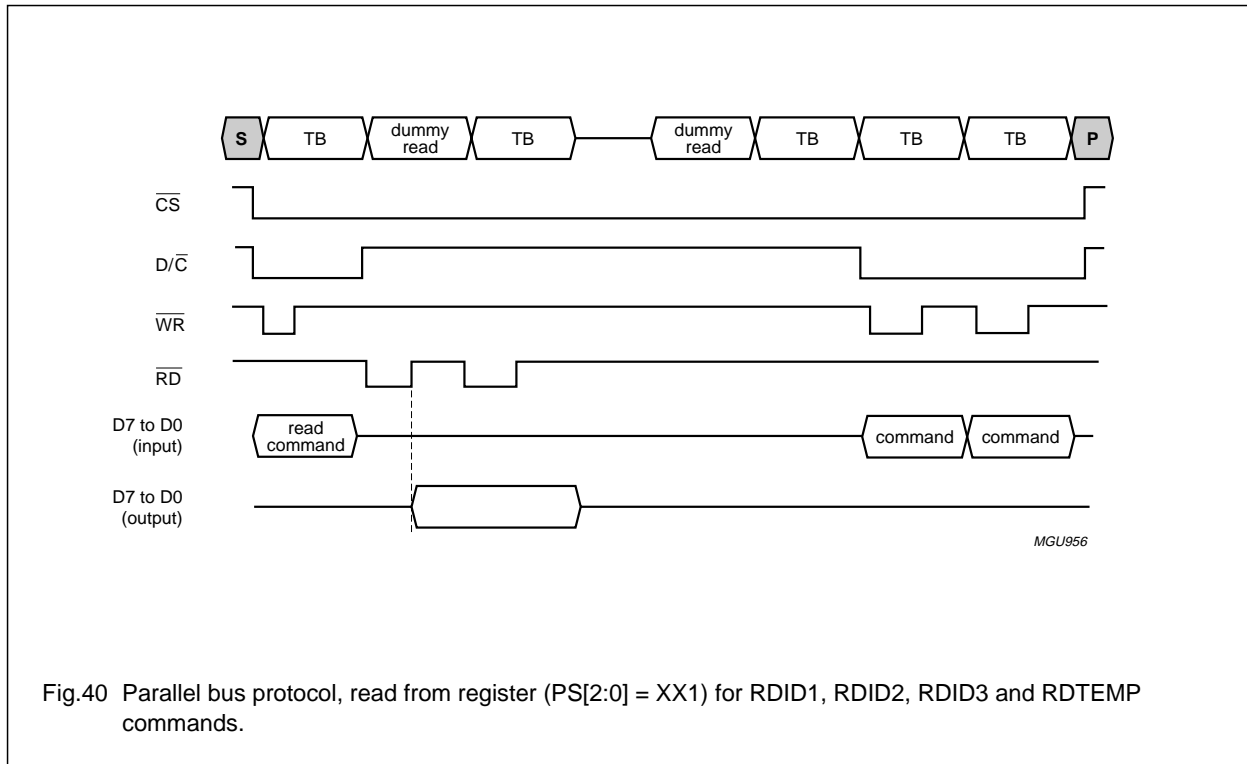


Fig.39 Parallel bus protocol, write to display RAM (PS[2:0] = XX1).

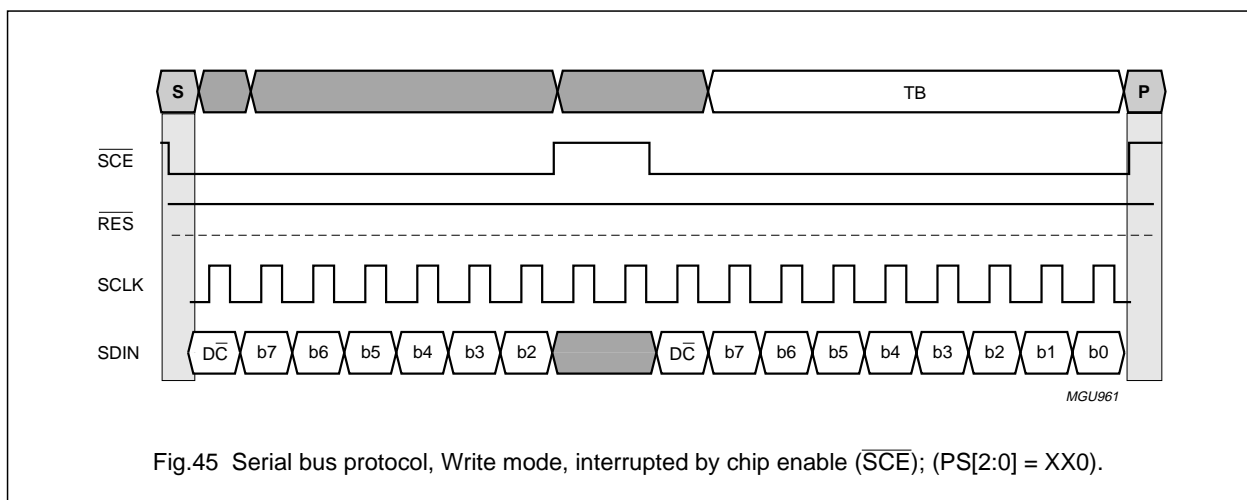
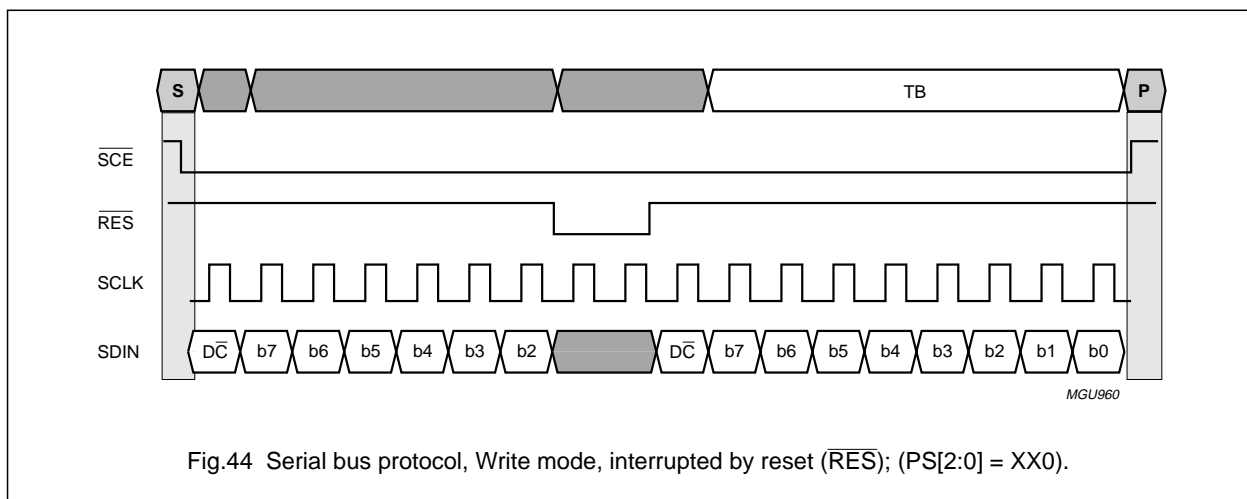
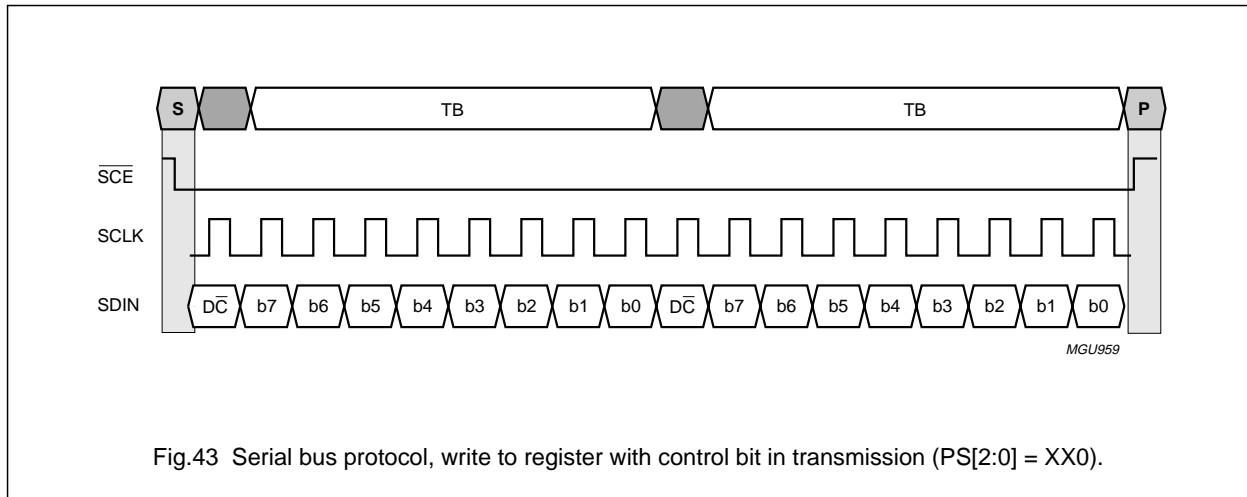
STN RGB - 132 × 132 × 3 driver

PCF8833



STN RGB - 132 × 132 × 3 driver

PCF8833



9.2 Read mode

The Read mode of the serial interface means that the microcontroller reads data from the PCF8833. The PCF8833 can send data back to the microcontroller in two different ways. The serial bus protocol for the RDID1, RDID2, RDID3 and RDTEMP commands is illustrated in Fig.46. Descriptions of these commands are given in Section 6.2. After a command has been issued, a byte is transmitted in the opposite direction (using SDOUT). In order to reach the timing characteristics as given in Chapter 13 data bit b7 must be handled as a don't care. When the speed of the clock is slowed down to at least half of maximum speed, at least for reading b7, the reading of data bit b7 is valid.

The PCF8833 samples the SDIN data at rising SCLK edges, but shifts SDOUT data at falling SCLK edges. Thus the microcontroller is supposed to read SDOUT data at rising SCLK edges.

After the read command has been sent, the SDIN line must be set to 3-state not later than the falling SCLK edge of the last bit (see Fig.46).

When using the RDDIDIF (see Section 6.2.6) or RDDST (see Section 6.2.7) commands the PCF8833 sends 24 or 32 data bits respectively back to the microcontroller. The serial bus protocols for the RDDIDIF and RDDST commands are illustrated in Figs. 47 and 48. After one of these commands has been sent 3 or 4 bytes respectively are transmitted in the opposite direction (using SDOUT) after one dummy clock cycle is given.

The 8th read bit is shorter than the others because it is terminated by the rising SCLK edge; see Figs 46, 47 and 48. The last rising SCLK edge sets SDOUT to 3-state.

The serial interface timing diagram is illustrated in Fig.51. For the dummy read cycle the time t_{ACC} is referenced to the rising edge of the SCLK signal.

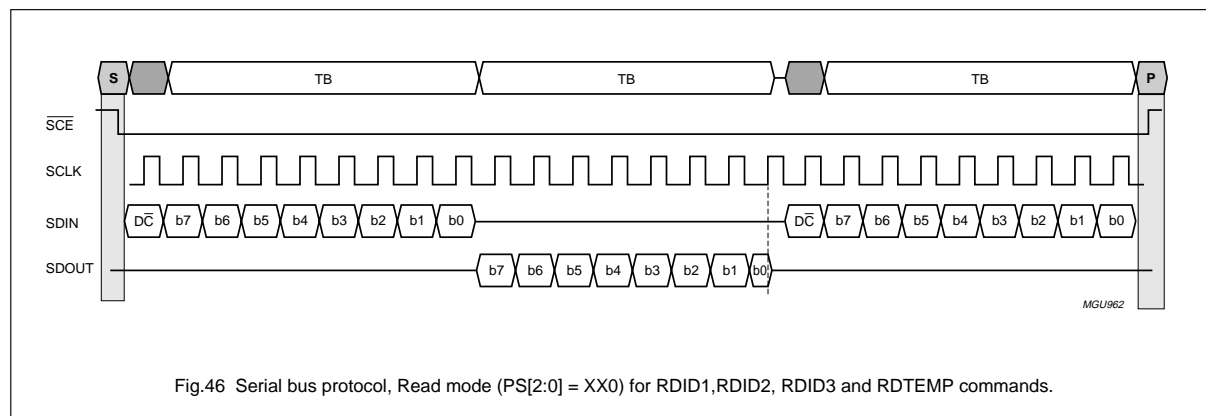


Fig.46 Serial bus protocol, Read mode (PS[2:0] = XX0) for RDID1,RDID2, RDID3 and RDTEMP commands.

STN RGB - 132 × 132 × 3 driver

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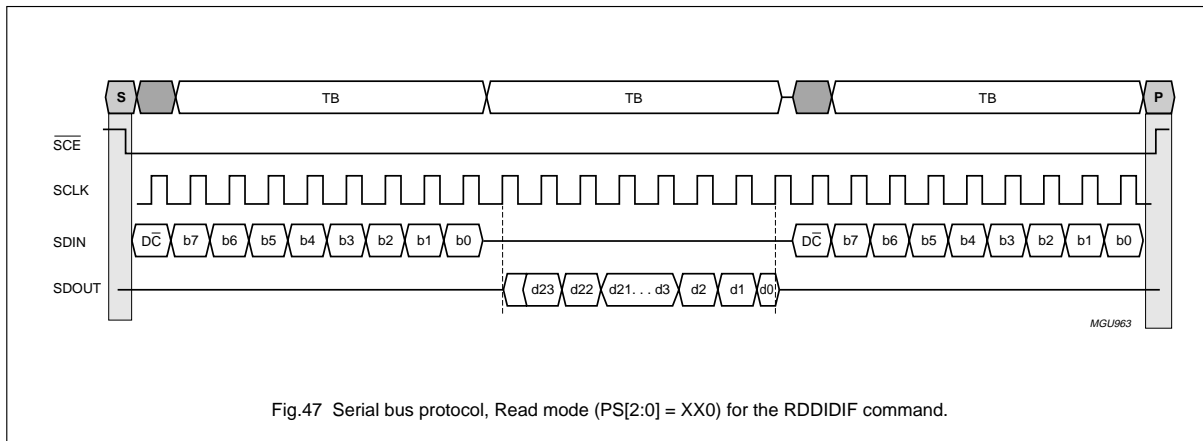


Fig.47 Serial bus protocol, Read mode (PS[2:0] = XX0) for the RDDIDIF command.

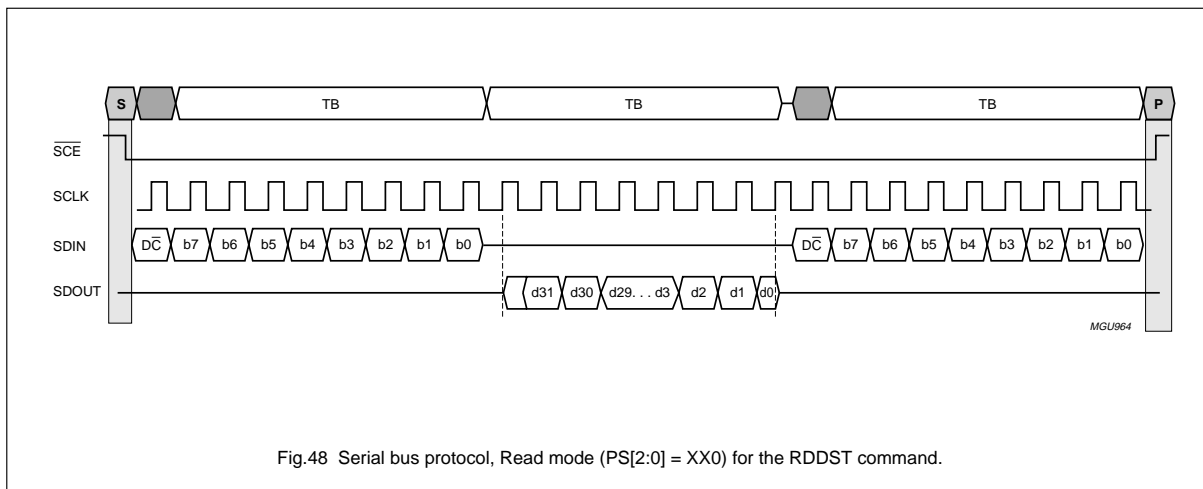


Fig.48 Serial bus protocol, Read mode (PS[2:0] = XX0) for the RDDST command.

STN RGB - 132 × 132 × 3 driver

PCF8833

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---------------------------------|--|------|-------------------------|------|
| V _{SS2} | system ground voltage | -0.5 | +0.5 | V |
| V _{DD1} | logic supply voltage 1 | -0.5 | +4.0 | V |
| V _{DD2} | supply voltage 2 for the internal voltage generator | -0.5 | +6.5 | V |
| V _{DD3} | analog supply 3 for the internal voltage generator | -0.5 | +4.0 | V |
| V _{LCDIN1} | LCD supply voltage input 1 | -0.5 | +16 | V |
| V _{LCDIN2} | LCD supply voltage input 2 | -0.5 | +20 | V |
| V _{LCDSENSE} | voltage multiplier input voltage | -0.5 | +20 | V |
| V _{OTP(gate)} | supply voltage 1 for OPT programming | -0.5 | +10 | V |
| V _{OTP(drain)} | supply voltage 2 for OPT programming (V _{write}) | -0.5 | +10 | V |
| I _{DDn} | supply current at all V _{DD} pins | -50 | +50 | mA |
| I _{SSn} | negative supply current at all V _{SS} pins | -50 | +50 | mA |
| V _I , V _O | input/output voltage except for row and column outputs | -0.5 | V _{DD} + 0.5 | V |
| | output voltage for row and column outputs | -0.5 | V _{LCD2} + 0.5 | V |
| I _I | DC input current | -10 | +10 | mA |
| I _O | DC output current | -10 | +10 | mA |
| P _{tot} | total power dissipation | - | 300 | mW |
| T _{stg} | storage temperature | -55 | +125 | °C |
| T _j | junction temperature | - | 125 | °C |

Note

- Parameters are valid over the operating temperature range; all voltages are referenced to V_{SS1}; unless otherwise specified.

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

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12 DC CHARACTERISTICS

$V_{DD1} = 1.5$ to 3.3 V; $V_{DD2} = V_{DD3} = 2.4$ to 3.5 V; $V_{SS} = 0$ V; $V_{LCD} = 3.8$ to 20.0 V; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------------------------|---|--|--------------|------|--------------|------|
| Supplies | | | | | | |
| V_{DD1} | logic supply voltage 1 | | 1.5 | – | 3.3 | V |
| V_{DD2} | supply voltage 2 for the internal voltage generator | note 1 | 2.4 | – | 4.5 | V |
| V_{DD3} | supply voltage 3 for the internal voltage generator | note 1 | 2.4 | – | 3.5 | V |
| V_{LCDIN1} | LCD supply voltage input 1 | LCD input voltage 1 externally supplied (both voltage multipliers are disabled) | – | – | 16.0 | V |
| V_{LCDIN2} | LCD supply voltage input 2 | LCD input voltage 2 externally supplied (both voltage multipliers are disabled) | – | – | 20.0 | V |
| $V_{LCDOUT1}$ | LCD supply voltage output 1 | LCD voltage internally generated with voltage multiplier 1 (voltage generator enabled); note 2 | 3.8 | – | 10.0 | V |
| $V_{LCDOUT2}$ | LCD supply voltage output 2 | LCD voltage internally generated with voltage multiplier 2 (voltage generator enabled); note 2 | 3.8 | – | 20.0 | V |
| $V_{LCD(tol)}$ | tolerance of generated V_{LCD} | with calibration; note 3 | –70 | – | +70 | mV |
| Static current consumption | | | | | | |
| I_{DD1} | logic supply current | notes 5 and 6 | – | 1.5 | 5 | μA |
| I_{DD2}, I_{DD3} | supply current for the internal voltage generator | notes 5 and 6 | – | 0.5 | 1 | μA |
| Dynamic current consumption | | | | | | |
| I_{DD1} | logic supply current | Normal mode; note 5 | – | 100 | – | μA |
| I_{DD1} | logic supply current during RAM access | Normal mode; notes 5 and 7; see Fig.49 | – | 1000 | – | μA |
| I_{DD2}, I_{DD3} | supply current for the internal voltage generator | Normal mode; note 5 | – | tbf | – | μA |
| $I_{DD(tot)}$ | total supply current ($V_{DD1} + V_{DD2}, V_{DD3}$) | Normal mode; note 5 | – | tbf | – | μA |
| Logic inputs and outputs | | | | | | |
| V_{OL} | LOW-level output voltage | $I_{OL} = 0.5$ mA | V_{SS1} | – | $0.2V_{DD1}$ | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = -0.5$ mA | $0.8V_{DD1}$ | – | V_{DD1} | V |
| V_{IL} | LOW-level input voltage | | V_{SS1} | – | $0.3V_{DD1}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD1}$ | – | V_{DD1} | V |
| I_L | leakage current | $V_I = V_{DD1}$ or V_{SS1} | –1 | – | +1 | μA |

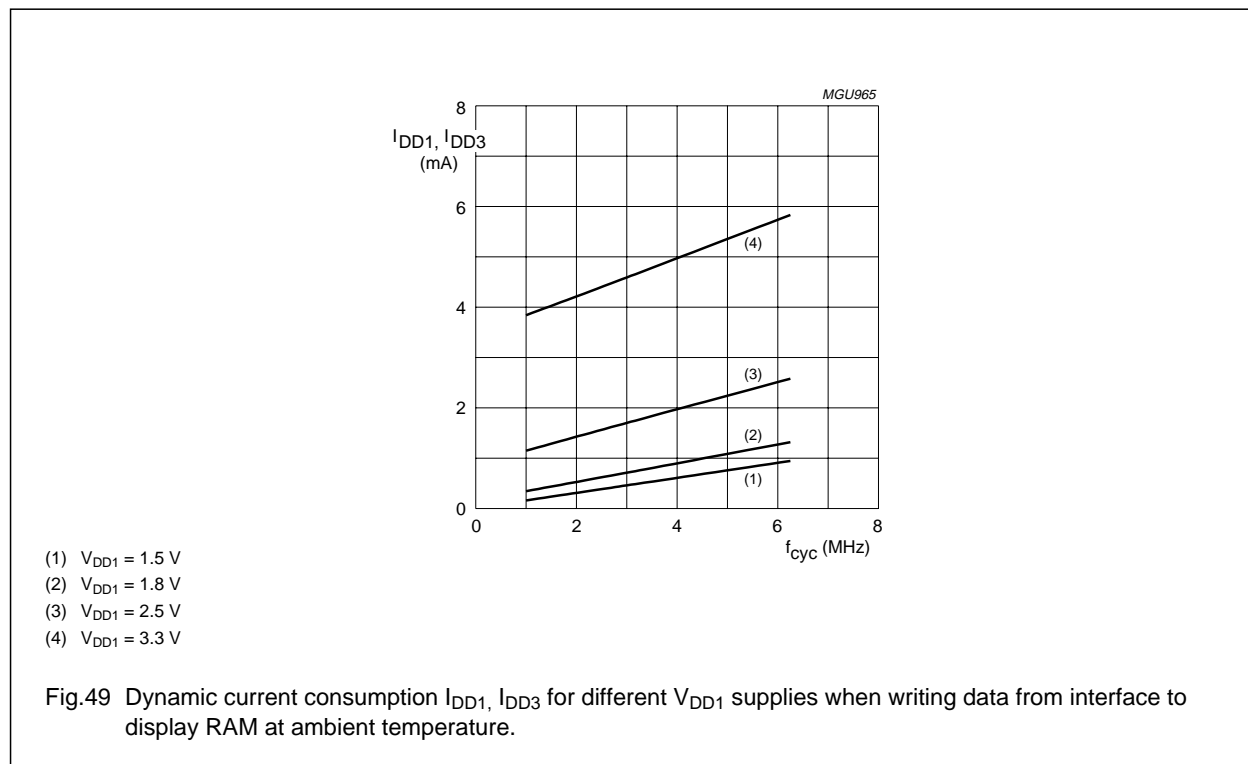
STN RGB - 132 × 132 × 3 driver

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-------------------------------|--|--------------------------|------|------|------|-----------|
| Column and row outputs | | | | | | |
| $R_{o(col)}$ | column output resistance C0 to C395 | $V_{LCD2} = 10\text{ V}$ | – | – | 5 | $k\Omega$ |
| $R_{o(row)}$ | row output resistance R0 to R131 | $V_{LCD2} = 10\text{ V}$ | – | – | 5 | $k\Omega$ |
| $V_{bias(col)}$ | bias tolerance C0 to C395 | | –100 | 0 | 100 | mV |
| $V_{bias(row)}$ | bias tolerance R0 to R131 | | –100 | 0 | 100 | mV |

Notes

- V_{DD2} and V_{DD3} always have to be higher than or equal to V_{DD1} .
- The maximum possible V_{LCD} voltage that may be generated is dependent on supply voltage V_{DD2} , temperature and (display) load.
- Valid for values of temperature, V_{PR} and TC used at the calibration and with temperature calibration disabled.
- Power-save mode.
- Conditions are: $V_{DD1} = 2.75\text{ V}$, $V_{DD2} = 2.75\text{ V}$, $V_{LCD2} = 13.9\text{ V}$, voltage multiplier 1 at $5 \times V_{DD2}$, inputs at V_{DD1} or V_{SS1} , interface inactive, internal V_{LCD} generation, V_{LCD2} output is loaded by $400\ \mu\text{A}$ and V_{LCD1} output is loaded by $0\ \mu\text{A}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.
- During power-down all static currents are switched off.
- $V_{DD1} = 1.8\text{ V}$ and interface cycle time $T_{cyc} = 333\text{ ns}$.



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13 AC CHARACTERISTICS

$V_{DD1} = 1.5$ to 3.3 V; $V_{DD2} = V_{DD3} = 2.4$ to 3.5 V; $V_{SS1} = V_{SS2} = 0$ V; $T_{amb} = -40$ to $+85$ °C; note 1; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|---|------|------|------|------|
| f_{frame} | LCD frame frequency (internal clock) | $V_{DD1} = 3.0$ V | – | tbf | – | Hz |
| f_{osc} | oscillator frequency | notes 2 and 3 | – | 600 | – | kHz |
| $f_{clk(ext)}$ | external clock frequency | | – | tbf | – | kHz |
| Reset; see Fig.50 | | | | | | |
| $t_{W(RESL)}$ | reset LOW pulse width | note 4 | 500 | – | – | ns |
| t_{RSS} | reset spike suppression | | – | – | 100 | ns |
| $t_{SU,RESL}$ | reset LOW pulse set-up time after power-on | | 0 | – | 1 | µs |
| t_{RT} | initialization | note 5 | 0 | – | 5 | ms |
| t_{RI} | interface ready after reset pulse | | 0 | – | 1 | µs |
| Serial interface; $V_{DD1(min)} = 1.65$ V; note 6; see Fig.51 | | | | | | |
| T_{SCYC} | serial clock SCLK period (SCLK) | | 150 | – | – | ns |
| t_{SHW} | SCLK pulse width HIGH | | 60 | – | – | ns |
| t_{SLW} | SCLK pulse width LOW | | 60 | – | – | ns |
| t_{SDS} | SDIN data set-up time | | 60 | – | – | ns |
| t_{SDH} | SDIN data hold time | | 60 | – | – | ns |
| t_{ACC} | SDOUT access time | $C_L = 30$ pF | 10 | – | 50 | ns |
| t_{OH} | SDOUT output disable time | $C_L = 5$ pF; $R = 3$ kΩ | 25 | – | 50 | ns |
| t_{SCC} | SCLK to \overline{SCE} time | | 20 | – | – | ns |
| t_{CHW} | \overline{SCE} pulse width HIGH | | 40 | – | – | ns |
| t_{CSS} | \overline{SCE} to SCLK set-up time | | 60 | – | – | ns |
| t_{CSH} | \overline{SCE} to SCLK hold time | | 65 | – | – | ns |
| 8-bit parallel (8080-type) interface; $V_{DD1(min)} = 1.65$ V; note 6; see Fig.52 | | | | | | |
| t_{CS} | \overline{CS} -WR and \overline{CS} -RD time | note 7 | 10 | – | – | ns |
| t_{AH} | D/ \overline{C} address hold time | | 10 | – | – | ns |
| t_{AS} | address set-up time | | 10 | – | – | ns |
| T_{CYC} | system cycle time | | 160 | – | – | ns |
| t_{CCLW} | \overline{WR} control pulse width LOW | Write mode | 38 | – | – | ns |
| t_{CCLR} | \overline{RD} control pulse width LOW | Read mode | 38 | – | – | ns |
| t_{CCHW} | \overline{WR} control pulse width HIGH | Write mode | 90 | – | – | ns |
| t_{CCHR} | \overline{RD} control pulse width HIGH | Read mode | 90 | – | – | ns |
| t_{DS} | D0 to D7 data set-up time | | 10 | – | – | ns |
| t_{DH} | D0 to D7 data hold time | | 10 | – | – | ns |
| t_{ACC} | read access time | note 8; $C_L = 30$ pF | – | – | 30 | ns |
| t_{OH} | output disable time | note 8; $C_L = 5$ pF; $R = 3$ kΩ; note 9 | 30 | – | 160 | ns |

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Notes

1. V_{DD2} and V_{DD3} always have to be larger than or equal to V_{DD1} .
2. Not directly observable at any pin.
3. After calibration the following f_{osc} can be expected at 25 °C: 600 kHz \pm 4%; at different temperatures an additional variation of +0.12%/°C will not be exceeded.
4. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS1} to V_{DD1} .
5. The initialization incorporates the start-up of the internal circuitry including the readout of the OTP cells. The start-up time for the internal voltage generation is not included.
6. The input signal rise time and fall time (t_r and t_f) are specified at 15 ns or less. When the cycle time is used at high speed, the specification is $t_r + t_f \leq (t_{CYC} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \leq (t_{CYC} - t_{CCLR} - t_{CCHR})$.
7. \overline{CS} can be permanently tied LOW.
8. The output disable time and read access time is applicable after the second read cycle (see Fig.40).
9. For $V_{DD1} = 1.8$ V possible variation of t_{OH} is between 40 and 80 ns for a temperature range of -40 to +85 °C.

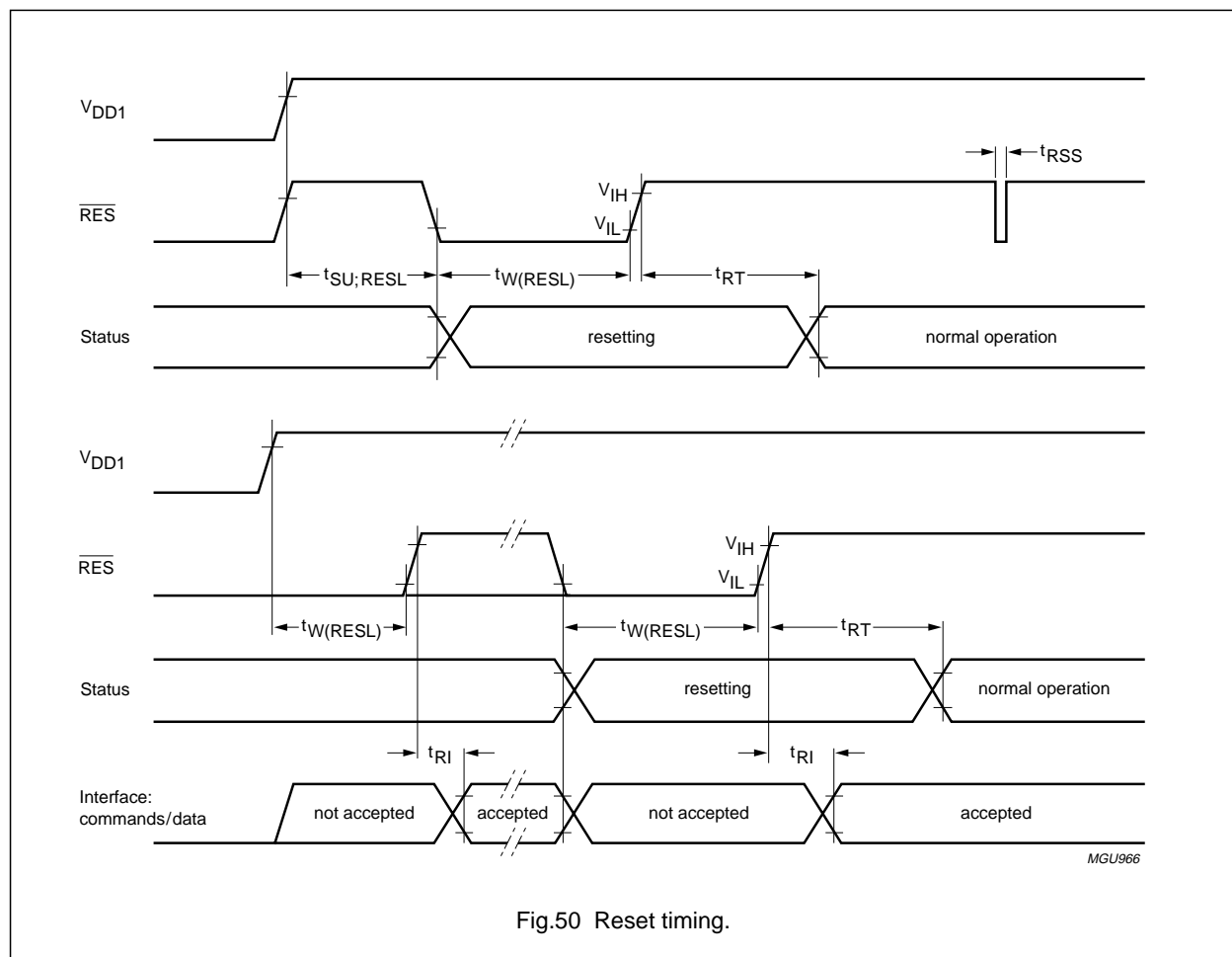
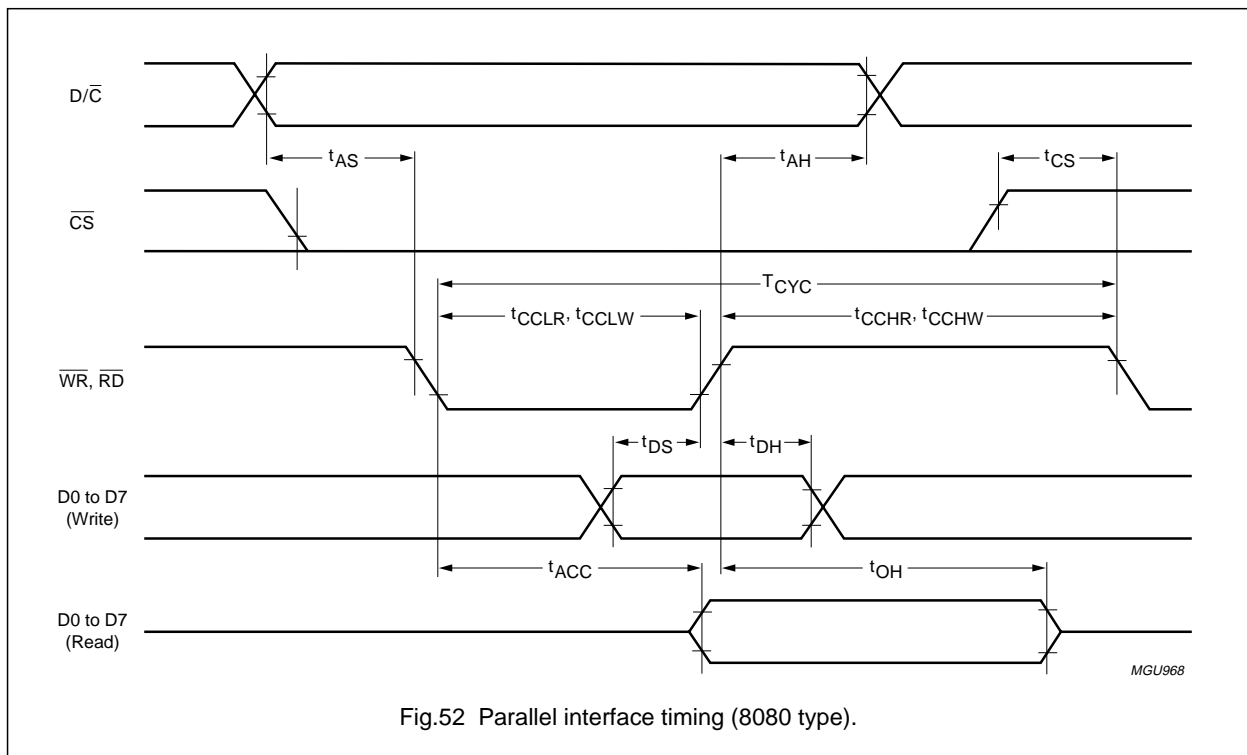
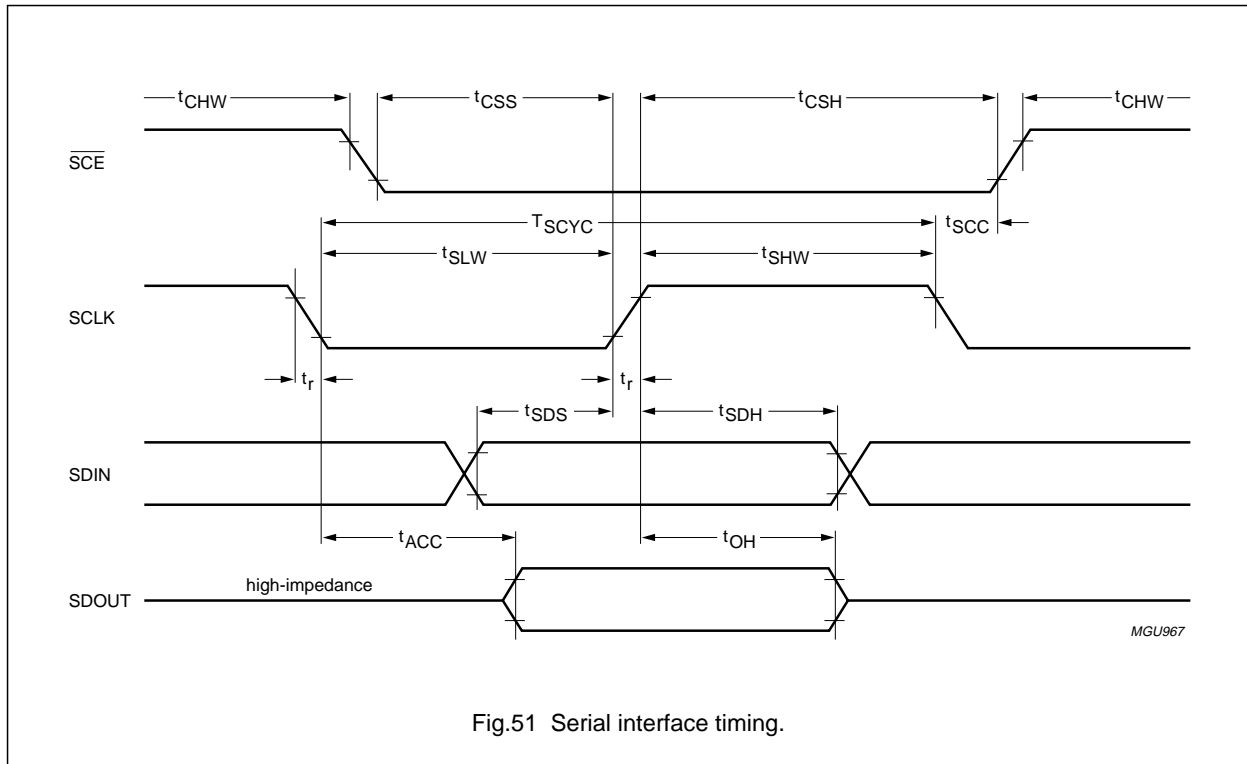


Fig.50 Reset timing.

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STN RGB - 132 × 132 × 3 driver

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14 APPLICATION INFORMATION

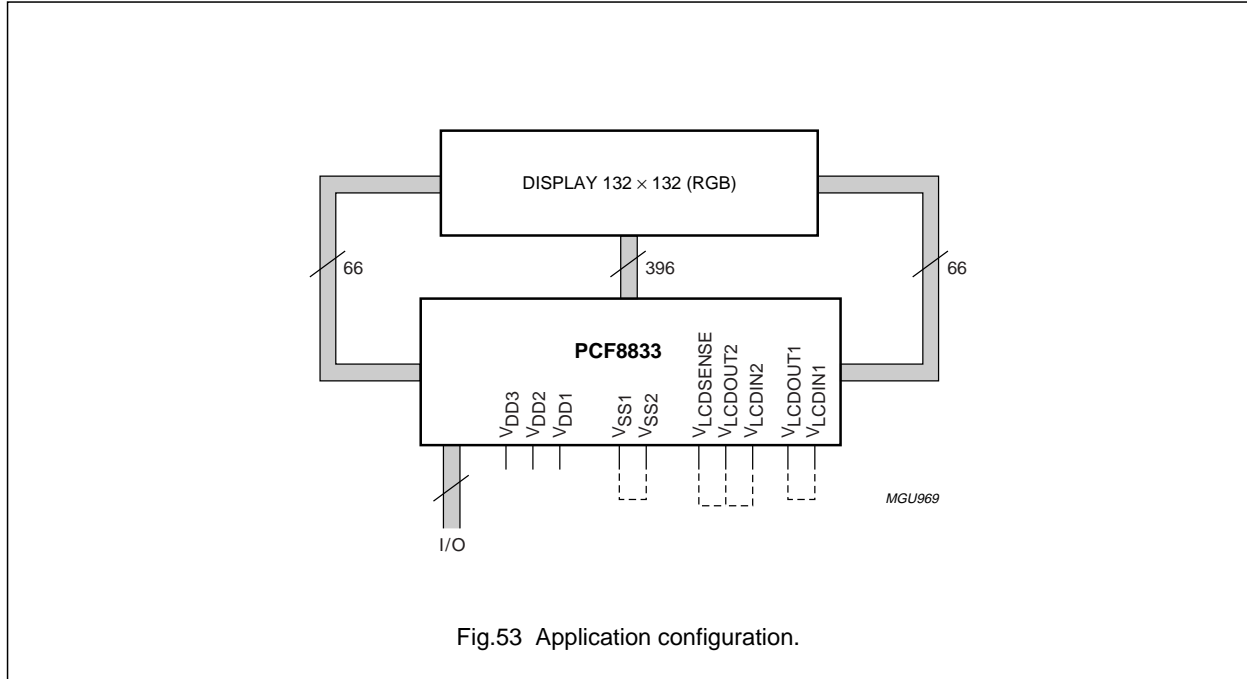
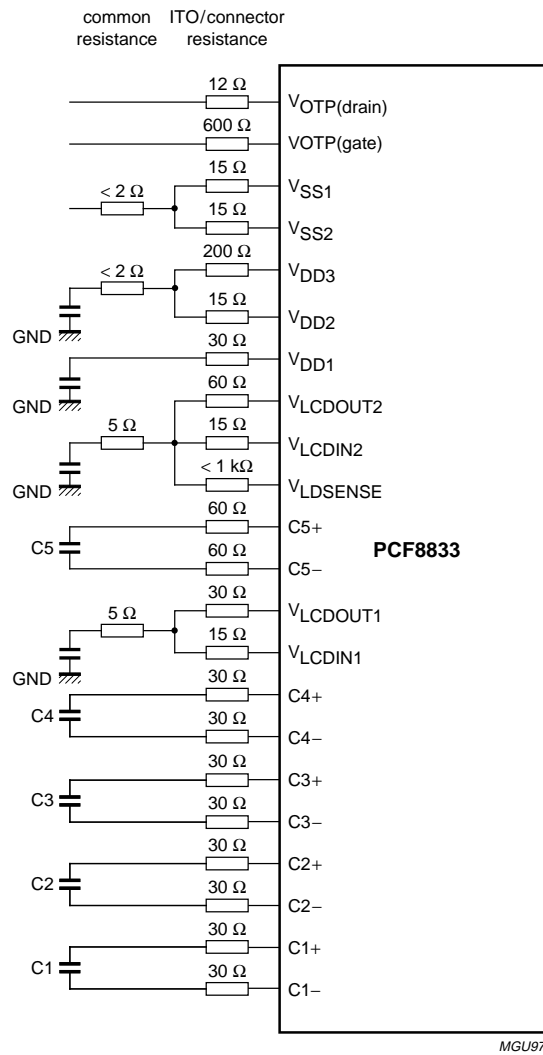


Fig.53 Application configuration.

Figure 54 shows a typical supply and capacitor connections for the PCF8833.

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The indicated resistor values are the maximum recommended values. The recommended capacitor values are given in Table 85.

Fig.54 I/O configuration for the PCF8833.

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15 MODULE MAKER PROGRAMMING

The One Time Programmable (OTP) technology has been implemented in the PCF8833. It enables the module maker to perform an LCD supply voltage calibration after it has been assembled on an LCD module. The module maker can also pre-define command set registers in order to provide the setmaker with a 'plug and play' module where only display related data has to be sent.

The PCF8833 features the following module maker programming facilities:

- V_{LCD} calibration
- Multiplication factor $S[1:0]$ to $FS[1:0]$ for full Display mode and $PS[1:0]$ for partial Display mode
- Set $VPR[8:0]$ to $FVPR[8:0]$ for full Display mode and $PVPR[8:0]$ for partial Display mode
- Set bias system $VB[3:0]$ to $FVB[3:0]$ for full Display mode and $PVB[3:0]$ for partial Display mode
- Segmented temperature compensation slopes for V_{LCD} , $SLA[2:0]$, $SLB[2:0]$, $SLC[2:0]$ and $SLD[2:0]$
- Segmented temperature frame frequencies $DFA[6:0]$, $DFB[6:0]$, $DFC[6:0]$ and $DFD[6:0]$
- Frame frequency 8-colour mode $DF8[6:0]$

- Identification bits $ID2[7:0]$ and $ID3[7:0]$
- TRS and BRS
- Factory default bit EFD
- Seal bit.

15.1 V_{LCD} calibration

The first feature included is the ability to adjust the V_{LCD} voltage with a 6-bit code (MMVOPCAL). This code is implemented in twos complement notation giving rise to a positive or negative offset to the V_{PR} register. The adder in the circuit has underflow and overflow protection. In the event of an overflow, the output will be clamped to $V_{OP} = 445$; during an underflow the output will be clamped to 0.

Figure 55 illustrates how the high voltage generator setting V_{OP} is controlled. Compared to equation (1) in Section 6.2.31, Fig.55 also takes the temperature compensation V_T into account (see Section 6.2.40), which is reflected in the following equation:

$$V_{LCD} = a + (V_T[7:0] + MMVOPCAL[5:0] + VCON[6:0] + VPR[8:0]) \times b$$

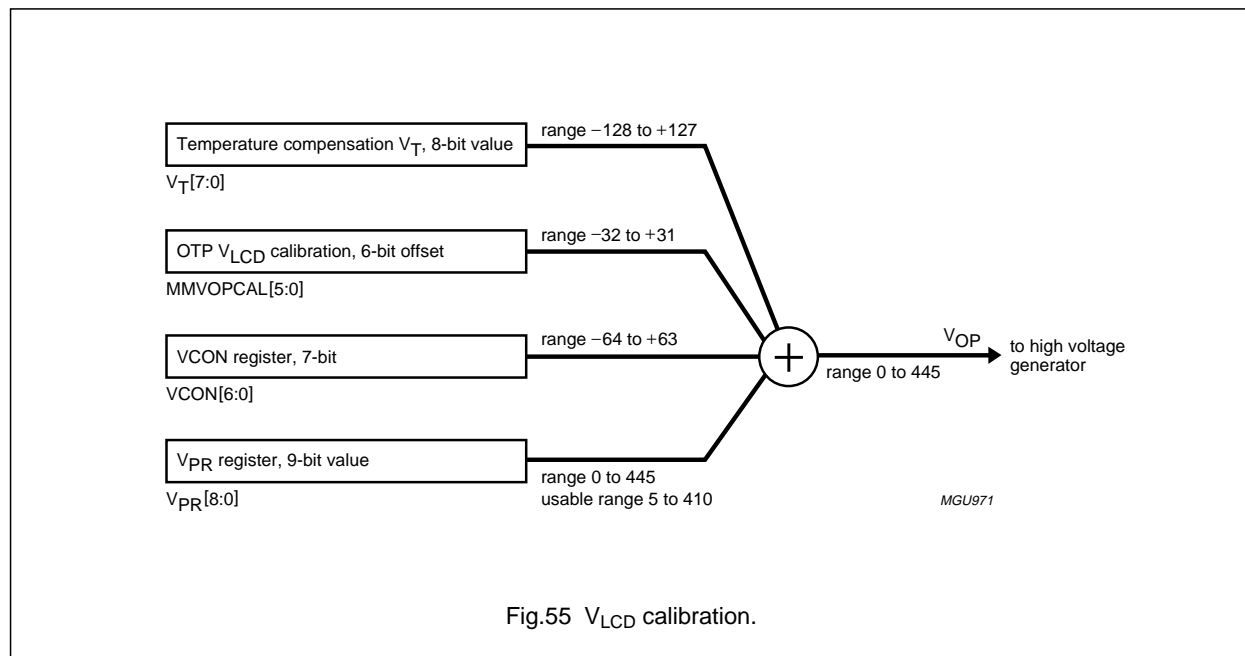


Fig.55 V_{LCD} calibration.

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Table 87 Possible MMVOPCAL values

| MMVOPCAL[5:0] | DECIMAL EQUIVALENT | V _{LCD} OFFSET |
|---------------|--------------------|-------------------------|
| 011111 | 31 | +1240 mV |
| 011110 | 30 | +1200 mV |
| 011101 | 29 | +1160 mV |
| : | : | : |
| 000010 | 2 | +80 mV |
| 000001 | 1 | +40 mV |
| 000000 | 0 | 0 mV |
| 111111 | -1 | -40 mV |
| 111110 | -2 | -80 mV |
| : | : | : |
| 100010 | -30 | -1200 mV |
| 100001 | -31 | -1240 mV |
| 100000 | -32 | -1280 mV |

15.2 Factory defaults

The factory default setting of the following features can be predefined with OTP cells:

- Multiplication factor S[1:0] for full and partial Display mode
- Set VPR[8:0] for full and partial Display mode
- Set bias system VB[3:0] for full and partial Display mode
- Segmented temperature compensation slopes for V_{LCD}, SLA[2:0], SLB[2:0], SLC[2:0] and SLD[2:0]
- Segmented temperature frame frequencies DFA[6:0], DFB[6:0], DFC[6:0] and DFD[6:0]
- Frame frequency 8-colour mode DF8[6:0]
- TRS and BRS
- Identification bits ID2[7:0] and ID3[7:0].

It is possible to change to settings defined by registers which can be set via the interface, except ID2[7:0] and ID3[7:0] which are defined only by OTP cells. The selection of the factory defaults mode is made by setting the factory default OTP bit EFD.

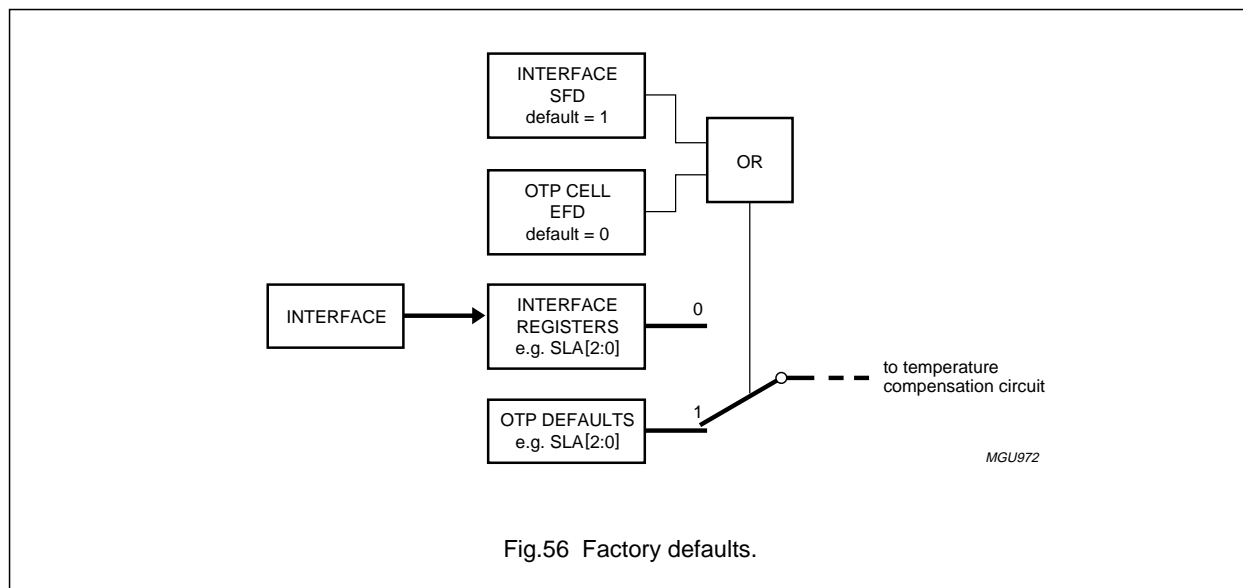
The operation can be thought of as a switch that selects between two sources for the data. When the factory defaults are selected (EFD = 1), changing the values via the interface is not possible, not even by sending the SFD command.

Table 88 Factory default bit EFD

| EFD | ACTION |
|-----|--|
| 0 | configuration data is taken from the interface if SFD = 0 or from the OTP if SFD = 1 |
| 1 | OTP values are used for configuration |

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15.3 Seal bit

The module maker programming is performed in the Calibration mode. This mode is entered via a special interface command (CALMM). To prevent erroneous programming, a seal bit has been implemented which prevents the device from entering Calibration mode. This seal bit, once programmed, cannot be reversed, thus further changes in programmed values are not possible. Applying the programming voltage when not in CALMM mode will have no effect on the programmed values.

Table 89 Seal bit definition

| SEAL BIT | ACTION |
|----------|---------------------------|
| 0 | Calibration mode enabled |
| 1 | Calibration mode disabled |

15.4 OTP architecture

An OTP cell is divided into a non-volatile programmable instance containing the value and a register, where the value is made accessible to the rest of the chip.

In the PCF8833 104 OTP cells are available for the module maker. These cells are organised in a matrix of 7 rows and 15 columns, where the last row is only partially used; see Table 90. All the rows of one particular column of the matrix are filled in parallel by sending 1 byte of data with the OTPSHTIN command. Byte 15 is sent first (containing PVB[3:0], BRS and TRS) and byte 0 last (containing MMVOP[5:0] or SEAL).

Bit 7 of every data byte is not used. An example sequence on how to fill the matrix is given in Table 96.

The default value of the OTP cells is shown in Table 91. These values may be changed by programming the OTP cell. The programming of a cell will invert the default value. This inversion may only happen once per cell, as the programming is irreversible.

Table 93 shows an example on how to program the OTP cells to receive the values given in Table 92. Some examples are given below:

1. The default for DFA[0] is 0; see Table 91, and it is required to have DFA[0] = 1; see Table 92. This means that the value needs to be inverted. Therefore the OTP cell has to be programmed (a 1 in Table 93).
2. The default for DFA[4] is 1; see Table 91, and it is required to have DFA[4] = 0; see Table 92. This means that the value needs to be inverted. Therefore the OTP cell has to be programmed (a 1 in Table 93).
3. The default for DFA[5] is 1; see Table 91, and it is required to have DFA[5] = 1; see Table 92. This means that it is not necessary to change the value. Therefore it is not necessary to program the OTP cell (a 0 in Table 93).
4. The default for DFA[6] is 0; see Table 91, and it is required to have DFA[6] = 0; see Table 92. This means that it is not necessary to change the value. Therefore it is not necessary to program the OTP cell (a 0 in Table 93).

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Table 90 OTP array: content

| BIT | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|-----|--------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|--------------------------------|------------------|------------------|-------------------|-------------------|-------------------|------------------|------------------|
| 0 | SEAL | DFA ₀ | DFB ₀ | DFC ₀ | DFD ₀ | DF8 ₀ | ID2 ₀ | ID2 ₇ | ID3 ₆ | SLA ₀ | SLC ₀ | FVPR ₀ | FVPR ₆ | PVPR ₃ | EFD | TRS |
| 1 | MMVOP ₀ | DFA ₁ | DFB ₁ | DFC ₁ | DFD ₁ | DF8 ₁ | ID2 ₁ | ID3 ₀ | ID3 ₇ | SLA ₁ | SLC ₁ | FVPR ₁ | FVPR ₇ | PVPR ₄ | VCBW | BRS |
| 2 | MMVOP ₁ | DFA ₂ | DFB ₂ | DFC ₂ | DFD ₂ | DF8 ₂ | ID2 ₂ | ID3 ₁ | FS ₀ ⁽¹⁾ | SLA ₂ | SLC ₂ | FVPR ₂ | FVPR ₈ | PVPR ₅ | FVB ₀ | PVB ₀ |
| 3 | MMVOP ₂ | DFA ₃ | DFB ₃ | DFC ₃ | DFD ₃ | DF8 ₃ | ID2 ₃ | ID3 ₂ | FS ₁ ⁽¹⁾ | SLB ₀ | SLD ₀ | FVPR ₃ | PVPR ₀ | PVPR ₆ | FVB ₁ | PVB ₁ |
| 4 | MMVOP ₃ | DFA ₄ | DFB ₄ | DFC ₄ | DFD ₄ | DF8 ₄ | ID2 ₄ | ID3 ₃ | PS ₀ ⁽²⁾ | SLB ₁ | SLD ₁ | FVPR ₄ | PVPR ₁ | PVPR ₇ | FVB ₂ | PVB ₂ |
| 5 | MMVOP ₄ | DFA ₅ | DFB ₅ | DFC ₅ | DFD ₅ | DF8 ₅ | ID2 ₅ | ID3 ₄ | PS ₁ ⁽²⁾ | SLB ₂ | SLD ₂ | FVPR ₅ | PVPR ₂ | PVPR ₈ | FVB ₃ | PVB ₃ |
| 6 | MMVOP ₅ | DFA ₆ | DFB ₆ | DFC ₆ | DFD ₆ | DF8 ₆ | ID2 ₆ | ID3 ₅ | not used | | | | | | | |

Notes

1. FS[1:0] is the multiplication factor used in full Display mode, compare to S[1:0]; see Section 6.2.39.
2. PS[1:0] is the multiplication factor used in partial Display mode, compare to S[1:0]; see Section 6.2.39.

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Table 91 OTP array: default values

| BIT | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|-----|---|---|---|---|---|---|---|---|----------|---|----|----|----|----|----|----|
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 3 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 5 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | not used | | | | | | | |

Table 92 OTP array: desired values

| BIT | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|-----|---|---|---|---|---|---|---|---|----------|---|----|----|----|----|----|----|
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 2 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 3 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 5 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | not used | | | | | | | |

Table 93 OTP array: values to be programmed

| BIT | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|-----|---|---|---|---|---|---|---|---|----------|---|----|----|----|----|----|----|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | not used | | | | | | | |

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15.5 Interface commands

Table 94 contains a list of all OTP related commands.

Table 94 OTP related commands

| NAME | D/C | COMMAND BYTE ⁽¹⁾ | | | | | | | | HEX | DESCRIPTION |
|-----------|-----|-----------------------------|----------------|------------------|------------------|------------------|----------------|----------------|----------------|-------|--|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| CALMM | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F0 | CALMM command |
| | 1 | X | X | ORA ₂ | ORA ₁ | ORA ₀ | X | OPE | CALMM | | entry CALMM mode (CALMM) enable programming (OPE) set address (ORA) |
| Sleep_OUT | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 | generate a refresh of the OTP if CALMM = 0 |
| OTPSHTIN | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | F1 | start shifting data in the shift register; the shifting is executed as long as D/C = 1 |
| | 1 | X | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | | |
| SFD | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | SFD | EE/EF | set factory default (see Sections 6.2.47 and 15.2) |

Note

1. X = don't care. For hexadecimal representation, don't care bits are assumed to be 0.

15.5.1 CALIBRATION MODULE MAKER MODE

When CALMM = 1 the device enters the calibration module maker mode. This mode enables the filling of the OTP matrix and allows programming of the non-volatile OTP cells to take place.

The V_{OTP(drain)} pad is not connected directly to the OTP cells, but through a switch that must be closed for programming by setting OPE to logic 1.

The OTP row to be programmed may be chosen by setting the OTP row address ORA[2:0].

15.5.2 REFRESH

The action of the refresh instruction is to force the registers of the OTP matrix to load the value from the non-volatile part of the OTP cell. This instruction takes up to 1 ms to complete. During this time all other instructions may be sent.

In the PCF8833 the refresh instruction is associated with the Sleep_OUT instruction such that the shift register is automatically refreshed every time the Sleep_OUT instruction is sent.

No refresh may be started when in CALMM mode, i.e. whenever CALMM = 1.

15.5.3 SHIFT IN

The OTP matrix (see Table 90) is filled using the OTSHTIN command, which is similar to the RAM write command. First the appropriate command is sent, then the following data bytes are shifted bitwise into the OTP matrix from left to right, i.e. the new byte is loaded into byte 0, whereas the data of byte 0 is shifted into byte 1 and so on. Bit 7 of the data is not used. The shifting is enabled as long as D/C remains at logic 1.

15.6 Suggestion on how to calibrate V_{LCD2} using MMVOP

In order to calibrate the programming of V_{LCD2}, the sequence in Table 95 is suggested to determine what MMVOP value has to be programmed.

It is assumed that the relevant parameters, the V_{LCD2} programming, V_{PR} and the number of stages S, are set via the interface. This implies that SFD is set to logic 0 and that all OTP settings except MMVOP are ignored.

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Table 95 Sequence to determine MMVOP

| STEP | D/C | COMMAND BYTE ⁽¹⁾ | | | | | | | | ADDR | DESCRIPTION | |
|------|-----|-----------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|------------------|------|-------------|--|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01H | reset (may also be hardware reset) |
| 2 | – | – | – | – | – | – | – | – | – | – | – | wait 1 ms for refresh to take effect |
| 3 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | EEH | set SFD = 0 in order to use interface values |
| 4 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 28H | send DISPOFF to prevent rows and columns to toggle |
| 5 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | B0H | set V _{PR} to desired value |
| | 1 | X | X | X | X | VPR ₈ | VPR ₇ | VPR ₆ | VPR ₅ | – | – | |
| | 1 | X | X | X | VPR ₄ | VPR ₃ | VPR ₂ | VPR ₁ | VPR ₀ | – | – | |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | C2H | set multiplication stages to desired value |
| | 1 | X | X | X | X | X | X | S ₁ | S ₀ | – | – | |
| 7 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F0H | enter CALMM mode |
| | 1 | X | X | 0 | 0 | 0 | x | 0 | 0 | 1 | 01H | ORA = 000 OPE = 0 CALMM = 1 |
| 8 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 11H | send Sleep_OUT (no refresh because CALMM = 1) |
| 9 | – | – | – | – | – | – | – | – | – | – | – | wait until D31 = 1 (V stable); note 2 |
| 10 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | F1H | send OTPSHTIN; note 3 |
| | 1 | X | MMVOP ₅ | MMVOP ₄ | MMVOP ₃ | MMVOP ₂ | MMVOP ₁ | MMVOP ₀ | 0 | 0 | – | set MMVOP[5:0] and SEAL = 0 |
| 11 | – | – | – | – | – | – | – | – | – | – | – | check V _{LCD2} after V _{LCD2} has settled |
| 12 | – | – | – | – | – | – | – | – | – | – | – | repeat steps 10 to 11 until desired V _{LCD2} is reached |
| 13 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F0H | exit CALMM mode; if required |
| | 1 | X | X | 0 | 0 | 0 | 0 | x | 0 | 0 | 00H | ORA = 000 OPE = 0 CALMM = 0 |

Notes

1. X = don't care. For hexadecimal representation, don't care bits are assumed to be logic 0.
2. D31 is the booster voltage status bit; see Section 6.2.7.
3. The chip stays in shift operation as long as D/C is logic 1.

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15.7 Example of filling the shift register

Table 96 shows the sequence of commands to fill the OTP matrix as defined in Table 93.

Table 96 Sequence for filling the OTP matrix

| STEP | D/C | COMMAND BYTE ⁽¹⁾ | | | | | | | | ADDR | DESCRIPTION | |
|---------|-----|-----------------------------|---|---|---|---|---|---|---|------|-------------|--------------------------------------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01H | reset (may also be hardware reset) |
| 2 | | | | | | | | | | | | wait 1 ms for refresh to take effect |
| 3 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F0H | enter CALMM mode |
| | 1 | X | X | 0 | 0 | 0 | X | 0 | 1 | 0 | 01H | ORA = 000; OPE = 0; CALMM = 1 |
| 4 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | F1H | send OTPSHTIN; note 2 |
| shift15 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set PVB[3:0]; BRS and TRS |
| shift14 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set FVB[3:0]; 0 and EFD |
| shift13 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set PVPR[8:3] |
| shift12 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set PVPR[2:0] and FVPR[8:6] |
| shift11 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set FVPR[5:0] |
| shift10 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set SLD[2:0] and SLC[2:0] |
| shift9 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set SLB[2:0] and SLA[2:0] |
| shift8 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set PS[1:0]; FS[1:0] and ID3[7:6] |
| shift7 | 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set ID3[5:0] and ID2[7] |
| shift6 | 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set ID2[6:0] |
| shift5 | 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set DF8[6:0] |
| shift4 | 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set DFD[6:0] |
| shift3 | 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | set DFC[6:0] |
| shift2 | 1 | X | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07H | set DFB[6:0] |
| shift1 | 1 | X | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 11H | set DFA[6:0] |
| shift0 | 1 | X | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1AH | set MMVOP[5:0] and SEAL |
| 5 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F0H | exit CALMM mode; if required |
| | 1 | X | X | 0 | 0 | 0 | X | 0 | 0 | 0 | 00H | ORA = 000; OPE = 0; CALMM = 0 |

Notes

1. X = don't care. For hexadecimal representation, don't care bits are assumed to be logic 0.
2. The chip stays in shift operation as long as D/C is logic 1.

15.8 Programming flow

In order to program an OTP cell, the associated register must be set to logic 1 and a programming voltage of 8 V should be applied to pins $V_{OTP(gate)}$ and $V_{OTP(drain)}$ for 50 ms. It is strongly recommended to use the sequence shown in Table 97 to program the OTP cells. In any event the requirements stated in Section 15.9 must be met.

Important: Whenever a new row in the OTP matrix is selected (change of ORA[2:0]), the OTP cells must not be connected to pin $V_{OTP(drain)}$ (set OPE = 0). For an example see steps 9 to 11 in Table 97.

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Table 97 Sequence to program OTP cells

| STEP | D/C | COMMAND BYTE ⁽¹⁾ | | | | | | | | ADDR | DESCRIPTION | |
|---------|-----|-----------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|-----|------|-------------|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 0 | | | | | | | | | | | | set V _{OTP(gate)} = 0 V; V _{OTP(drain)} = 0 V |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | reset (may also be hardware reset) |
| 2 | | | | | | | | | | | | wait 1 ms for refresh to take effect |
| 3 | | | | | | | | | | | | set V _{OTP(gate)} = 8 V; V _{OTP(drain)} = 8 V |
| 4 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F0 | enter CALMM mode |
| | 1 | X | X | 0 | 0 | 0 | X | 0 | 1 | 01 | 01 | ORA = 000; OPE = 0; CALMM = 1 |
| 5 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | F1 | send OTPSHTIN; note 2 |
| shift15 | 1 | X | X | PVB ₃ | PVB ₂ | PVB ₁ | PVB ₀ | BRS | TRS | | | set PVB[3:0]; BRS and TRS |
| shift14 | 1 | X | X | FVB ₃ | FVB ₂ | FVB ₁ | FVB ₀ | VCBW | EFD | | | set FVB[3:0]; VCBW and EFD; note 3 |
| : | | | | | | | | | | | | |
| shift0 | 1 | x | MMVOP ₅ | MMVOP ₄ | MMVOP ₃ | MMVOP ₂ | MMVOP ₁ | MMVOP ₀ | 0 | | | set MMVOP[5:0] and SEAL = 0 |
| 6 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F0 | select row 0 in OTP matrix |
| | 1 | X | X | 0 | 0 | 0 | X | 0 | 1 | 01 | 01 | ORA = 000; OPE = 0; CALMM = 1 |
| 7 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F0 | enable programming |
| | 1 | X | X | 0 | 0 | 0 | X | 1 | 1 | 03 | 03 | ORA = 000; OPE = 1; CALMM = 1 |
| 8 | | | | | | | | | | | | wait for 50 ms until OTP cells are programmed |
| 9 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F0 | disable programming |
| | 1 | X | X | 0 | 0 | 0 | X | 0 | 1 | 01 | 01 | ORA = 000; OPE = 0; CALMM = 1 |
| 10 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F0 | select row 1 in OTP matrix |
| | 1 | X | X | 0 | 0 | 1 | X | 0 | 1 | 09 | 09 | ORA = 001; OPE = 0; CALMM = 1 |
| 11 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F0 | enable programming |
| | 1 | X | X | 0 | 0 | 1 | X | 1 | 1 | 0B | 0B | ORA = 001; OPE = 1; CALMM = 1 |

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| STEP | D/ \bar{C} | COMMAND BYTE ⁽¹⁾ | | | | | | | | ADDR | DESCRIPTION |
|------|--------------|-----------------------------|---|---|---|---|---|---|---|------|--|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 12 | | | | | | | | | | | wait for 50 ms until OTP cells are programmed |
| 13 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F0 | disable programming |
| | 1 | X | X | 0 | 0 | 1 | X | 0 | 1 | 09 | ORA = 001; OPE = 0; CALMM = 1 |
| 14 | | | | | | | | | | | repeat steps 10 to 13 for rows 2 to 6 |
| 15 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F0 | exit CALMM mode |
| | 1 | X | X | 0 | 0 | 0 | X | 0 | 0 | 00 | ORA = 000; OPE = 0; CALMM = 0 |
| 16 | | | | | | | | | | | set $V_{OTP(gate)} = 0\text{ V}$; $V_{OTP(drain)} = 0\text{ V}$ |

Notes

1. X = don't care. For hexadecimal representation, don't care bits are assumed to be logic 0.
2. The chip stays in shift operation as long as D/ \bar{C} is logic 1.
3. When VCBW = 1 the VC buffer is switched to a weak buffer. Default is VCBW = 0, where the VC buffer is powerful. To save power a capacitor could be connected to VC pad. Depending on the application it might be advantageous or even necessary to program VCBW = 1.

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15.9 Programming specification

For programming OTP cells, the $V_{OTP(gate)}$ and $V_{OTP(drain)}$ voltages have to be applied as indicated in Fig.57. Voltages $V_{OTP(gate)}$ and $V_{OTP(drain)}$ can be applied at the same time or can have a staggered sequence as indicated by cases a and b of Fig.57.

Depending on the series resistance in the supply wires, up to 16 OTP bits can be programmed at the same time. Each OTP cell can only be programmed once.

Table 98 Programming specification (see Fig.57)

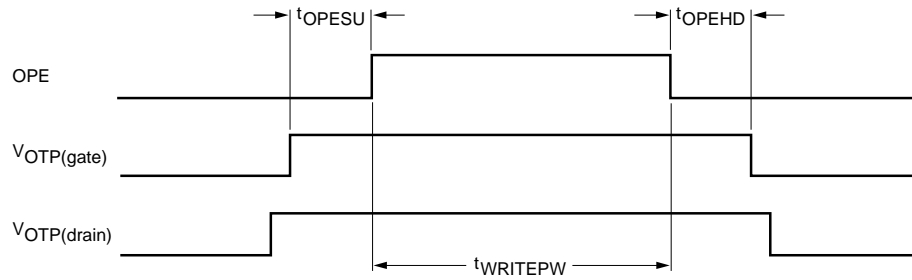
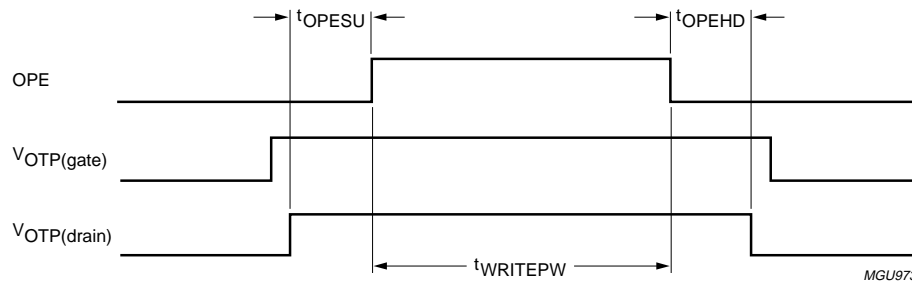
| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--|--|------|------|------|--------------|
| $V_{OTP(gate)}$ | voltage applied to $V_{OTP(gate)}$ pin relative to V_{SS1} | programming active; note 1 | tbf | 8 | tbf | V |
| | | programming inactive | tbf | 0 | tbf | V |
| $V_{OTP(drain)}$ | voltage applied to $V_{OTP(drain)}$ pin relative to V_{SS1} | programming active; note 1 | tbf | 8 | tbf | V |
| | | programming inactive | tbf | 0 | tbf | V |
| $I_{OTP(gate)}$ | current drawn by $V_{OTP(gate)}$ during programming | | tbf | 100 | tbf | μ A |
| $I_{OTP(drain)}$ | current drawn by $V_{OTP(drain)}$ during programming | per programmed OTP cell | tbf | 500 | tbf | μ A |
| $T_{amb(prog)}$ | ambient temperature during programming | | 0 | 25 | 40 | $^{\circ}$ C |
| t_{OPESU} | set-up time of OPE as a function of $V_{OTP(gate)}$ and $V_{OTP(drain)}$ | $V_{OTP(gate)}$ and $V_{OTP(drain)} > 0$ V | 1 | – | – | ms |
| t_{OPEHD} | hold time of OPE as a function of $V_{OTP(gate)}$ and $V_{OTP(drain)}$ | $V_{OTP(gate)}$ and $V_{OTP(drain)} > 0$ V | 1 | – | – | ms |
| $t_{WRITEPW}$ | pulse width of programming voltage | | 45 | 50 | 55 | ms |

Note

1. The voltage drop across the ITO track and any connector must be taken into account to guarantee a sufficiently high voltage at the chip pins.

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(a) $V_{OTP(drain)}$ applied before $V_{OTP(gate)}$ (b) $V_{OTP(gate)}$ applied before $V_{OTP(drain)}$

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Fig.57 Programming waveforms, OPE rises after $V_{OTP(gate)}$ and $V_{OTP(drain)}$.

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16 INTERNAL PROTECTION CIRCUITS

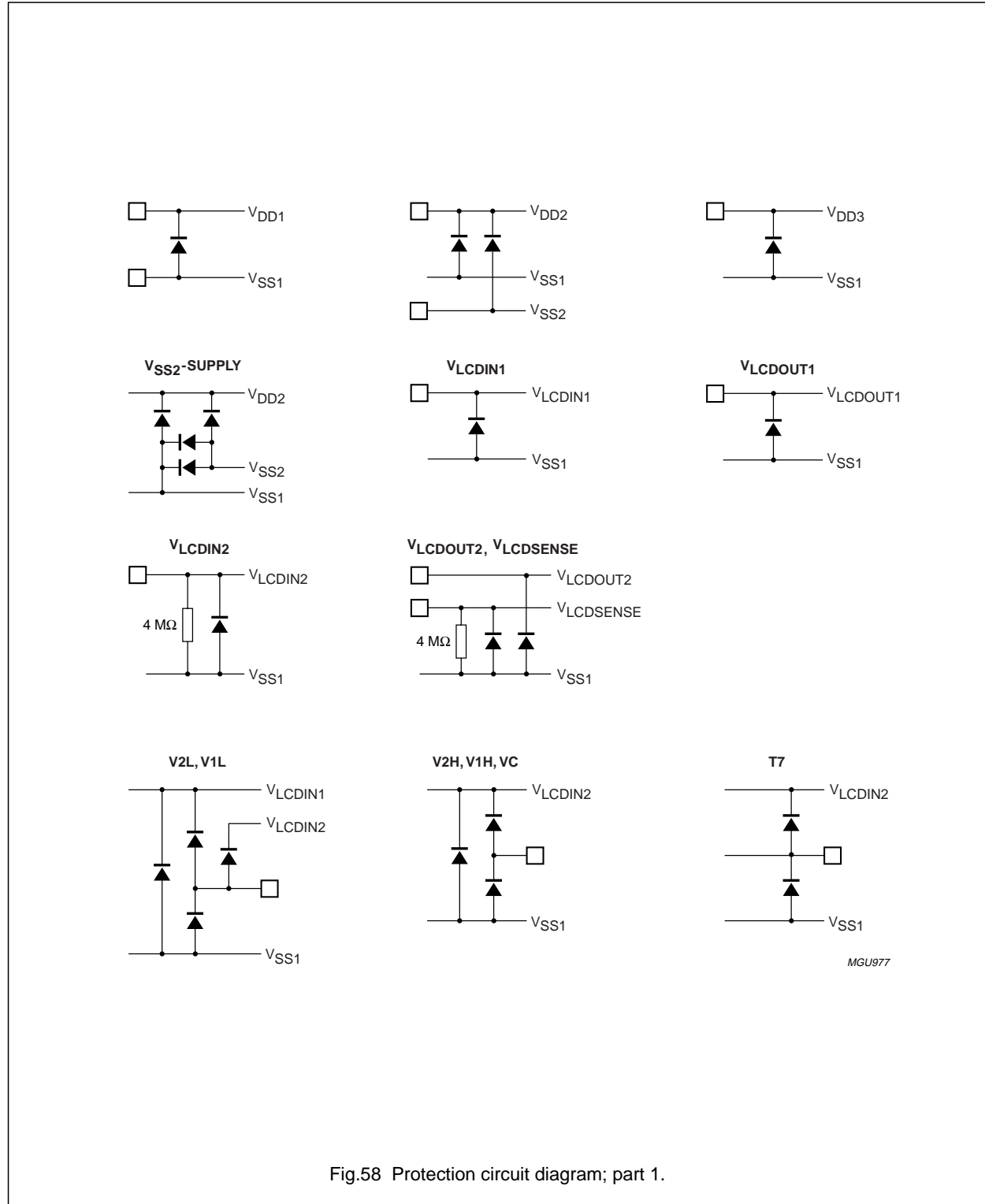


Fig.58 Protection circuit diagram; part 1.

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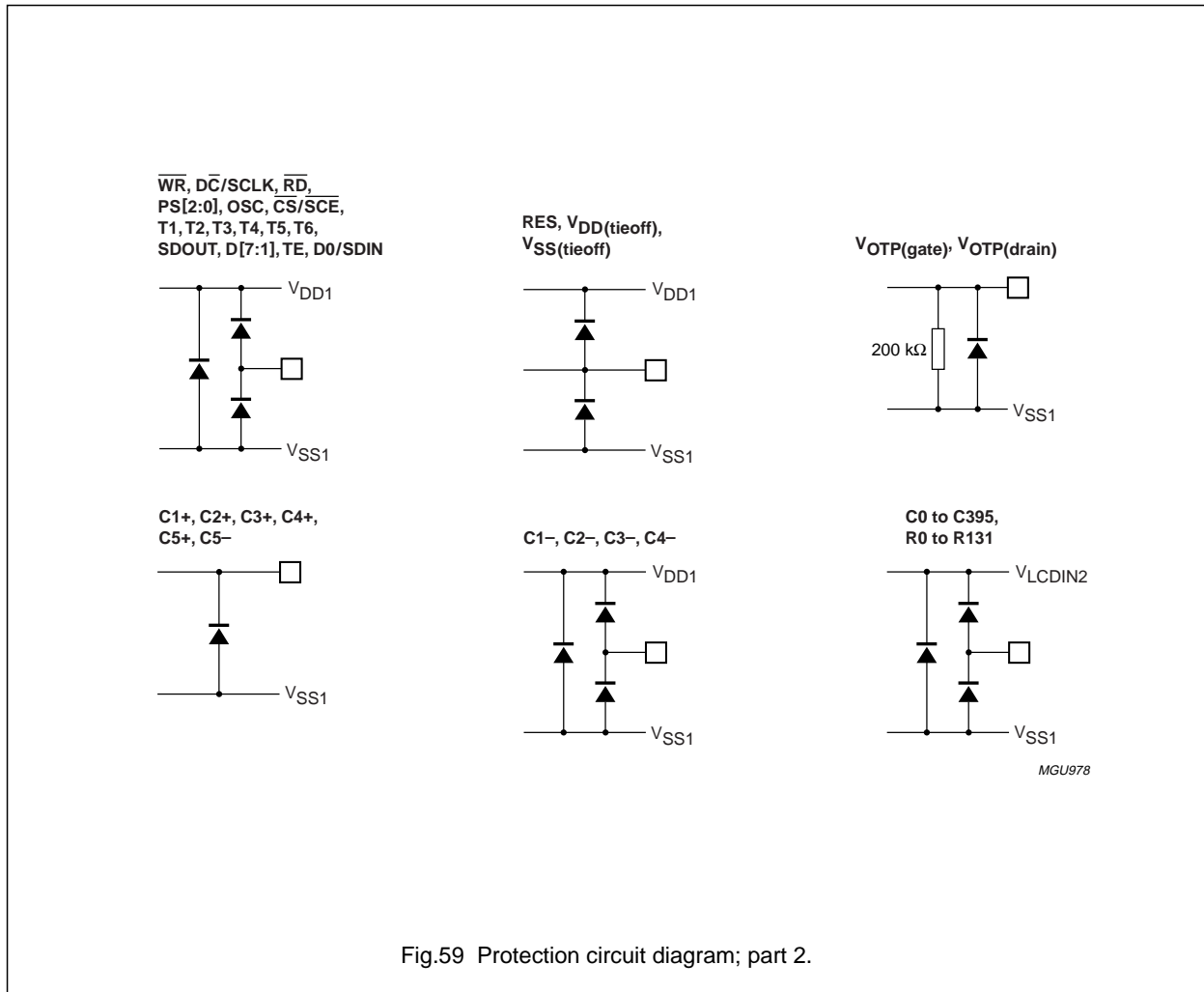
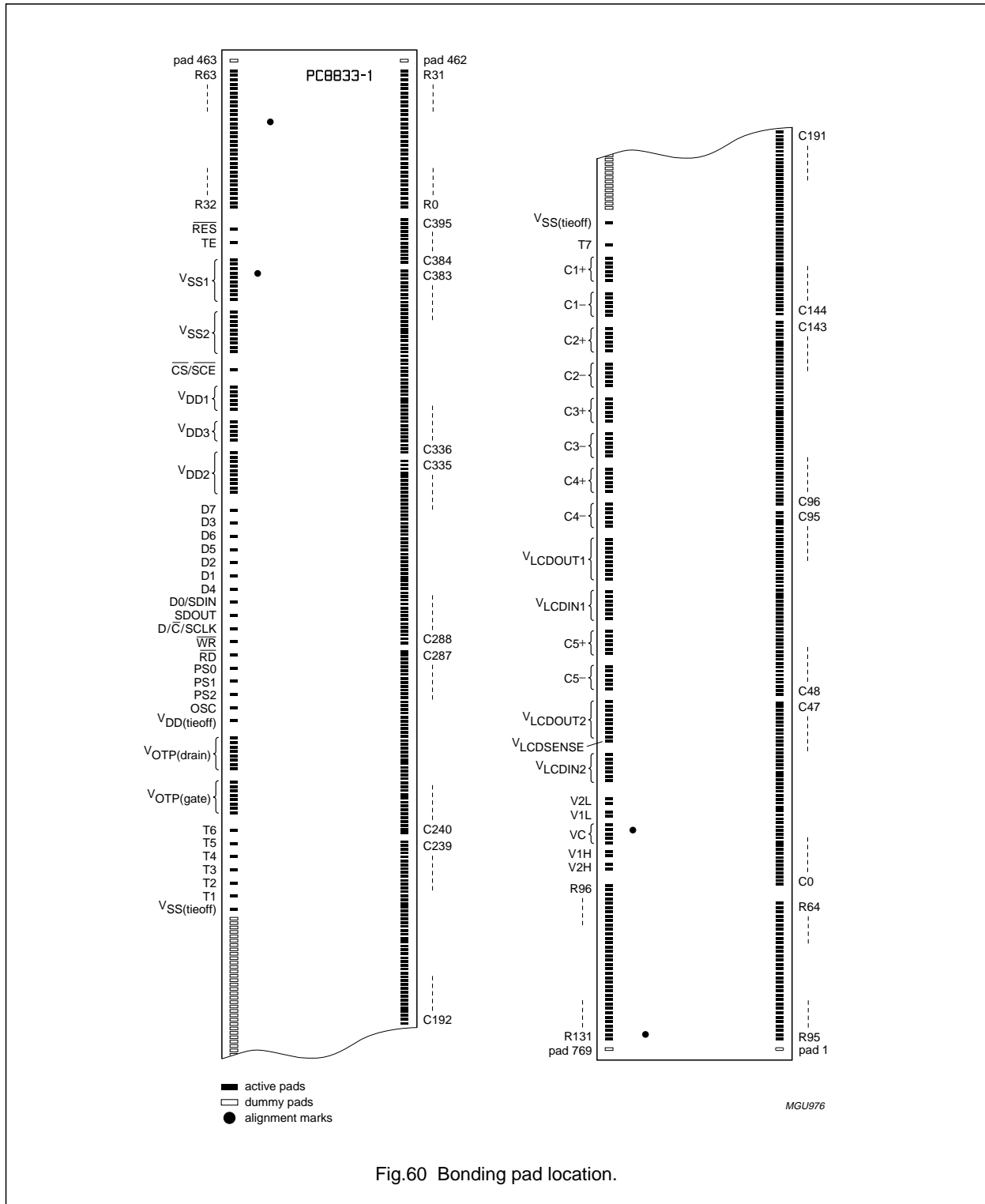


Fig.59 Protection circuit diagram; part 2.

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17 BONDING PAD INFORMATION



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Table 99 Bonding pad locations

All x and y coordinates are referenced to the centre of the chip (dimensions in μm ; see Fig.61).

| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|-----------|
| | | x | y |
| dummy | 1 | -11351.208 | -1035.694 |
| R95 | 2 | -11231.880 | -1035.694 |
| R94 | 3 | -11179.080 | -1035.694 |
| R93 | 4 | -11126.280 | -1035.694 |
| R92 | 5 | -11073.480 | -1035.694 |
| R91 | 6 | -11020.680 | -1035.694 |
| R90 | 7 | -10967.880 | -1035.694 |
| R89 | 8 | -10915.080 | -1035.694 |
| R88 | 9 | -10862.280 | -1035.694 |
| R87 | 10 | -10809.480 | -1035.694 |
| R86 | 11 | -10756.680 | -1035.694 |
| R85 | 12 | -10703.880 | -1035.694 |
| R84 | 13 | -10651.080 | -1035.694 |
| R83 | 14 | -10598.280 | -1035.694 |
| R82 | 15 | -10545.480 | -1035.694 |
| R81 | 16 | -10492.680 | -1035.694 |
| R80 | 17 | -10439.880 | -1035.694 |
| R79 | 18 | -10387.080 | -1035.694 |
| R78 | 19 | -10334.280 | -1035.694 |
| R77 | 20 | -10281.480 | -1035.694 |
| R76 | 21 | -10228.680 | -1035.694 |
| R75 | 22 | -10175.880 | -1035.694 |
| R74 | 23 | -10123.080 | -1035.694 |
| R73 | 24 | -10070.280 | -1035.694 |
| R72 | 25 | -10017.480 | -1035.694 |
| R71 | 26 | -9964.680 | -1035.694 |
| R70 | 27 | -9911.880 | -1035.694 |
| R69 | 28 | -9859.080 | -1035.694 |
| R68 | 29 | -9806.280 | -1035.694 |
| R67 | 30 | -9753.480 | -1035.694 |
| R66 | 31 | -9700.680 | -1035.694 |
| R65 | 32 | -9647.880 | -1035.694 |
| R64 | 33 | -9595.080 | -1035.694 |
| C0 | 34 | -9369.448 | -1030.568 |
| C1 | 35 | -9322.984 | -1030.568 |
| C2 | 36 | -9276.520 | -1030.568 |
| C3 | 37 | -9230.056 | -1030.568 |

| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|-----------|
| | | x | y |
| C4 | 38 | -9183.592 | -1030.568 |
| C5 | 39 | -9137.128 | -1030.568 |
| C6 | 40 | -9090.664 | -1030.568 |
| C7 | 41 | -9044.200 | -1030.568 |
| C8 | 42 | -8997.736 | -1030.568 |
| C9 | 43 | -8951.272 | -1030.568 |
| C10 | 44 | -8904.808 | -1030.568 |
| C11 | 45 | -8858.344 | -1030.568 |
| C12 | 46 | -8811.880 | -1030.568 |
| C13 | 47 | -8765.416 | -1030.568 |
| C14 | 48 | -8718.952 | -1030.568 |
| C15 | 49 | -8672.488 | -1030.568 |
| C16 | 50 | -8626.024 | -1030.568 |
| C17 | 51 | -8579.560 | -1030.568 |
| C18 | 52 | -8533.096 | -1030.568 |
| C19 | 53 | -8486.632 | -1030.568 |
| C20 | 54 | -8440.168 | -1030.568 |
| C21 | 55 | -8393.704 | -1030.568 |
| C22 | 56 | -8347.240 | -1030.568 |
| C23 | 57 | -8300.776 | -1030.568 |
| C24 | 58 | -8254.312 | -1030.568 |
| C25 | 59 | -8207.848 | -1030.568 |
| C26 | 60 | -8161.384 | -1030.568 |
| C27 | 61 | -8114.920 | -1030.568 |
| C28 | 62 | -8068.456 | -1030.568 |
| C29 | 63 | -8021.992 | -1030.568 |
| C30 | 64 | -7975.528 | -1030.568 |
| C31 | 65 | -7929.064 | -1030.568 |
| C32 | 66 | -7882.600 | -1030.568 |
| C33 | 67 | -7836.136 | -1030.568 |
| C34 | 68 | -7789.672 | -1030.568 |
| C35 | 69 | -7743.208 | -1030.568 |
| C36 | 70 | -7696.744 | -1030.568 |
| C37 | 71 | -7650.280 | -1030.568 |
| C38 | 72 | -7603.816 | -1030.568 |
| C39 | 73 | -7557.352 | -1030.568 |
| C40 | 74 | -7510.888 | -1030.568 |
| C41 | 75 | -7464.424 | -1030.568 |
| C42 | 76 | -7417.960 | -1030.568 |

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| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|-----------|
| | | x | y |
| C43 | 77 | -7371.496 | -1030.568 |
| C44 | 78 | -7325.032 | -1030.568 |
| C45 | 79 | -7278.568 | -1030.568 |
| C46 | 80 | -7232.104 | -1030.568 |
| C47 | 81 | -7185.640 | -1030.568 |
| C48 | 82 | -7081.976 | -1030.568 |
| C49 | 83 | -7035.512 | -1030.568 |
| C50 | 84 | -6989.048 | -1030.568 |
| C51 | 85 | -6942.584 | -1030.568 |
| C52 | 86 | -6896.120 | -1030.568 |
| C53 | 87 | -6849.656 | -1030.568 |
| C54 | 88 | -6803.192 | -1030.568 |
| C55 | 89 | -6756.728 | -1030.568 |
| C56 | 90 | -6710.264 | -1030.568 |
| C57 | 91 | -6663.800 | -1030.568 |
| C58 | 92 | -6617.336 | -1030.568 |
| C59 | 93 | -6570.872 | -1030.568 |
| C60 | 94 | -6524.408 | -1030.568 |
| C61 | 95 | -6477.944 | -1030.568 |
| C62 | 96 | -6431.480 | -1030.568 |
| C63 | 97 | -6385.016 | -1030.568 |
| C64 | 98 | -6338.552 | -1030.568 |
| C65 | 99 | -6292.088 | -1030.568 |
| C66 | 100 | -6245.624 | -1030.568 |
| C67 | 101 | -6199.160 | -1030.568 |
| C68 | 102 | -6152.696 | -1030.568 |
| C69 | 103 | -6106.232 | -1030.568 |
| C70 | 104 | -6059.768 | -1030.568 |
| C71 | 105 | -6013.304 | -1030.568 |
| C72 | 106 | -5966.840 | -1030.568 |
| C73 | 107 | -5920.376 | -1030.568 |
| C74 | 108 | -5873.912 | -1030.568 |
| C75 | 109 | -5827.448 | -1030.568 |
| C76 | 110 | -5780.984 | -1030.568 |
| C77 | 111 | -5734.520 | -1030.568 |
| C78 | 112 | -5688.056 | -1030.568 |
| C79 | 113 | -5641.592 | -1030.568 |
| C80 | 114 | -5595.128 | -1030.568 |
| C81 | 115 | -5548.664 | -1030.568 |

| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|-----------|
| | | x | y |
| C82 | 116 | -5502.200 | -1030.568 |
| C83 | 117 | -5455.736 | -1030.568 |
| C84 | 118 | -5409.272 | -1030.568 |
| C85 | 119 | -5362.808 | -1030.568 |
| C86 | 120 | -5316.344 | -1030.568 |
| C87 | 121 | -5269.880 | -1030.568 |
| C88 | 122 | -5223.416 | -1030.568 |
| C89 | 123 | -5176.952 | -1030.568 |
| C90 | 124 | -5130.488 | -1030.568 |
| C91 | 125 | -5084.024 | -1030.568 |
| C92 | 126 | -5037.560 | -1030.568 |
| C93 | 127 | -4991.096 | -1030.568 |
| C94 | 128 | -4944.632 | -1030.568 |
| C95 | 129 | -4898.168 | -1030.568 |
| C96 | 130 | -4794.504 | -1030.568 |
| C97 | 131 | -4748.040 | -1030.568 |
| C98 | 132 | -4701.576 | -1030.568 |
| C99 | 133 | -4655.112 | -1030.568 |
| C100 | 134 | -4608.648 | -1030.568 |
| C101 | 135 | -4562.184 | -1030.568 |
| C102 | 136 | -4515.720 | -1030.568 |
| C103 | 137 | -4469.256 | -1030.568 |
| C104 | 138 | -4422.792 | -1030.568 |
| C105 | 139 | -4376.328 | -1030.568 |
| C106 | 140 | -4329.864 | -1030.568 |
| C107 | 141 | -4283.400 | -1030.568 |
| C108 | 142 | -4236.936 | -1030.568 |
| C109 | 143 | -4190.472 | -1030.568 |
| C110 | 144 | -4144.008 | -1030.568 |
| C111 | 145 | -4097.544 | -1030.568 |
| C112 | 146 | -4051.080 | -1030.568 |
| C113 | 147 | -4004.616 | -1030.568 |
| C114 | 148 | -3958.152 | -1030.568 |
| C115 | 149 | -3911.688 | -1030.568 |
| C116 | 150 | -3865.224 | -1030.568 |
| C117 | 151 | -3818.760 | -1030.568 |
| C118 | 152 | -3772.296 | -1030.568 |
| C119 | 153 | -3725.832 | -1030.568 |
| C120 | 154 | -3679.368 | -1030.568 |

STN RGB - 132 × 132 × 3 driver

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| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|------------|
| | | x | y |
| C121 | 155 | -3632.904 | -1 030.568 |
| C122 | 156 | -3586.440 | -1 030.568 |
| C123 | 157 | -3539.976 | -1 030.568 |
| C124 | 158 | -3493.512 | -1 030.568 |
| C125 | 159 | -3447.048 | -1 030.568 |
| C126 | 160 | -3400.584 | -1 030.568 |
| C127 | 161 | -3354.120 | -1 030.568 |
| C128 | 162 | -3307.656 | -1 030.568 |
| C129 | 163 | -3261.192 | -1 030.568 |
| C130 | 164 | -3214.728 | -1 030.568 |
| C131 | 165 | -3168.264 | -1 030.568 |
| C132 | 166 | -3121.800 | -1 030.568 |
| C133 | 167 | -3075.336 | -1 030.568 |
| C134 | 168 | -3028.872 | -1 030.568 |
| C135 | 169 | -2982.408 | -1 030.568 |
| C136 | 170 | -2935.944 | -1 030.568 |
| C137 | 171 | -2889.480 | -1 030.568 |
| C138 | 172 | -2843.016 | -1 030.568 |
| C139 | 173 | -2796.552 | -1 030.568 |
| C140 | 174 | -2750.088 | -1 030.568 |
| C141 | 175 | -2703.624 | -1 030.568 |
| C142 | 176 | -2657.160 | -1 030.568 |
| C143 | 177 | -2610.696 | -1 030.568 |
| C144 | 178 | -2507.032 | -1 030.568 |
| C145 | 179 | -2460.568 | -1 030.568 |
| C146 | 180 | -2414.104 | -1 030.568 |
| C147 | 181 | -2367.640 | -1 030.568 |
| C148 | 182 | -2321.176 | -1 030.568 |
| C149 | 183 | -2274.712 | -1 030.568 |
| C150 | 184 | -2228.248 | -1 030.568 |
| C151 | 185 | -2181.784 | -1 030.568 |
| C152 | 186 | -2135.320 | -1 030.568 |
| C153 | 187 | -2088.856 | -1 030.568 |
| C154 | 188 | -2042.392 | -1 030.568 |
| C155 | 189 | -1995.928 | -1 030.568 |
| C156 | 190 | -1949.464 | -1 030.568 |
| C157 | 191 | -1903.000 | -1 030.568 |
| C158 | 192 | -1856.536 | -1 030.568 |
| C159 | 193 | -1810.072 | -1 030.568 |

| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|------------|
| | | x | y |
| C160 | 194 | -1763.608 | -1 030.568 |
| C161 | 195 | -1717.144 | -1 030.568 |
| C162 | 196 | -1670.680 | -1 030.568 |
| C163 | 197 | -1624.216 | -1 030.568 |
| C164 | 198 | -1577.752 | -1 030.568 |
| C165 | 199 | -1531.288 | -1 030.568 |
| C166 | 200 | -1484.824 | -1 030.568 |
| C167 | 201 | -1438.360 | -1 030.568 |
| C168 | 202 | -1391.896 | -1 030.568 |
| C169 | 203 | -1345.432 | -1 030.568 |
| C170 | 204 | -1298.968 | -1 030.568 |
| C171 | 205 | -1252.504 | -1 030.568 |
| C172 | 206 | -1206.040 | -1 030.568 |
| C173 | 207 | -1159.576 | -1 030.568 |
| C174 | 208 | -1113.112 | -1 030.568 |
| C175 | 209 | -1066.648 | -1 030.568 |
| C176 | 210 | -1020.184 | -1 030.568 |
| C177 | 211 | -973.720 | -1 030.568 |
| C178 | 212 | -927.256 | -1 030.568 |
| C179 | 213 | -880.792 | -1 030.568 |
| C180 | 214 | -834.328 | -1 030.568 |
| C181 | 215 | -787.864 | -1 030.568 |
| C182 | 216 | -741.400 | -1 030.568 |
| C183 | 217 | -694.936 | -1 030.568 |
| C184 | 218 | -648.472 | -1 030.568 |
| C185 | 219 | -602.008 | -1 030.568 |
| C186 | 220 | -555.544 | -1 030.568 |
| C187 | 221 | -509.080 | -1 030.568 |
| C188 | 222 | -462.616 | -1 030.568 |
| C189 | 223 | -416.152 | -1 030.568 |
| C190 | 224 | -369.688 | -1 030.568 |
| C191 | 225 | -323.224 | -1 030.568 |
| C192 | 226 | -219.560 | -1 030.568 |
| C193 | 227 | -173.096 | -1 030.568 |
| C194 | 228 | -126.632 | -1 030.568 |
| C195 | 229 | -80.168 | -1 030.568 |
| C196 | 230 | -33.704 | -1 030.568 |
| C197 | 231 | +12.760 | -1 030.568 |
| C198 | 232 | +59.224 | -1 030.568 |

STN RGB - 132 × 132 × 3 driver

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| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|------------|
| | | x | y |
| C199 | 233 | +105.688 | -1 030.568 |
| C200 | 234 | +152.152 | -1 030.568 |
| C201 | 235 | +198.616 | -1 030.568 |
| C202 | 236 | +245.080 | -1 030.568 |
| C203 | 237 | +291.544 | -1 030.568 |
| C204 | 238 | +338.008 | -1 030.568 |
| C205 | 239 | +384.472 | -1 030.568 |
| C206 | 240 | +430.936 | -1 030.568 |
| C207 | 241 | +477.400 | -1 030.568 |
| C208 | 242 | +523.864 | -1 030.568 |
| C209 | 243 | +570.328 | -1 030.568 |
| C210 | 244 | +616.792 | -1 030.568 |
| C211 | 245 | +663.256 | -1 030.568 |
| C212 | 246 | +709.720 | -1 030.568 |
| C213 | 247 | +756.184 | -1 030.568 |
| C214 | 248 | +802.648 | -1 030.568 |
| C215 | 249 | +849.112 | -1 030.568 |
| C216 | 250 | +895.576 | -1 030.568 |
| C217 | 251 | +942.040 | -1 030.568 |
| C218 | 252 | +988.504 | -1 030.568 |
| C219 | 253 | +1 034.968 | -1 030.568 |
| C220 | 254 | +1 081.432 | -1 030.568 |
| C221 | 255 | +1 127.896 | -1 030.568 |
| C222 | 256 | +1 174.360 | -1 030.568 |
| C223 | 257 | +1 220.824 | -1 030.568 |
| C224 | 258 | +1 267.288 | -1 030.568 |
| C225 | 259 | +1 313.752 | -1 030.568 |
| C226 | 260 | +1 360.216 | -1 030.568 |
| C227 | 261 | +1 406.680 | -1 030.568 |
| C228 | 262 | +1 453.144 | -1 030.568 |
| C229 | 263 | +1 499.608 | -1 030.568 |
| C230 | 264 | +1 546.072 | -1 030.568 |
| C231 | 265 | +1 592.536 | -1 030.568 |
| C232 | 266 | +1 639.000 | -1 030.568 |
| C233 | 267 | +1 685.464 | -1 030.568 |
| C234 | 268 | +1 731.928 | -1 030.568 |
| C235 | 269 | +1 778.392 | -1 030.568 |
| C236 | 270 | +1 824.856 | -1 030.568 |
| C237 | 271 | +1 871.320 | -1 030.568 |

| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|------------|
| | | x | y |
| C238 | 272 | +1 917.784 | -1 030.568 |
| C239 | 273 | +1 964.248 | -1 030.568 |
| C240 | 274 | +2 067.912 | -1 030.568 |
| C241 | 275 | +2 114.376 | -1 030.568 |
| C242 | 276 | +2 160.840 | -1 030.568 |
| C243 | 277 | +2 207.304 | -1 030.568 |
| C244 | 278 | +2 253.768 | -1 030.568 |
| C245 | 279 | +2 300.232 | -1 030.568 |
| C246 | 280 | +2 346.696 | -1 030.568 |
| C247 | 281 | +2 393.160 | -1 030.568 |
| C248 | 282 | +2 439.624 | -1 030.568 |
| C249 | 283 | +2 486.088 | -1 030.568 |
| C250 | 284 | +2 532.552 | -1 030.568 |
| C251 | 285 | +2 579.016 | -1 030.568 |
| C252 | 286 | +2 625.480 | -1 030.568 |
| C253 | 287 | +2 671.944 | -1 030.568 |
| C254 | 288 | +2 718.408 | -1 030.568 |
| C255 | 289 | +2 764.872 | -1 030.568 |
| C256 | 290 | +2 811.336 | -1 030.568 |
| C257 | 291 | +2 857.800 | -1 030.568 |
| C258 | 292 | +2 904.264 | -1 030.568 |
| C259 | 293 | +2 950.728 | -1 030.568 |
| C260 | 294 | +2 997.192 | -1 030.568 |
| C261 | 295 | +3 043.656 | -1 030.568 |
| C262 | 296 | +3 090.120 | -1 030.568 |
| C263 | 297 | +3 136.584 | -1 030.568 |
| C264 | 298 | +3 183.048 | -1 030.568 |
| C265 | 299 | +3 229.512 | -1 030.568 |
| C266 | 300 | +3 275.976 | -1 030.568 |
| C267 | 301 | +3 322.440 | -1 030.568 |
| C268 | 302 | +3 368.904 | -1 030.568 |
| C269 | 303 | +3 415.368 | -1 030.568 |
| C270 | 304 | +3 461.832 | -1 030.568 |
| C271 | 305 | +3 508.296 | -1 030.568 |
| C272 | 306 | +3 554.760 | -1 030.568 |
| C273 | 307 | +3 601.224 | -1 030.568 |
| C274 | 308 | +3 647.688 | -1 030.568 |
| C275 | 309 | +3 694.152 | -1 030.568 |
| C276 | 310 | +3 740.616 | -1 030.568 |

STN RGB - 132 × 132 × 3 driver

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| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|-----------|
| | | x | y |
| C277 | 311 | +3787.080 | -1030.568 |
| C278 | 312 | +3833.544 | -1030.568 |
| C279 | 313 | +3880.008 | -1030.568 |
| C280 | 314 | +3926.472 | -1030.568 |
| C281 | 315 | +3972.936 | -1030.568 |
| C282 | 316 | +4019.400 | -1030.568 |
| C283 | 317 | +4065.864 | -1030.568 |
| C284 | 318 | +4112.328 | -1030.568 |
| C285 | 319 | +4158.792 | -1030.568 |
| C286 | 320 | +4205.256 | -1030.568 |
| C287 | 321 | +4251.720 | -1030.568 |
| C288 | 322 | +4355.384 | -1030.568 |
| C289 | 323 | +4401.848 | -1030.568 |
| C290 | 324 | +4448.312 | -1030.568 |
| C291 | 325 | +4494.776 | -1030.568 |
| C292 | 326 | +4541.240 | -1030.568 |
| C293 | 327 | +4587.704 | -1030.568 |
| C294 | 328 | +4634.168 | -1030.568 |
| C295 | 329 | +4680.632 | -1030.568 |
| C296 | 330 | +4727.096 | -1030.568 |
| C297 | 331 | +4773.560 | -1030.568 |
| C298 | 332 | +4820.024 | -1030.568 |
| C299 | 333 | +4866.488 | -1030.568 |
| C300 | 334 | +4912.952 | -1030.568 |
| C301 | 335 | +4959.416 | -1030.568 |
| C302 | 336 | +5005.880 | -1030.568 |
| C303 | 337 | +5052.344 | -1030.568 |
| C304 | 338 | +5098.808 | -1030.568 |
| C305 | 339 | +5145.272 | -1030.568 |
| C306 | 340 | +5191.736 | -1030.568 |
| C307 | 341 | +5238.200 | -1030.568 |
| C308 | 342 | +5284.664 | -1030.568 |
| C309 | 343 | +5331.128 | -1030.568 |
| C310 | 344 | +5377.592 | -1030.568 |
| C311 | 345 | +5424.056 | -1030.568 |
| C312 | 346 | +5470.520 | -1030.568 |
| C313 | 347 | +5516.984 | -1030.568 |
| C314 | 348 | +5563.448 | -1030.568 |
| C315 | 349 | +5609.912 | -1030.568 |

| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|-----------|
| | | x | y |
| C316 | 350 | +5656.376 | -1030.568 |
| C317 | 351 | +5702.840 | -1030.568 |
| C318 | 352 | +5749.304 | -1030.568 |
| C319 | 353 | +5795.768 | -1030.568 |
| C320 | 354 | +5842.232 | -1030.568 |
| C321 | 355 | +5888.696 | -1030.568 |
| C322 | 356 | +5935.160 | -1030.568 |
| C323 | 357 | +5981.624 | -1030.568 |
| C324 | 358 | +6028.088 | -1030.568 |
| C325 | 359 | +6074.552 | -1030.568 |
| C326 | 360 | +6121.016 | -1030.568 |
| C327 | 361 | +6167.480 | -1030.568 |
| C328 | 362 | +6213.944 | -1030.568 |
| C329 | 363 | +6260.408 | -1030.568 |
| C330 | 364 | +6306.872 | -1030.568 |
| C331 | 365 | +6353.336 | -1030.568 |
| C332 | 366 | +6399.800 | -1030.568 |
| C333 | 367 | +6446.264 | -1030.568 |
| C334 | 368 | +6492.728 | -1030.568 |
| C335 | 369 | +6539.192 | -1030.568 |
| C336 | 370 | +6642.856 | -1030.568 |
| C337 | 371 | +6689.320 | -1030.568 |
| C338 | 372 | +6735.784 | -1030.568 |
| C339 | 373 | +6782.248 | -1030.568 |
| C340 | 374 | +6828.712 | -1030.568 |
| C341 | 375 | +6875.176 | -1030.568 |
| C342 | 376 | +6921.640 | -1030.568 |
| C343 | 377 | +6968.104 | -1030.568 |
| C344 | 378 | +7014.568 | -1030.568 |
| C345 | 379 | +7061.032 | -1030.568 |
| C346 | 380 | +7107.496 | -1030.568 |
| C347 | 381 | +7153.960 | -1030.568 |
| C348 | 382 | +7200.424 | -1030.568 |
| C349 | 383 | +7246.888 | -1030.568 |
| C350 | 384 | +7293.352 | -1030.568 |
| C351 | 385 | +7339.816 | -1030.568 |
| C352 | 386 | +7386.280 | -1030.568 |
| C353 | 387 | +7432.744 | -1030.568 |
| C354 | 388 | +7479.208 | -1030.568 |

STN RGB - 132 × 132 × 3 driver

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| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|-----------|
| | | x | y |
| C355 | 389 | +7525.672 | -1030.568 |
| C356 | 390 | +7572.136 | -1030.568 |
| C357 | 391 | +7618.600 | -1030.568 |
| C358 | 392 | +7665.064 | -1030.568 |
| C359 | 393 | +7711.528 | -1030.568 |
| C360 | 394 | +7757.992 | -1030.568 |
| C361 | 395 | +7804.456 | -1030.568 |
| C362 | 396 | +7850.920 | -1030.568 |
| C363 | 397 | +7897.384 | -1030.568 |
| C364 | 398 | +7943.848 | -1030.568 |
| C365 | 399 | +7990.312 | -1030.568 |
| C366 | 400 | +8036.776 | -1030.568 |
| C367 | 401 | +8083.240 | -1030.568 |
| C368 | 402 | +8129.704 | -1030.568 |
| C369 | 403 | +8176.168 | -1030.568 |
| C370 | 404 | +8222.632 | -1030.568 |
| C371 | 405 | +8269.096 | -1030.568 |
| C372 | 406 | +8315.560 | -1030.568 |
| C373 | 407 | +8362.024 | -1030.568 |
| C374 | 408 | +8408.488 | -1030.568 |
| C375 | 409 | +8454.952 | -1030.568 |
| C376 | 410 | +8501.416 | -1030.568 |
| C377 | 411 | +8547.880 | -1030.568 |
| C378 | 412 | +8594.344 | -1030.568 |
| C379 | 413 | +8640.808 | -1030.568 |
| C380 | 414 | +8687.272 | -1030.568 |
| C381 | 415 | +8733.736 | -1030.568 |
| C382 | 416 | +8780.200 | -1030.568 |
| C383 | 417 | +8826.664 | -1030.568 |
| C384 | 418 | +8930.328 | -1030.568 |
| C385 | 419 | +8976.792 | -1030.568 |
| C386 | 420 | +9023.256 | -1030.568 |
| C387 | 421 | +9069.720 | -1030.568 |
| C388 | 422 | +9116.184 | -1030.568 |
| C389 | 423 | +9162.648 | -1030.568 |
| C390 | 424 | +9209.112 | -1030.568 |
| C391 | 425 | +9255.576 | -1030.568 |
| C392 | 426 | +9302.040 | -1030.568 |
| C393 | 427 | +9348.504 | -1030.568 |

| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|-----------|
| | | x | y |
| C394 | 428 | +9394.968 | -1030.568 |
| C395 | 429 | +9441.432 | -1030.568 |
| R0 | 430 | +9596.664 | -1035.694 |
| R1 | 431 | +9649.464 | -1035.694 |
| R2 | 432 | +9702.264 | -1035.694 |
| R3 | 433 | +9755.064 | -1035.694 |
| R4 | 434 | +9807.864 | -1035.694 |
| R5 | 435 | +9860.664 | -1035.694 |
| R6 | 436 | +9913.464 | -1035.694 |
| R7 | 437 | +9966.264 | -1035.694 |
| R8 | 438 | +10019.064 | -1035.694 |
| R9 | 439 | +10071.864 | -1035.694 |
| R10 | 440 | +10124.664 | -1035.694 |
| R11 | 441 | +10177.464 | -1035.694 |
| R12 | 442 | +10230.264 | -1035.694 |
| R13 | 443 | +10283.064 | -1035.694 |
| R14 | 444 | +10335.864 | -1035.694 |
| R15 | 445 | +10388.664 | -1035.694 |
| R16 | 446 | +10441.464 | -1035.694 |
| R17 | 447 | +10494.264 | -1035.694 |
| R18 | 448 | +10547.064 | -1035.694 |
| R19 | 449 | +10599.864 | -1035.694 |
| R20 | 450 | +10652.664 | -1035.694 |
| R21 | 451 | +10705.464 | -1035.694 |
| R22 | 452 | +10758.264 | -1035.694 |
| R23 | 453 | +10811.064 | -1035.694 |
| R24 | 454 | +10863.864 | -1035.694 |
| R25 | 455 | +10916.664 | -1035.694 |
| R26 | 456 | +10969.464 | -1035.694 |
| R27 | 457 | +11022.264 | -1035.694 |
| R28 | 458 | +11075.064 | -1035.694 |
| R29 | 459 | +11127.864 | -1035.694 |
| R30 | 460 | +11180.664 | -1035.694 |
| R31 | 461 | +11233.464 | -1035.694 |
| dummy | 462 | +11358.424 | -1035.694 |
| dummy | 463 | +11358.424 | +1035.694 |
| R63 | 464 | +11233.464 | +1035.694 |
| R62 | 465 | +11180.664 | +1035.694 |
| R61 | 466 | +11127.864 | +1035.694 |

STN RGB - 132 × 132 × 3 driver

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| SYMBOL | PAD | COORDINATES | |
|------------------|-----|-------------|-----------|
| | | x | y |
| R60 | 467 | +11075.064 | +1035.694 |
| R59 | 468 | +11022.264 | +1035.694 |
| R58 | 469 | +10969.464 | +1035.694 |
| R57 | 470 | +10916.664 | +1035.694 |
| R56 | 471 | +10863.864 | +1035.694 |
| R55 | 472 | +10811.064 | +1035.694 |
| R54 | 473 | +10758.264 | +1035.694 |
| R53 | 474 | +10705.464 | +1035.694 |
| R52 | 475 | +10652.664 | +1035.694 |
| R51 | 476 | +10599.864 | +1035.694 |
| R50 | 477 | +10547.064 | +1035.694 |
| R49 | 478 | +10494.264 | +1035.694 |
| R48 | 479 | +10441.464 | +1035.694 |
| R47 | 480 | +10388.664 | +1035.694 |
| R46 | 481 | +10335.864 | +1035.694 |
| R45 | 482 | +10283.064 | +1035.694 |
| R44 | 483 | +10230.264 | +1035.694 |
| R43 | 484 | +10177.464 | +1035.694 |
| R42 | 485 | +10124.664 | +1035.694 |
| R41 | 486 | +10071.864 | +1035.694 |
| R40 | 487 | +10019.064 | +1035.694 |
| R39 | 488 | +9966.264 | +1035.694 |
| R38 | 489 | +9913.464 | +1035.694 |
| R37 | 490 | +9860.664 | +1035.694 |
| R36 | 491 | +9807.864 | +1035.694 |
| R35 | 492 | +9755.064 | +1035.694 |
| R34 | 493 | +9702.264 | +1035.694 |
| R33 | 494 | +9649.464 | +1035.694 |
| R32 | 495 | +9596.664 | +1035.694 |
| RES | 496 | +9332.664 | +1035.694 |
| TE | 497 | +9174.264 | +1035.694 |
| V _{SS1} | 498 | +8963.064 | +1035.694 |
| V _{SS1} | 499 | +8910.264 | +1035.694 |
| V _{SS1} | 500 | +8857.464 | +1035.694 |
| V _{SS1} | 501 | +8804.664 | +1035.694 |
| V _{SS1} | 502 | +8751.864 | +1035.694 |
| V _{SS1} | 503 | +8699.064 | +1035.694 |
| V _{SS1} | 504 | +8646.264 | +1035.694 |
| V _{SS1} | 505 | +8593.464 | +1035.694 |

| SYMBOL | PAD | COORDINATES | |
|------------------|-----|-------------|-----------|
| | | x | y |
| V _{SS1} | 506 | +8540.664 | +1035.694 |
| V _{SS1} | 507 | +8487.864 | +1035.694 |
| V _{SS2} | 508 | +8329.464 | +1035.694 |
| V _{SS2} | 509 | +8276.664 | +1035.694 |
| V _{SS2} | 510 | +8223.864 | +1035.694 |
| V _{SS2} | 511 | +8171.064 | +1035.694 |
| V _{SS2} | 512 | +8118.264 | +1035.694 |
| V _{SS2} | 513 | +8065.464 | +1035.694 |
| V _{SS2} | 514 | +8012.664 | +1035.694 |
| V _{SS2} | 515 | +7959.864 | +1035.694 |
| V _{SS2} | 516 | +7907.064 | +1035.694 |
| V _{SS2} | 517 | +7854.264 | +1035.694 |
| CS/SCE | 518 | +7643.064 | +1035.694 |
| V _{DD1} | 519 | +7431.864 | +1035.694 |
| V _{DD1} | 520 | +7379.064 | +1035.694 |
| V _{DD1} | 521 | +7326.264 | +1035.694 |
| V _{DD1} | 522 | +7273.464 | +1035.694 |
| V _{DD1} | 523 | +7220.664 | +1035.694 |
| V _{DD1} | 524 | +7167.864 | +1035.694 |
| V _{DD3} | 525 | +7009.464 | +1035.694 |
| V _{DD3} | 526 | +6956.664 | +1035.694 |
| V _{DD3} | 527 | +6903.864 | +1035.694 |
| V _{DD3} | 528 | +6851.064 | +1035.694 |
| V _{DD3} | 529 | +6798.264 | +1035.694 |
| V _{DD2} | 530 | +6639.864 | +1035.694 |
| V _{DD2} | 531 | +6587.064 | +1035.694 |
| V _{DD2} | 532 | +6534.264 | +1035.694 |
| V _{DD2} | 533 | +6481.464 | +1035.694 |
| V _{DD2} | 534 | +6428.664 | +1035.694 |
| V _{DD2} | 535 | +6375.864 | +1035.694 |
| V _{DD2} | 536 | +6323.064 | +1035.694 |
| V _{DD2} | 537 | +6270.264 | +1035.694 |
| V _{DD2} | 538 | +6217.464 | +1035.694 |
| V _{DD2} | 539 | +6164.664 | +1035.694 |
| D7 | 540 | +5953.464 | +1035.694 |
| D3 | 541 | +5795.064 | +1035.694 |
| D6 | 542 | +5636.664 | +1035.694 |
| D2 | 543 | +5478.264 | +1035.694 |
| D5 | 544 | +5319.864 | +1035.694 |

STN RGB - 132 × 132 × 3 driver

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| SYMBOL | PAD | COORDINATES | |
|-----------------------|-----|-------------|-----------|
| | | x | y |
| D1 | 545 | +5161.464 | +1035.694 |
| D4 | 546 | +5003.064 | +1035.694 |
| D0/SDIN | 547 | +4844.664 | +1035.694 |
| SDOUT | 548 | +4686.264 | +1035.694 |
| $\overline{DC}/SCLK$ | 549 | +4527.864 | +1035.694 |
| \overline{WR} | 550 | +4369.464 | +1035.694 |
| \overline{RD} | 551 | +4211.064 | +1035.694 |
| PS0 | 552 | +4052.664 | +1035.694 |
| PS1 | 553 | +3894.264 | +1035.694 |
| PS2 | 554 | +3735.864 | +1035.694 |
| OSC | 555 | +3577.464 | +1035.694 |
| V _{DDTIEOFF} | 556 | +3419.064 | +1035.694 |
| V _{OTPdrain} | 557 | +3207.864 | +1035.694 |
| V _{OTPdrain} | 558 | +3155.064 | +1035.694 |
| V _{OTPdrain} | 559 | +3102.264 | +1035.694 |
| V _{OTPdrain} | 560 | +3049.464 | +1035.694 |
| V _{OTPdrain} | 561 | +2996.664 | +1035.694 |
| V _{OTPdrain} | 562 | +2943.864 | +1035.694 |
| V _{OTPdrain} | 563 | +2891.064 | +1035.694 |
| V _{OTPdrain} | 564 | +2838.264 | +1035.694 |
| V _{OTPgate} | 565 | +2679.864 | +1035.694 |
| V _{OTPgate} | 566 | +2627.064 | +1035.694 |
| V _{OTPgate} | 567 | +2574.264 | +1035.694 |
| V _{OTPgate} | 568 | +2521.464 | +1035.694 |
| V _{OTPgate} | 569 | +2468.664 | +1035.694 |
| V _{OTPgate} | 570 | +2415.864 | +1035.694 |
| V _{OTPgate} | 571 | +2363.064 | +1035.694 |
| V _{OTPgate} | 572 | +2310.264 | +1035.694 |
| T6 | 573 | +2099.064 | +1035.694 |
| T5 | 574 | +1940.664 | +1035.694 |
| T4 | 575 | +1782.264 | +1035.694 |
| T3 | 576 | +1623.864 | +1035.694 |
| T2 | 577 | +1465.464 | +1035.694 |
| T1 | 578 | +1307.064 | +1035.694 |
| V _{SSTIEOFF} | 579 | +1148.664 | +1035.694 |
| dummy | 580 | +1037.080 | +1035.694 |
| dummy | 581 | +984.280 | +1035.694 |
| dummy | 582 | +931.480 | +1035.694 |
| dummy | 583 | +878.680 | +1035.694 |

| SYMBOL | PAD | COORDINATES | |
|--------|-----|-------------|-----------|
| | | x | y |
| dummy | 584 | +825.880 | +1035.694 |
| dummy | 585 | +773.080 | +1035.694 |
| dummy | 586 | +720.280 | +1035.694 |
| dummy | 587 | +667.480 | +1035.694 |
| dummy | 588 | +614.680 | +1035.694 |
| dummy | 589 | +561.880 | +1035.694 |
| dummy | 590 | +509.080 | +1035.694 |
| dummy | 591 | +456.280 | +1035.694 |
| dummy | 592 | +403.480 | +1035.694 |
| dummy | 593 | +350.680 | +1035.694 |
| dummy | 594 | +297.880 | +1035.694 |
| dummy | 595 | +245.080 | +1035.694 |
| dummy | 596 | +192.280 | +1035.694 |
| dummy | 597 | +139.480 | +1035.694 |
| dummy | 598 | +86.680 | +1035.694 |
| dummy | 599 | +33.880 | +1035.694 |
| dummy | 600 | -18.920 | +1035.694 |
| dummy | 601 | -71.720 | +1035.694 |
| dummy | 602 | -124.520 | +1035.694 |
| dummy | 603 | -177.320 | +1035.694 |
| dummy | 604 | -230.120 | +1035.694 |
| dummy | 605 | -282.920 | +1035.694 |
| dummy | 606 | -335.720 | +1035.694 |
| dummy | 607 | -388.520 | +1035.694 |
| dummy | 608 | -441.320 | +1035.694 |
| dummy | 609 | -494.120 | +1035.694 |
| dummy | 610 | -546.920 | +1035.694 |
| dummy | 611 | -599.720 | +1035.694 |
| dummy | 612 | -652.520 | +1035.694 |
| dummy | 613 | -705.320 | +1035.694 |
| dummy | 614 | -758.120 | +1035.694 |
| dummy | 615 | -810.920 | +1035.694 |
| dummy | 616 | -863.720 | +1035.694 |
| dummy | 617 | -916.520 | +1035.694 |
| dummy | 618 | -969.320 | +1035.694 |
| dummy | 619 | -1022.120 | +1035.694 |
| dummy | 620 | -1074.920 | +1035.694 |
| dummy | 621 | -1127.720 | +1035.694 |
| dummy | 622 | -1180.520 | +1035.694 |

STN RGB - 132 × 132 × 3 driver

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| SYMBOL | PAD | COORDINATES | |
|-----------------------|-----|-------------|-----------|
| | | x | y |
| dummy | 623 | -1233.320 | +1035.694 |
| V _{SSTIEOFF} | 624 | -1410.904 | +1035.694 |
| T7 | 625 | -1683.176 | +1035.694 |
| C1+ | 626 | -1841.576 | +1035.694 |
| C1+ | 627 | -1894.376 | +1035.694 |
| C1+ | 628 | -1947.176 | +1035.694 |
| C1+ | 629 | -1999.976 | +1035.694 |
| C1+ | 630 | -2052.776 | +1035.694 |
| C1+ | 631 | -2105.576 | +1035.694 |
| C1- | 632 | -2263.976 | +1035.694 |
| C1- | 633 | -2316.776 | +1035.694 |
| C1- | 634 | -2369.576 | +1035.694 |
| C1- | 635 | -2422.376 | +1035.694 |
| C1- | 636 | -2475.176 | +1035.694 |
| C1- | 637 | -2527.976 | +1035.694 |
| C2+ | 638 | -2686.376 | +1035.694 |
| C2+ | 639 | -2739.176 | +1035.694 |
| C2+ | 640 | -2791.976 | +1035.694 |
| C2+ | 641 | -2844.776 | +1035.694 |
| C2+ | 642 | -2897.576 | +1035.694 |
| C2+ | 643 | -2950.376 | +1035.694 |
| C2- | 644 | -3108.776 | +1035.694 |
| C2- | 645 | -3161.576 | +1035.694 |
| C2- | 646 | -3214.376 | +1035.694 |
| C2- | 647 | -3267.176 | +1035.694 |
| C2- | 648 | -3319.976 | +1035.694 |
| C2- | 649 | -3372.776 | +1035.694 |
| C3+ | 650 | -3531.176 | +1035.694 |
| C3+ | 651 | -3583.976 | +1035.694 |
| C3+ | 652 | -3636.776 | +1035.694 |
| C3+ | 653 | -3689.576 | +1035.694 |
| C3+ | 654 | -3742.376 | +1035.694 |
| C3+ | 655 | -3795.176 | +1035.694 |
| C3- | 656 | -3953.576 | +1035.694 |
| C3- | 657 | -4006.376 | +1035.694 |
| C3- | 658 | -4059.176 | +1035.694 |
| C3- | 659 | -4111.976 | +1035.694 |
| C3- | 660 | -4164.776 | +1035.694 |
| C3- | 661 | -4217.576 | +1035.694 |

| SYMBOL | PAD | COORDINATES | |
|----------------------|-----|-------------|-----------|
| | | x | y |
| C4+ | 662 | -4375.976 | +1035.694 |
| C4+ | 663 | -4428.776 | +1035.694 |
| C4+ | 664 | -4481.576 | +1035.694 |
| C4+ | 665 | -4534.376 | +1035.694 |
| C4+ | 666 | -4587.176 | +1035.694 |
| C4+ | 667 | -4639.976 | +1035.694 |
| C4- | 668 | -4798.376 | +1035.694 |
| C4- | 669 | -4851.176 | +1035.694 |
| C4- | 670 | -4903.976 | +1035.694 |
| C4- | 671 | -4956.776 | +1035.694 |
| C4- | 672 | -5009.576 | +1035.694 |
| C4- | 673 | -5062.376 | +1035.694 |
| V _{LCDOUT1} | 674 | -5220.776 | +1035.694 |
| V _{LCDOUT1} | 675 | -5273.576 | +1035.694 |
| V _{LCDOUT1} | 676 | -5326.376 | +1035.694 |
| V _{LCDOUT1} | 677 | -5379.176 | +1035.694 |
| V _{LCDOUT1} | 678 | -5431.976 | +1035.694 |
| V _{LCDOUT1} | 679 | -5484.776 | +1035.694 |
| V _{LCDOUT1} | 680 | -5537.576 | +1035.694 |
| V _{LCDOUT1} | 681 | -5590.376 | +1035.694 |
| V _{LCDOUT1} | 682 | -5643.176 | +1035.694 |
| V _{LCDOUT1} | 683 | -5695.976 | +1035.694 |
| V _{LCDIN1} | 684 | -5854.376 | +1035.694 |
| V _{LCDIN1} | 685 | -5907.176 | +1035.694 |
| V _{LCDIN1} | 686 | -5959.976 | +1035.694 |
| V _{LCDIN1} | 687 | -6012.776 | +1035.694 |
| V _{LCDIN1} | 688 | -6065.576 | +1035.694 |
| V _{LCDIN1} | 689 | -6118.376 | +1035.694 |
| V _{LCDIN1} | 690 | -6171.176 | +1035.694 |
| C5+ | 691 | -6329.576 | +1035.694 |
| C5+ | 692 | -6382.376 | +1035.694 |
| C5+ | 693 | -6435.176 | +1035.694 |
| C5+ | 694 | -6487.976 | +1035.694 |
| C5+ | 695 | -6540.776 | +1035.694 |
| C5+ | 696 | -6593.576 | +1035.694 |
| C5- | 697 | -6751.976 | +1035.694 |
| C5- | 698 | -6804.776 | +1035.694 |
| C5- | 699 | -6857.576 | +1035.694 |
| C5- | 700 | -6910.376 | +1035.694 |

STN RGB - 132 × 132 × 3 driver

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| SYMBOL | PAD | COORDINATES | |
|-----------------------|-----|-------------|-----------|
| | | x | y |
| C5- | 701 | -6963.176 | +1035.694 |
| C5- | 702 | -7015.976 | +1035.694 |
| V _{LCDOUT2} | 703 | -7174.376 | +1035.694 |
| V _{LCDOUT2} | 704 | -7227.176 | +1035.694 |
| V _{LCDOUT2} | 705 | -7279.976 | +1035.694 |
| V _{LCDOUT2} | 706 | -7332.776 | +1035.694 |
| V _{LCDOUT2} | 707 | -7385.576 | +1035.694 |
| V _{LCDOUT2} | 708 | -7438.376 | +1035.694 |
| V _{LCDOUT2} | 709 | -7491.176 | +1035.694 |
| V _{LCDOUT2} | 710 | -7543.976 | +1035.694 |
| V _{LCDOUT2} | 711 | -7596.776 | +1035.694 |
| V _{LCDSENSE} | 712 | -7649.576 | +1035.694 |
| V _{LCDIN2} | 713 | -7807.976 | +1035.694 |
| V _{LCDIN2} | 714 | -7860.776 | +1035.694 |
| V _{LCDIN2} | 715 | -7913.576 | +1035.694 |
| V _{LCDIN2} | 716 | -7966.376 | +1035.694 |
| V _{LCDIN2} | 717 | -8019.176 | +1035.694 |
| V _{LCDIN2} | 718 | -8071.976 | +1035.694 |
| V _{LCDIN2} | 719 | -8124.776 | +1035.694 |
| V2L | 720 | -8341.212 | +1035.694 |
| V2L | 721 | -8394.012 | +1035.694 |
| V1L | 722 | -8499.612 | +1035.694 |
| V1L | 723 | -8552.412 | +1035.694 |
| VC | 724 | -8658.012 | +1035.694 |
| VC | 725 | -8710.812 | +1035.694 |
| VC | 726 | -8763.612 | +1035.694 |
| VC | 727 | -8816.412 | +1035.694 |
| VC | 728 | -8869.212 | +1035.694 |
| V1H | 729 | -8974.812 | +1035.694 |
| V1H | 730 | -9027.612 | +1035.694 |
| V2H | 731 | -9133.212 | +1035.694 |
| V2H | 732 | -9186.012 | +1035.694 |
| R96 | 733 | -9383.880 | +1035.694 |
| R97 | 734 | -9436.680 | +1035.694 |
| R98 | 735 | -9489.480 | +1035.694 |
| R99 | 736 | -9542.280 | +1035.694 |
| R100 | 737 | -9595.080 | +1035.694 |
| R101 | 738 | -9647.880 | +1035.694 |
| R102 | 739 | -9700.680 | +1035.694 |

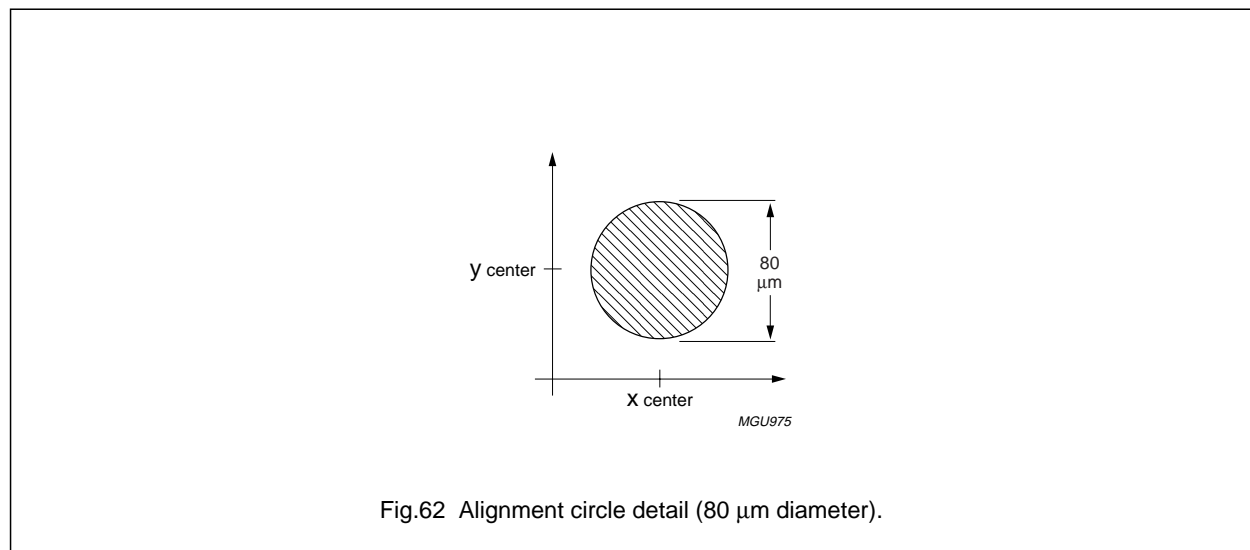
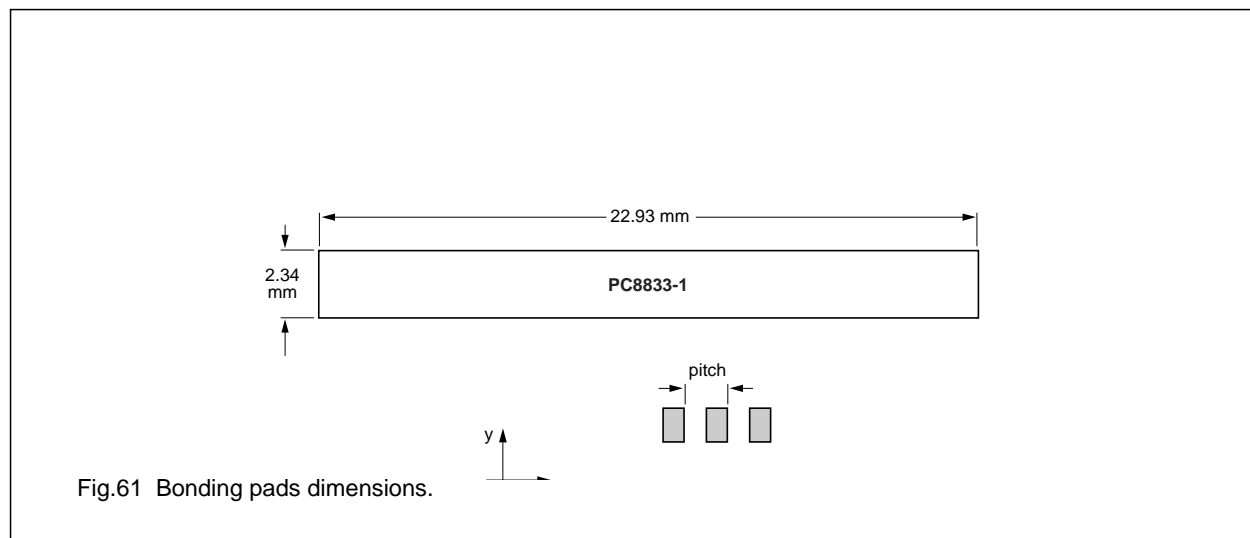
| SYMBOL | PAD | COORDINATES | |
|-------------------------------------|-----|-------------|-----------|
| | | x | y |
| R103 | 740 | -9753.480 | +1035.694 |
| R104 | 741 | -9806.280 | +1035.694 |
| R105 | 742 | -9859.080 | +1035.694 |
| R106 | 743 | -9911.880 | +1035.694 |
| R107 | 744 | -9964.680 | +1035.694 |
| R108 | 745 | -10017.480 | +1035.694 |
| R109 | 746 | -10070.280 | +1035.694 |
| R110 | 747 | -10123.080 | +1035.694 |
| R111 | 748 | -10175.880 | +1035.694 |
| R112 | 749 | -10228.680 | +1035.694 |
| R113 | 750 | -10281.480 | +1035.694 |
| R114 | 751 | -10334.280 | +1035.694 |
| R115 | 752 | -10387.080 | +1035.694 |
| R116 | 753 | -10439.880 | +1035.694 |
| R117 | 754 | -10492.680 | +1035.694 |
| R118 | 755 | -10545.480 | +1035.694 |
| R119 | 756 | -10598.280 | +1035.694 |
| R120 | 757 | -10651.080 | +1035.694 |
| R121 | 758 | -10703.880 | +1035.694 |
| R122 | 759 | -10756.680 | +1035.694 |
| R123 | 760 | -10809.480 | +1035.694 |
| R124 | 761 | -10862.280 | +1035.694 |
| R125 | 762 | -10915.080 | +1035.694 |
| R126 | 763 | -10967.880 | +1035.694 |
| R127 | 764 | -11020.680 | +1035.694 |
| R128 | 765 | -11073.480 | +1035.694 |
| R129 | 766 | -11126.280 | +1035.694 |
| R130 | 767 | -11179.080 | +1035.694 |
| R131 | 768 | -11231.880 | +1035.694 |
| dummy | 769 | -11351.208 | +1035.694 |
| Alignment marks (see Fig.62) | | | |
| Alignment circle 1 | | -11175.032 | +593.120 |
| Alignment circle 2 | | +11184.888 | +593.120 |
| Alignment circle 3 | | -8717.192 | +746.240 |
| Alignment circle 4 | | +9362.408 | +746.240 |

STN RGB - 132 × 132 × 3 driver

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Table 100 Bonding pad dimensions

| ITEM | DIMENSIONS | UNIT |
|-----------------------------------|----------------------------|------|
| Minimum bump pitch | columns: 46.464 | μm |
| | all other: 52.800 | |
| Bump dimensions | columns: 28.424 × 105.248 | μm |
| | all other: 32.736 × 95.348 | |
| Bump height | 15 | μm |
| Wafer thickness (excluding bumps) | 381 | μm |



STN RGB - 132 × 132 × 3 driver

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18 TRAY INFORMATION

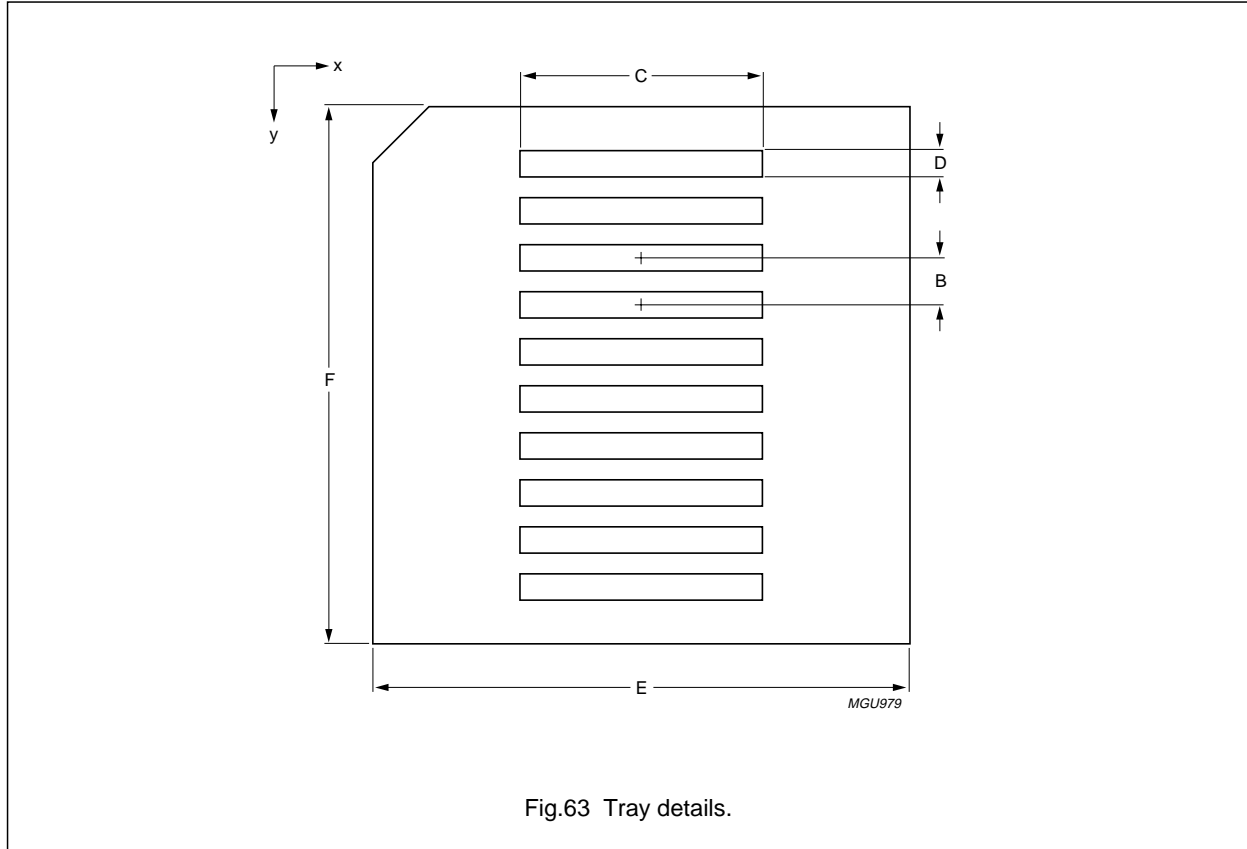
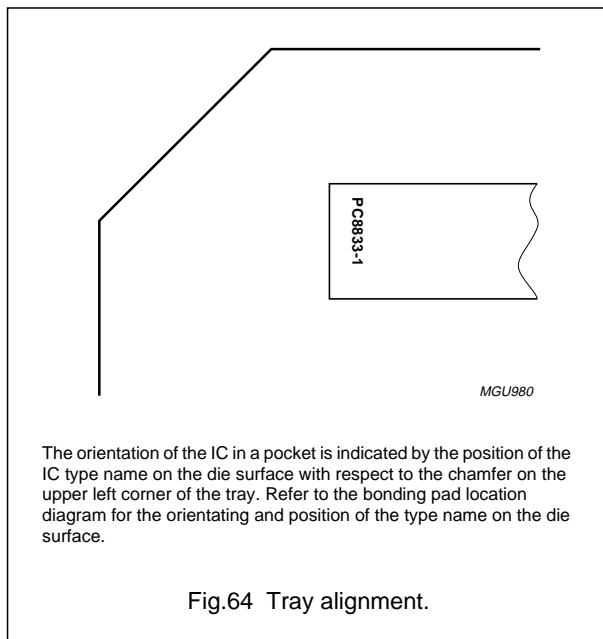


Fig.63 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.64 Tray alignment.

Table 101 Tray dimensions

| DIMENSIONS | DESCRIPTION | VALUE |
|------------|----------------------------------|----------|
| B | pocket pitch y direction | 4.45 mm |
| C | pocket width x direction | 23.07 mm |
| D | pocket width y direction | 2.47 mm |
| E | tray width x direction | 50.8 mm |
| F | tray width y direction | 50.8 mm |
| x | number of pockets in x direction | 1 |
| y | number of pockets in y direction | 10 |

STN RGB - 132 × 132 × 3 driver

PCF8833

19 DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾⁽³⁾ | DEFINITION |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

20 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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STN RGB - 132 × 132 × 3 driver**PCF8833**

Bare die — All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of Philips' delivery. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post packing tests performed on individual die or wafer. Philips Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

STN RGB - 132 × 132 × 3 driver

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NOTES

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Contact information

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Printed in The Netherlands

403512/01/pp112

Date of release: 2003 Feb 14

Document order number: 9397 750 10059

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