PCA8534A

Universal LCD driver for low multiplex rates

Rev. 02 — 1 June 2010 Product data sheet

1. General description

The PCA8534A is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 60 segments. It can be easily cascaded for larger LCD applications. The PCA8534A is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing, and by display memory switching (static and duplex drive modes).

AEC-Q100 compliant for automotive applications.

2. Features and benefits

- Single-chip LCD controller and driver
- Selectable backplane drive configurations: static, 2, 3, or 4 backplane multiplexing
- 60 segment outputs allowing to drive:
  - 30 7-segment alphanumeric characters
  - 16 14-segment alphanumeric characters
  - Any graphics of up to 240 elements
- Cascading supported for larger applications
- 60 × 4-bit display data storage RAM
- Wide LCD supply range: from 2.5 V for low threshold LCDs up to 6.5 V for guest-host LCDs and high threshold (automobile) twisted nematic LCDs
- Internal LCD bias generation with voltage follower buffers
- Selectable display bias configurations: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Wide logic power supply range: from 1.8 V to 5.5 V
- LCD and logic supplies may be separated
- Low power consumption
- 400 kHz I^2C-bus interface
- Compatible with any microprocessors or microcontrollers
- No external components
- Display memory bank switching in static and duplex drive modes
- Auto-incremented display data loading
- Versatile blinking modes
- Silicon gate CMOS process

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 16.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Name	Description	Delivery form	Version
PCA8534AH/Q900	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	tape and reel	SOT315-1

4. Marking

Table 2. Marking codes

Type number	Marking code
PCA8534AH/Q900	PCA8534A/Q900

5. Block diagram

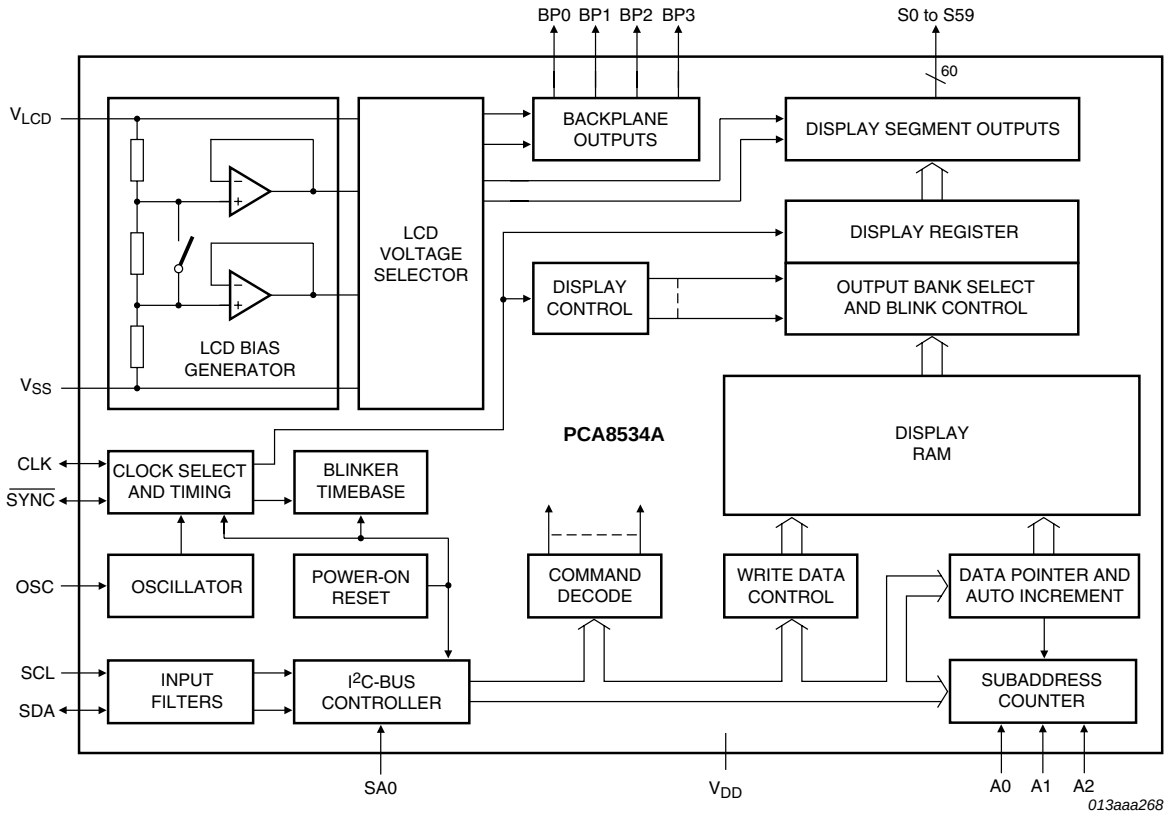
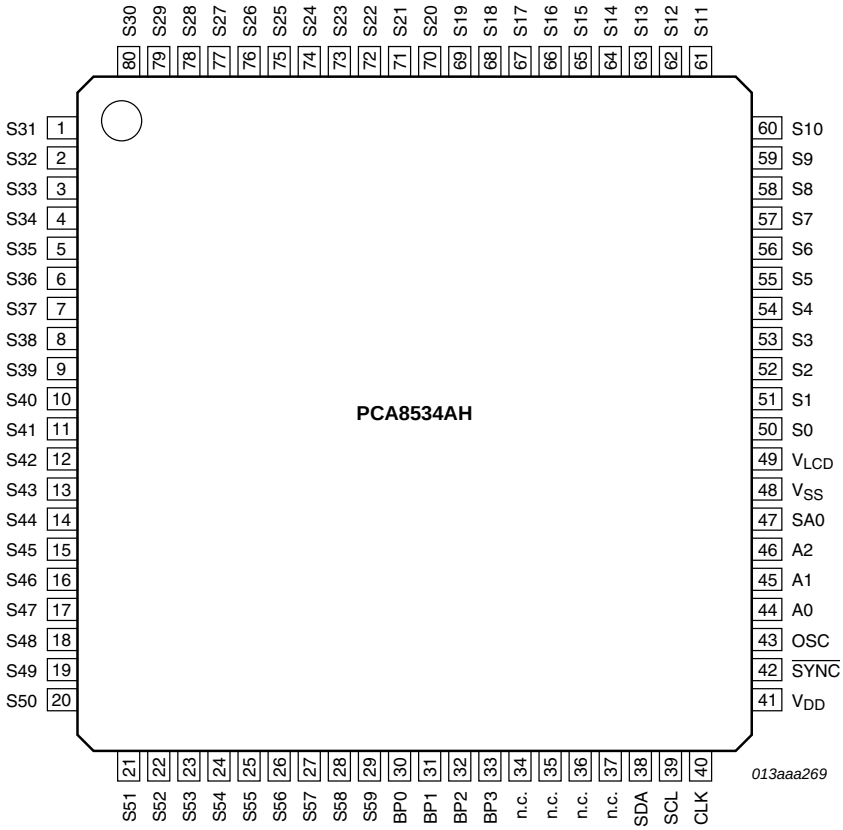


Fig 1. Block diagram of PCA8534A

6. Pinning information

6.1 Pinning



Top view. For mechanical details, see Figure 24.

Fig 2. Pin configuration for LQFP80 (PCA8534AH)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
S31 to S59	1 to 29	output	LCD segment output 31 to 59
BP0 to BP3	30 to 33	output	LCD backplane output 0 to 3
n.c.	34 to 37	-	not connected; do not connect and do not use as feed through
SDA	38	input/output	I^2C-bus serial data input and output
SCL	39	input	I^2C-bus serial clock input
CLK	40	input/output	external clock input and internal clock output
V_{DD}	41	supply	supply voltage
$\overline{SYNC}$	42	input/output	cascade synchronization input and output (active LOW)
OSC	43	input	enable input for internal oscillator
A0 to A2	44 to 46	input	subaddress counter input 0 to 2
SA0	47	input	I^2C-bus slave address input 0
V_{SS}	48	supply	ground supply voltage
V_{LCD}	49	input	LCD supply voltage
S0 to S30	50 to 80	output	LCD segment output 0 to 30

7. Functional description

The PCA8534A is a versatile peripheral device designed to interface any microprocessor or microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 60 segments.

The possible display configurations of the PCA8534A depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 4. All of these configurations can be implemented in the typical system shown in Figure 3.

Table 4. Selection of display configurations

Number of		7-segment alphanumeric		14-segment alphanumeric		Dot matrix
Backplanes	Elements	Digits	Indicator symbols	Characters	Indicator symbols	
4	240	30	30	16	16	240 (4 × 60)
3	180	22	26	12	12	180 (3 × 60)
2	120	15	15	8	8	120 (2 × 60)
1	60	7	11	4	4	60 (1 × 60)

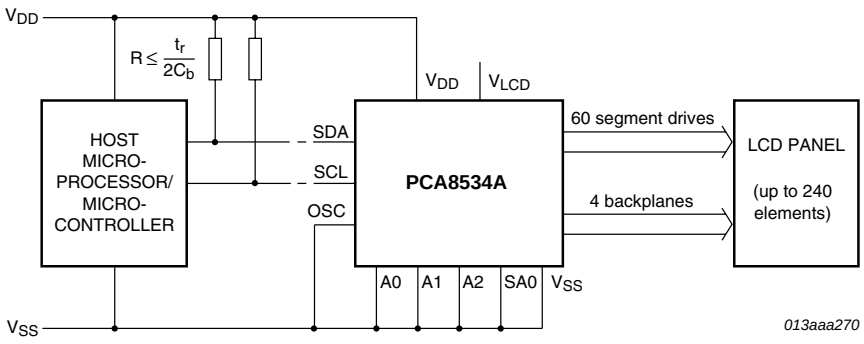


Fig 3. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I²C-bus communication channel with the PCA8534A.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel selected for the application.

7.1 Power-On Reset (POR)

At power-on the PCA8534A resets to a default starting condition:

- All backplane and segment outputs are set to V_{LCD}
- The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I²C-bus interface is initialized

- The data pointer and the subaddress counter are cleared (set to logic 0)
- The display is disabled

Remark: Do not transfer data on the I^2C-bus after a power-on for at least 1 ms to allow the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between pins V_{LCD} and V_{SS}. The center resistor is bypassed by switch if the $\frac{1}{2}$ bias voltage level for the 1:2 multiplex drive mode configuration is selected.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 5.

Table 5. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1:2 multiplex	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1:3 multiplex	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1:4 multiplex	4	4	$\frac{1}{3}$	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for $\frac{1}{2}$ bias

a = 2 for $\frac{1}{3}$ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (1)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

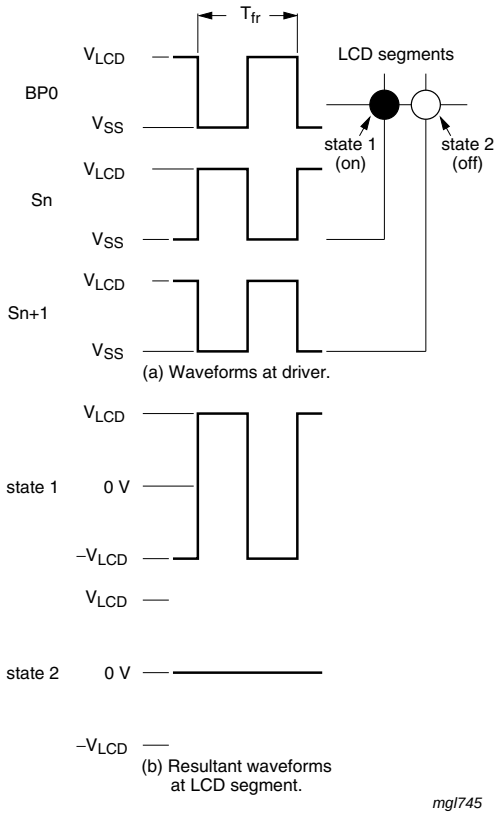
These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 4.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

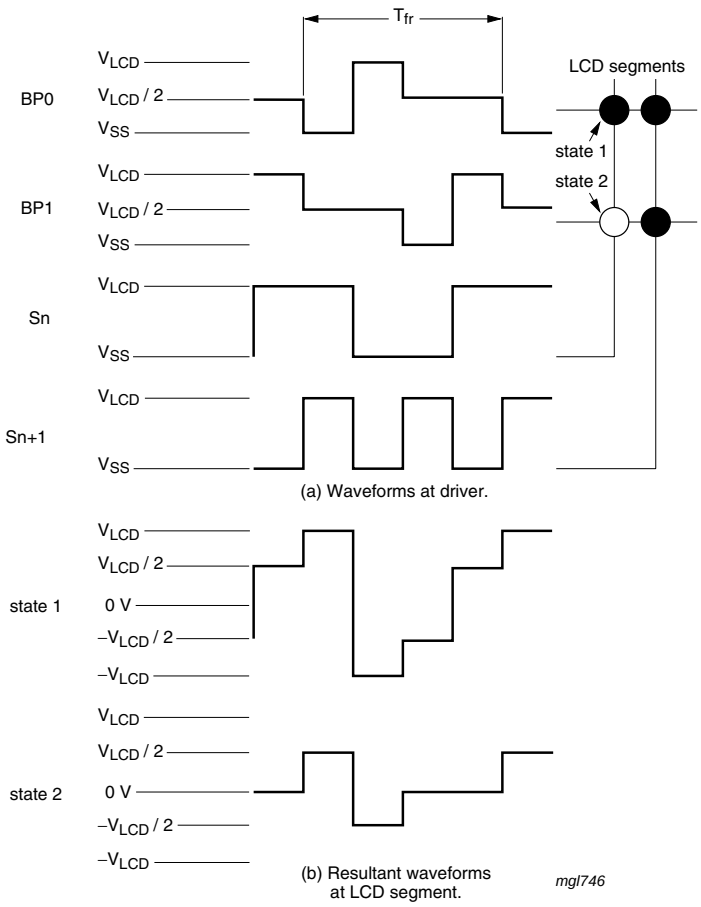
$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 4. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCA8534A allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 5 and Figure 6.



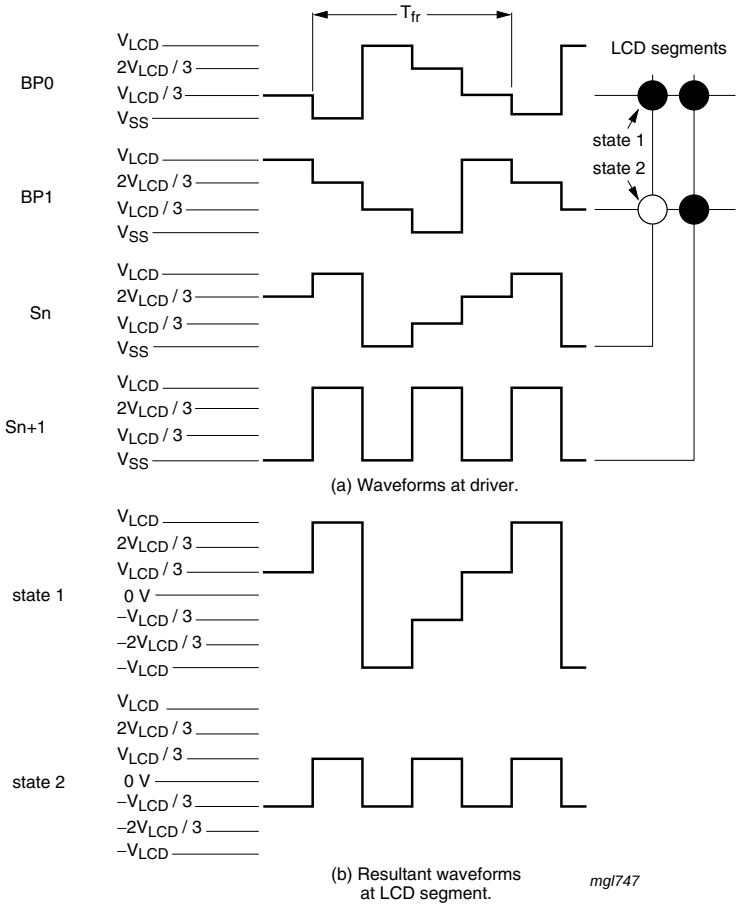
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

Fig 5. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

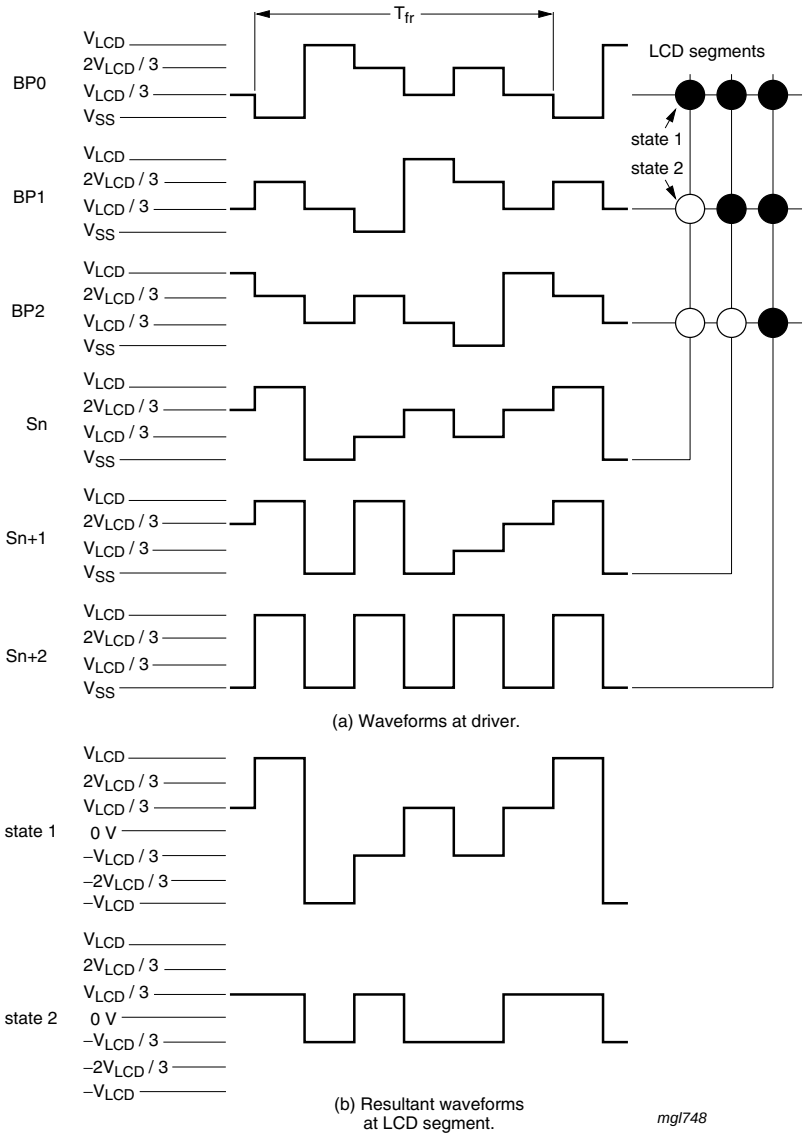
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 6. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 7.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

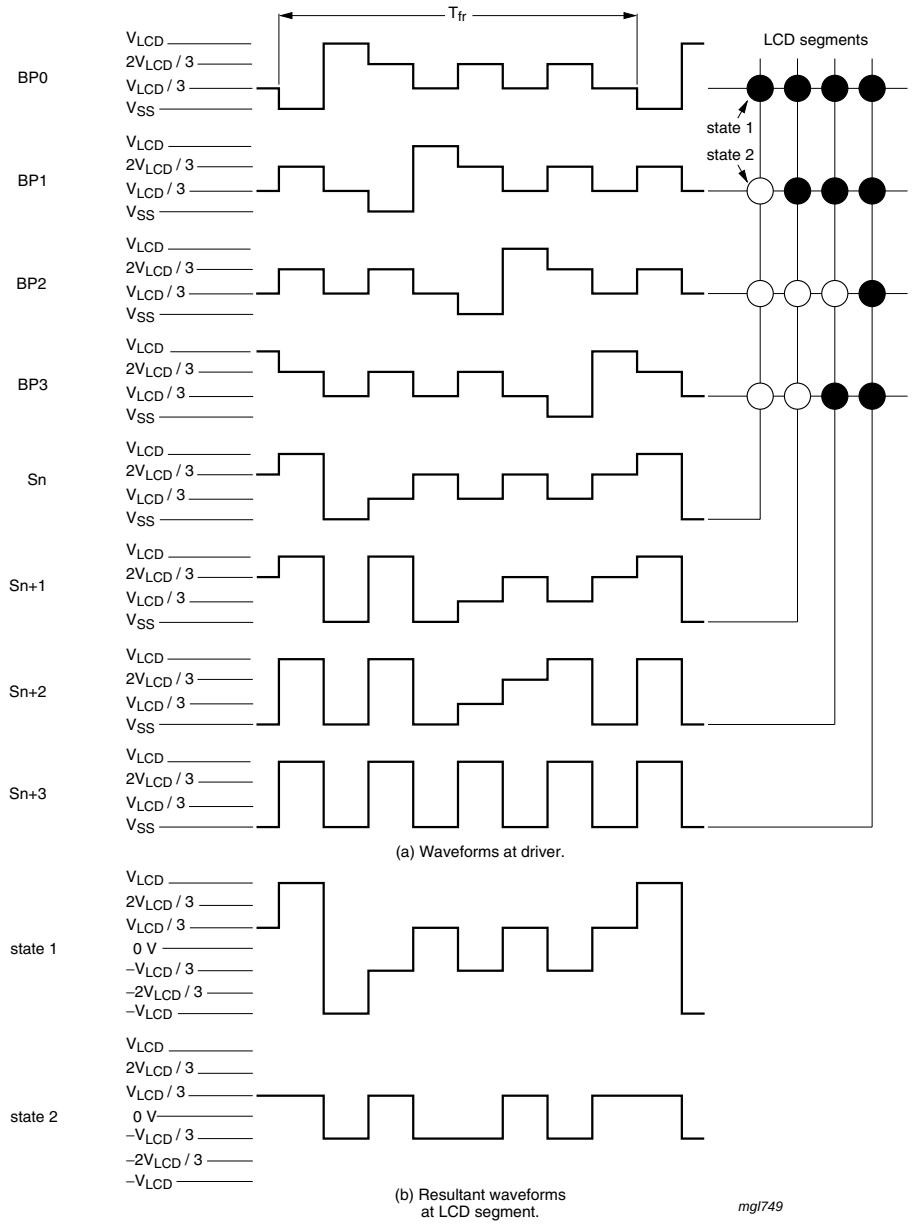
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 7. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 8.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 8. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

7.5 Oscillator

The internal logic and the LCD drive signals of the PCA8534A are timed by the frequency f_{clk}, which equals either the built-in oscillator frequency f_{osc} or the external clock frequency $f_{clk(ext)}$. The clock frequency f_{clk} determines the LCD frame frequency (f_{fr}).

7.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. In this case, the output from pin CLK is the clock signal for any cascaded PCA8534A in the system.

7.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}. The LCD frame signal frequency is determined by the clock frequency (f_{clk}).

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.6 Timing

The PCA8534A timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCA8534A in the system is maintained by the synchronization signal at pin $\overline{\text{SYNC}}$. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock.

Table 6. LCD frame frequencies

Frame frequency	Nominal frame frequency (Hz)
$f_{fr} = \frac{f_{clk}}{24}$	64

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

7.8 Segment outputs

The LCD drive section includes 60 segment outputs (S0 to S59) which should be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data resident in the display register. When less than 60 segment outputs are required, the unused segment outputs must be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated based on the selected LCD drive mode.

- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required the unused outputs can be left as an open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, BP1 and BP3 respectively carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

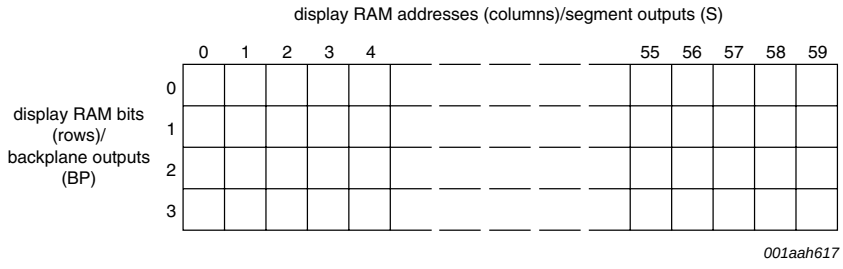
The display RAM is a static 60 × 4-bit RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

Logic 1 in the RAM bit map indicates the on-state of the corresponding LCD segment, logic 0 indicates the off-state.

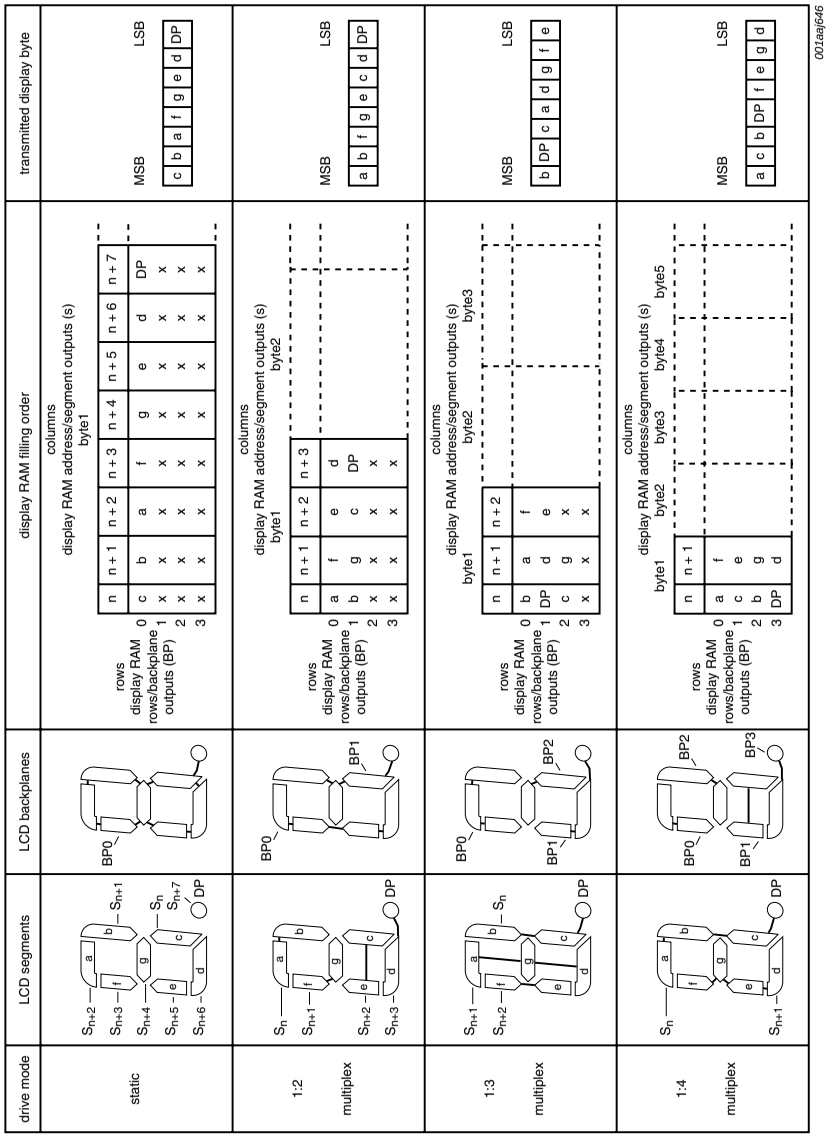
The display RAM bit map, Figure 9, shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 59 which correspond with the segment outputs S0 to S59. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.



The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs; and between the bits in a RAM row and the backplane outputs.

Fig 9. Display RAM bit map

When display data is transmitted to the PCA8534A the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triples or quadruples. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 10; the RAM filling organization depicted applies equally to other LCD types.



x = data bit unchanged.

Fig 10. Relationship between LCD layout, drive mode, display RAM storage order, and display data transmitted over the I²C-bus

The following applies to Figure 10:

- Static mode: the eight transmitted data bits are placed in row 0 to eight successive display RAM addresses.
- 1:2 multiplex mode: the eight transmitted data bits are placed in row 0 and 1 to four successive display RAM addresses.
- 1:3 multiplex mode: the eight transmitted data bits are placed in row 0, 1, and 2 to three successive addresses. However, bit 2 of the third address is left unchanged. This last bit can, if necessary, be controlled by an additional transfer to this address but avoid overriding adjacent data because full bytes are always transmitted.
- 1:4 multiplex mode: the eight transmitted data bits are placed in row 0, 1, 2, and 3 to two successive display RAM addresses.

7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 12). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 10.

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an I^2C-bus data access is terminated early then the state of the data pointer is unknown. The data pointer should be re-written prior to further RAM accesses.

7.12 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 13). If the content of the subaddress counter and the hardware subaddress do not match then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

In cascaded applications each PCA8534A in the cascade must be addressed separately. Initially, the first PCA8534A is selected by sending the device-select command matching the first device's hardware subaddress. Then the data pointer is set to the preferred display RAM address by sending the load-data-pointer command.

Once the display RAM of the first PCA8534A has been written, the second PCA8534A is selected by sending the device-select command again. This time however the command matches the second device's hardware subaddress. Next the load-data-pointer command is sent to select the preferred display RAM address of the second PCA8534A.

This last step is very important because during writing data to the first PCA8534A, the data pointer of the second PCA8534A is incremented. In addition, the hardware subaddress should not be changed whilst the device is being accessed on the I^2C-bus interface.

7.13 Output bank selector

The output bank selector (see Table 14), selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode: all RAM addresses of row 0 are selected, followed sequentially by the contents of row 1, row 2, and then row 3.
- In 1:3 multiplex mode: rows 0, 1, and 2 are selected sequentially.
- In 1:2 multiplex mode: rows 0 and 1 are selected.
- In the static mode: row 0 is selected.

The $\overline{\text{SYNC}}$ signal resets these sequences to the following starting points: row 3 for 1:4 multiplex, row 2 for 1:3 multiplex, row 1 for 1:2 multiplex and row 0 for static mode.

The PCA8534A includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In 1:2 multiplex drive mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This enables preparation of display information in an alternative bank and the ability to switch to it once it has been assembled.

7.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command. The input bank selector functions independently to the output bank selector.

7.15 Blinker

The display blinking capabilities of the PCA8534A are very versatile. The whole display can be blinked at frequencies set by the blink-select command (see Table 15). The blinking frequencies are fractions of the clock frequency. The ratios between the clock and blinking frequencies depend on the mode in which the device is operating (see Table 7).

Table 7. Blink frequencies

Assuming that f_{clk} = 1536 Hz.

Blink mode	Operating mode ratio	Blink frequency
Off	-	Blinking off
1	$f_{blink} = \frac{f_{clk}}{768}$	2 Hz
2	$f_{blink} = \frac{f_{clk}}{1536}$	1 Hz
3	$f_{blink} = \frac{f_{clk}}{3072}$	0.5 Hz

An additional feature is for the arbitrary selection of LCD segments to be blinked. This applies to the static and 1:2 multiplex drive modes and is implemented without any communication overheads. Using the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display needs to be blinked at a frequency other than the nominal blinking frequency, this can be done using the mode-set command to set and reset the display enable bit E at the required rate (see Table 11).

7.16 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 11).

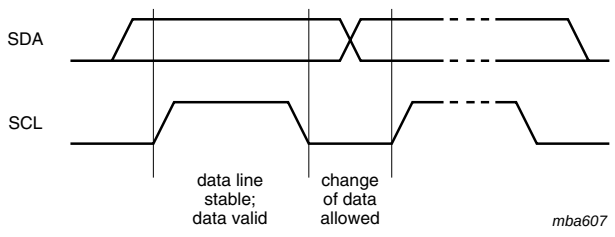


Fig 11. Bit transfer

7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 12).

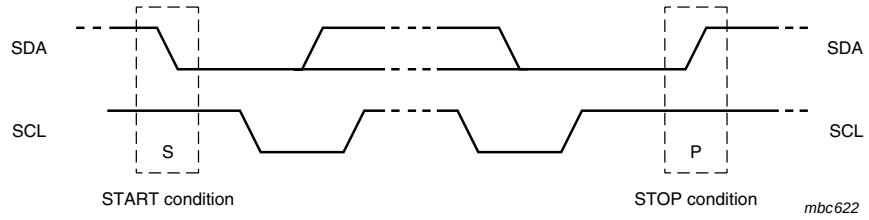


Fig 12. Definition of START and STOP conditions

7.16.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 13).

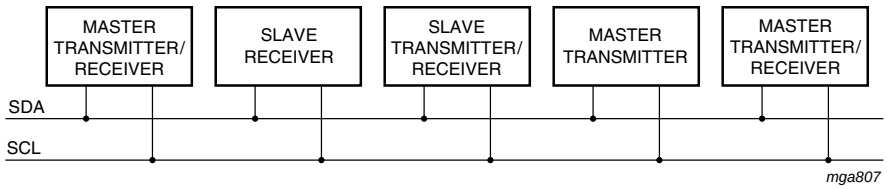


Fig 13. System configuration

7.16.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus is illustrated in Figure 14.

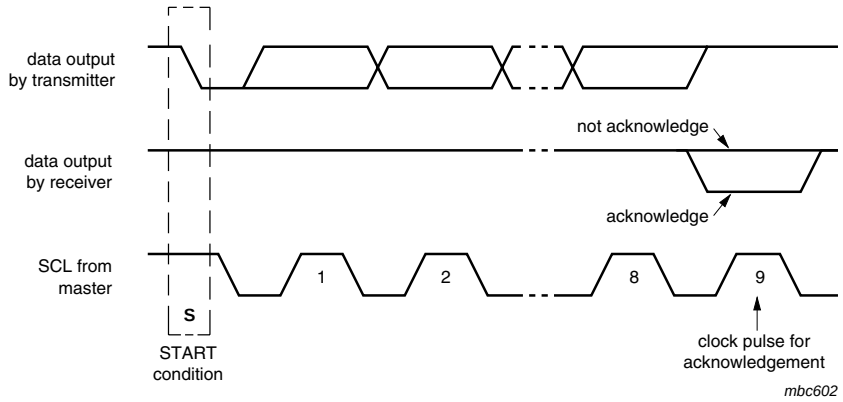


Fig 14. Acknowledgement of the I²C-bus

7.16.5 I²C-bus controller

The PCA8534A acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCA8534A are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1, and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1, and A2 are tied to V_{SS} or V_{DD} using a binary coding scheme, so that no two devices with a common I²C-bus slave address have the same hardware subaddress.

7.16.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.16.7 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are used to address the PCA8534A. The entire I²C-bus slave address byte is shown in Table 8.

Table 8. I²C slave address byte

Bit	Slave address							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	MSB							**LSB**
	0	1	1	1	0	0	SA0	R/$\overline{W}$

The PCA8534A is a write-only device and will not respond to a read access, therefore bit 0 should always be logic 0. Bit 1 of the slave address byte that a PCA8534A will respond to, is defined by the level tied to its SA0 input (V_{SS} for logic 0 and V_{DD} for logic 1).

Having two reserved slave addresses allows the following on the same I²C-bus:

- Up to 16 PCA8534A for very large LCD applications
- The use of two types of LCD multiplex drive

The I²C-bus protocol is shown in Figure 15. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of two possible PCA8534A slave addresses available. All PCA8534A whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCA8534A whose SA0 inputs are set to the alternative level.

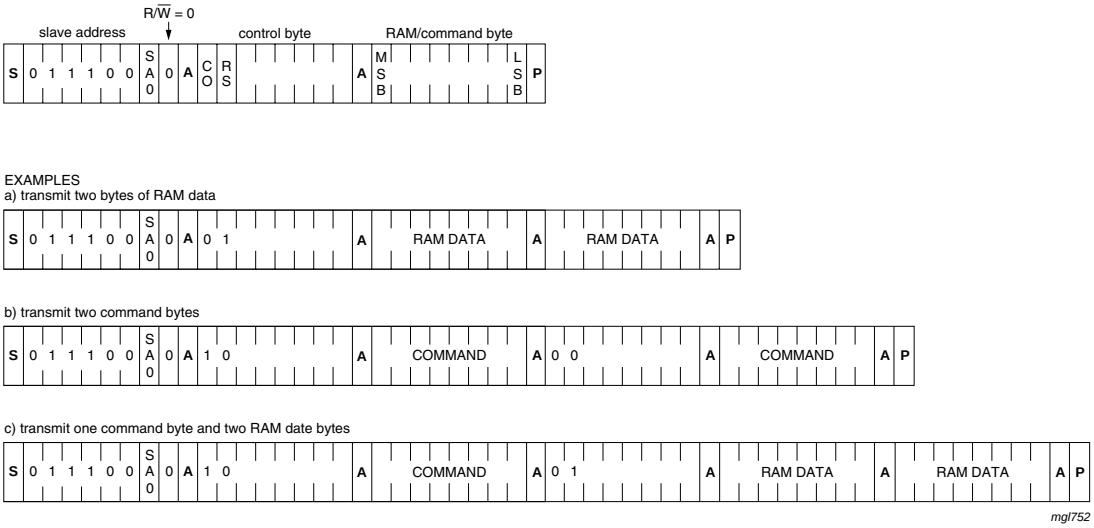


Fig 15. I²C-bus protocol

After an acknowledgement, one or more command bytes follow that define the status of each addressed PCA8534A.

The last command byte sent is identified by resetting its most significant bit, continuation bit CO (see Figure 16). The command bytes are also acknowledged by all addressed PCA8534A on the bus.

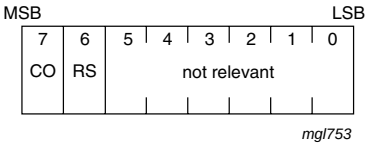


Fig 16. Control byte format

Table 9. Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6	RS		**register selection**
		0	command register
		1	data register
5 to 0	-		not relevant

The command bytes and control bytes are also acknowledged by all addressed PCA8534A connected to the bus.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated.

The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCA8534A. After the last display byte, the I^2C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART I^2C-bus access.

7.17 Command decoder

The command decoder identifies command bytes that arrive on the I^2C-bus. There are five commands:

Table 10. Definition of commands

Command	Operation Code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
Mode-set	1	1	0	0	E	B	M1	M0	Table 11
Load-data-pointer	0	P6	P5	P4	P3	P2	P1	P0	Table 12
Device-select	1	1	1	0	0	A2	A1	A0	Table 13
Bank-select	1	1	1	1	1	0	I	O	Table 14
Blink-select	1	1	1	1	0	A	BF1	BF0	Table 15

Table 11. Mode-set command bit description

Bit	Symbol	Value	Description
7 to 4	-	1100	fixed value
3	E		**display status** the possibility to disable the display allows implementation of blinking under external control
		0	disabled
		1	enable
2	B		**LCD bias configuration**
		0	$\frac{1}{3}$ bias
		1	$\frac{1}{2}$ bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; 1 backplane
		10	1:2 multiplex; 2 backplanes
		11	1:3 multiplex; 3 backplanes
		00	1:4 multiplex; 4 backplanes

Table 12. Load-data-pointer command bit description

Bit	Symbol	Value	Description
7	-	0	fixed value
6 to 0	P[6:0]	000 0000 to 011 1011	7-bit binary value of 0 to 59

Table 13. Device-select command bit description

Bit	Symbol	Value	Description
7 to 3	-	11100	fixed value
2 to 0	A[2:0]	000 to 111	3-bit binary value of 0 to 7

Table 14. Bank-select command bit description

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
7 to 2	-	111110	fixed value	
1	I		**input bank selection**: storage of arriving display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3
0	O		**output bank selection**: retrieval of LCD display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3

[1] The bank select command has no effect in 1:3 or 1:4 multiplex drive modes.

Table 15. Blink-select command bit description

Bit	Symbol	Value	Description
7 to 3	-	11110	fixed value
2	A		**blink mode selection**
		0	normal blinking[1]
		1	blinking by alternating display RAM banks
1 to 0	BF[1:0]		**blink frequency selection**[2]
		00	off
		01	1
		10	2
		11	3

[1] Only normal blinking can be selected in multiplexer 1:3 or 1:4 drive modes.

[2] The blink frequencies are shown in Table 7.

7.18 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCA8534A and coordinates their effects.
The controller also loads display data into the display RAM as required by the storage order.

8. Internal circuitry

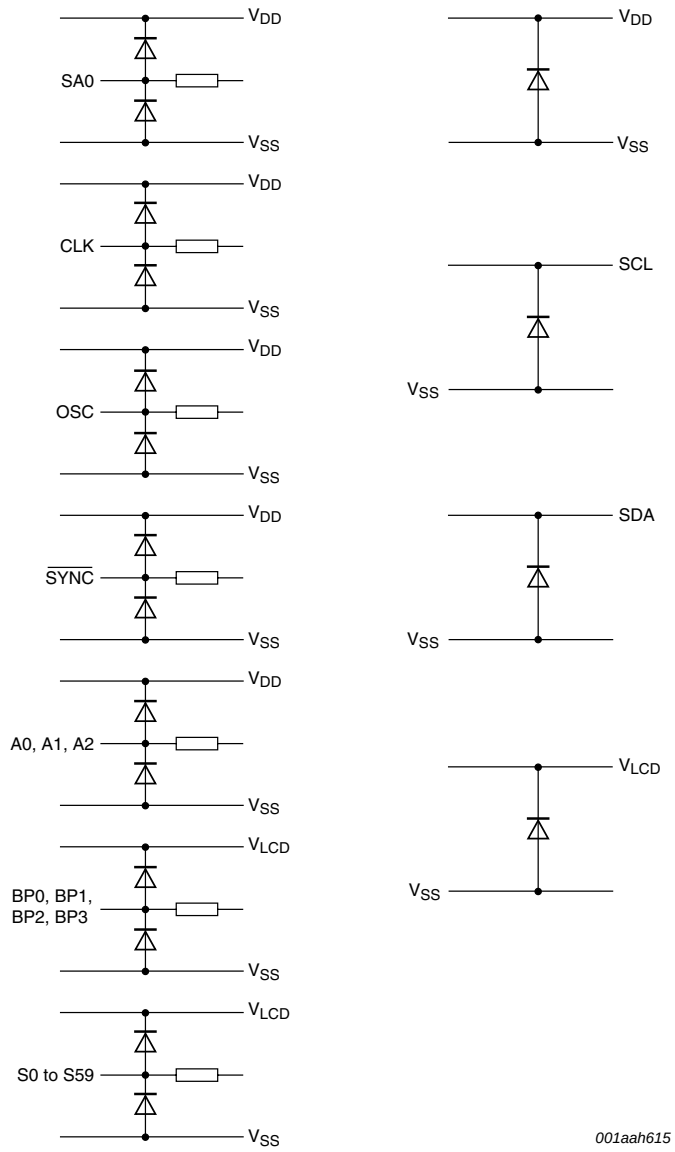


Fig 17. Device protection diagram

9. Limiting values

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 16. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+6.5	V
I_{DD}	supply current			−50	+50	mA
V_{LCD}	LCD supply voltage			−0.5	+7.5	V
$I_{DD(LCD)}$	LCD supply current			−50	+50	mA
I_{SS}	ground supply current			−50	+50	mA
V_I	input voltage		[1]	−0.5	+6.5	V
I_I	input current		[1]	−10	+10	mA
V_O	output voltage		[1]	−0.5	+6.5	V
			[2]	−0.5	+7.5	V
I_O	output current		[1][2]	−10	+10	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	±3000	V
		MM	[4]	-	±200	V
		CDM	[5]	-	±1000	V
I_{lu}	latch-up current		[6]	-	200	mA
T_{stg}	storage temperature		[7]	−65	+150	°C
T_{oper}	operating temperature			−40	+85	°C

[1] Pins SDA, SCL, CLK, $\overline{\text{SYNC}}$, SA0, OSC and A0 to A2.

[2] Pins S0 to S59 and BP0 to BP3.

[3] Pass level; Human Body Model (HBM), according to Ref. 5 “JESD22-A114”.

[4] Pass level; Machine Model (MM), according to Ref. 6 “JESD22-A115”.

[5] Pass level; Charged-Device Model (CDM), according to Ref. 7 “JESD22-C101”

[6] Pass level; latch-up testing according to Ref. 8 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[7] According to the NXP store and transport requirements (see Ref. 10 “NX3-00092”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

10. Static characteristics

Table 17. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage			2.5	-	6.5	V
I_{DD}	supply current	$f_{clk(ext)}$ = 1536 Hz	[1][2]	-	-	20	µA
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)}$ = 1536 Hz	[1][3]	-	-	60	µA
Logic							
V_I	input voltage			V_{SS} − 0.5		V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0		V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0		$0.7V_{DD}$	-	V_{DD}	V
V_{POR}	power-on reset voltage			1.0	1.3	1.6	V
I_{OL}	LOW-level output current	output sink current; $\overline{V_{OL}}$ = 0.4 V; V_{DD} = 5 V; on pins CLK and $\overline{SYNC}$		1	-	-	mA
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD} = 5 V; on pin CLK		1	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}; on pins SA0, A0 to A2 and CLK		−1	-	+1	µA
		$V_I = V_{DD}$; on pin OSC		−1	-	+1	µA
C_I	input capacitance		[4]	-	-	7	pF
I^2C-bus; pins SDA and SCL							
V_I	input voltage			V_{SS} − 0.5	-	5.5	V
V_{IL}	LOW-level input voltage	pin SCL		V_{SS}	-	$0.3V_{DD}$	V
		pin SDA		V_{SS}	-	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V; on pin SDA		3	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}		−1	-	+1	µA
C_i	input capacitance		[4]	-	-	7	pF
LCD outputs							
Output pins BP0, BP1, BP2 and BP3							
V_{BP}	voltage on pin BP	C_{bpl} = 35 nF		−100	-	+100	mV
R_{BP}	resistance on pin BP	V_{LCD} = 5 V	[5]	-	1.5	10	kΩ
Output pins S0 to S59							
V_S	voltage on pin S	C_{sgm} = 35 nF		−100	-	+100	mV
R_S	resistance on pin S	V_{LCD} = 5 V	[5]	-	6.0	13.5	kΩ

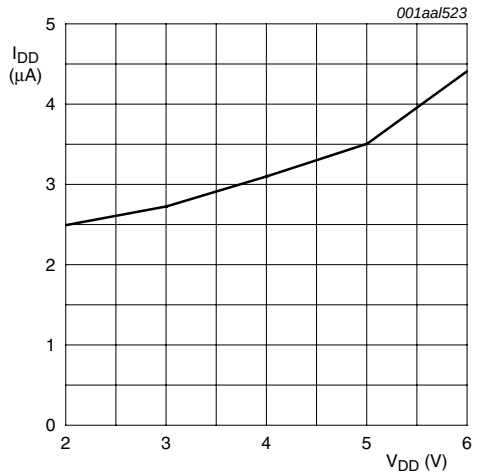
[1] LCD outputs are open circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I^2C-bus inactive.

[2] For typical values, see Figure 18.

[3] For typical values, see Figure 19.

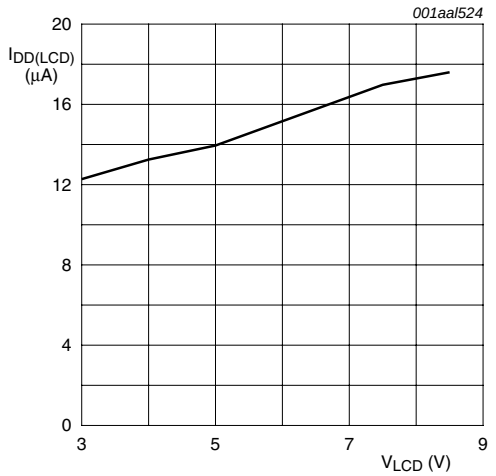
[4] Not tested, design specification only.

[5] Outputs measured individually and sequentially.



T_{amb} = 30 °C; 1:4 multiplex; V_{LCD} = 6.5 V; $f_{clk(ext)}$ = 1.536 kHz; all RAM written with logic 1; no display connected; I^2C-bus inactive.

Fig 18. Typical I_{DD} with respect to V_{DD}



T_{amb} = 30 °C; 1:4 multiplex; $f_{clk(ext)}$ = 1.536 kHz; all RAM written with logic 1; no display connected.

Fig 19. Typical $I_{DD(LCD)}$ with respect to V_{LCD}

11. Dynamic characteristics

Table 18. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
Internal: output pin CLK							
f_{osc}	oscillator frequency	V_{DD} = 5 V	[1]	960	1536	3046	Hz
External: input pin CLK							
$f_{clk(ext)}$	external clock frequency	V_{DD} = 5 V		797	1536	3046	Hz
$t_{clk(H)}$	HIGH-level clock time			130	-	-	µs
$t_{clk(L)}$	LOW-level clock time			130	-	-	µs
Synchronization: input pin $\overline{SYNC}$							
$t_{PD(SYNC\_N)}$	$\overline{SYNC}$ propagation delay			-	30	-	ns
t_{SYNC_NL}	$\overline{SYNC}$ LOW time			1	-	-	µs
Outputs: pins BP0 to BP3 and S0 to S59							
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V		-	-	30	µs
I^2C-bus: timing[2]							
Pin SCL							
f_{SCL}	SCL frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
Pin SDA							
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
Pins SCL and SDA							
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals			-	-	0.3	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{w(spike)}$	spike pulse width			-	-	50	ns

[1] Typical output (duty cycle δ = 50 %).

[2] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

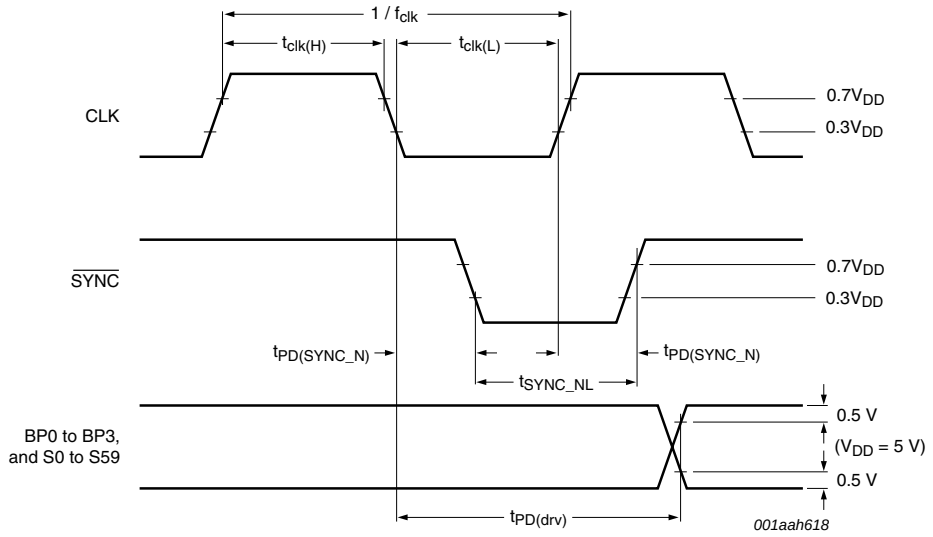


Fig 20. Driver timing waveforms

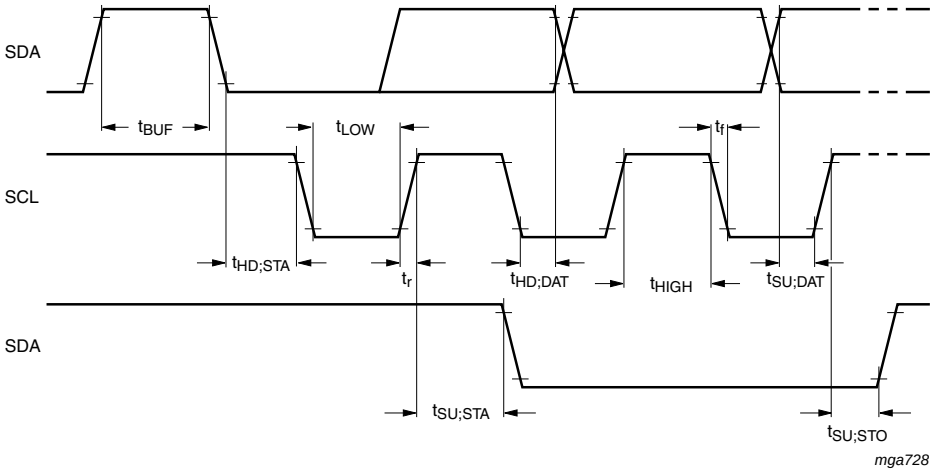


Fig 21. I^2C-bus timing waveforms

12. Application information

12.1 Cascaded operation

Large display configurations of up to 16 PCA8534A can be recognized on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1, and A2) and the programmable I^2C-bus slave address (SA0).

Table 19. Addressing cascaded PCA8534A

Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

If cascaded PCA8534A are synchronized, they can share the backplane signals from one of the devices in the cascade. This is cost-effective in large LCD applications because the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCA8534A in the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Figure 22).

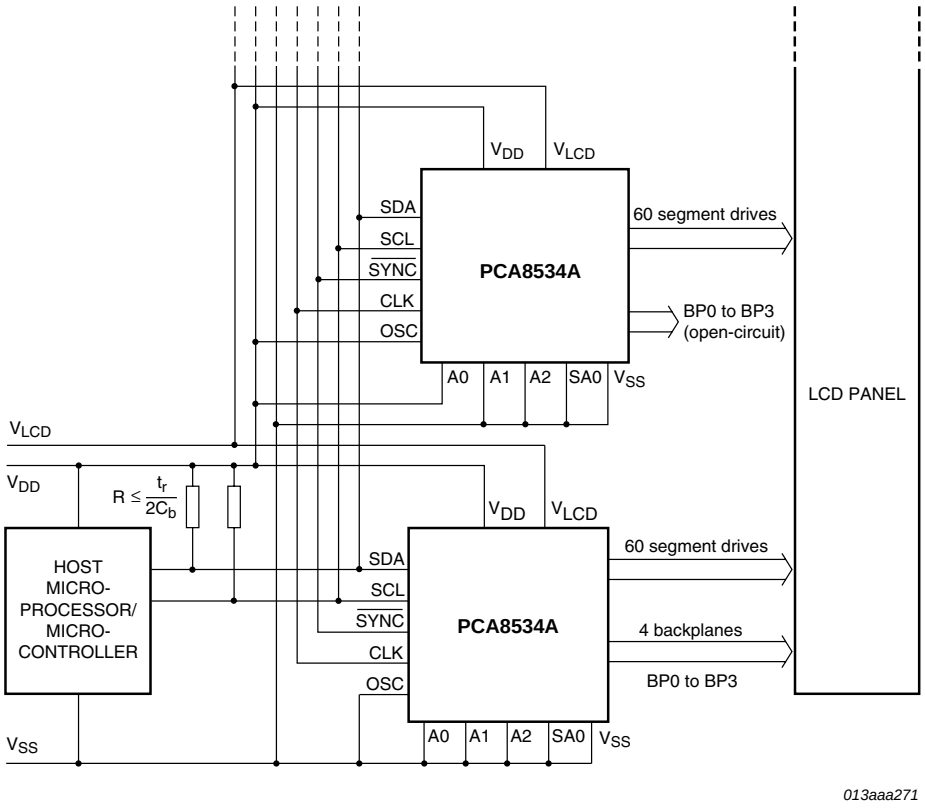


Fig 22. Cascaded PCA8534A configuration

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCA8534A. Synchronization is guaranteed after a power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments or by defining a multiplex mode when PCA8534A with different SA0 levels are cascaded).

$\overline{\text{SYNC}}$ is organized as an input/output pin. The output selection is realized as an open-drain driver with an internal pull-up resistor. A PCA8534A asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first PCA8534A to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCA8534A are shown in Figure 23.

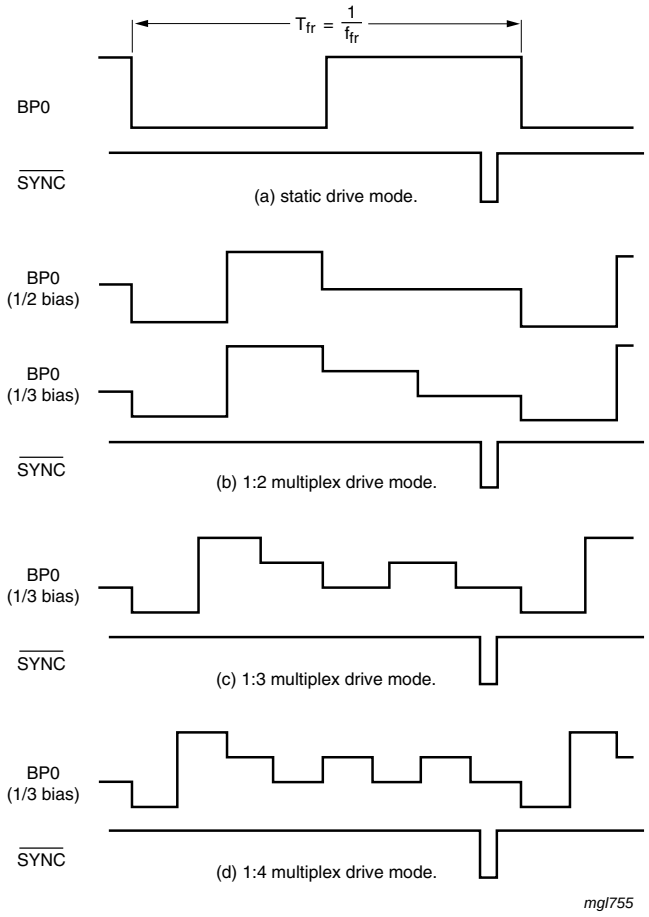


Fig 23. Synchronization of the cascade for various PCA8534A drive modes

The contact resistance between the $\overline{\text{SYNC}}$ pins of cascaded devices must be controlled. If the resistance is too high, the device will not be able to synchronize properly. Table 20 shows the maximum contact resistance values.

Table 20. $\overline{\text{SYNC}}$ contact resistance

Number of devices	Maximum contact resistance
2	6000 Ω
3 to 5	2200 Ω
6 to 10	1200 Ω
11 to 16	700 Ω

The PCA8534A can always be cascaded with other devices of the same type or conditionally with other devices of the same family. This allows optimal drive selection for a given number of pixels to display. Figure 20 and Figure 23 show the timing of the synchronization signals.

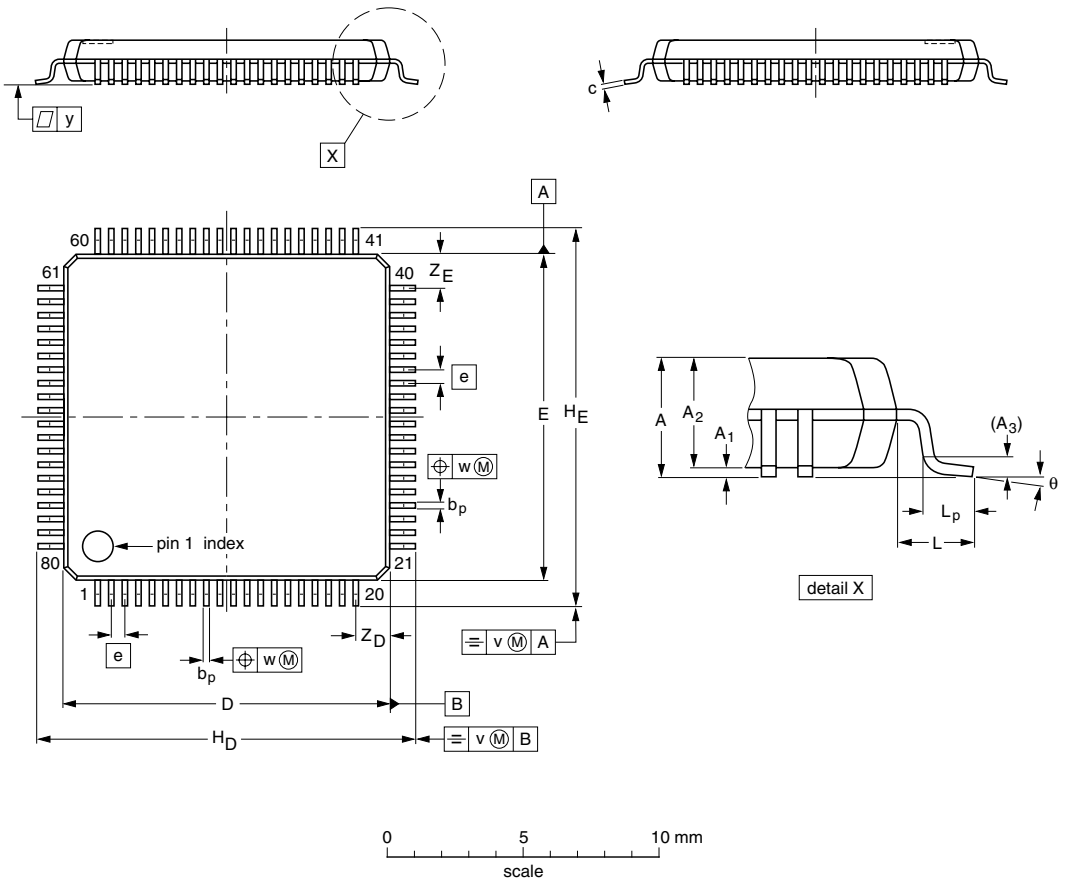
In a cascaded configuration only one PCA8534A master must be used as clock source. All other PCA8534A in the cascade must be configured as slave such that they receive the clock from the master.

If an external clock source is used, all PCA8534A in the cascade must be configured such as to receive the clock from that external source (pin OSC connected to V_{DD}). Thereby it must be ensured that the clock tree is designed such that on all PCA8534A the clock propagation delay from the clock source to all PCA8534A in the cascade is as equal as possible since otherwise synchronization artefacts may occur.

In mixed cascading configurations, care has to be taken that the specifications of the individual cascaded devices are met at all times.

13. Package outline

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT315-1	136E15	MS-026				~~00-01-19~~ 03-02-25

Fig 24. Package outline SOT315-1 (LQFP80)

14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 21 and 22

Table 21. SnPb eutectic process (from J-STD-020C)

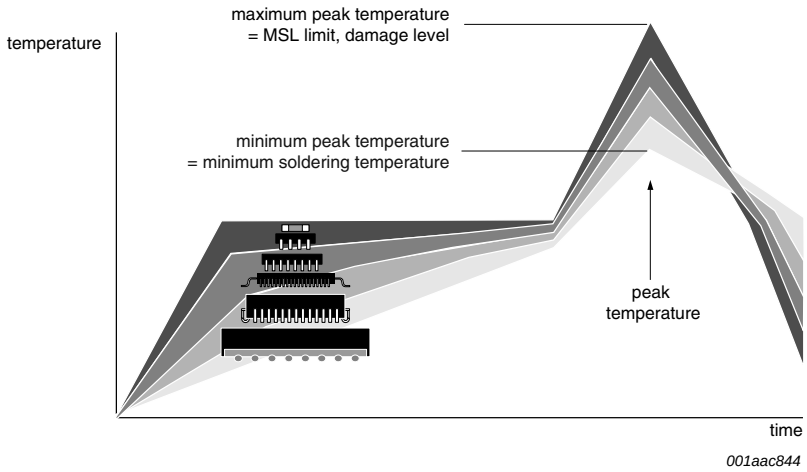
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 22. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.



MSL: Moisture Sensitivity Level

Fig 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Abbreviations

Table 23. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
CMOS	Complementary Metal-Oxide Semiconductor
CDM	Charged Device Model
DC	Direct Current
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
POR	Power-On Reset
RAM	Random Access Memory
RC	Resistance and Capacitance
RMS	Root Mean Square
SCL	Serial Clock Line
SDA	Serial DAta line
SMD	Surface-Mount Device

17. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[3] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[4] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[5] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[6] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[7] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **NX3-00092 —** NXP store and transport requirements

[11] **SNV-FA-01-02 —** Marking Formats Integrated Circuits

[12] **UM10204 —** I^2C-bus specification and user manual

18. Revision history

Table 24. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA8534A_2	20100601	Product data sheet	-	PCA8534A_1
Modifications:	• Corrected marking code in Table 2			
PCA8534A_1	20100415	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contents

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