

DATA SHEET

74LVC157A Quad 2-input multiplexer

Product specification
Supersedes data of 2003 Jun 17

2003 Dec 02

Quad 2-input multiplexer

74LVC157A

FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74LVC157A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC157A is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input (\bar{E}) is active LOW. When pin \bar{E} is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all the other input conditions. Moving the data from two groups of registers to four common output buses is a common use of the 74LVC157A. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any 4 of the 16 different functions of two variables with one variable common.

The 74LVC157A is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to pin S.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 2.5$ ns.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|-------------------|---|---|-------------------|----------------|
| t_{PHL}/t_{PLH} | propagation delay nI0, nI1 to nY \bar{E} to nY S to nY | $C_L = 50$ pF; $V_{CC} = 3.3$ V $C_L = 50$ pF; $V_{CC} = 3.3$ V $C_L = 50$ pF; $V_{CC} = 3.3$ V | 2.6 2.8 2.6 | ns ns ns |
| C_I | input capacitance | | 5.0 | pF |
| C_{PD} | power dissipation capacitance per gate | $V_{CC} = 3.3$ V; notes 1 and 2 | 15 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in Volts;
 N = total load switching outputs;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_I = \text{GND}$ to V_{CC} .

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FUNCTION TABLE

See note 1.

| INPUT | | | | OUTPUT |
|-----------|---|-----|-----|--------|
| \bar{E} | S | nI0 | nI1 | nY |
| H | X | X | X | L |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

Note

1. H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

ORDERING INFORMATION

| TYPE NUMBER | TEMPERATURE RANGE | PACKAGE | | | |
|-------------|-------------------|---------|----------|----------|----------|
| | | PINS | PACKAGE | MATERIAL | CODE |
| 74LVC157AD | -40 to +125 °C | 16 | SO16 | plastic | SOT109-1 |
| 74LVC157ADB | -40 to +125 °C | 16 | SSOP16 | plastic | SOT338-1 |
| 74LVC157APW | -40 to +125 °C | 16 | TSSOP16 | plastic | SOT403-1 |
| 74LVC157ABQ | -40 to +125 °C | 16 | DHVQFN16 | plastic | SOT763-1 |

PINNING

| PIN | SYMBOL | DESCRIPTION |
|-----|-----------------|---------------------------|
| 1 | S | common data select input |
| 2 | 1I0 | data input from source 0 |
| 3 | 1I1 | data input from source 1 |
| 4 | 1Y | multiplexer output |
| 5 | 2I0 | data input from source 0 |
| 6 | 2I1 | data input from source 1 |
| 7 | 2Y | multiplexer output |
| 8 | GND | ground (0 V) |
| 9 | 3Y | multiplexer output |
| 10 | 3I1 | data input from source 1 |
| 11 | 3I0 | data input from source 0 |
| 12 | 4Y | multiplexer output |
| 13 | 4I1 | data input from source 1 |
| 14 | 4I0 | data input from source 0 |
| 15 | \bar{E} | enable input (active LOW) |
| 16 | V _{CC} | supply voltage |

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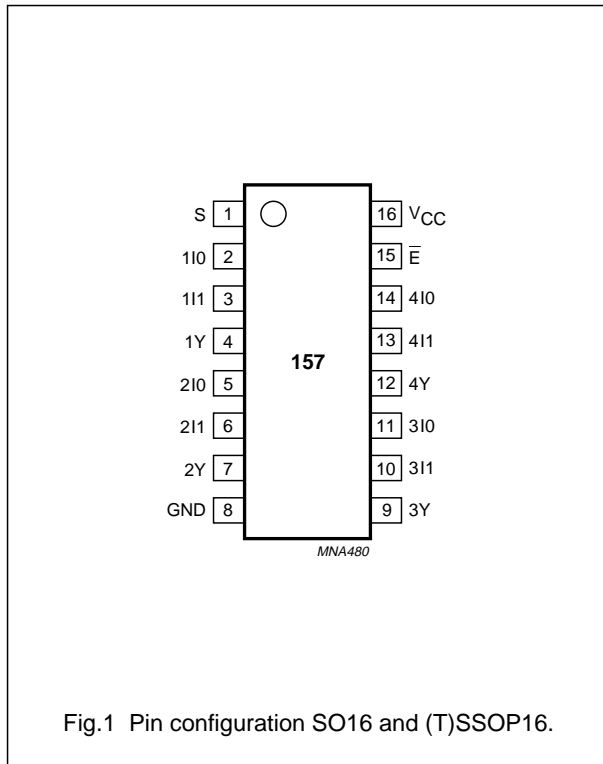
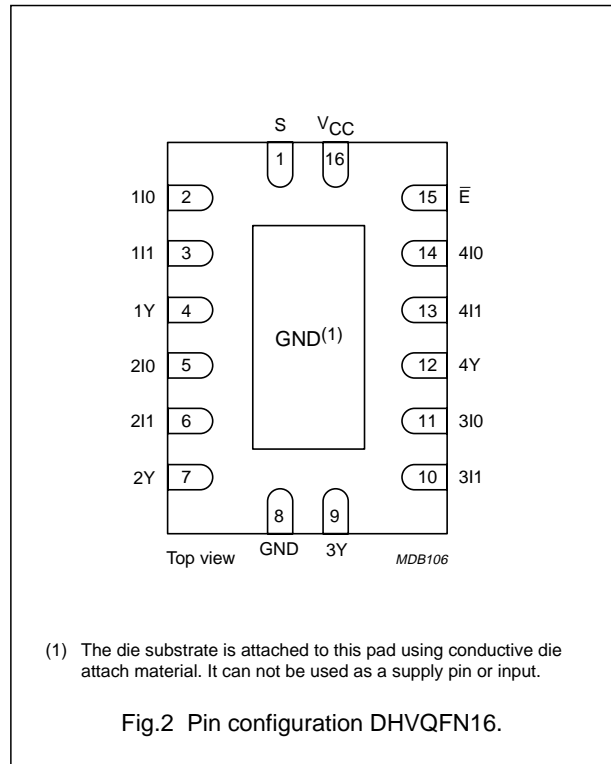


Fig.1 Pin configuration SO16 and (T)SSOP16.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN16.

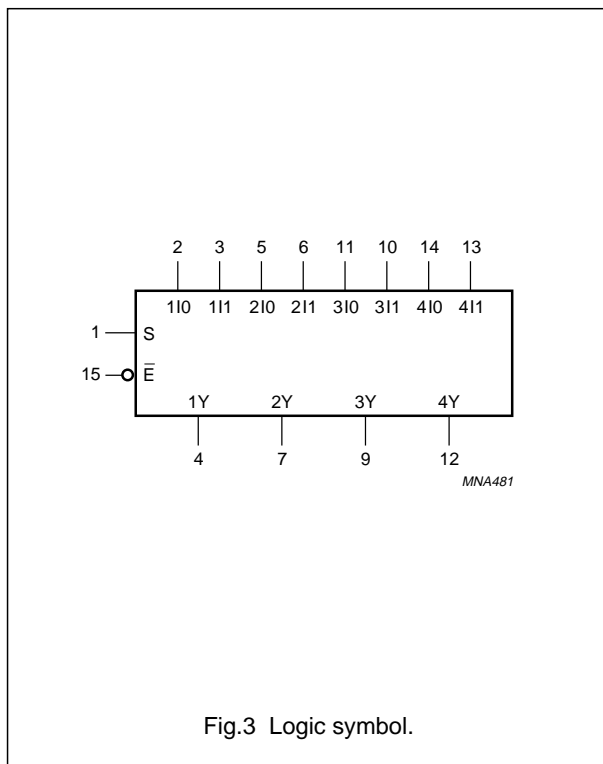


Fig.3 Logic symbol.

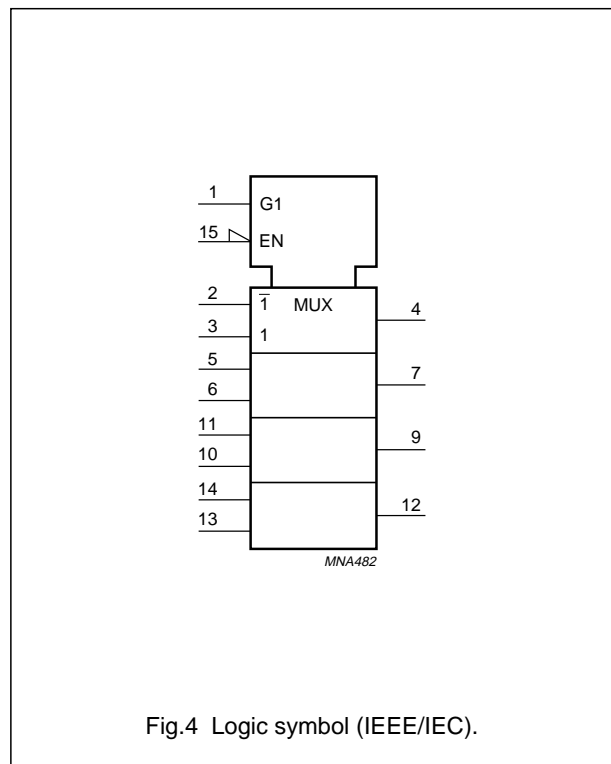
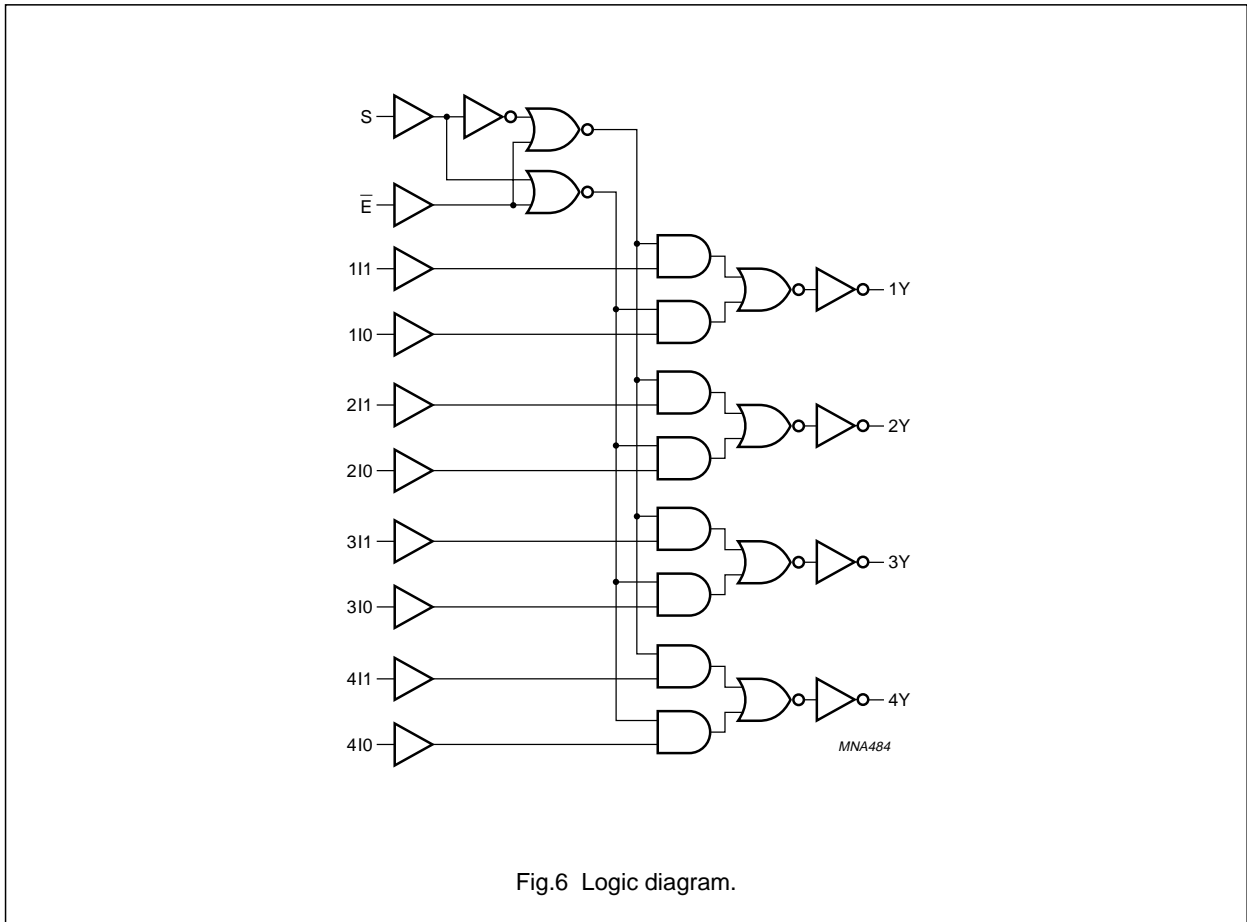
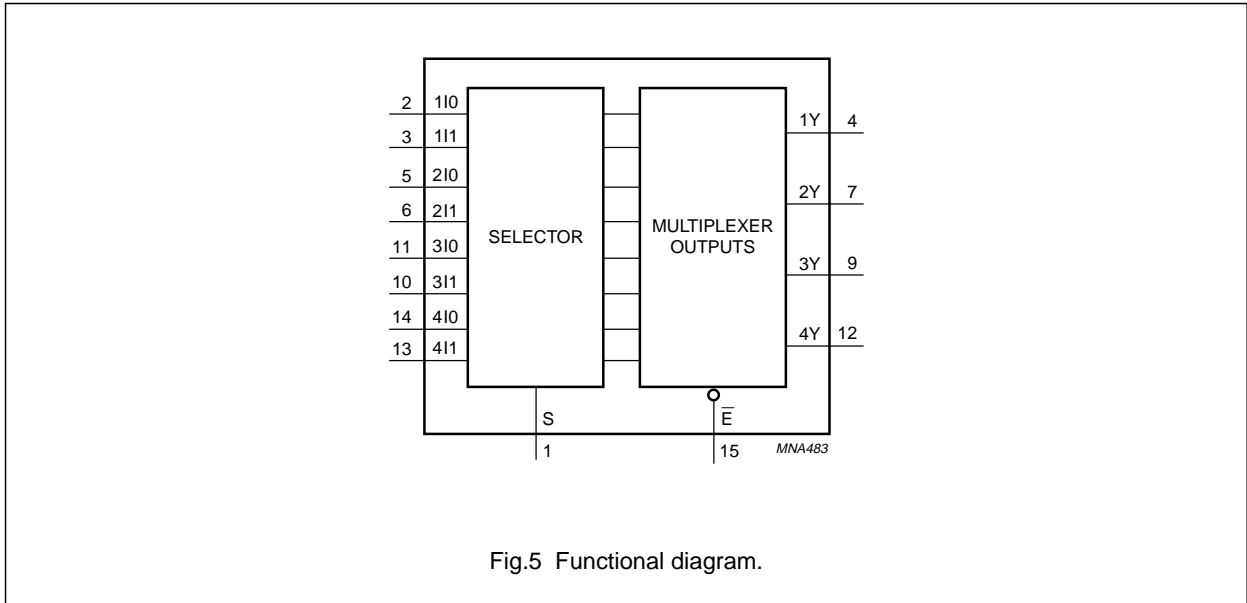


Fig.4 Logic symbol (IEEE/IEC).

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------|-------------------------------|-------------------------------|------|----------|------|
| V_{CC} | supply voltage | for maximum speed performance | 2.7 | 3.6 | V |
| | | for low voltage applications | 1.2 | 3.6 | V |
| V_I | input voltage | | 0 | 5.5 | V |
| V_O | output voltage | | 0 | V_{CC} | V |
| T_{amb} | operating ambient temperature | | -40 | +125 | °C |
| t_r, t_f | input rise and fall times | $V_{CC} = 1.2$ to 2.7 V | 0 | 20 | ns/V |
| | | $V_{CC} = 2.7$ to 3.6 V | 0 | 10 | ns/V |

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-------------------|-------------------------------|--------------------------------------|------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | input diode current | $V_I < 0$ | - | -50 | mA |
| V_I | input voltage | note 1 | -0.5 | +6.5 | V |
| I_{OK} | output diode current | $V_O > V_{CC}$ or $V_O < 0$ | - | ±50 | mA |
| V_O | output voltage | note 1 | -0.5 | $V_{CC} + 0.5$ | V |
| I_O | output source or sink current | $V_O = 0$ to V_{CC} | - | ±50 | mA |
| I_{CC}, I_{GND} | V_{CC} or GND current | | - | ±100 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_D | power dissipation | $T_{amb} = -40$ to $+125$ °C; note 2 | - | 500 | mW |

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO16 packages: above 70 °C the value of P_D derates linearly with 8 mW/K.
For (T)SSOP16 packages: above 60 °C the value of P_D derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P_D derates linearly with 4.5 mW/K.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. ⁽¹⁾ | MAX. | UNIT |
|--|---|---|---------------------|-----------------------|---------------------|------|------|
| | | OTHER | V _{CC} (V) | | | | |
| T_{amb} = -40 to +85 °C | | | | | | | |
| V _{IH} | HIGH-level input voltage | | 1.2 | V _{CC} | – | – | V |
| | | | 2.7 to 3.6 | 2.0 | – | – | V |
| V _{IL} | LOW-level input voltage | | 1.2 | – | – | GND | V |
| | | | 2.7 to 3.6 | – | – | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} I _O = -100 µA | 2.7 to 3.6 | V _{CC} - 0.2 | – | – | V |
| | | I _O = -12 mA | 2.7 | V _{CC} - 0.5 | – | – | V |
| | | I _O = -18 mA | 3.0 | V _{CC} - 0.6 | – | – | V |
| | | I _O = -24 mA | 3.0 | V _{CC} - 0.8 | – | – | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} I _O = 100 µA | 2.7 to 3.6 | – | – | 0.2 | V |
| | | I _O = 12 mA | 2.7 | – | – | 0.4 | V |
| | | I _O = 24 mA | 3.0 | – | – | 0.55 | V |
| I _{LI} | input leakage current | V _I = 5.5 V or GND | 3.6 | – | ±0.1 | ±5 | µA |
| I _{CC} | quiescent supply current | V _I = V _{CC} or GND; I _O = 0 | 3.6 | – | 0.1 | 10 | µA |
| ΔI _{CC} | additional quiescent supply current per input pin | V _I = V _{CC} - 0.6 V; I _O = 0 | 2.7 to 3.6 | – | 5 | 500 | µA |

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| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. ⁽¹⁾ | MAX. | UNIT |
|---|---|---|---------------------|------------------------|---------------------|------|------|
| | | OTHER | V _{CC} (V) | | | | |
| T_{amb} = -40 to +125 °C | | | | | | | |
| V _{IH} | HIGH-level input voltage | | 1.2 | V _{CC} | – | – | V |
| | | | 2.7 to 3.6 | 2.0 | – | – | V |
| V _{IL} | LOW-level input voltage | | 1.2 | – | – | GND | V |
| | | | 2.7 to 3.6 | – | – | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | 2.7 to 3.6 | V _{CC} – 0.3 | – | – | V |
| | | I _O = –100 μA | | V _{CC} – 0.65 | – | – | V |
| | | I _O = –12 mA | | V _{CC} – 0.75 | – | – | V |
| | | I _O = –18 mA | | V _{CC} – 1 | – | – | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | 2.7 to 3.6 | – | – | 0.3 | V |
| | | I _O = 100 μA | | – | – | 0.6 | V |
| | | I _O = 12 mA | | – | – | 0.8 | V |
| | | I _O = 24 mA | | – | – | – | V |
| I _{LI} | input leakage current | V _I = 5.5 V or GND | 3.6 | – | – | ±20 | μA |
| I _{CC} | quiescent supply current | V _I = V _{CC} or GND; I _O = 0 | 3.6 | – | – | 40 | μA |
| ΔI _{CC} | additional quiescent supply current per input pin | V _I = V _{CC} – 0.6 V; I _O = 0 | 2.7 to 3.6 | – | – | 5000 | μA |

Note

1. All typical values are measured at T_{amb} = 25 °C.

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AC CHARACTERISTICSGND = 0 V; $t_r = t_f \leq 2.5$ ns.

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|--|-----------------------------------|------------------|---------------------|------|--------------------|------|------|
| | | WAVEFORMS | V _{CC} (V) | | | | |
| T_{amb} = -40 to +85 °C; note 1 | | | | | | | |
| t _{PHL} /t _{PLH} | propagation delay nI0, nI1 to nY | see Figs 8 and 9 | 1.2 | – | 16 | – | ns |
| | | | 2.7 | 1.0 | 3.0 | 5.9 | ns |
| | | | 3.0 to 3.6 | 1.0 | 2.6 ⁽²⁾ | 5.2 | ns |
| | propagation delay \bar{E} to nY | see Figs 7 and 9 | 1.2 | – | 17 | – | ns |
| | | | 2.7 | 1.0 | 3.4 | 7.8 | ns |
| | | | 3.0 to 3.6 | 1.0 | 2.8 ⁽²⁾ | 6.5 | ns |
| | propagation delay S to nY | see Figs 8 and 9 | 1.2 | – | 16 | – | ns |
| | | | 2.7 | 1.0 | 3.0 | 7.3 | ns |
| | | | 3.0 to 3.6 | 1.0 | 2.6 ⁽²⁾ | 6.3 | ns |
| t _{sk(0)} | skew | note 3 | 3.0 to 3.6 | – | – | 1.0 | ns |
| T_{amb} = -40 to +125 °C | | | | | | | |
| t _{PHL} /t _{PLH} | propagation delay nI0, nI1 to nY | see Figs 8 and 9 | 1.2 | – | – | – | ns |
| | | | 2.7 | 1.0 | – | 7.5 | ns |
| | | | 3.0 to 3.6 | 1.0 | – | 6.5 | ns |
| | propagation delay \bar{E} to nY | see Figs 7 and 9 | 1.2 | – | – | – | ns |
| | | | 2.7 | 1.0 | – | 10.0 | ns |
| | | | 3.0 to 3.6 | 1.0 | – | 8.5 | ns |
| | propagation delay S to nY | see Figs 8 and 9 | 1.2 | – | – | – | ns |
| | | | 2.7 | 1.0 | – | 9.5 | ns |
| | | | 3.0 to 3.6 | 1.0 | – | 8.0 | ns |
| t _{sk(0)} | skew | note 3 | 3.0 to 3.6 | – | – | 1.5 | ns |

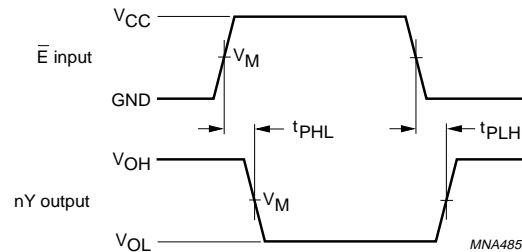
Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. This typical value is measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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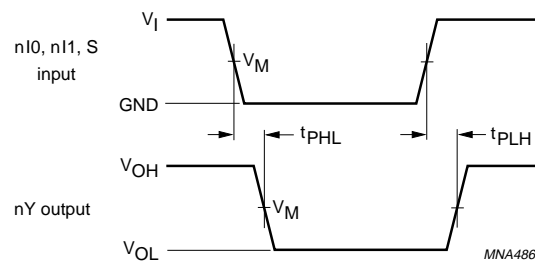
AC WAVEFORMS



| V_{CC} | V_M | INPUT | |
|--------------|---------------------|----------|---------------|
| | | V_I | $t_r = t_f$ |
| 1.2 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.5 ns |
| 2.7 V | 1.5 V | 2.7 V | ≤ 2.5 ns |
| 3.0 to 3.6 V | 1.5 V | 2.7 V | ≤ 2.5 ns |

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 Enable input (\bar{E}) to output (nY) propagation delays.



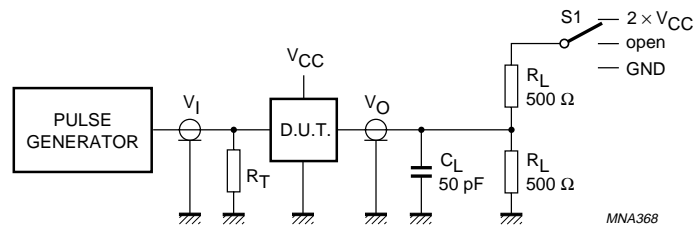
| V_{CC} | V_M | INPUT | |
|--------------|---------------------|----------|---------------|
| | | V_I | $t_r = t_f$ |
| 1.2 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.5 ns |
| 2.7 V | 1.5 V | 2.7 V | ≤ 2.5 ns |
| 3.0 to 3.6 V | 1.5 V | 2.7 V | ≤ 2.5 ns |

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.8 Data inputs (nI0, nI1) and common data select input (S) to output (nY) propagation delays.

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| V_{CC} | V_I | C_L | R_L | V_{EXT} | | |
|--------------|----------|-------|-----------------------------|-------------------|-------------------|-------------------|
| | | | | t_{PLH}/t_{PHL} | t_{PZH}/t_{PHZ} | t_{PZL}/t_{PLZ} |
| 1.2 V | V_{CC} | 50 pF | 500 Ω ⁽¹⁾ | open | GND | $2 \times V_{CC}$ |
| 2.7 V | 2.7 V | 50 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |
| 3.0 to 3.6 V | 2.7 V | 50 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |

Note

- The circuit performs better when $R_L = 1000 \Omega$.

Definitions for test circuits:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.9 Load circuitry for switching times.

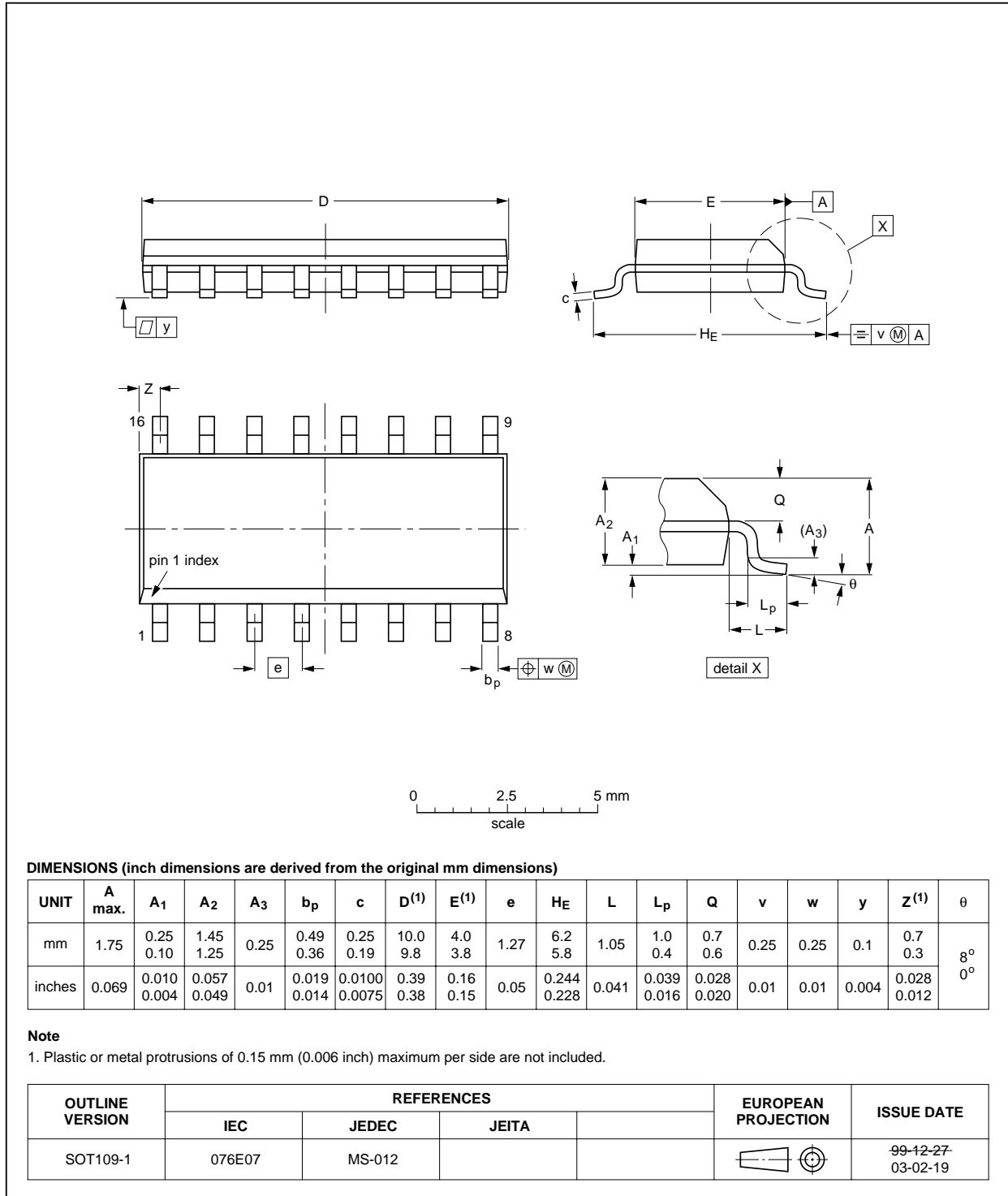
Quad 2-input multiplexer

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PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

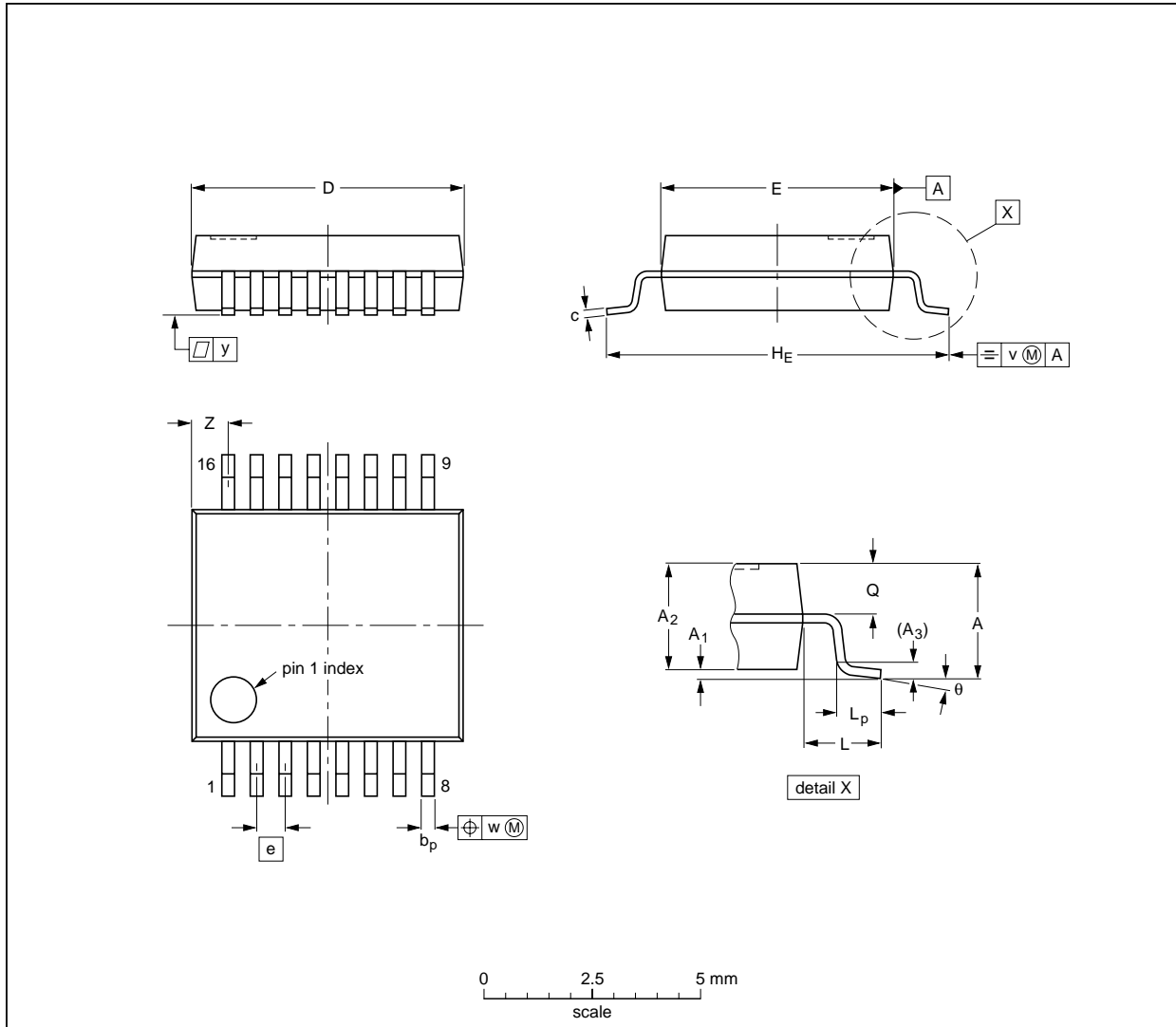


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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm | 2 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 6.4 6.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 1.00 0.55 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

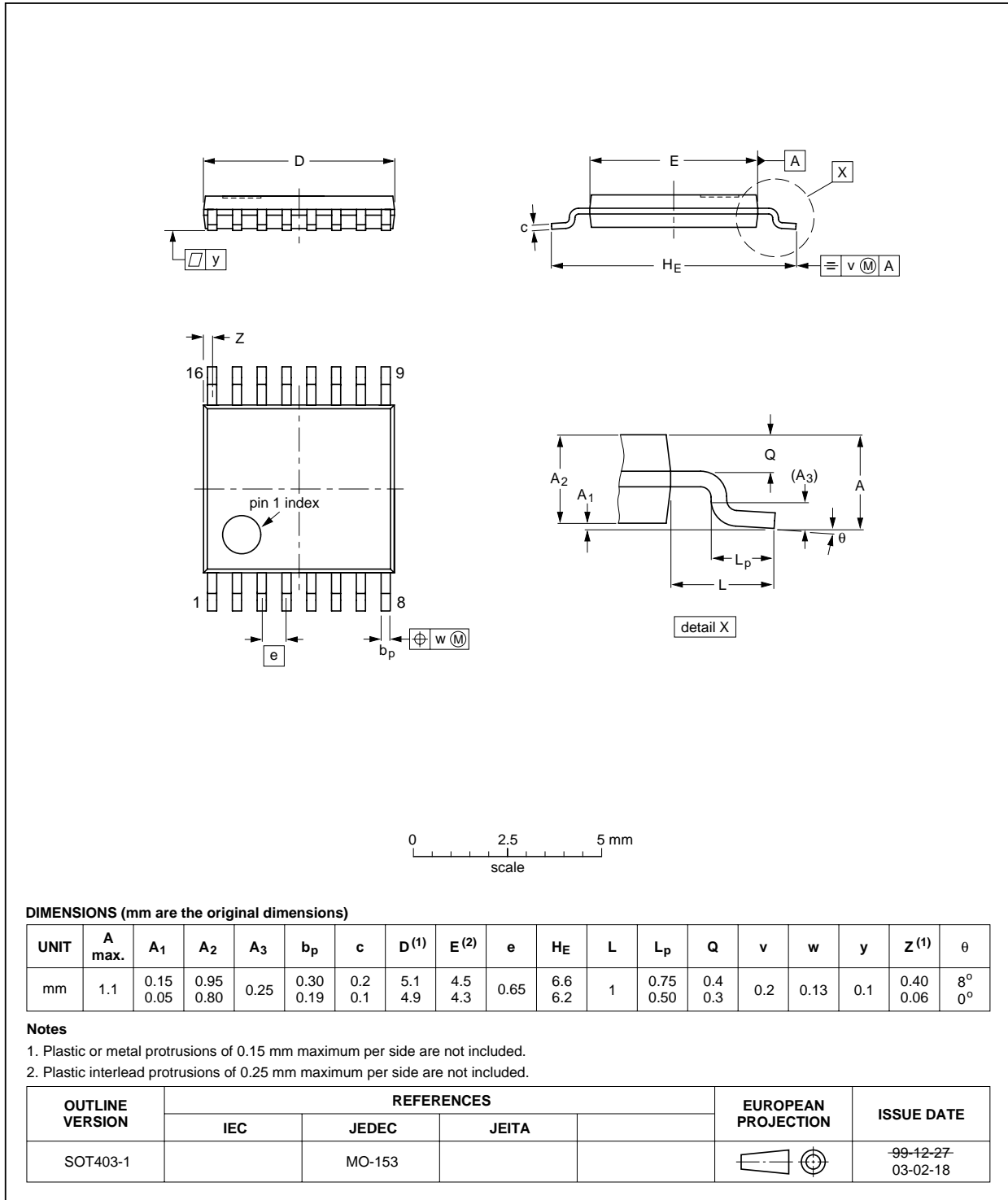
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT338-1 | | MO-150 | | | | 99-12-27 03-02-19 |

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

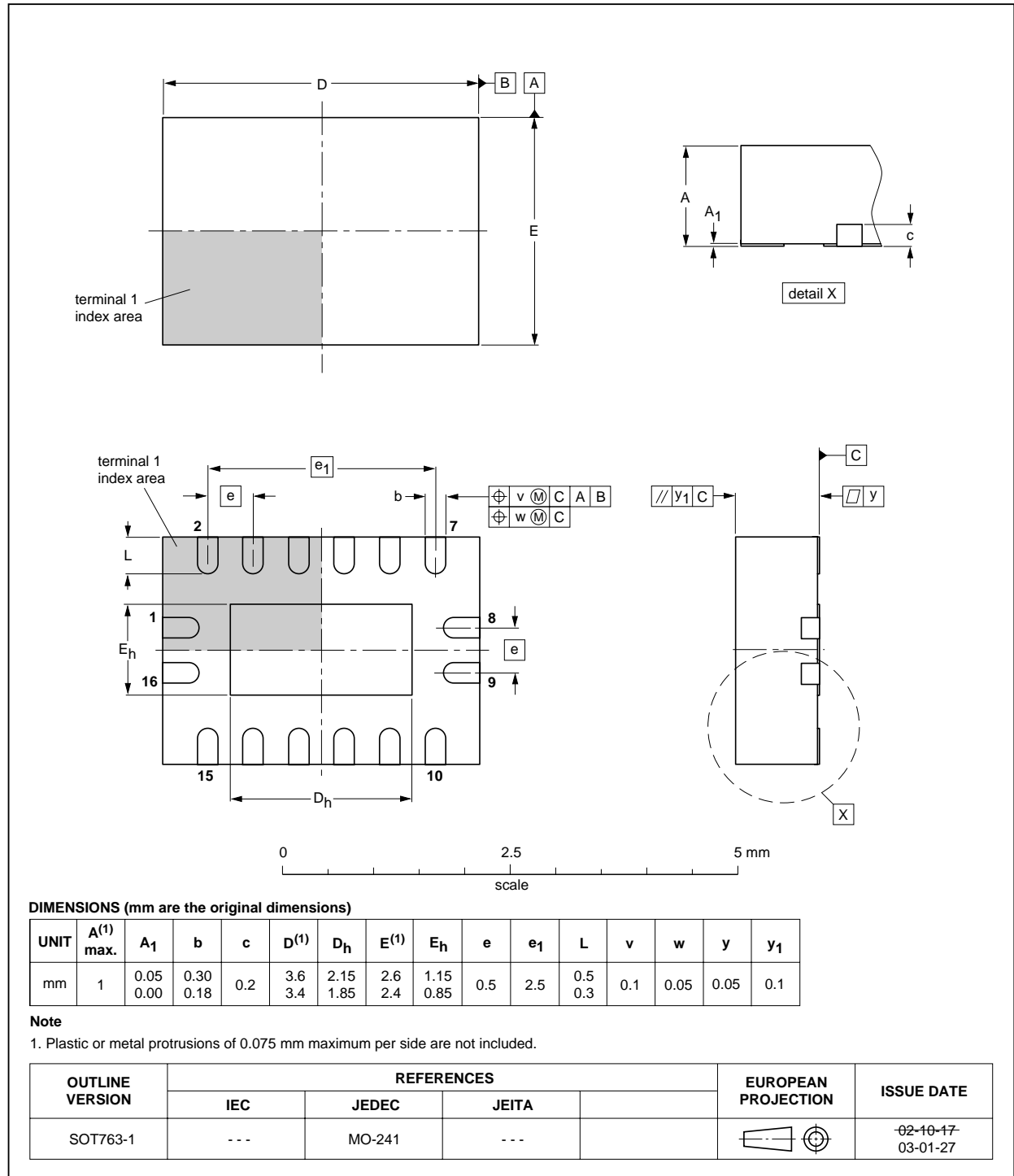
SOT403-1



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DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1



Quad 2-input multiplexer

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DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾⁽³⁾ | DEFINITION |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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