PCF8523

Real-Time Clock (RTC) and calendar

Rev. 3 — 30 March 2011 **Product data sheet**

1. General description

The PCF8523 is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low power consumption. Data is transferred serially via an I^2C-bus with a maximum data rate of 1000 kbit/s. Alarm and timer functions are available with the possibility to generate a wake-up signal on an interrupt pin. An offset register allows fine-tuning of the clock. The PCF8523 has a backup battery switch-over circuit, which detects power failures and automatically switches to the battery supply when a power failure occurs.

2. Features and benefits

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Resolution: seconds to years
- Clock operating voltage: 1.0 V to 5.5 V
- Low backup current: typical 150 nA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 2 line bidirectional 1 MHz Fast-mode Plus (Fm+) I^2C interface
- Battery backup input pin and switch-over circuit
- Freely programmable timer and alarm with interrupt capability
- Selectable integrated oscillator load capacitors for C_L = 7 pF or C_L = 12.5 pF
- Internal Power-On Reset (POR)
- Open-drain interrupt or clock output pins
- Programmable offset register for frequency adjustment

3. Applications

- Time keeping application
- Battery powered devices
- Metering

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 19.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8523T/1	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCF8523TS/1	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
PCF8523TK/1	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 4 × 4 × 0.85 mm	SOT909-1
PCF8523U/12AA/1	PCF8523U	bare die; 12 bumps (6-6)[1]	PCF8523U

[1] Delivery form: sawn 6-inch wafer (see Figure 41 on page 57) with gold bumps on Film Frame Carrier (FFC) for 8-inch wafer (see Figure 42 on page 57).

5. Marking

Table 2. Marking codes

Type number	Marking code
PCF8523T/1	8523T
PCF8523TS/1	8523TS
PCF8523TK/1	8523
PCF8523U/12AA/1	PC8523-1

6. Block diagram

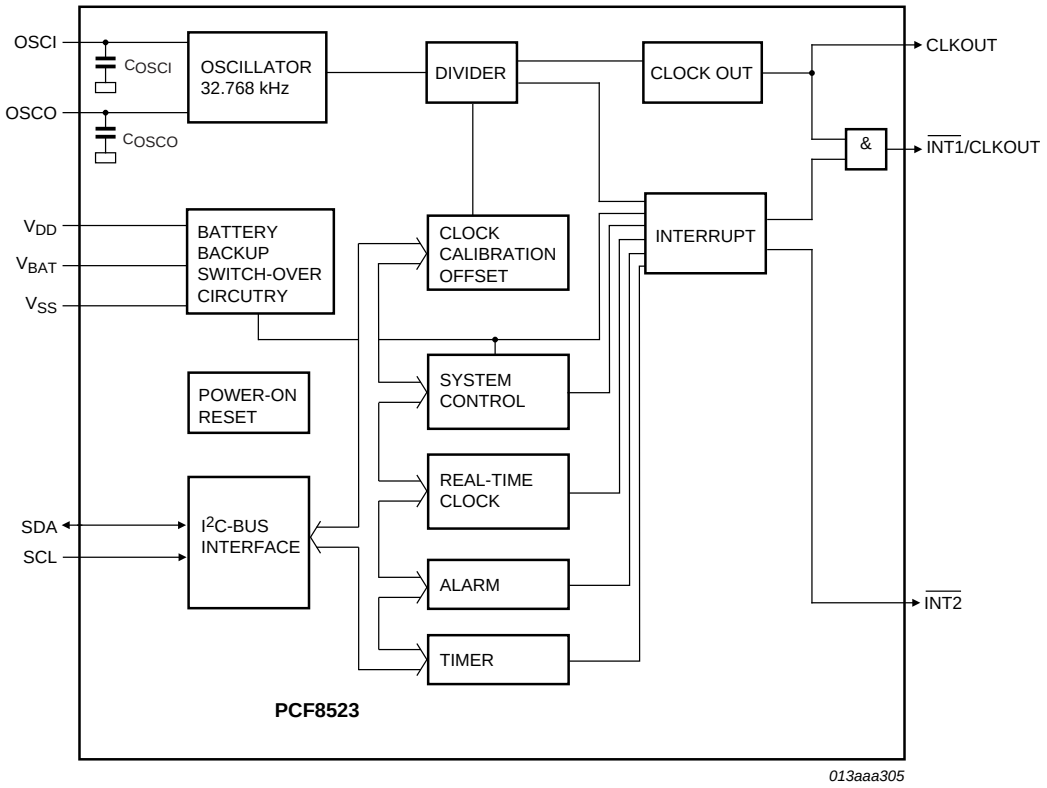
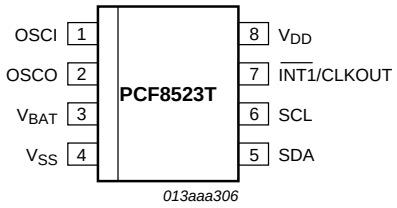


Fig 1. Block diagram of PCF8523

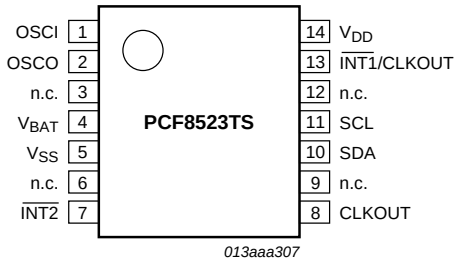
7. Pinning information

7.1 Pinning



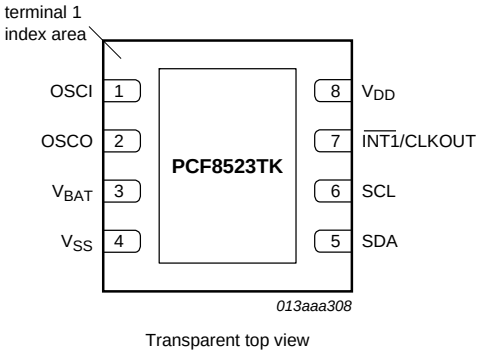
Top view. For mechanical details, see Figure 36 on page 52.

Fig 2. Pin configuration for SO8 (PCF8523T)



Top view. For mechanical details, see Figure 37 on page 53.

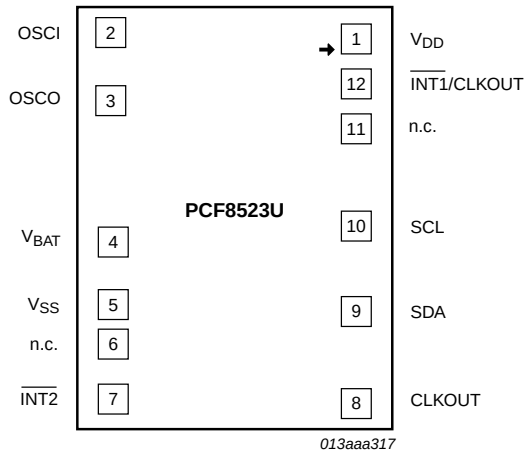
Fig 3. Pin configuration for TSSOP14 (PCF8523TS)



Transparent top view

For mechanical details, see Figure 38 on page 54.

Fig 4. Pin configuration for HVSON8 (PCF8523TK)



Viewed from active side. For mechanical details, see Figure 39 on page 55.

Fig 5. Pin configuration for PCF8523U

7.2 Pin description

Table 3. Pin description

Symbol	Pin				Type	Description
	SO8 (PCF8523T)	TSSOP14 (PCF8523TS)	HVSON8 (PCF8523TK)	PCF8523U		
OSCI	1	1	1	2	input	oscillator input; high-impedance node[1]
OSCO	2	2	2	3	output	oscillator output; high-impedance node[1]
n.c.	-	3, 6, 9, 12[2]	-	6 and 11[2]	-	not connected; do not connect and do not use it as feed through
V_{BAT}	3	4	3	4	supply	battery supply voltage
V_{SS}	4	5	4[3]	5[4]	supply	ground supply voltage
$\overline{INT2}$	-	7	-	7	output	interrupt 2 (open-drain, active LOW)
CLKOUT	-	8	-	8	output	clock output (open-drain)
SDA	5	10	5	9	input/output	serial data input/output
SCL	6	11	6	10	input	serial clock input
$\overline{INT1}$/CLKOUT	7	13	7	12	output	interrupt 1/clock output (open-drain)
V_{DD}	8	14	8	1	supply	supply voltage

[1] Wire length between quartz and package should be minimized.

[2] For manufacturing tests only; do not connect it and do not use it.

[3] The die paddle (exposed pad) is connected to V_{SS} and should be electrically isolated.

[4] The substrate (rear side of the die) is connected to V_{SS} and should be electrically isolated.

8. Functional description

The PCF8523 contains

- 20 8-bit registers with an auto-incrementing address register,
- An on-chip 32.768 kHz oscillator with two integrated load capacitors,
- A frequency divider, which provides the source clock for the Real-Time Clock (RTC),
- A programmable clock output,
- A 1 Mbit/s I^2C-bus interface,
- And an offset register, which allows fine-tuning of the clock.

All 20 registers are designed as addressable 8-bit registers although not all bits are implemented.

- The first three registers (memory address 00h, 01h, and 02h) are used as control and status registers.
- The addresses 03h through 09h are used as counters for the clock function (seconds up to years).
- Addresses 0Ah through 0Dh define the alarm condition.
- Address 0Eh defines the offset calibration.
- Address 0Fh defines the clock-out mode and the addresses 10h and 12h the timer mode.
- Addresses 11h and 13h are used for the timers.

The registers Seconds, Minutes, Hours, Days, Weekdays, Months, and Years are all coded in Binary Coded Decimal (BCD) format. Other registers are either bit-wise or standard binary. When one of the RTC registers is read, the contents of all counters are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented.

The PCF8523 has a battery backup input pin and battery switch-over circuit, which monitors the main power supply and automatically switches to the backup battery when a power failure condition is detected. Accurate timekeeping is maintained even when the main power supply is interrupted.

A battery low detection circuit monitors the status of the battery. When the battery voltage goes below a certain threshold value, a flag is set to indicate that the battery must be replaced soon. This ensures the integrity of the data during periods of battery backup.

8.1 Register overview

The 20 registers of the PCF8523 are auto-incrementing after each read or write data byte up to register 13h. After register 13h, the auto-incrementing will wrap around to address 00h (see Figure 6).

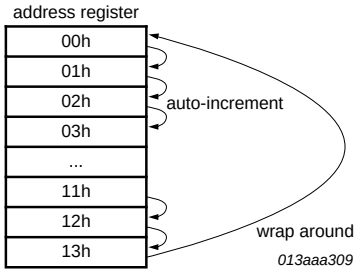


Fig 6. Auto-incrementing of the registers

Table 4. Registers overview

Bit positions labeled as - are not implemented and will return a 0 when read. Bit T must always be written with logic 0.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Control registers									
00h	Control_1	CAP_SEL	T	STOP	SR	12_24	SIE	AIE	CIE
01h	Control_2	WTAF	CTAF	CTBF	SF	AF	WTAIE	CTAIE	CTBIE
02h	Control_3	PM[2:0]			-	BSF	BLF	BSIE	BLIE
Time and date registers									
03h	Seconds	OS	SECONDS (0 to 59)						
04h	Minutes	-	MINUTES (0 to 59)						
05h	Hours	-	-	AMPM	HOURS (1 to 12 in 12 hour mode)				
				HOURS (0 to 23 in 24 hour mode)					
06h	Days	-	-	DAYS (1 to 31)					
07h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)		
08h	Months	-	-	-	MONTHS (1 to 12)				
09h	Years	YEARS (0 to 99)							
Alarm registers									
0Ah	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)						
0Bh	Hour_alarm	AE_H	-	AMPM	HOUR_ALARM (1 to 12 in 12 hour mode)				
			-	HOUR_ALARM (0 to 23 in 24 hour mode)					
0Ch	Day_alarm	AE_D	-	DAY_ALARM (1 to 31)					
0Dh	Weekday_alarm	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)		
Offset register									
0Eh	Offset	MODE	OFFSET[6:0]						

Table 4. Registers overview *...continued*

Bit positions labeled as - are not implemented and will return a 0 when read. Bit T must always be written with logic 0.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
CLOCKOUT and timer registers									
0Fh	Tmr_CLKOUT_ctrl	TAM	TBM	COF[2:0]			TAC[1:0]		TBC
10h	Tmr_A_freq_ctrl	-	-	-	-	-	TAQ[2:0]		
11h	Tmr_A_reg	TIMER_A_VALUE[7:0]							
12h	Tmr_B_freq_ctrl	-	TBW[2:0]			-	TBQ[2:0]		
13h	Tmr_B_reg	TIMER_B_VALUE[7:0]							

8.2 Control and status registers

8.2.1 Register Control_1

Table 5. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value	Description
7	CAP_SEL		internal oscillator capacitor selection for quartz crystals with a corresponding load capacitance
		0[1]	7 pF
		1	12.5 pF
6	T	0[1][2]	unused
5	STOP	0[1]	RTC time circuits running
		1	RTC time circuits frozen; RTC divider chain flip-flops are asynchronously set logic 0; CLKOUT at 32.768 kHz, 16.384 kHz, or 8.192 kHz is still available
4	SR	0[1][3]	no software reset
		1	initiate software reset
3	12_24	0[1]	24 hour mode is selected
		1	12 hour mode is selected
2	SIE	0[1]	second interrupt disabled
		1	second interrupt enabled
1	AIE	0[1]	alarm interrupt disabled
		1	alarm interrupt enabled
0	CIE	0[1]	no correction interrupt generated
		1	interrupt pulses will be generated at every correction cycle (see Section 8.8)

[1] Default value.

[2] Must always be written with logic 0.

[3] For a software reset, 01011000 (58h) must be sent to register Control_1 (see Section 8.3). Bit SR will always return 0 when read.

8.2.2 Register Control_2

Table 6. Control_2 - control and status register 2 (address 01h) bit description

Bit	Symbol	Value	Description
7	WTAF	0[1]	no watchdog timer A interrupt generated
		1	flag set when watchdog timer A interrupt generated; flag is read-only and cleared by reading register Control_2
6	CTAF	0[1]	no countdown timer A interrupt generated
		1	flag set when countdown timer A interrupt generated; flag must be cleared to clear interrupt
5	CTBF	0[1]	no countdown timer B interrupt generated
		1	flag set when countdown timer B interrupt generated; flag must be cleared to clear interrupt
4	SF	0[1]	no second interrupt generated
		1	flag set when second interrupt generated; flag must be cleared to clear interrupt
3	AF	0[1]	no alarm interrupt generated
		1	flag set when alarm triggered; flag must be cleared to clear interrupt
2	WTAIE	0[1]	watchdog timer A interrupt is disabled
		1	watchdog timer A interrupt is enabled
1	CTAIE	0[1]	countdown timer A interrupt is disabled
		1	countdown timer A interrupt is enabled
0	CTBIE	0[1]	countdown timer B interrupt is disabled
		1	countdown timer B interrupt is enabled

[1] Default value.

8.2.3 Register Control_3

Table 7. Control_3 - control and status register 3 (address 02h) bit description

Bit	Symbol	Value	Description
7 to 5	PM[2:0]	see Table 9[1]	battery switch-over and battery low detection control
4	-	-	unused
3	BSF	0[2]	no battery switch-over interrupt generated
		1	flag set when battery switch-over occurs; flag must be cleared to clear interrupt
2	BLF	0[2]	battery status ok
		1	battery status low; flag is read-only
1	BSIE	0[2]	no interrupt generated from battery switch-over flag, BSF
		1	interrupt generated when BSF is set
0	BLIE	0[2]	no interrupt generated from battery low flag, BLF
		1	interrupt generated when BLF is set

[1] Default value is 111.

[2] Default value.

8.3 Reset

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command. Software reset command means setting bits 6, 4, and 3 in register Control_1 (00h) logic 1 and all other bits logic 0 by sending the bit sequence 01011000 (58h), see Figure 7.

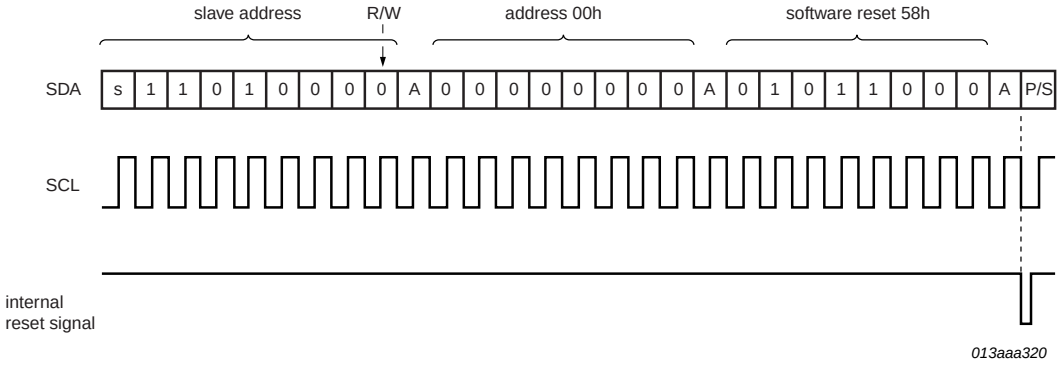


Fig 7. Software reset command

Table 8. Register reset values

Bits labeled X are undefined at power-on and unchanged by subsequent resets. Bits labeled - are not implemented.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	0	0	0	0	0	0	0	0
01h	Control_2	0	0	0	0	0	0	0	0
02h	Control_3	1	1	1	-	0	0	0	0
03h	Seconds	1	X	X	X	X	X	X	X
04h	Minutes	-	X	X	X	X	X	X	X
05h	Hours	-	-	X	X	X	X	X	X
06h	Days	-	-	X	X	X	X	X	X
07h	Weekdays	-	-	-	-	-	X	X	X
08h	Months	-	-	-	X	X	X	X	X
09h	Years	X	X	X	X	X	X	X	X
0Ah	Minute_alarm	1	X	X	X	X	X	X	X
0Bh	Hour_alarm	1	-	X	X	X	X	X	X
0Ch	Day_alarm	1	-	X	X	X	X	X	X
0Dh	Weekday_alarm	1	-	-	-	-	X	X	X
0Eh	Offset	0	0	0	0	0	0	0	0
0Fh	Tmr_CLKOUT_ctrl	0	0	0	0	0	0	0	0
10h	Tmr_A_freq_ctrl	-	-	-	-	-	1	1	1
11h	Tmr_A_reg	X	X	X	X	X	X	X	X
12h	Tmr_B_freq_ctrl	-	0	0	0	-	1	1	1
13h	Tmr_B_reg	X	X	X	X	X	X	X	X

After reset, the following mode is entered:

- 32.768 kHz CLKOUT active
- 24 hour mode is selected
- Register Offset is set logic 0
- No alarms set
- Timers disabled
- No interrupts enabled
- Battery switch-over is disabled
- Battery low detection is disabled
- 7 pF of internal oscillator capacitor selected

8.4 Interrupt function

Active low interrupt signals are available at pin $\overline{\text{INT1}}$/CLKOUT and $\overline{\text{INT2}}$. Pin $\overline{\text{INT1}}$/CLKOUT has both functions of $\overline{\text{INT1}}$ and CLKOUT combined.

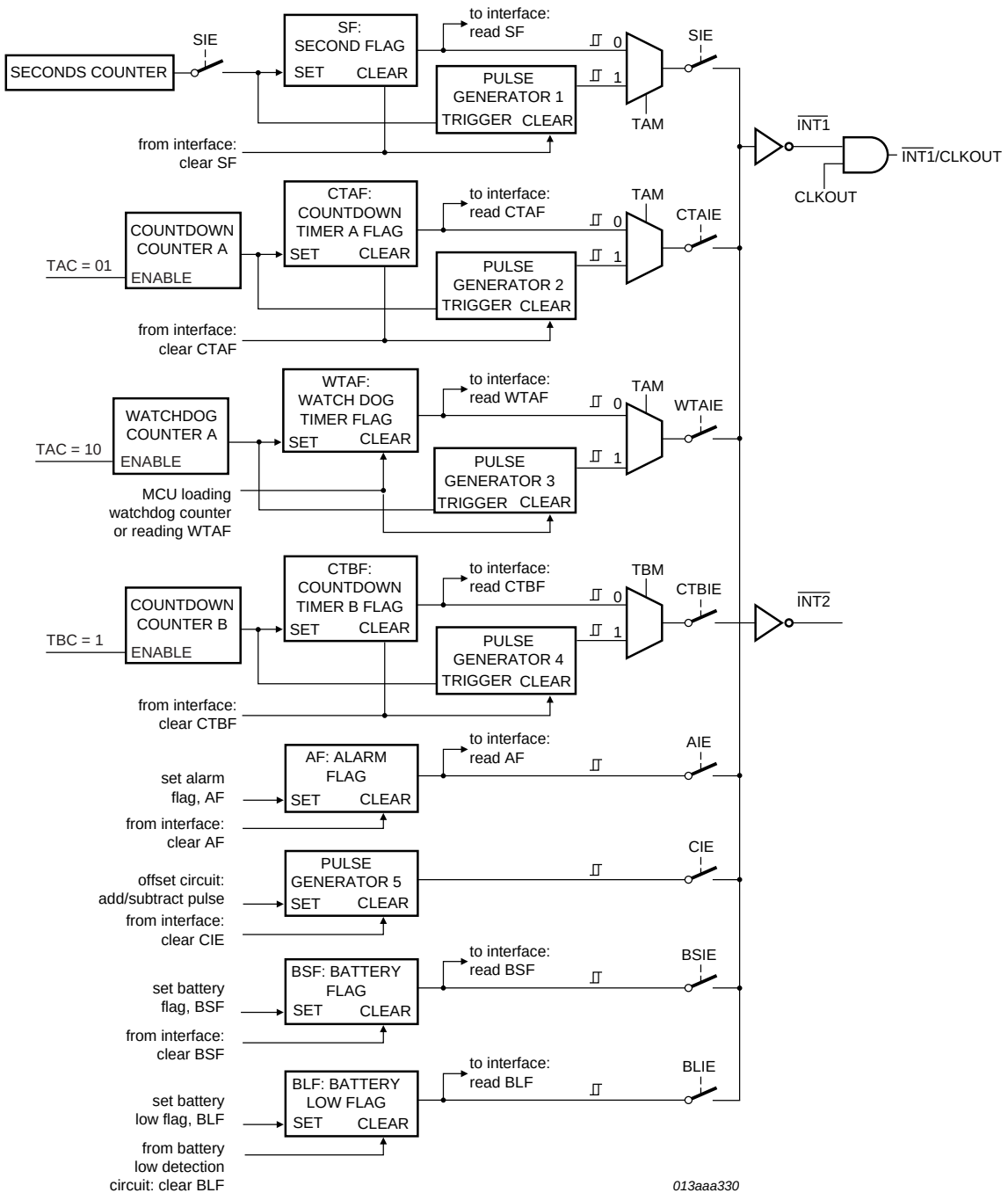
$\overline{\text{INT1}}$ Interrupt output may be sourced from different places:

- Second timer
- Timer A
- Timer B
- Alarm
- Battery Switch-over
- Battery Low Detection
- Clock offset correction pulse

$\overline{\text{INT2}}$ interrupt output is sourced only from timer B:

The control bit TAM (register Tmr_CLKOUT_ctrl) is used to configure whether the interrupts generated from the second interrupt timer and timer A are pulsed signals or a permanently active signal. The control bit TBM (register Tmr_CLKOUT_ctrl) is used to configure whether the interrupt generated from timer B is a pulsed signal or a permanently active signal. All the other interrupt sources generate a permanently active interrupt signal, which follows the status of the corresponding flags.

- The flags SF, CTAF, CTBF, AF, and BSF can be cleared by using the interface.
- WTAF is read only. A read of the register Control_2 (01h) will automatically reset WTAF (WTAF = 0) and clear the interrupt.
- The flag BLF is read only. It is cleared automatically from the battery low detection circuit when the battery is replaced.



When SIE, CTAIE, WTAIE, CTBIE, AIE, CIE, BSIE, BLIE, and clock-out are disabled, then $\overline{INT1}$ will remain high-impedance. When CTBIE is disabled, then $\overline{INT2}$ will remain high-impedance.

Fig 8. Interrupt block diagram

8.5 Power management functions

The PCF8523 has two power supply pins:

- V_{DD} - the main power supply input pin,
- V_{BAT} - the battery backup input pin.

The PCF8523 has two power management functions implemented:

- Battery switch-over function,
- Battery low detection function.

The power management functions are controlled by the control bits PM[2:0] in register Control_3 (02h):

Table 9. Power management function control bits

PM[2:0]	Function
000	battery switch-over function is enabled in standard mode; battery low detection function is enabled
001	battery switch-over function is enabled in direct switching mode; battery low detection function is enabled
010[1]	battery switch-over function is disabled - only one power supply (V_{DD}); battery low detection function is enabled
100	battery switch-over function is enabled in standard mode; battery low detection function is disabled
101	battery switch-over function is enabled in direct switching mode; battery low detection function is disabled
110	not allowed
111[1][2]	battery switch-over function is disabled - only one power supply (V_{DD}); battery low detection function is disabled

[1] When the battery switch-over function is disabled, the PCF8523 works only with the power supply V_{DD}; V_{BAT} must be put to ground and the battery low detection function is disabled.

[2] Default value.

8.5.1 Standby mode

When the device is first powered up from the battery (V_{BAT}) but without a main supply (V_{DD}), the PCF8523 automatically enters the standby mode. In standby mode the PCF8523 will not draw any power from the backup battery until the device is powered up from the main power supply V_{DD}. Thereafter, the device will switch over to battery backup mode whenever the main power supply V_{DD} is lost.

It is also possible to enter into standby mode when the chip is already supplied by main power supply V_{DD} and a backup battery is connected. To enter the standby mode, the power management control bits PM[2:0] have to be set logic 111. Then the main power supply V_{DD} must be removed, as a result of this the PCF8523 will enter the standby mode and will not draw any current from the backup battery before it is powered up again from main supply V_{DD}.

8.5.2 Battery switch-over function

The PCF8523 has a backup battery switch-over circuit, which monitors the main power supply V_{DD} and automatically switches to the backup battery when a power failure condition is detected.

One of two operation modes can be selected:

- **Standard mode:** the power failure condition happens when: $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$
- **Direct switching mode:** the power failure condition happens when $V_{DD} < V_{BAT}$. Direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below $V_{th(sw)bat}$

$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V.

Generation of interrupts from the battery switch-over is controlled via the BSIE bit (see register Control_2). If BSIE is enabled, the $\overline{INT1}$ follows the status of bit BLF (register Control_3). Clearing BLF immediately clears $\overline{INT1}$.

When a power failure condition occurs and the power supply switches to the battery the following sequence occurs:

1. The battery switch flag BSF (register Control_3) is set logic 1.
2. An interrupt is generated if the control bit BSIE (register Control_3) is enabled.

The battery switch flag BSF can be cleared by using the interface after the power supply has switched to V_{DD}. It must be cleared to clear the interrupt.

The interface is disabled in battery backup operation:

- Interface inputs are not recognized, preventing extraneous data being written to the device.
- Interface outputs are high-impedance.

8.5.2.1 Standard mode

If $V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$ the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$ the internal power supply is V_{BAT}.

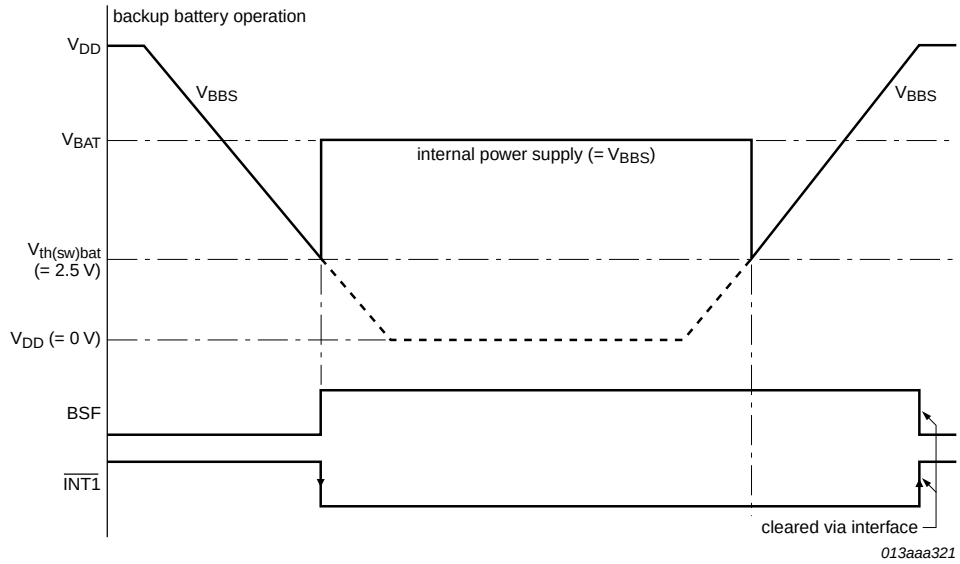


Fig 9. Battery switch-over behavior in standard mode and with bit BSIE set logic 1 (enabled)

8.5.2.2 Direct switching mode

If $V_{DD} > V_{BAT}$ the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$ the internal power supply is V_{BAT}.

The direct switching mode is useful in systems where V_{DD} is higher than V_{BAT} at all times (e.g. V_{DD} = 5 V, V_{BAT} = 3.5 V). The direct switching mode is not recommended if the V_{DD} and V_{BAT} values are similar (e.g. V_{DD} = 3.3 V, $V_{BAT} \geq$ 3.0 V). In direct switching mode the power consumption is reduced compared to the standard mode because the monitoring of V_{DD} and $V_{th(sw)bat}$ is not performed.

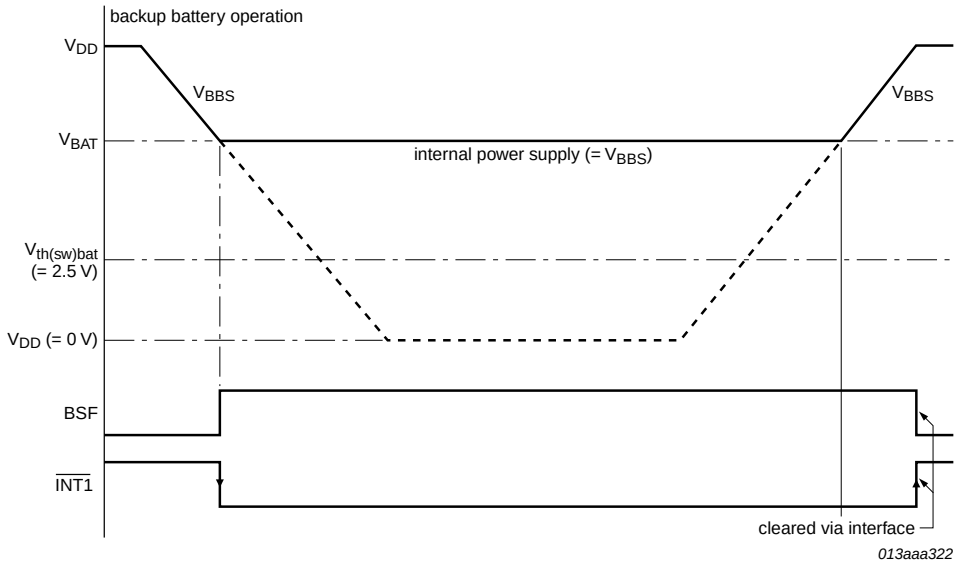


Fig 10. Battery switch-over behavior in direct switching mode and with bit BSIE set logic 1 (enabled)

8.5.2.3 Battery switch-over disabled, only one power supply (V_{DD})

When the battery switch-over function is disabled:

- The power supply is applied on the V_{DD} pin.
- The V_{BAT} pin must be connected to ground.
- The battery flag (BSF) is always logic 0.

8.5.3 Battery low detection function

The PCF8523 has a battery low detection circuit, which monitors the status of the battery V_{BAT}.

Generation of interrupts from the battery low detection is controlled via bit BLIE (register Control_3). If BLIE is enabled the $\overline{INT1}$ will follow the status of bit BLF (register Control_3).

When V_{BAT} drops below the threshold value $V_{th(bat)low}$ (typically 2.5 V) the BLF flag (register Control_3) is set to indicate that the battery is low and that it must be replaced. Monitoring of the battery voltage also occurs during battery operation.

An unreliable battery will not ensure data integrity during periods of backup battery operation.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$, the following sequence occurs (see Figure 11):

1. The battery low flag BLF is set logic 1.
2. An interrupt is generated if the control bit BLIE (register Control_3) is enabled. The interrupt remains active until the battery is replaced (BLF set logic 0) or when bit BLIE is disabled (BLIE set logic 0).
3. The flag BLF (register Control_3) remains logic 1 until the battery is replaced. BLF cannot be cleared using the interface. It is cleared automatically by the battery low detection circuit when the battery is replaced.

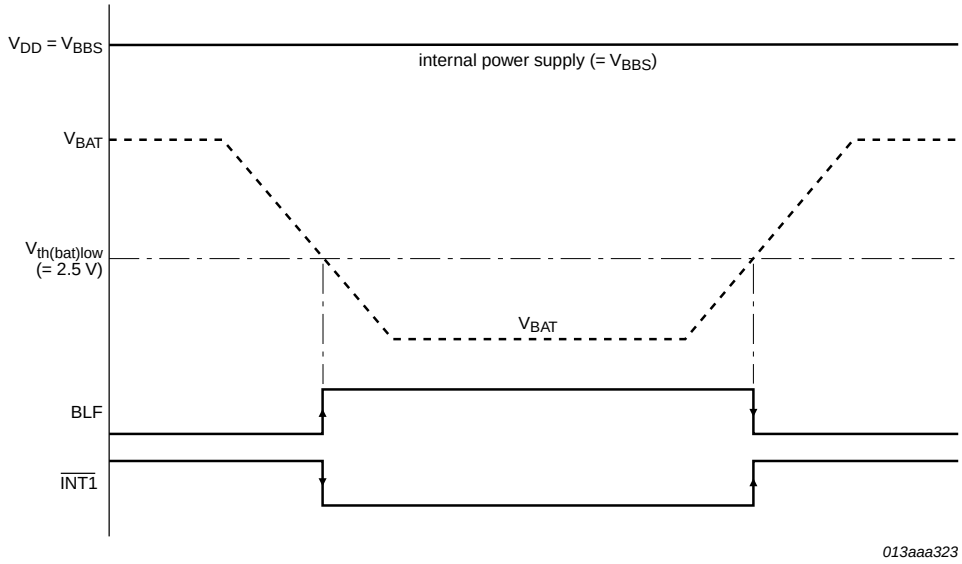


Fig 11. Battery low detection behavior with bit BLIE set logic 1 (enabled)

8.6 Time and date registers

Most of these registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use. An example is shown for the array SECONDS in Table 11.

8.6.1 Register Seconds

Table 10. Seconds - seconds and clock integrity status register (address 03h) bit description

Bit	Symbol	Value	Place value	Description
7	OS	0	-	clock integrity is guaranteed
		1[1]	-	clock integrity is not guaranteed; oscillator has stopped or been interrupted
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format
3 to 0		0 to 9	unit place	

[1] Start-up value.

Table 11. SECONDS coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit			Bit			
	6	5	4	3	2	1	0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

8.6.1.1 Oscillator stop flag

The OS flag is set whenever the oscillator is stopped (see Figure 12). The flag will remain set until cleared by using the interface. When the oscillator is not running, then the OS flag cannot be cleared. This method can be used to monitor the oscillator.

The oscillator may be stopped, for example, by grounding one of the oscillator pins, OSCI or OSCO. The oscillator is also considered to be stopped during the time between power-on and stable crystal resonance. This time may be in a range of 200 ms to 2 s, depending on crystal type, temperature, and supply voltage. At power-on, the OS flag is always set.

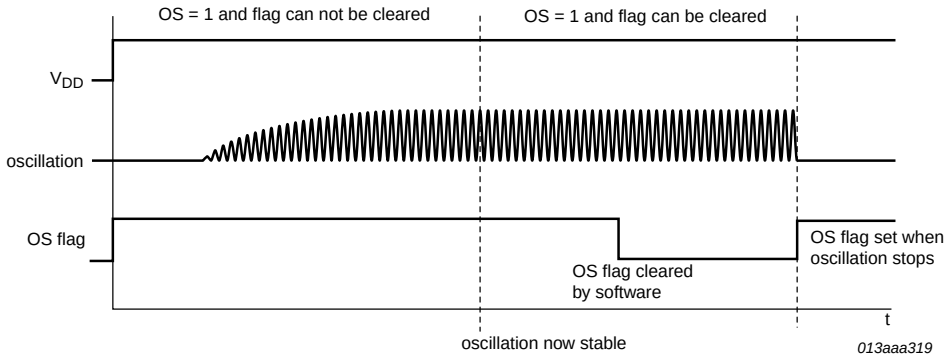


Fig 12. OS flag

8.6.2 Register Minutes

Table 12. Minutes - minutes register (address 04h) bit description

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	MINUTES	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

8.6.3 Register Hours

Table 13. Hours - hours register (address 05h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
12 hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOURS	0 to 1	ten's place	actual hours in 12 hour mode coded in BCD format
3 to 0		0 to 9	unit place	
24 hour mode[1]				
5 to 4	HOURS	0 to 2	ten's place	actual hours in 24 hour mode coded in BCD format
3 to 0		0 to 9	unit place	

[1] Hour mode is set by bit 12_24 in register Control_1 (see Table 5).

8.6.4 Register Days

Table 14. Days - days register (address 06h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] The PCF8523 compensates for leap years by adding a 29th day to February if the year counter contains a value, which is exactly divisible by 4, including the year 00.

8.6.5 Register Weekdays

Table 15. Weekdays - weekdays register (address 07h) bit description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday, values see Table 16

Table 16. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be re-assigned by the user.

8.6.6 Register Months

Table 17. Months - months register (address 08h) bit description

Bit	Symbol	Value	Place value	Description
7 to 5	-	-	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format; assignments see Table 18
3 to 0		0 to 9	unit place	

Table 18. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit	Bit			
	4	3	2	1	0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.6.7 Register Years

Table 19. Years - years register (09h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format
3 to 0		0 to 9	unit place	

8.6.8 Data flow of the time function

Figure 13 shows the data flow and data dependencies starting from the 1 Hz clock tick.

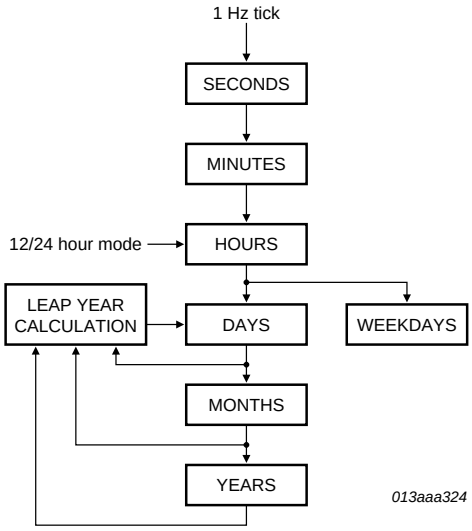


Fig 13. Data flow diagram of the time function

During read/write operations, the time counting circuits (memory locations 03h through 09h) are blocked.

This prevents:

- Faulty reading of the clock and calendar during a carry condition,
- Incrementing the time registers during the read cycle.

After this read/write-access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of one request can be stored; therefore, all accesses must be completed within 1 second (see Figure 14).

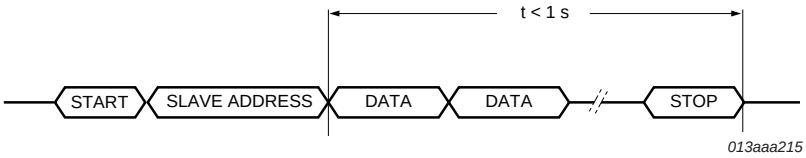


Fig 14. Access time for read/write operations

Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time will increment between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next. Therefore, it is advised to read all time and date registers in one access.

8.7 Alarm registers

The registers at addresses 0Ah through 0Dh contain the alarm information.

8.7.1 Register Minute_alarm

Table 20. Minute_alarm - minute alarm register (address 0Ah) bit description

Bit	Symbol	Value	Place value	Description
7	AE_M	0	-	minute alarm is enabled
		1[1]	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.7.2 Register Hour_alarm

Table 21. Hour_alarm - hour alarm register (address 0Bh) bit description

Bit	Symbol	Value	Place value	Description
7	AE_H	0	-	hour alarm is enabled
		1[1]	-	hour alarm is disabled
6	-	-	-	unused
12 hour mode[2]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOUR_ALARM	0 to 1	ten's place	hour alarm information in 12 hour mode coded in BCD format
3 to 0		0 to 9	unit place	
24 hour mode[2]				
5 to 4	HOURS	0 to 2	ten's place	hour alarm information in 24 hour mode coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

[2] Hour mode is set by bit 12_24 in register Control_1 (see Table 5).

8.7.3 Register Day_alarm

Table 22. Day_alarm - day alarm register (address 0Ch) bit description

Bit	Symbol	Value	Place value	Description
7	AE_D	0	-	day alarm is enabled
		1[1]	-	day alarm is disabled
6	-	-	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

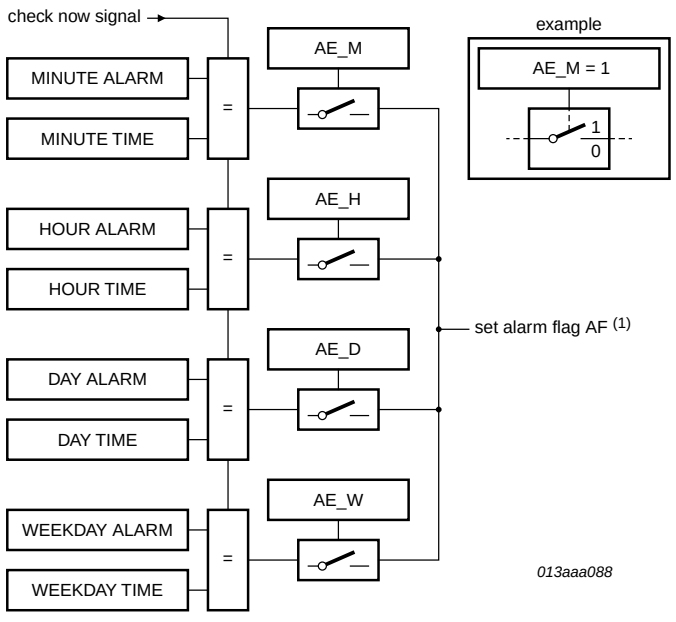
8.7.4 Register Weekday_alarm

Table 23. Weekday_alarm - weekday alarm register (address 0Dh) bit description

Bit	Symbol	Value	Description
7	AE_W	0	weekday alarm is enabled
		1[1]	weekday alarm is disabled
6 to 3	-	-	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information

[1] Default value.

8.7.5 Alarm flag



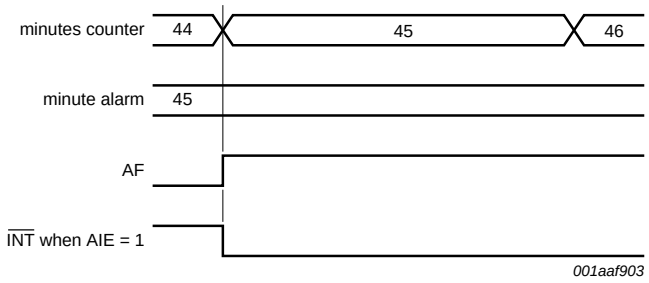
(1) Only when all enabled alarm settings are matching.
It's only on increment to a matched case that the alarm flag is set, see Section 8.7.5.

Fig 15. Alarm function block diagram

When one or several alarm registers are loaded with a valid minute, hour, day, or weekday value and its corresponding alarm enable bit (AE_x) is logic 0, then that information is compared with the current minute, hour, day, and weekday value. When all enabled comparisons first match, the alarm flag, AF (register Control_2), is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE (register Control_1). If bit AIE is enabled, then the $\overline{INT1}$ pin follows the condition of bit AF. AF will remain set until cleared by the interface. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers, which have their AE_x bit logic 1 are ignored. The generation of interrupts from the alarm function is described more detailed in Section 8.4.

Table 24 and Table 25 show an example for clearing bit AF. Clearing the flag is made by a write command, therefore bits 2, 1, and 0 must be re-written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 16. Alarm flag timing

To prevent the timer flags being overwritten while clearing bit AF, logic AND is performed during a write access. A flag is cleared by writing logic 0 whilst a flag is not cleared by writing logic 1. Writing logic 1 will result in the flag value remaining unchanged.

Table 24. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	WTAF	CTAF	CTBF	SF	AF	-	-	-

Table 25 shows what instruction must be sent to clear bit AF. In this example, bit CTAF, CTBG, and bit SF are unaffected.

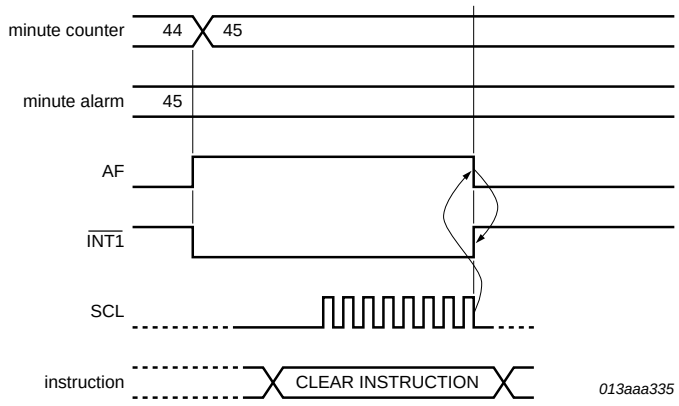
Table 25. Example to clear only AF (bit 3)[1]

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	0	1	1	1	0	-	-	-

[1] The bits labelled as - have to be rewritten with the previous values.

8.7.6 Alarm interrupts

Generation of interrupts from the alarm function is controlled via the bit AIE (register Control_1). If AIE is enabled, the $\overline{INT1}$ will follow the status of bit AF (register Control_2). Clearing AF will immediately clear $\overline{INT1}$. No pulse generation is possible for alarm interrupts.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 17. AF timing

8.8 Register Offset

The PCF8523 incorporates an offset register (address 0Eh), which can be used to implement several functions, like:

- Aging adjustment,
- Temperature compensation,
- Accuracy tuning.

Table 26. Offset - offset register (address 0Eh) bit description

Bit	Symbol	Value	Description
7	MODE	0[1]	offset is made once every two hours
		1	offset is made once every minute
6 to 0	OFFSET[6:0]	see Table 27	offset value

[1] Default value.

Each LSB will introduce an offset of 4.34 ppm for MODE = 0 and 4.069 ppm for MODE = 1. The values of 4.34 ppm and 4.069 ppm are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63 LSB to −64 LSB.

Table 27. Offset values

OFFSET[6:0]	Offset value in decimal	Offset value in ppm	
		Every two hours (MODE = 0)	Every minute (MODE = 1)
0111111	+63	+273.420	+256.347
0111110	+62	+269.080	+252.278
:	:	:	:
0000010	+2	+8.680	+8.138
0000001	+1	+4.340	+4.069
0000000	0[1]	0[1]	0[1]
1111111	−1	−4.340	−4.069
1111110	−2	−8.680	−8.138
:	:	:	:
1000001	−63	−273.420	−256.347
1000000	−64	−277.760	−260.416

[1] Default mode.

The correction is made by adding or subtracting clock correction pulses, thereby changing the period of a single second.

It is possible to monitor when correction pulses are applied. To enable correction interrupt generation, bit CIE (register Control_1) has to be set logic 1. At every correction cycle a $^1/_{4096}$ s pulse will be generated on pin INT1. In the case that multiple correction pulses are applied, a $^1/_{4096}$ s interrupt pulse will be generated for each correction pulse applied.

8.8.1 Correction when MODE = 0

The correction is triggered once per two hours and then correction pulses are applied once per minute until the programmed correction values have been implemented.

Table 28. Correction pulses for MODE = 0

Correction value	Hour	Minute	Correction pulses on INT1 per minute[1]
+1 or −1	02	00	1
+2 or −2	02	00 and 01	1
+3 or −3	02	00, 01, and 02	1
:	:	:	:
+59 or −59	02	00 to 58	1
+60 or −60	02	00 to 59	1
+61 or −61	02	00 to 59	1
	03	00	1
+62 or −62	02	00 to 59	1
	03	00 and 01	1
+63 or −63	02	00 to 59	1
	03	00, 01, and 02	1
−64	02	00 to 59	1
	03	00, 01, 02, and 03	1

[1] The correction pulses on pin $\overline{INT1}$ are $^1/_{64}$ s wide.

In MODE = 0, any timer or clock output using a frequency below 64 Hz will be affected by the clock correction (see Table 29).

Table 29. Effect of clock correction for MODE = 0

CLKOUT frequency (Hz)	Effect of correction	Timer source clock frequency (Hz)	Effect of correction
32768	no effect	4096	no effect
16384	no effect	64	no effect
8192	no effect	1	effected
4096	no effect	$^1/_{60}$	effected
1024	no effect	$^1/_{3600}$	effected
32	effected	-	-
1	effected	-	-

8.8.2 Correction when MODE = 1

The correction is triggered once per minute and then correction pulses are applied once per second up to a maximum of 60 pulses. When correction values greater than 60 pulses are used, additional correction pulses are made in the 59th second.

Clock correction is made more frequently in MODE = 1; however, this can result in higher power consumption.

Table 30. Correction pulses for MODE = 1

Correction value	Minute	Second	Correction pulses on INT1 per second[1]
+1 or −1	02	00	1
+2 or −2	02	00 and 01	1
+3 or −3	02	00, 01, and 02	1
:	:	:	:
+59 or −59	02	00 to 58	1
+60 or −60	02	00 to 59	1
+61 or −61	02	00 to 58	1
	02	59	2
+62 or −62	02	00 to 58	1
	02	59	2
+63 or −63	02	00 to 58	1
	02	59	4
−64	02	00 to 58	1
	02	59	5

[1] The correction pulses on pin $\overline{\text{INT1}}$ are $^1/_{4096}$ s wide. For multiple pulses they are repeated at an interval of $^1/_{2048}$ s.

In MODE = 1, any timer source clock using a frequency below 4.096 kHz will be also affected by the clock correction (see Table 31).

Table 31. Effect of clock correction for MODE = 1

CLKOUT frequency (Hz)	Effect of correction	Timer source clock frequency (Hz)	Effect of correction
32768	no effect	4096	no effect
16384	no effect	64	effected
8192	no effect	1	effected
4096	no effect	$^1/_{60}$	effected
1024	no effect	$^1/_{3600}$	effected
32	effected	-	-
1	effected	-	-

8.9 Timer function

The PCF8523 has three timers:

- Timer A can be used as a watchdog timer or a countdown timer (see Section 8.9.2). It can be configured by using TAC[1:0] in the Tmr_CLKOUT_ctrl register (0Fh).
- Timer B can be used as a countdown timer (see Section 8.9.3). It can be configured by using TBC in the Tmr_CLKOUT_ctrl register (0Fh).
- Second interrupt timer is used to generate an interrupt once per second (see Section 8.9.4).

Timer A and timer B both have five selectable source clocks allowing for countdown periods from less than 1 ms to 255 h. To control the timer functions and timer output, the registers 01h, 0Fh, 10h, 11h, 12h, and 13h are used.

8.9.1 Timer registers

8.9.1.1 Register Tmr_CLKOUT_ctrl and clock output

Table 32. Tmr_CLKOUT_ctrl - timer and CLKOUT control register (address 0Fh) bit description

Bit	Symbol	Value	Description
7	TAM	0[1]	permanent active interrupt for timer A and for the second interrupt timer
		1	pulsed interrupt for timer A and the second interrupt timer
6	TBM	0[1]	permanent active interrupt for timer B
		1	pulsed interrupt for timer B
5 to 3	COF[2:0]	see Table 33	CLKOUT frequency selection
2 to 1	TAC[1:0]	00[1] to 11	timer A is disabled
		01	timer A is configured as countdown timer if CTAIE (register Control_2) is set logic 1, the interrupt is activated when the countdown timed out
		10	timer A is configured as watchdog timer if WTAIE (register Control_2) is set logic 1, the interrupt is activated when timed out
0	TBC	0[1]	timer B is disabled
		1	timer B is enabled if CTBIE (register Control_2) is set logic 1, the interrupt is activated when the countdown timed out

[1] Default value.

CLKOUT frequency selection: Clock output operation is controlled by the COF[2:0] in the Tmr_CLKOUT_ctrl register. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated (see Table 33) for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

A programmable square wave is available at pin INT1/CLKOUT and pin CLKOUT, which are both open-drain outputs. Pin INT1/CLKOUT has both functions of INT1 and CLKOUT combined.

The duty cycle of the selected clock is not controlled but due to the nature of the clock generation, all clock frequencies except 32.768 kHz have a duty cycle of 50 : 50.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When STOP is active, the INT1/CLKOUT and CLKOUT pins will be high-impedance for all frequencies except of 32.768 kHz, 16.384 kHz and 8.192 kHz. For more details, see Section 8.10.

Table 33. CLKOUT frequency selection

COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1]	Effect of STOP bit
000[2]	32768	60 : 40 to 40 : 60	no effect
001	16384	50 : 50	no effect
010	8192	50 : 50	no effect
011	4096	50 : 50	CLKOUT = high-Z
100	1024	50 : 50	CLKOUT = high-Z
101	32	50 : 50[3]	CLKOUT = high-Z
110	1	50 : 50[3]	CLKOUT = high-Z
111	CLKOUT disabled (high-Z)		

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] Default value.

[3] Clock frequencies may be affected by offset correction.

8.9.1.2 Register Tmr_A_freq_ctrl

Table 34. Tmr_A_freq_ctrl - timer A frequency control register (address 10h) bit description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	TAQ[2:0]		source clock for timer A (see Table 38)
		000	4.096 kHz
		001	64 Hz
		010	1 Hz
		011	$1/60$ Hz
		111[1] 110 100	$1/3600$ Hz

[1] Default value.

8.9.1.3 Register Tmr_A_reg

Table 35. Tmr_A_reg - timer A value register (address 11h) bit description

Bit	Symbol	Value	Description
7 to 0	TIMER_A_VALUE[7:0]	00 to FF	timer-period in seconds $timerperiod = \frac{n}{sourceclockfrequency}$ where n is the countdown value

8.9.1.4 Register Tmr_B_freq_ctrl

Table 36. Tmr_B_freq_ctrl - timer B frequency control register (address 12h) bit description

Bit	Symbol	Value	Description
7	-	-	unused
6 to 4	TBW[2:0]		low pulse width for pulsed timer B interrupt
		000[1]	46.875 ms
		001	62.500 ms
		010	78.125 ms
		011	93.750 ms
		100	125.000 ms
		101	156.250 ms
		110	187.500 ms
		111	218.750 ms
3	-	-	unused
2 to 0	TBQ[2:0]		source clock for timer B (see Table 38)
		000	4.096 kHz
		001	64 Hz
		010	1 Hz
		011	$1/60$ Hz
		111[1] 110 100	$1/3600$ Hz

[1] Default value.

8.9.1.5 Register Tmr_B_reg

Table 37. Tmr_B_reg - timer B value register (address 13h) bit description

Bit	Symbol	Value	Description
7 to 0	TIMER_B_VALUE[7:0]	00 to FF	timer-period in seconds $timerperiod = \frac{n}{sourceclockfrequency}$ where n is the countdown value

8.9.1.6 Programmable timer characteristics

Table 38. Programmable timer characteristics

TAQ[2:0] TBQ[2:0]	Timer source clock frequency	Units	Minimum timer-period (n = 1)	Units	Maximum timer-period (n = 255)	Units
000	4.096	kHz	244	µs	62.256	ms
001	64	Hz	15.625	ms	3.984	s
010	1	Hz	1	s	255	s
011	$1/60$	Hz	1	min	255	min
111 110 100	$1/3600$	Hz	1	hour	255	hour

8.9.2 Timer A

With the bit field TAC[1:0] in register Tmr_CLKOUT_ctrl (0Fh) Timer A can be configured as a countdown timer (TAC[1:0] = 01) or watchdog timer (TAC[1:0] = 10).

8.9.2.1 Watchdog timer function

The three bits TAQ[2:0] in register Tmr_A_freq_ctrl (10h) determine one of the five source clock frequencies for the watchdog timer: 4.096 kHz, 64 Hz, 1 Hz, $1/60$ Hz or $1/3600$ Hz (see Table 34).

The generation of interrupts from the watchdog timer is controlled by using WTAIE bit (register Control_2).

When configured as a watchdog timer (TAC[1:0] = 10), the 8-bit timer value in register Tmr_A_reg (11h) determines the watchdog timer-period.

The watchdog timer counts down from value n in register Tmr_A_reg (11h). When the counter reaches 1, the watchdog timer flag WTAF (register Control_2) is set logic 1 on the next rising edge of the timer clock (see Figure 18). In that case:

- If WTAIE = 1, an interrupt will be generated.
- If WTAIE = 0, no interrupt will be generated.

The interrupt generated by the watchdog timer function of timer A may be generated as pulsed signal or a permanent active signal. The TAM bit (register Tmr_CLKOUT_ctrl) is used to control the interrupt generation mode.

The counter does not automatically reload. When loading the counter with any valid value of n, except 0:

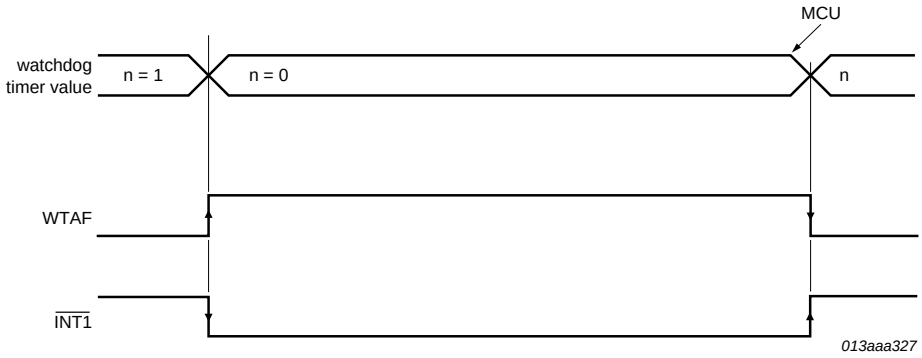
- The flag WTAF is reset (WTAF = 0),
- Interrupt is cleared,
- The watchdog timer starts.

When loading the counter with 0:

- The flag WTAF is reset (WTAF = 0),
- Interrupt is cleared,

- The watchdog timer stops.

WTAF is read only. A read of the register Control_2 (01h) will automatically reset WTAF (WTAF = 0) and clear the interrupt.



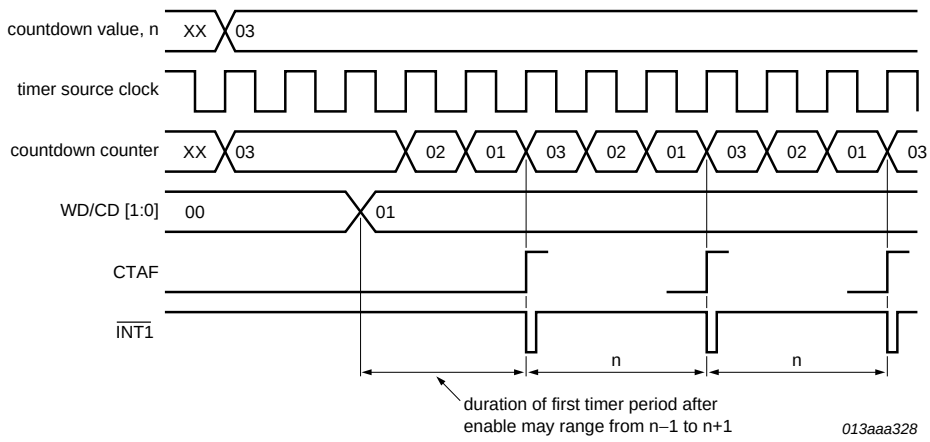
TAC[1:0] = 10, WTAIE = 1, WTAF = 1, an interrupt is generated.

Fig 18. Watchdog activates an interrupt when timed out

8.9.2.2 Countdown timer function

When configured as a countdown timer (TAC[1:0] = 01), timer A counts down from the software programmed 8-bit binary value n in register Tmr_A_reg (11h). When the counter reaches 1, the following events occur on the next rising edge of the timer clock (see Figure 19):

- The countdown timer flag CTAF (register Control_2) is set logic 1.
- When the interrupt generation is enabled (CTAIE = 1) an interrupt signal on $\overline{\text{INT1}}$ will be generated.
- The counter automatically reloads.
- The next timer-period starts.



In this example it is assumed that the countdown timer flag (CTAF) is cleared before the next countdown period expires and that interrupt output is set to pulse mode.

Fig 19. General countdown timer behavior

At the end of every countdown, the timer sets the countdown timer flag CTAF (register Control_2). CTAF may only be cleared by using the interface. Instructions, how to clear a flag, is given in Section 8.7.5.

When reading the timer, the current countdown value is returned and **not** the initial value n. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

If a new value of n is written before the end of the actual timer-period, this value will take immediate effect. It is not recommended to change n without first disabling the counter by setting TAC[1:0] = 00 (register Tmr_CLKOUT_ctrl). The update of n is asynchronous to the timer clock. Therefore changing it on the fly could result in a corrupted value loaded into the countdown counter. This can result in an undetermined countdown period for the first period. The countdown value n will be correctly stored and correctly loaded on subsequent timer-periods.

Loading the counter with 0 effectively stops the timer.

When starting the countdown timer for the first time, only the first period will not have a fixed duration. The amount of inaccuracy for the first timer-period, depends on the chosen source clock, see Table 39.

Table 39. First period delay for timer counter value n

Timer source clock	Minimum timer-period	Maximum timer-period
4.096 kHz	n	n + 1
64 Hz	n	n + 1
1 Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz
$\frac{1}{60}$ Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz
$\frac{1}{3600}$ Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz

The generation of interrupts from the countdown timer is controlled via the CTAIE bit (register Control_2).

When the interrupt generation is enabled (CTAIE = 1) and the countdown timer flag CTAF is set logic 1, an interrupt signal on $\overline{INT1}$ will be generated. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal, which follows the condition of CTAF (register Control_2). The TAM bit (register Tmr_CLKOUT_ctrl) is used to control this mode selection. The interrupt output may be disabled with the CTAIE bit (register Control_2).

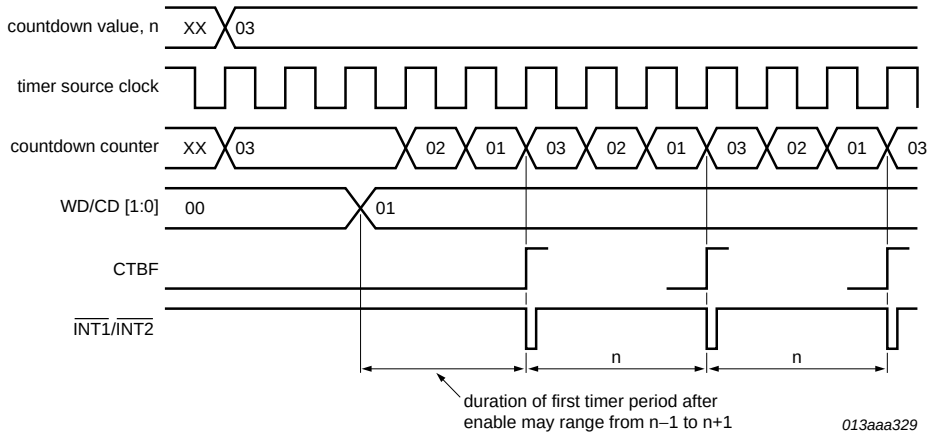
8.9.3 Timer B

Timer B can only be used as a countdown timer and can be switched on and off by the TBC bit in register Tmr_CLKOUT_ctrl (0Fh).

The generation of interrupts from the countdown timer is controlled via the CTBIE bit (register Control_2).

When enabled, it counts down from the software programmed 8 bit binary value n in register Tmr_B_reg (13h). When the counter reaches 1, on the next rising edge of the timer clock the following events occur (see Figure 20):

- The countdown timer flag CTBF (register Control_2) is set logic 1.
- When the interrupt generation is enabled (CTBIE = 1), interrupt signals on $\overline{INT1}$ and $\overline{INT2}$ will be generated.
- The counter automatically reloads.
- The next timer-period starts.



In this example, it is assumed that the countdown timer flag (CTBF) is cleared before the next countdown period expires and that interrupt output is set to pulse mode.

Fig 20. General countdown timer behavior

At the end of every countdown, the timer sets the countdown timer flag CTBF (register Control_2). CTBF may only be cleared by using the interface. Instructions, how to clear a flag, is given in Section 8.7.5.

When reading the timer, the current countdown value is returned and **not** the initial value n. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

If a new value of n is written before the end of the actual timer-period, this value will take immediate effect. It is not recommended to change n without first disabling the counter by setting TBC logic 0 (register Tmr_CLKOUT_ctrl). The update of n is asynchronous to the timer clock. Therefore changing it on the fly could result in a corrupted value loaded into the countdown counter. This can result in an undetermined countdown period for the first period. The countdown value n will be correctly stored and correctly loaded on subsequent timer-periods.

Loading the counter with 0 effectively stops the timer.

When starting the countdown timer for the first time, only the first period will not have a fixed duration. The amount of inaccuracy for the first timer-period depends on the chosen source clock; see Table 39.

When the interrupt generation is enabled (CTBIE = 1) and the countdown timer flag CTAF is set logic 1 interrupt signals on $\overline{INT1}$ and $\overline{INT2}$ are generated. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal, which follows the condition of CTBF (register Control_2). The TBM bit (register Tmr_CLKOUT_ctrl) is used to control this mode selection. Interrupt output may be disabled with the CTBIE bit (register Control_2).

8.9.4 Second interrupt timer

PCF8523 has a pre-defined timer, which is used to generate an interrupt once per second. The pulse generator for the second interrupt timer operates from an internal 64 Hz clock and generates a pulse of $^{1}/_{64}$ s in duration. It is independent of the watchdog or countdown timer and can be switched on and off by the SIE bit in register Control_1 (00h).

The interrupt generated by the second interrupt timer may be generated as pulsed signal every second or as a permanent active signal. The TAM bit (register Tmr_CLKOUT_ctrl) is used to control the interrupt generation mode.

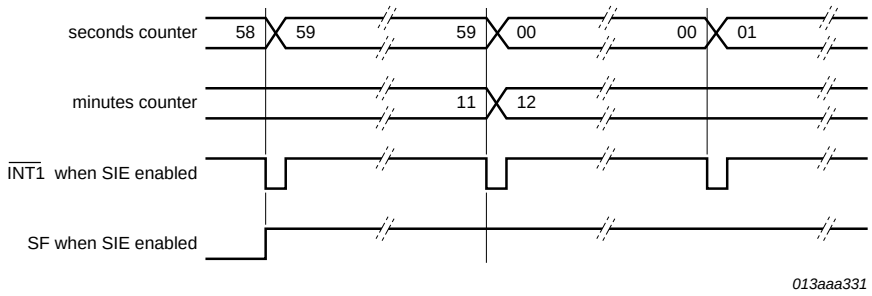
When the second interrupt timer is enabled (SIE = 1), then the timer sets the flag SF (register Control_2) every second (see Table 40). SF may only be cleared by using the interface. Instructions, how to clear a flag, is given in Section 8.7.5.

Table 40. Effect of bit SIE on $\overline{INT1}$ and bit SF

SIE	Result on $\overline{INT1}$	Result on SF
0	no interrupt generated	SF never set
1	an interrupt once per second	SF set when **seconds** counter increments

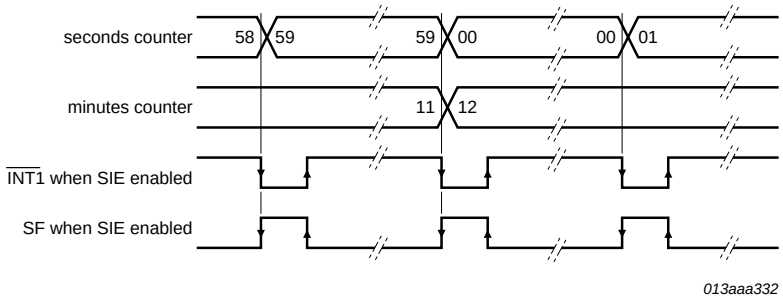
When SF is logic 1:

- If TAM (register Tmr_CLKOUT_ctrl) is logic 1 the interrupt is generated as a pulsed signal every second.
- If TAM is logic 0, the interrupt is a permanently active signal that remains, until SF is cleared.



In this example, bit TAM is set logic 1 and the SF flag is not cleared after an interrupt.

Fig 21. Example for second interrupt when TAM = 1



In this example, bit TAM is set logic 0 and the SF flag is cleared after an interrupt.

Fig 22. Example for second interrupt when TAM = 0

8.9.5 Timer interrupt pulse

The timer interrupt is generated as a pulsed signal when TAM or TBM are set logic 1. The pulse generator for the timer interrupt also uses an internal clock, but this time it is dependent on the selected source clock for the timer and on the timer register value n. Consequently, the width of the interrupt pulse varies; see Table 41 and Table 42.

Table 41. Interrupt low pulse width for timer A

Pulse mode, bit TAM set logic 1.

Source clock (Hz)	Interrupt pulse width	
	n = 1[1]	n > 1[1]
4096	122 μs	244 μs
64	7.812 ms	15.625 ms
1	15.625 ms	15.625 ms
$^1/_{60}$	15.625 ms	15.625 ms
$^1/_{3600}$	15.625 ms	15.625 ms

[1] n = loaded timer register value. Timer stops when n = 0.

For timer B, interrupt pulse width is programmable via bit TBW (register Tmr_B_freq_ctrl).

Table 42. Interrupt low pulse width for timer B

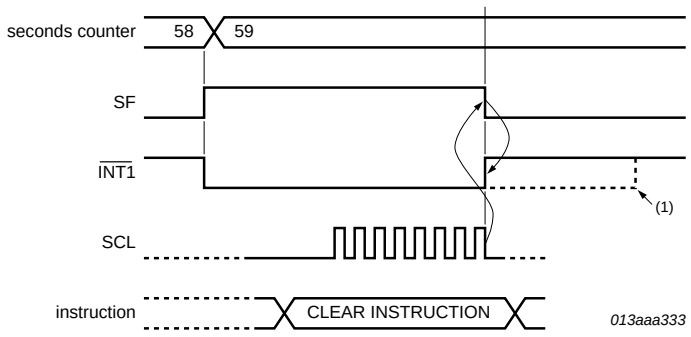
Pulse mode, bit TBM set logic 1.

Source clock (Hz).	Interrupt pulse width	
	n = 1[1]	n > 1[1]
4096	122 μs	244 μs
64	7.812 ms	see Table 36[2]
1	see Table 36	:
$^1/_{60}$	:	:
$^1/_{3600}$	:	:

[1] n = loaded timer register value. Timer stops when n = 0.

[2] If pulse period is shorter than the setting via bit TBW, the interrupt pulse width is set to 15.625 ms.

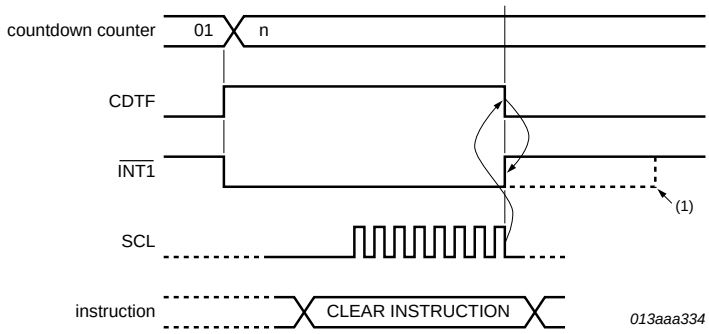
When flags like SF, CTAF, WTAF, and CTBF are cleared before the end of the interrupt pulse, then the interrupt pulse is shortened. This allows the source of a system interrupt to be cleared immediately when it is serviced, i.e. the system does not have to wait for the completion of the pulse before continuing; see Figure 23 and Figure 24. Instructions for clearing flags can be found in Section 8.7.5. Instructions for clearing the bit WTAF can be found in Section 8.9.2.1.



(1) Indicates normal duration of $\overline{INT1}$ pulse.

The timing shown for clearing bit SF is also valid for the non-pulsed interrupt mode, i.e. when TAM set logic 0, where the $\overline{INT1}$ pulse may be shortened by setting SIE logic 0.

Fig 23. Example of shortening the $\overline{INT1}$ pulse by clearing the SF flag



(1) Indicates normal duration of $\overline{INT1}$ pulse.

The timing shown for clearing CTAF is also valid for the non-pulsed interrupt mode, i.e. when TAM set logic 0, where the $\overline{INT1}$ pulse may be shortened by setting CTAIE logic 0.

Fig 24. Example of shortening the $\overline{INT1}$ pulse by clearing the CTAF flag

8.10 STOP bit function

The STOP bit function allows the accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler (F_2 to F_{14}) to be held in reset and thus no 1 Hz ticks will be generated. The time circuits can then be set and will not increment until the STOP bit is released (see Figure 25).

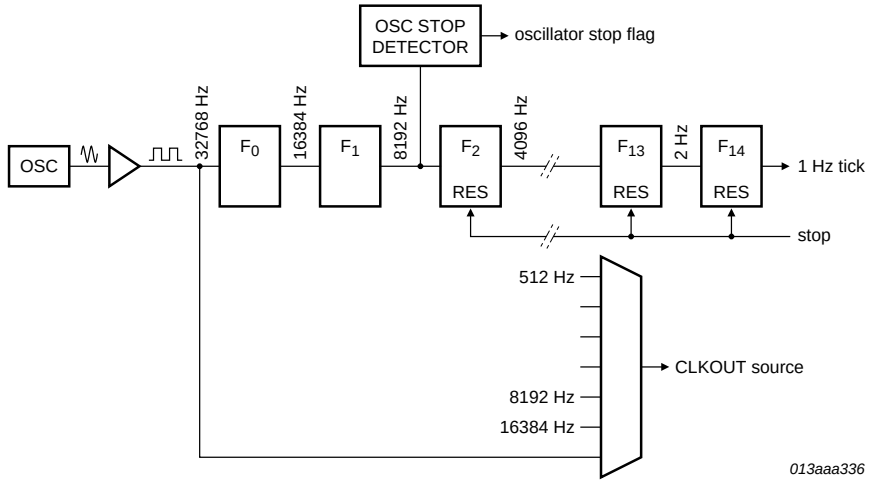


Fig 25. STOP bit

STOP will not affect the output of 32.768 kHz, 16.384 kHz or 8.192 kHz (see Section 8.9.1.1).

The lower two stages of the prescaler (F_0 and F_1) are not reset and because the I^2C-bus interface is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between 0 and one 8.192 kHz cycle (see Figure 26).

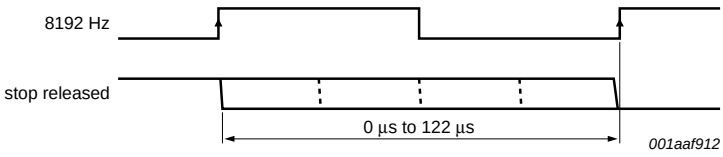
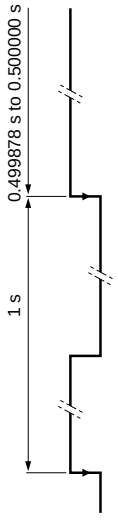


Fig 26. STOP bit release timing

The first increment of the time circuits is between 0.499878 s and 0.500000 s after stop is released. The uncertainty is caused by the prescaler bits F_0 and F_1 not being reset (see Table 43).

Table 43. First increment of time circuits after stop release

Bit	Prescaler bits[1]	1 Hz tick	Time	Comment
STOP	F_0F_1-F_2 to F_{14}		hh:mm:ss	
Clock is running normally				
0	01-0000111010100		12:45:12	prescaler counting normally
STOP is activated by user; F_0F_1 are not reset and values cannot be predicted externally				
1	XX-0000000000000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0000000000000		08:00:00	prescaler is reset; time circuits are frozen
STOP is released by user				
0	XX-0000000000000		08:00:00	prescaler is now running
0	XX-1000000000000		08:00:00	-
0	XX-0100000000000		08:00:00	-
0	XX-1100000000000		08:00:00	-
:	:		:	:
0	11-1111111111110		08:00:00	-
0	00-0000000000001		08:00:01	0 to 1 transition of F14 increments the time circuits
0	10-0000000000001		08:00:01	-
:	:		:	:
0	11-1111111111111		08:00:01	-
0	00-0000000000000		08:00:01	-
:	:		:	:
0	11-1111111111110		08:00:01	-
0	00-0000000000001		08:00:02	0 to 1 transition of F14 increments the time circuits



013aaa337

[1] F_0 is clocked at 32.768 kHz.

8.11 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines are connected to a positive supply via a pull-up resistor. Data transfer is initiated only when the bus is not busy.

8.11.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 27).

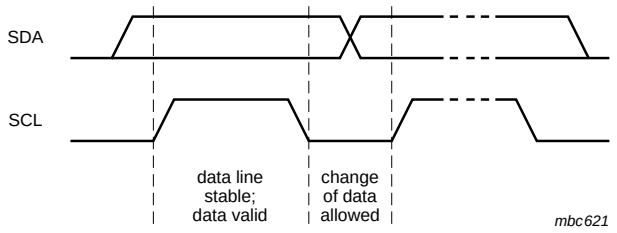


Fig 27. Bit transfer

8.11.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P) (see Figure 28).

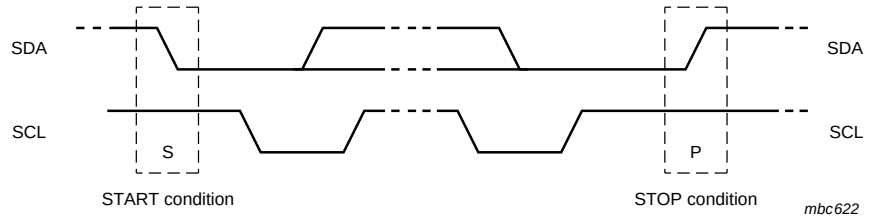


Fig 28. Definition of START and STOP conditions

For this device a repeated START is not allowed. Therefore, a STOP has to be released before the next START.

8.11.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices, which are controlled by the master, are the slaves.

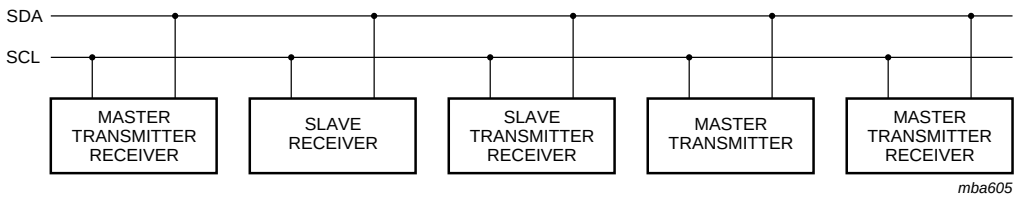


Fig 29. System configuration

The PCF8523 can act as a slave transmitter and a slave receiver.

8.11.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge cycle after the reception of each byte.
- Also a master receiver must generate an acknowledge cycle after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the related acknowledge clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge cycle on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is shown in Figure 30.

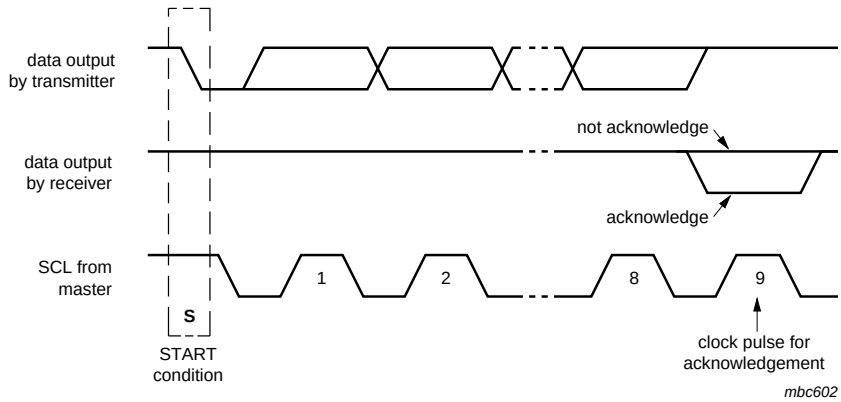


Fig 30. Acknowledgement on the I^2C-bus

8.11.5 I²C-bus protocol

One I²C-bus slave address (1101000) is reserved for the PCF8523. The entire I²C-bus slave address byte is shown in Table 44.

Table 44. I²C slave address byte

Bit	Slave address							
	7	6	5	4	3	2	1	0
	MSB							LSB
	1	1	0	1	0	0	0	R/$\overline{W}$

After a start condition, a valid hardware address has to be sent to a PCF8523 device.

The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the START condition (S), the STOP condition (P) and the acknowledge bit (A) refer to the I²C-bus characteristics. In the write mode, a data transfer is terminated by sending either a STOP condition or the START condition of the next data transfer.

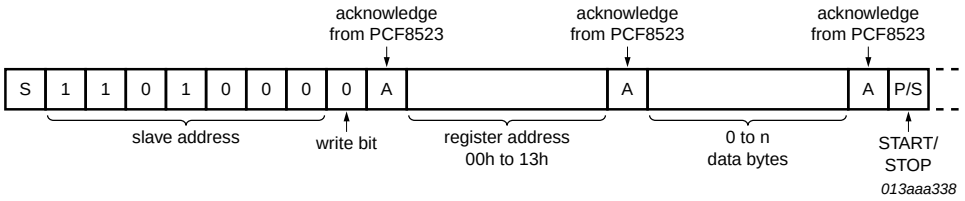


Fig 31. Bus protocol for write mode

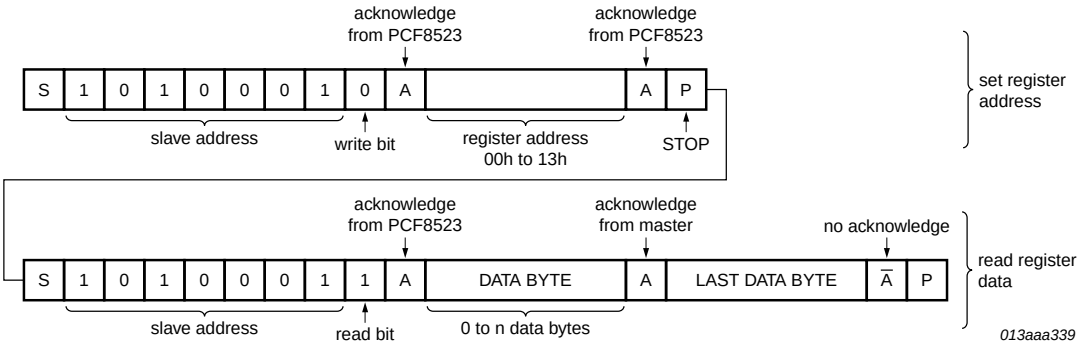


Fig 32. Bus protocol for read mode

9. Internal circuitry

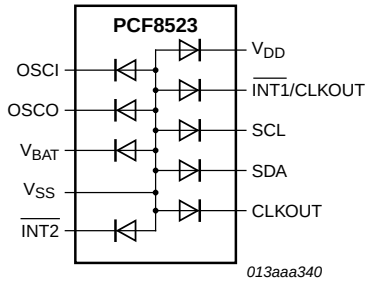


Fig 33. Device diode protection diagram of PCF8523

10. Limiting values

Table 45. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.5	V
I_{DD}	supply current			–50	+50	mA
V_I	input voltage			–0.5	+6.5	V
V_O	output voltage			–0.5	+6.5	V
I_I	input current			–10	+10	mA
I_O	output current			–10	+10	mA
V_{BAT}	battery supply voltage			–0.5	+6.5	V
P_{tot}	total power dissipation			-	300	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±2000	V
		CDM	[2]	-	±1500	V
I_{lu}	latch-up current		[3]	-	100	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+85	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 6 “JESD22-A114”.

[2] Pass level; Charged-Device Model (CDM), according to Ref. 7 “JESD22-C101”.

[3] Pass level; latch-up testing according to Ref. 8 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the NXP store and transport requirements (see Ref. 10 “NX3-00092”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long-term storage products, deviant conditions are described in that document.

11. Static characteristics

Table 46. Static characteristics

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 7 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage	I^2C-bus inactive; for clock data integrity					
		T_{amb} = −40 °C to +85 °C	[1]	1.2	-	5.5	V
		T_{amb} = +10 °C to +85 °C	[2]	1.0	-	5.5	V
		I^2C-bus active		1.6	-	5.5	V
		power management function active		1.8	-	5.5	V
SR	slew rate	of V_{DD}		-	-	±0.5	V/ms
V_{BAT}	battery supply voltage	power management function active		1.8	-	5.5	V
I_{DD}	supply current	I^2C-bus active; f_{SCL} = 1000 kHz		-	-	200	µA
		I^2C-bus inactive (f_{SCL} = 0 Hz); interrupts disabled					
		clock-out disabled; power management function disabled (PM[2:0] = 111)					
		T_{amb} = 25 °C; V_{DD} = 3.0 V	[3]	-	150	-	nA
		T_{amb} = −40 °C to +85 °C; V_{DD} = 2.0 V to 5.0 V	[3]	-	-	500	nA
		clock-out enabled at 32 kHz; power management function enabled (PM[2:0] = 000)					
		T_{amb} = 25 °C; V_{DD} = 3.0 V		-	1200	-	nA
		T_{amb} = −40 °C to +85 °C; V_{DD} = 2.0 V to 5.0 V		-	-	3600	nA
$I_{L(bat)}$	battery leakage current	V_{DD} active; V_{BAT} = 3.0 V		-	50	100	nA
Power management							
$V_{th(sw)bat}$	battery switch threshold voltage			2.28	2.5	2.7	V
Inputs							
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_I	input voltage			−0.5	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = V_{SS} or V_{DD}	[4]	-	0	-	nA
C_I	input capacitance		[5]	-	-	7	pF

Table 46. Static characteristics *…continued*

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 7 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Outputs							
V_O	output voltage	on pins $\overline{INT1}$/CLKOUT, CLKOUT, $\overline{INT2}$, SDA (refers to external pull-up voltage)		−0.5	-	5.5	V
V_{OL}	LOW-level output voltage			V_{SS}	-	0.4	V
I_{OL}	LOW-level output current	output sink current; on pins $\overline{INT1}$/CLKOUT, CLKOUT, $\overline{INT2}$; V_{OL} = 0.4 V; V_{DD} = 5 V	[6]	1.5	-	-	mA
		on pin SDA V_{OL} = 0.4 V; V_{DD} = 3.0 V	[6]	20	-	-	mA
I_{LO}	output leakage current	V_O = V_{SS} or V_{DD}	[4]	-	0	-	nA
$C_{L(itg)}$	integrated load capacitance	on pins OSCO, OSCI	[7][8]				
		C_L = 7 pF		3.3	7	14	pF
		C_L = 12.5 pF		6	12.5	25	pF
R_S	series resistance		[9]	-	-	100	kΩ

[1] For reliable oscillator start at power-up: V_{DD} = $V_{DD(min)}$ + 0.3 V.

[2] For reliable oscillator start at power-up: V_{DD} = $V_{DD(min)}$ + 0.5 V.

[3] Timer source clock = $^1/_{3600}$ Hz, level of pins SCL and SDA is V_{DD} or V_{SS}.

[4] In case of an ESD event, the value may increase slightly.

[5] Implicit by design.

[6] Tested on sample basis.

[7] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series: $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$.

[8] Tested at 25 °C.

[9] Crystal characteristic specification.

12. Dynamic characteristics

Table 47. I²C-bus interface timing

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of V_{SS} to V_{DD} (see Figure 34).

Symbol	Parameter	Conditions	Standard mode		Fast mode (FM)		Fast mode plus (Fm+)[1]		Unit
			Min	Max	Min	Max	Min	Max	
Pin SCL									
f_{SCL}	SCL clock frequency	[2]	-	100	-	400	-	1000	kHz
t_{LOW}	LOW period of the SCL clock	-	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	-	4.0	-	0.6	-	0.26	-	µs
Pin SDA									
$t_{SU;DAT}$	data set-up time	-	250	-	100	-	50	-	ns
$t_{HD;DAT}$	data hold time	-	0	-	0	-	0	-	ns
Pins SCL and SDA									
t_{BUF}	bus free time between a STOP and START condition	-	4.7	-	1.3	-	0.5	-	µs
$t_{SU;STO}$	set-up time for STOP condition	-	4.0	-	0.6	-	0.26	-	µs
$t_{HD;STA}$	hold time (repeated) START condition	-	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition	-	4.7	-	0.6	-	0.26	-	µs
t_r	rise time of both SDA and SCL signals	[3][4]	-	1000	$20 + 0.1C_b$	300	-	120	ns
t_f	fall time of both SDA and SCL signals	[3][4]	-	300	$20 + 0.1C_b$	300	-	120	ns
C_b	capacitive load for each bus line		-	400	-	400	-	550	pF
$t_{VD;ACK}$	data valid acknowledge time	[5]	-	3.45	-	0.9	-	0.45	µs
$t_{VD;DAT}$	data valid time	[6]	-	3.45	-	0.9	-	0.45	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[7]	-	50	-	50	-	50	ns

[1] Fast mode plus guaranteed at $3.0\ V < V_{DD} < 5.5\ V$.

[2] The minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus time-out feature must be disabled for DC operation.

[3] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4] The maximum t_f for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, t_f is 250 ns. This allows series protection resistors to be connected between the SDA pin, the SCL pin and the SDA/SCL bus lines without exceeding the maximum t_f.

[5] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output LOW.

[6] $t_{VD;DAT}$ = minimum time for valid SDA output following SCL LOW.

[7] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

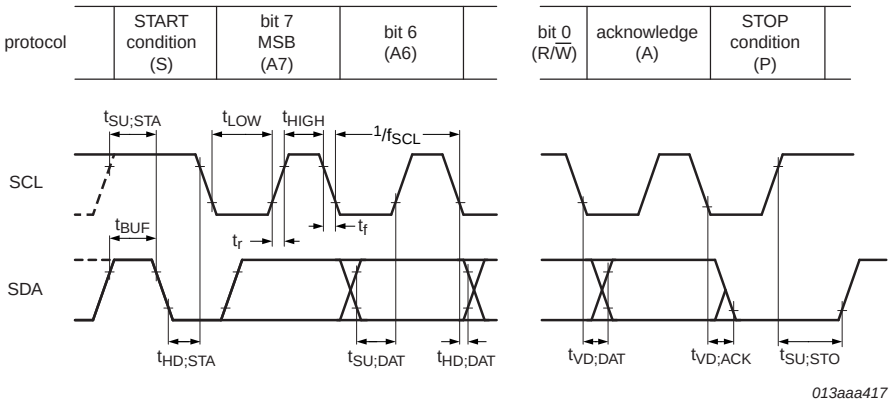
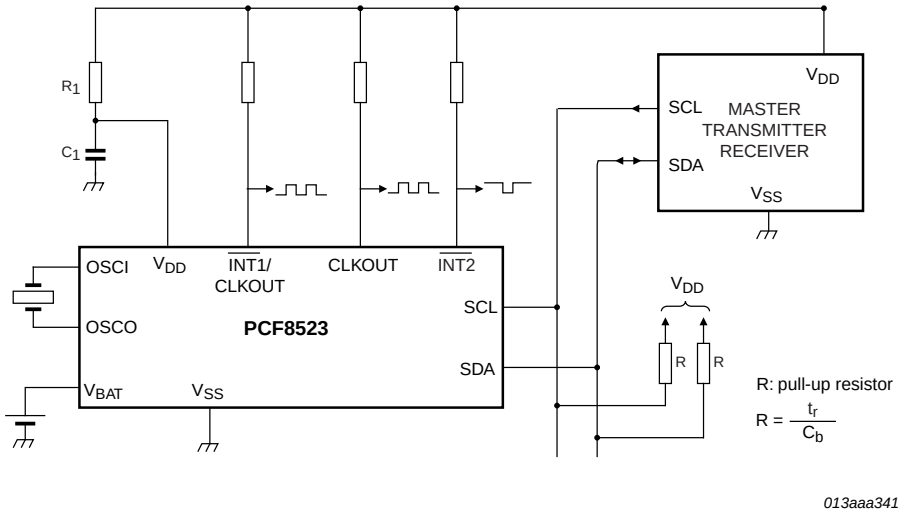


Fig 34. I²C-bus timing diagram; rise and fall times refer to 30 % and 70 %

13. Application information

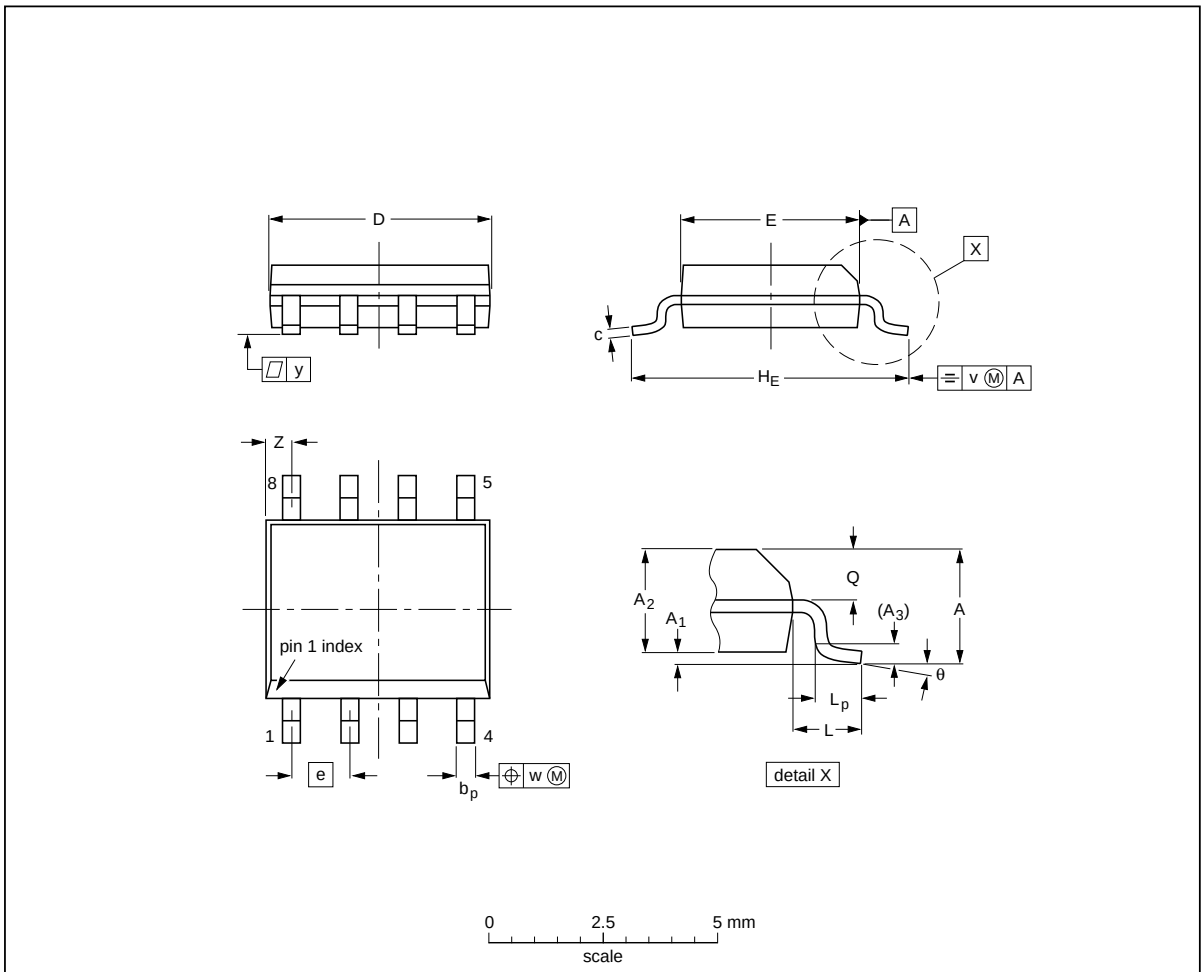


R_1 and C_1 are recommended to limit the Slew Rate (SR, see Table 46) of V_{DD}. If V_{DD} drops to fast, the internal supply switch to the battery is not guaranteed.

Fig 35. Application diagram

14. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

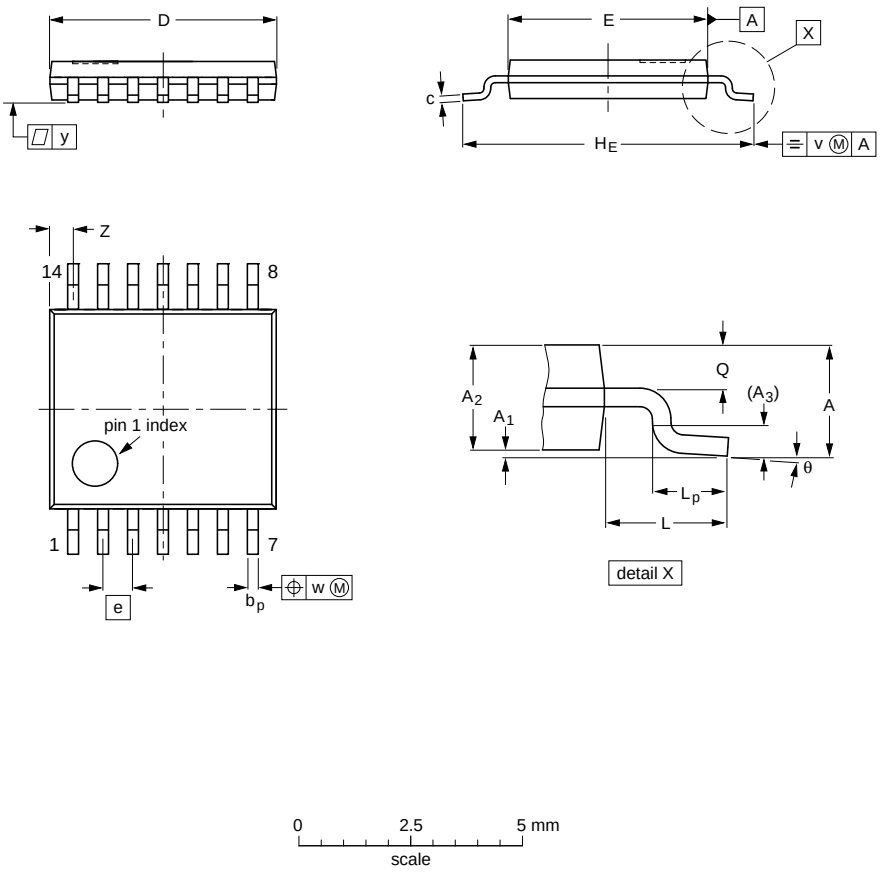
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 36. Package outline SOT96-1 (SO8) of PCF8523T

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

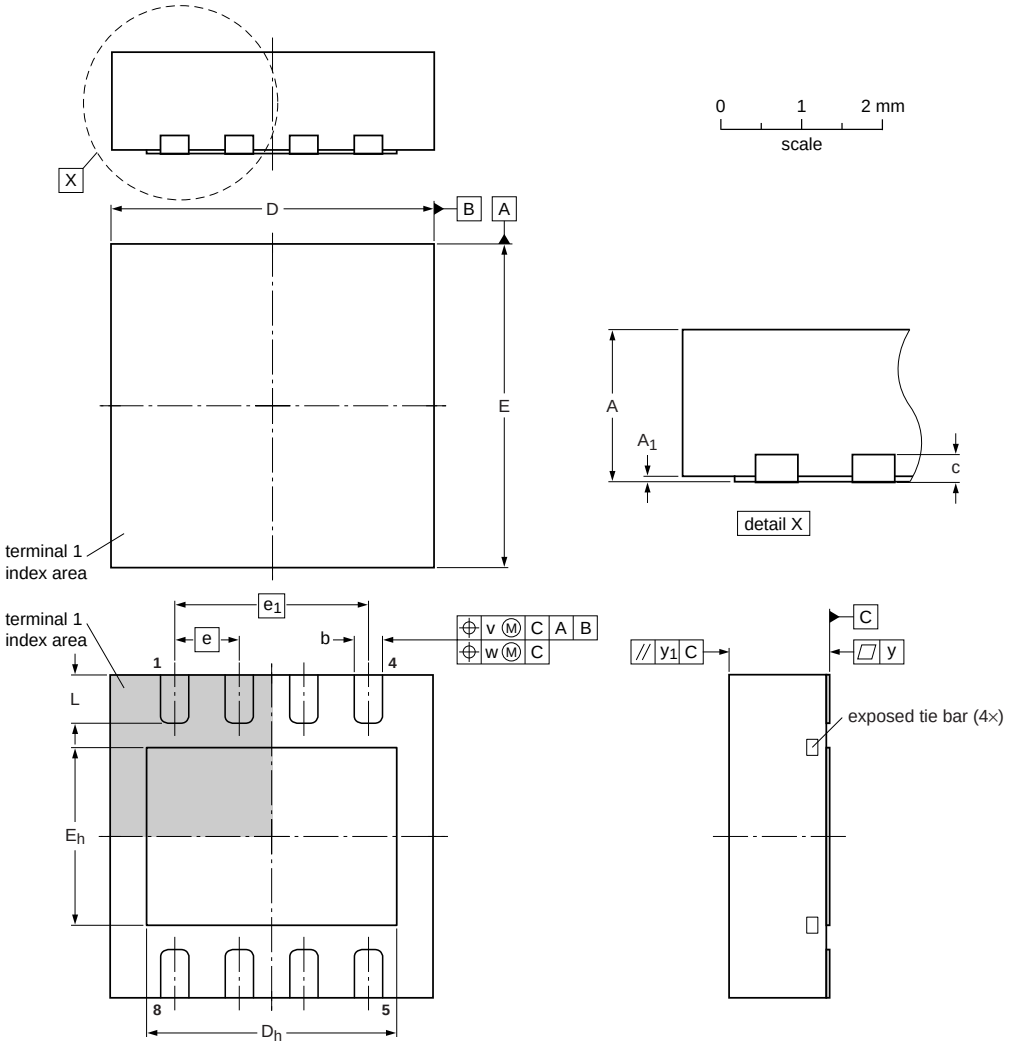
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 37. Package outline SOT402-1 (TSSOP14) of PCF8523TS

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 4 x 4 x 0.85 mm **SOT909-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.4 0.3	0.2	4.1 3.9	3.25 2.95	4.1 3.9	2.35 2.05	0.8	2.4	0.65 0.40	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT909-1		MO-229				~~05-09-26~~ 05-09-28

Fig 38. Package outline SOT909-1 (HVSON8) of PCF8523TK

15. Bare die outline

Bare die; 12 bumps (6-6) **PCF8523U**

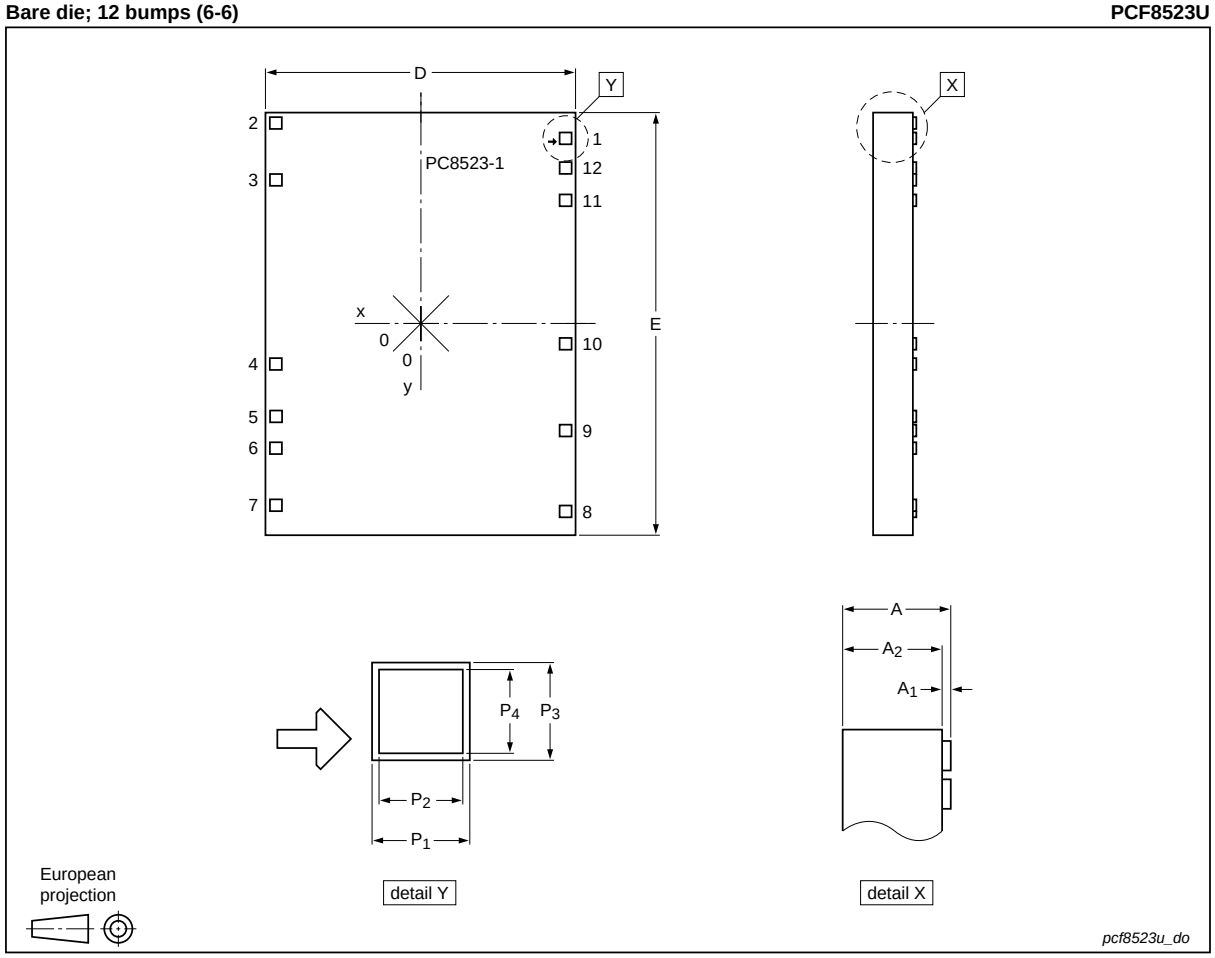


Fig 39. Bare die outline of PCF8523U (for dimensions see Table 48)

Table 48. Dimensions of PCF8523U

Original dimensions are in mm.

Unit (mm)	A	A_1	A_2	D[1]	E[1]	P_1[2]	P_2[3]	P_3[2]	P_4[3]	bump pitch
max	-	0.018	-	-	-	-	0.059	-	0.059	-
nom	0.22	0.015	0.2	1.58	2.15	0.065	0.056	0.065	0.056	-
min	-	0.012	-	-	-	-	0.053	-	0.053	0.149

[1] Dimension includes saw lane.

[2] P_1 and P_3: pad size.

[3] P_2 and P_4: bump size.

Table 49. Bump locations

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 39.

Symbol	Bump	Coordinates (μm)	
		X	Y
V_{DD}	1	714.4	911.7
OSCI	2	−714.4	988.3
OSCO	3	−714.4	707.3
V_{BAT}	4	−714.4	−199.3
V_{SS}	5	−714.4	−459.1
n.c.	6	−714.4	−616.7
$\overline{INT2}$	7	−714.4	−895.4
CLKOUT	8	714.4	−922.0
SDA	9	714.4	−528.8
SCL	10	714.4	−101.1
n.c.	11	714.4	607.6
$\overline{INT1}$/CLKOUT	12	714.4	763.2

Table 50. Alignment mark dimension and location

Coordinates	X	Y
Location[1]	631.3 μm	891.7 μm
Dimension[2]	44.25 μm	36.5 μm

[1] The x/y coordinates of the alignment mark location represent the position of the REF point (see Figure 40) with respect to the center (x/y = 0) of the chip; see Figure 39.

[2] The x/y values of the dimensions represent the extensions of the alignment mark in direction of the coordinate axis (see Figure 40).

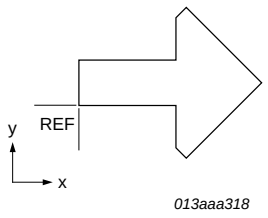
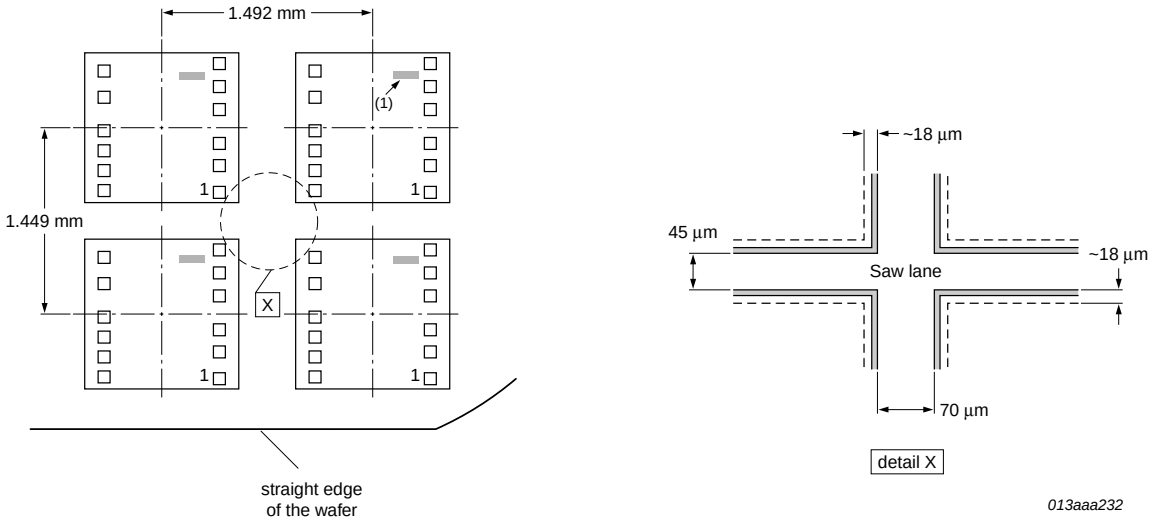


Fig 40. Alignment mark

16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

17. Packing information



(1) Die marking code.

Seal ring plus gap to active circuit ~18 µm. Wafer thickness 200 µm.

PCF8523U: bad die are marked in wafer mapping.

Fig 41. PCF8523U wafer information

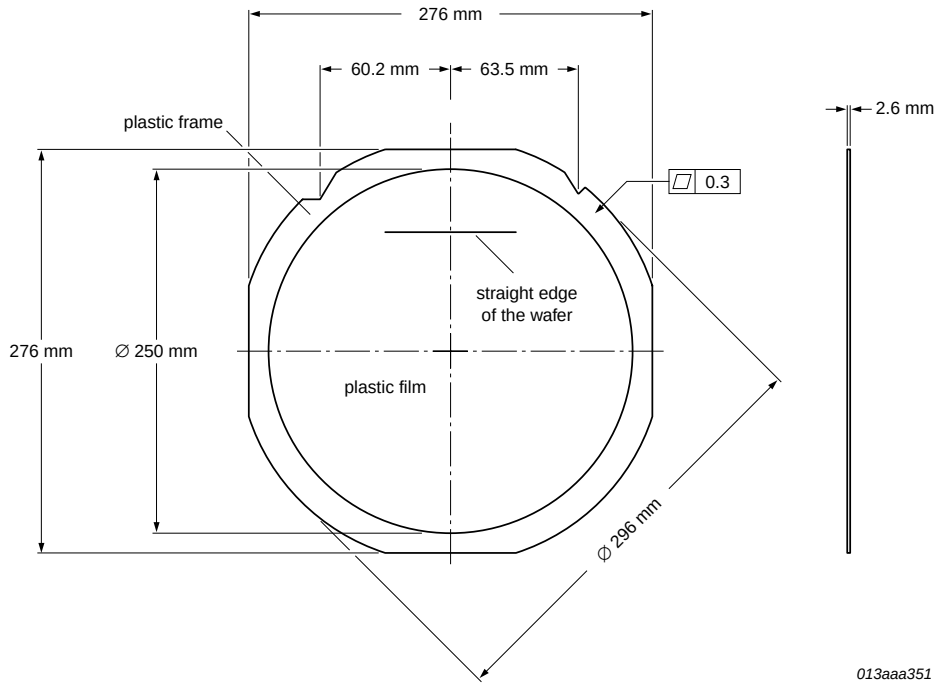


Fig 42. Film Frame Carrier (FFC) (for PCF8523U)

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 43) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 51 and 52

Table 51. SnPb eutectic process (from J-STD-020C)

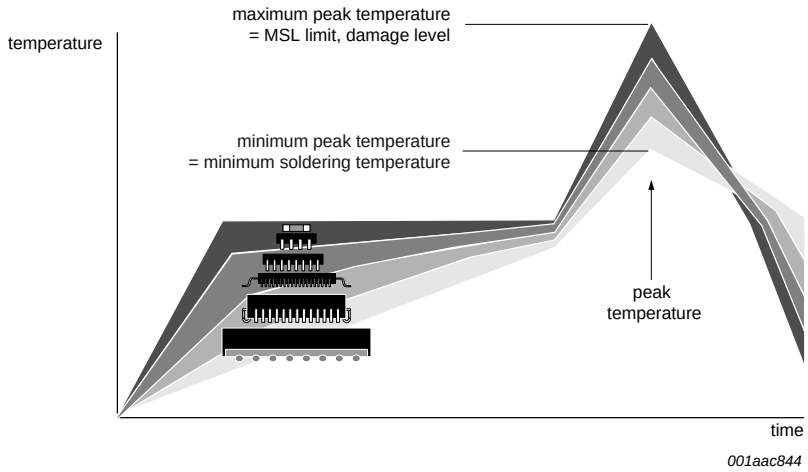
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 52. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 43.



MSL: Moisture Sensitivity Level

Fig 43. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 53. Abbreviations

Acronym	Description
AM	Ante Meridiem
BCD	Binary Coded Decimal
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
FFC	Film Frame Carrier
HBM	Human Body Model
I^2C	Inter-Integrated Circuit bus
IC	Integrated Circuit
LSB	Least Significant Bit
MCU	Microcontroller Unit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
PM	Post Meridiem
POR	Power-On Reset
PPM	Parts Per Million
RTC	Real-Time Clock
SCL	Serial CLock line
SDA	Serial DAta line
SMD	Surface Mount Device
SR	Slew Rate

20. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10706 —** Handling bare die

[3] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[4] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[5] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[6] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **NX3-00092 —** NXP store and transport requirements

[11] **SNV-FA-01-02 —** Marking Formats Integrated Circuits

[12] **UM10204 —** I^2C-bus specification and user manual

21. Revision history

Table 54. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8523 v.3	20110330	Product data sheet	-	PCF8523 v.2
Modifications:	• Enhanced supply voltage specification in Table 46			
PCF8523 v.2	20110127	Product data sheet	-	PCF8523 v.1
Modifications:	• Adjusted test criteria in Table 46 • Enhanced specification of battery switch threshold voltage in Table 46			
PCF8523 v.1	20101123	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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24. Contents

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