PCF2128

Integrated RTC / TCXO / Crystal

Rev. 00.03 — 4 June 2007   **Preliminary [short] data sheet**

1. General description

The PCF2128 is a ready to run CMOS real time clock/calendar with an integrated temperature compensated crystal oscillator (TCXO). In timekeeping applications the high accuracy of the PCF2128 allows it to be used as a replacement for costly and higher powered long wave receivers or GPS receivers. A programmable battery switch-over circuit enables an uninterruptible power supply and consequently continuous timekeeping. The PCF2128 additionally features 512 bytes of general purpose RAM, a programmable watchdog, a time stamp facility and a voltage monitoring facility. Programming is possible using either an SPI or an I^{2}C-bus interface.

2. Features

- Integration of a 32.768 kHz quartz crystal in the same package as the RTC
- temperature compensated crystal oscillator (TCXO) with integrated capacitors.
- accuracy:
  typically 3 ppm from −20 °C to +70 °C,
  typically 5 ppm from −40 °C to +85 °C
- provides year, month, day, weekday, hours, minutes and seconds
- programmable alarm function with interrupt capability
- programmable countdown timer with interrupt capability
- programmable watchdog timer with interrupt and reset capability
- timestamp function with interrupt capability
- battery backup input pin and switch-over circuitry
- extra power fail detection with input and output pins
- battery low detection
- battery backed output voltage pin

- 512 bytes of general purpose static RAM
- 1 second or 1 minute interrupt output
- oscillator stop detection
- two line bi-directional 1 MHz fast mode plus I^{2}C interface
- timestamp input
- power-on reset
- 3 line SPI interface with separate data input and output (maximum speed 6.5 Mbits/s)
- programmable square wave output pin
- I^{2}C-bus slave address: read A3H and write A2H
- clock operating voltage: <tbd> to 5.5 V
- low backup current; typical 0.95 μA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- selectable I^{2}C and SPI interface

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3. Quick reference data

Table 1. Quick reference data

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 ℃ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		1.8	-	5.5	V
I_{DD}	supply current	interface active				
		f_{SCL} = 6.5 MHz	-	-	800	µA
		f_{SCL} = 1.0 MHz	-	-	200	µA
		interface inactive (f_{SCL} = 0 kHz) timekeeping and power management configuration, CLKOUT disabled;				
		V_{DD} = 5.0 V	-	2700	-	nA
		V_{DD} = 3.0 V	-	2100	-	nA
		interface inactive (f_{SCL} = 0 kHz) timekeeping configuration; T_{amb} = +25 °C				
		V_{DD} = 5.0 V	-	850	-	nA
		V_{DD} = 3.0 V	-	450	-	nA
f_{SCL}	SCL clock frequency		0	-	6.5	MHz
$\Delta f / f$	frequency stability (f_o = 32.768 kHz)	T_{amb} = −40 to +85 °C	-	±5	-	ppm
		T_{amb} = −20 to +70 °C	-	±3	±5	ppm
T_{amb}	ambient temperature	operating	−40	-	+85	°C
T_{stg}	storage temperature		−65	-	+150	°C

4. Ordering information

Table 2: Ordering information

Type number	Topside mark	Package			
		Name	Description		Version
PCF2128T / 1	PCF2128T	SO20	plastic thin shrink small outline package; 20 leads; body width 4.4mm		SOT163-1

PCF2128_SDS_0

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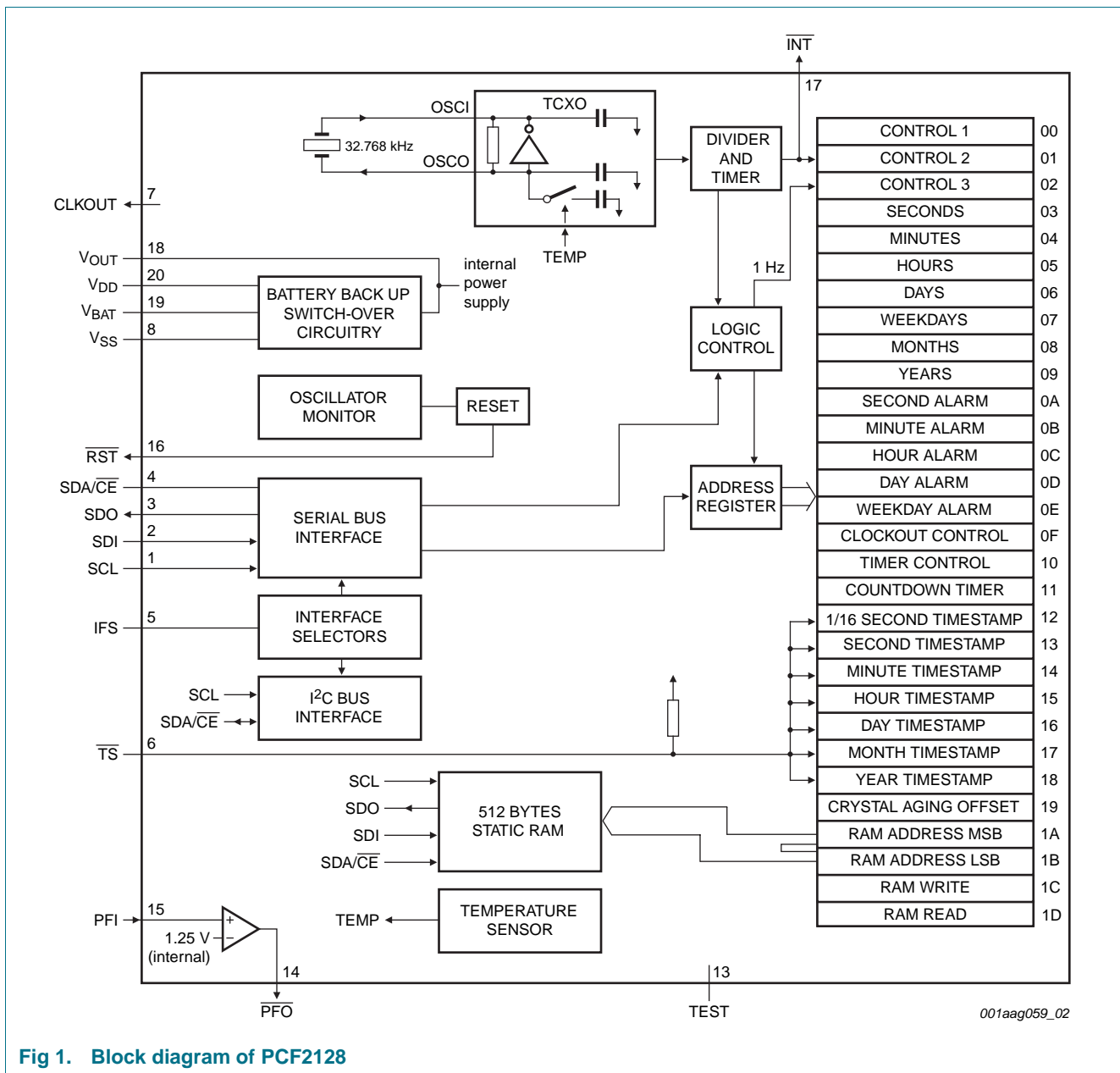
5. Block diagram

Fig 1.   Block diagram of PCF2128

6. Pinning information

6.1 Pinning

Fig 2. Pin configuration SO20

Fig 3. SO20 (3d)
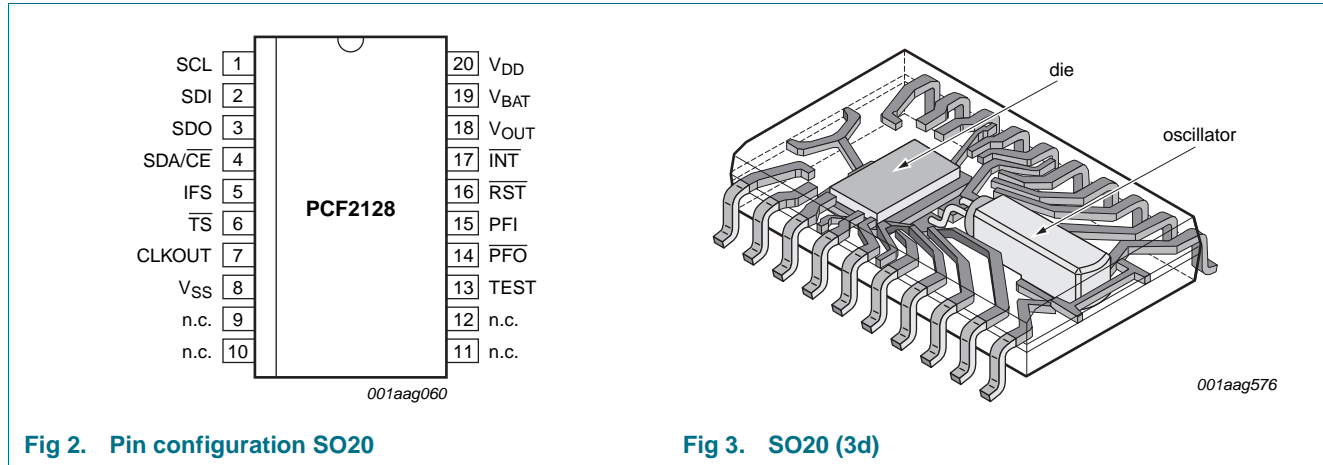
Table 3:   Pin description PCF2128

Symbol	Pin	Description	Symbol	Pin	Description
SCL	1	combined serial clock input for both I²C and SPI interface. May float when $\overline{CE}$ inactive.	V_{DD}	20	positive supply voltage
SDI	2	serial data input for SPI interface. May float when $\overline{CE}$ inactive.	V_{BAT}	19	battery backup supply voltage
SDO	3	serial data output for SPI interface, push-pull	V_{OUT}	18	battery backed output voltage
SDA / $\overline{CE}$	4	combined serial data input / output for the I²C interface and chip enable input (active LOW) for the SPI interface.	$\overline{INT}$	17	interrupt output (open-drain; active LOW)
IFS	5	interface selector input • connect to ground to select the SPI interface • connect to V_{OUT} (pin 18) to select the I²C interface	$\overline{RST}$	16	reset output (open drain; active LOW)
$\overline{TS}$	6	timestamp input (active LOW) with 200 kΩ internal pull-up resistor	PFI	15	power fail input
CLKOUT	7	clock output (open drain)	$\overline{PFO}$	14	power fail output (open drain; active LOW)
V_{SS}	8	ground	TEST	13	Do not connect and do not use as feed through.
nc	9	Do not connect and do not use as feed through.	nc	12	Do not connect and do not use as feed through.
nc	10	Do not connect and do not use as feed through.	nc	11	Do not connect and do not use as feed through.

7. Limiting values

Table 4: **Limiting values** *In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+6.5	V
V_{BAT}	backup battery supply voltage		−0.5	+6.5	V
I_{DD}	supply current		−50	+50	mA
V_I	input voltage		−0.5	+6.5	V
V_O	output voltage		−0.5	+6.5	V
I_I	input current		−10	+10	mA
I_O	output current		−10	+10	mA
P_{tot}	total power dissipation		-	300	mW
T_{amb}	ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C

7.1 ESD values

- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 2000 V CDM per JESD22-C101.
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA.

8. Application information

- The PCF2128 is a ready to run real time clock; no external quartz is required.
- You can set different configurations in your application depending on the PCF2128 functions you want to use.
- The integration of the quartz crystal in the same package as the RTC has the following advantages:
  - elimination of crystal procurement issues
  - elimination of RTC frequency tuning
  - no more crystal PCB layout issues.
- You can select the SPI or I^{2}C-bus interface using the IFS pin.
- By connecting a battery to V_{BAT} an uninterruptible power supply is guaranteed.
- You can use the battery backed voltage V_{OUT} to supply an external RAM to retain RAM data in battery backup mode.
- You can connect PFI through an external voltage divider to V_{DD} to allow extra power fail detection. If not used, connect PFI to V_{SS}.
- You can connect the timestamp input pin $\overline{TS}$ to a push button for tamper detection.

8.1 Application example

8.1.1 Timekeeping, power management, CLKOUT, timestamp and interface active

PCF2128 used for timekeeping, power management, CLKOUT and timestamp functions (see Figure 4). The interface is active. V_{out} supplies an external chip (e.g. SRAM).
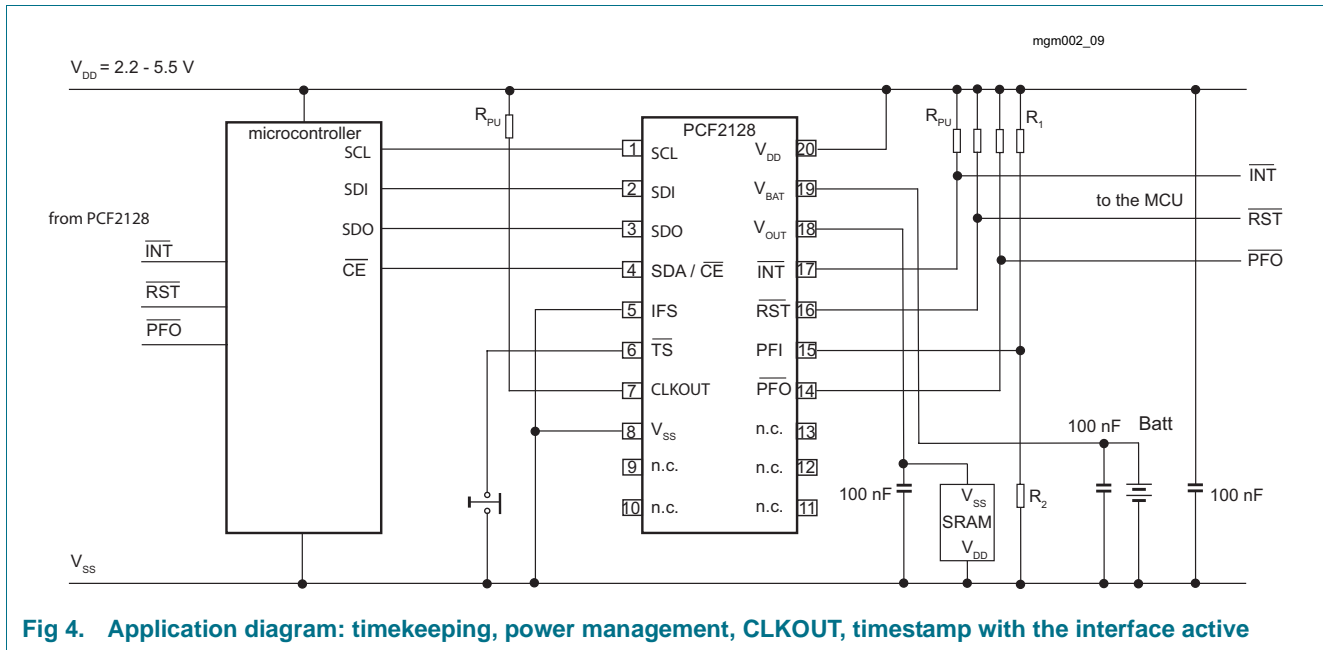

Fig 4. Application diagram: timekeeping, power management, CLKOUT, timestamp with the interface active

9. Revision history

Table 5.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF2128__SDS_00.03	<tbd>	Preliminary		PCF2128__SDS_00.02
Modifications:	• Added Figure 3.			
PCF2128__SDS_00.02	20070604	Preliminary		PCF2128__SDS_00.01
Modifications:	• Datasheet text ammended. Section 8.1 corrected.			
PCF2128__SDS_00.01	20070509	Preliminary short data sheet		-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Notes

12. Contents

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