PCF2123

SPI Real time clock/calendar

Rev. 01 — 19 November 2008 Product data sheet

1. General description

The PCF2123 is a CMOS real time clock and calendar optimized for low power applications. Data is transferred serially via a Serial Peripheral Interface bus (SPI-bus) with a maximum data rate of 6.25 Mbit/s. An alarm and timer function is also available providing the possibility to generate a wake-up signal on an interrupt pin. An offset register allows fine tuning of the clock.

2. Features

- Real time clock provides year, month, day, weekday, hours, minutes and seconds based on a 32.768 kHz quartz crystal
- Low backup current while running: typical 100 nA at V_{DD} = 2.0 V and T_{amb} = 25 °C
- Resolution: seconds to years
- Watchdog functionality
- Freely programmable timer and alarm with interrupt capability
- Clock operating voltage: 1.1 V to 5.5 V
- 3 line SPI-bus with separate combinable data input and output
- Serial interface at V_{DD} = 1.6 V to 5.5 V
- 1 second or 1 minute interrupt output
- Integrated oscillator load capacitors for C_L = 7 pF
- Internal power-on reset
- Open-drain interrupt and clock output pins
- Programmable offset register for frequency adjustment

3. Applications

- Time keeping application
- Battery powered devices
- Metering
- High duration timers
- Daily alarms
- Low standby power applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2123TS	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
PCF2123BS	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCF2123U	PCF2123U/10	wire bond die; 12 bonding pads; 1.492 × 1.449 × 0.20 mm[1]	PCF2123U/10

[1] Sawn wafer on Film Frame Carrier (FFC); 200 μm thickness.

5. Marking

Table 2. Marking codes

Type number	Marking code
PCF2123TS	PCF2123
PCF2123BS	123
PCF2123U	PC2123-1

6. Block diagram

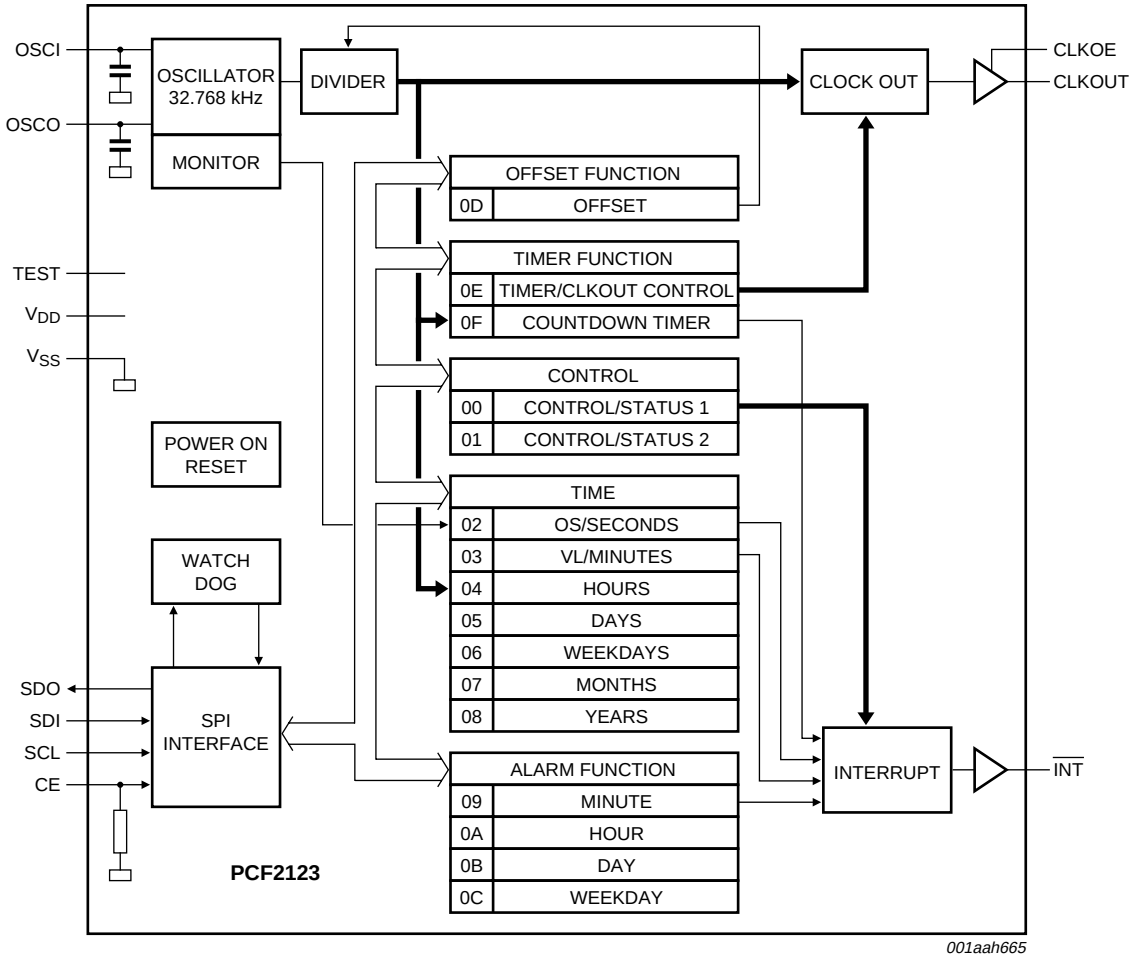
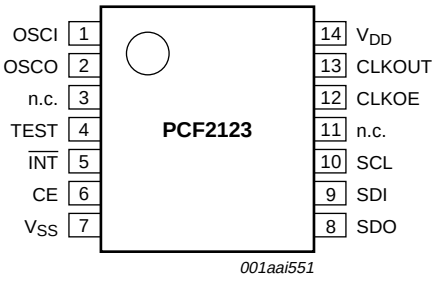


Fig 1. Block diagram of PCF2123

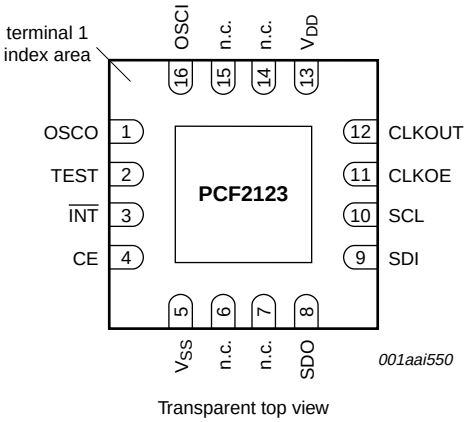
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 29.

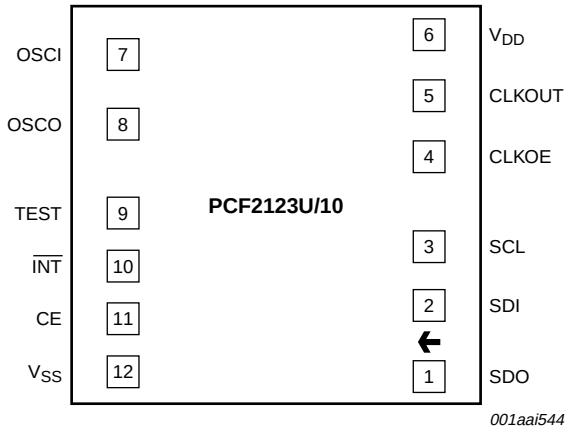
Fig 2. Pinning diagram of PCF2123TS (TSSOP14)



Transparent top view

For mechanical details, see Figure 30.

Fig 3. Pinning diagram of PCF2123BS (HVQFN16)



Top view. For mechanical details, see Figure 31 and Figure 33.

Fig 4. Pinning diagram of PCF2123U (bare die)

7.2 Pin description

Table 3. Pin description

Symbol	Pin			Description
	TSSOP14	HVQFN16	PCF2123U/10	
OSCI	1	16	7	oscillator input; high-impedance node; minimize wire length between quartz and package
OSCO	2	1	8	oscillator output; high-impedance node; minimize wire length between quartz and package
n.c.	3, 11	6, 7, 14, 15	-	do not connect and do not use as feed through; connect to V_{DD} if floating pins are not allowed
TEST	4	2	9	test pin; not user accessible; connect to V_{SS} or leave floating (internally pulled down)
$\overline{INT}$	5	3	10	interrupt output (open-drain; active LOW)
CE	6	4	11	chip enable input (active HIGH) with internal pull down
V_{SS}	7	5[1]	12[2]	ground
SDO	8	8	1	serial data output, push-pull; high-impedance when not driving; can be connected to SDI for single wire data line
SDI	9	9	2	serial data input; may float when CE is inactive
SCL	10	10	3	serial clock input; may float when CE is inactive
CLKOE	12	11	4	CLKOUT enable or disable pin; enable is active HIGH
CLKOUT	13	12	5	clock output (open-drain)
V_{DD}	14	13	6	supply voltage; positive or negative steps in V_{DD} may affect oscillator performance; recommend 10 nF decoupling close to device (see Figure 28)

[1] The die paddle (exposed pad) is wired to V_{SS} but should not be electrically connected.

[2] The substrate (rear side of the die) is wired to V_{SS} but should not be electrically connected.

8. Device protection diagram

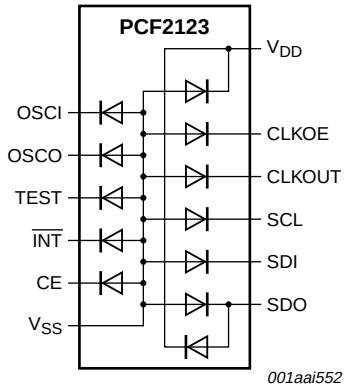


Fig 5. Device diode protection diagram of PCF2123

9. Functional description

The PCF2123 contains sixteen 8-bit registers with an auto-incrementing address counter, an on-chip 32.768 kHz oscillator with two integrated load capacitors, a frequency divider which provides the source clock for the Real Time Clock (RTC), a programmable clock output, and a 6.25 Mbit/s SPI-bus. An offset register allows fine tuning of the clock.

All sixteen registers are designed as addressable 8-bit parallel registers although not all bits are implemented.

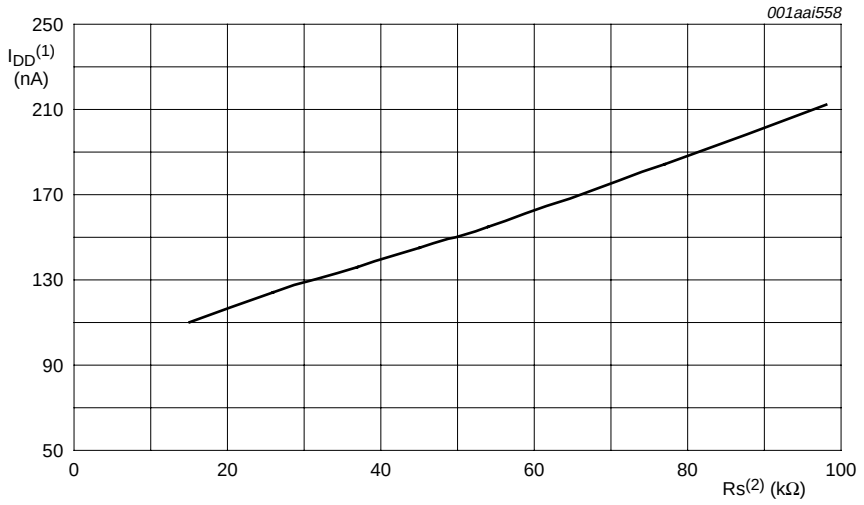
- The first two registers (memory address 00h and 01h) are used as control registers.
- The memory addresses 02h through 08h are used as counters for the clock function (seconds up to years). The Seconds, Minutes, Hours, Days, Weekdays, Months and Years registers are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented.
- Addresses 09h through 0Ch define the alarm condition.
- Address 0Dh defines the offset calibration.
- Address 0Eh defines the clock out and timer mode.
- Address registers 0Eh and 0Fh are used for the countdown timer function. The countdown timer has four selectable source clocks allowing for countdown periods in the range from 244 µs up to four hours. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. These are defined in register Control_2 (01h).

9.1 Low power operation

Minimum power operation will be achieved by reducing the number and frequency of switching signals inside the IC, i.e. low frequency timer clocks and a low frequency CLKOUT will result in lower operating power. A second prime consideration is the series resistance R_s of the quartz used.

9.1.1 Power consumption with respect to quartz series resistance

The series resistance acts as a loss element. Low R_S will reduce current consumption further.



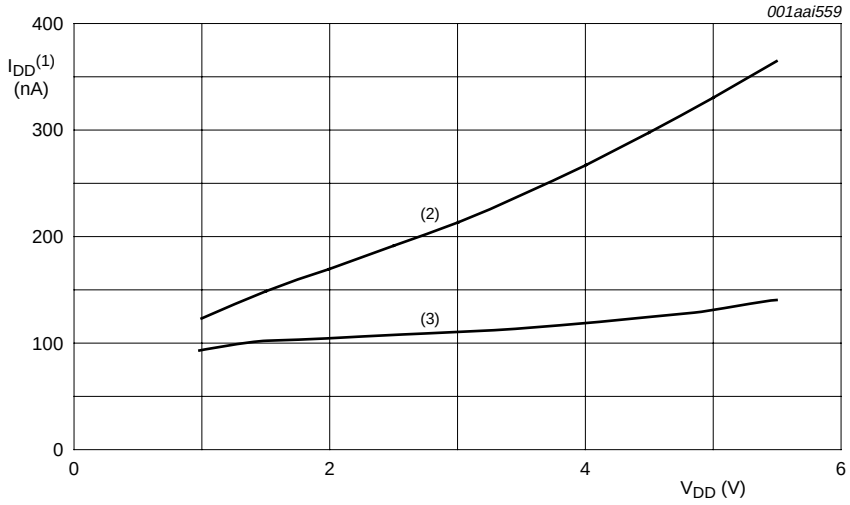
Configuration: CLKOUT disabled, V_{DD} = 3 V, timer clock set to $^1/_{60}$ Hz.

(1) I_{DD} (nA) minimum power mode.

Fig 6. I_{DD} with respect to quartz R_S

9.1.2 Power consumptions with respect to timer mode

Four source clocks are possible for the timer. The 4.096 kHz source clock will add the greatest part to the power consumption. The selection of 64 Hz, 1 Hz or $^{1}/_{60}$ Hz will be almost indistinguishable and add very little.



Configuration: CLKOUT disabled, quartz R_S = 15 kΩ.

(1) I_{DD} (nA) minimum power mode.

(2) Timer clock = 4 kHz.

(3) Timer clock = 64 Hz, 1 Hz, $^{1}/_{60}$ Hz.

Fig 7. I_{DD} with respect to timer clock selection

9.2 Register overview

16 registers are available. The time registers are encoded in the binary coded decimal format (BCD) to simplify application use. Other registers are either bit-wise or standard binary.

Table 4. Registers overview

Bit positions labelled as - are not implemented and will return a 0 when read. Bit positions labelled with 0 should always be written with logic 0[1].

Address	Register name	Bit							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	Control_1	EXT_TEST	0	STOP	SR	0	12_24	CIE	0
01h	Control_2	MI	SI	MSF	TI_TP	AF	TF	AIE	TIE
02h	Seconds	OS	SECONDS (0 to 59)						
03h	Minutes	-	MINUTES (0 to 59)						
04h	Hours	-	-	AMPM	HOURS (1 to 12) in 12 h mode				
				HOURS (0 to 23) in 24 h mode					
05h	Days	-	-	DAYS (1 to 31)					
06h	Weekdays	-	-	-	-	-	WEEKDAYS		
07h	Months	-	-	-	MONTHS (1 to 12)				
08h	Years	YEARS (0 to 99)							
09h	Minute_alarm	AEN_M	MINUTE_ALARM (0 to 59)						
0Ah	Hour_alarm	AEN_H	-	AMPM	HOUR_ALARM (1 to 12) in 12 h mode				
				HOUR_ALARM (0 to 23) in 24 h mode					
0Bh	Day_alarm	AEN_D	-	DAY_ALARM (1 to 31)					
0Ch	Weekday_alarm	AEN_W	-	-	-	-	WEEKDAY_ALARM		
0Dh	Offset_register	MODE	OFFSET						
0Eh	Timer_clkout	-	COF2	COF1	COF0	TE	-	CTD1	CTD0
0Fh	Countdown_timer	COUNTDOWN_TIMER							

[1] Except in the case of software reset, see Section 9.5

9.3 Control registers

9.3.1 Register Control_1

Table 5. Register Control_1 (address 00h) bits description

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0	normal mode	Section 9.12
		1	external clock test mode	
6	-	-	unused	-
5	STOP	0	the RTC source clock runs	Section 9.13
		1	the RTC clock is stopped; RTC divider chain flip-flops are asynchronously set to logic 0; CLKOUT at 32.768 kHz, 16.384 kHz or 8.192 kHz is still available	
4	SR	0	no software reset	Section 9.5
		1	initiate software reset[1]; this register will always return a 0 when read	
3	-	-	unused	-
2	12_24	0	24 hour mode is selected	-
		1	12 hour mode is selected	
1	CIE	0	no correction interrupt generated	Section 9.11
		1	interrupt pulses will be generated at every correction cycle	
0	-	-	unused	-

[1] To prevent an accidental software reset, 01011000 (58h) must be sent to register Control_1 (see Section 9.5).

9.3.2 Register Control_2

Table 6. Register Control_2 (address 01h) bits description

Bit	Symbol	Value	Description	Reference
7	MI	0	minute interrupt is disabled	Section 9.8.1
		1	minute interrupt is enabled	
6	SI	0	second interrupt is disabled	
		1	second interrupt is enabled	
5	MSF	0	no minute or second interrupt generated	
		1	flag set when minute or second interrupt generated; flag must be cleared to clear interrupt when TI_IP = 0	
4	TI_TP	0	interrupt pin follows timer flags	Section 9.9.2
		1	interrupt pin generates a pulse	
3	AF	0	no alarm interrupt generated	Section 9.7.1
		1	flag set when alarm triggered; flag must be cleared to clear interrupt	
2	TF	0	no countdown timer interrupt generated	-
		1	flag set when countdown timer interrupt generated; flag must be cleared to clear interrupt when TI_IP = 0	
1	AIE	0	no interrupt generated from the alarm flag	Section 9.9.3
		1	interrupt generated when alarm flag set	
0	TIE	0	no interrupt generated from the countdown timer	Section 9.9.2
		1	interrupt generated by the countdown timer	

9.4 OS flag

The PCF2123 includes a flag (bit OS) which is set whenever the oscillator is stopped (see Figure 8 and Figure 9). The flag will remain set until cleared by software. If the flag cannot be cleared, then the PCF2123 oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

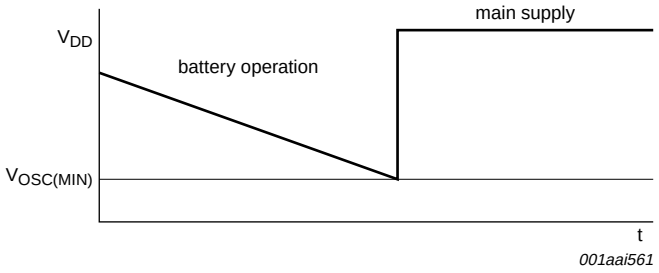


Fig 8. OS set by failing V_{DD}

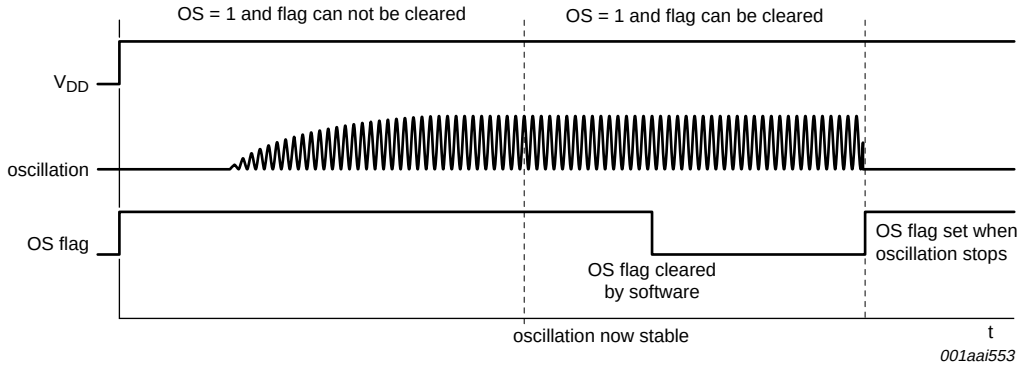


Fig 9. OS flag

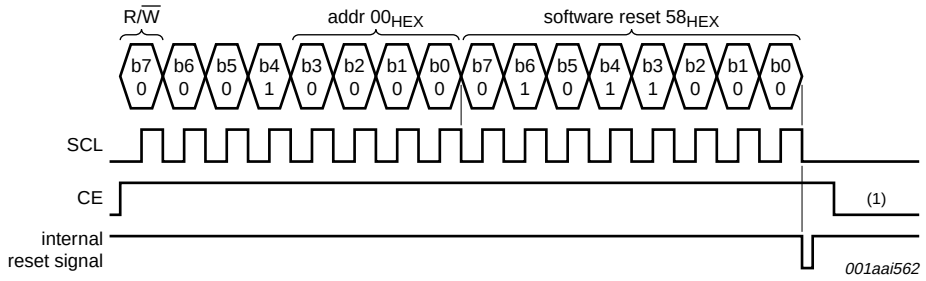
The oscillator may be stopped, for example, by grounding one of the oscillator pins, OSCI or OSCO. The oscillator is also considered to be stopped during the time between power-on and stable crystal resonance. This time may be in the range of 200 ms to 2 s depending on crystal type, temperature and supply voltage. At power-on the OS flag is always set.

9.5 Reset

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command. It is generally recommended to make a software reset after power-on.

A software reset can be initiated by setting the bits 6, 4 and 3 in register Control_1 to logic 1 and all other bits to logic 0 by sending the bit sequence 01011000 (58h), see Figure 10. If this bit sequence is not correct, the software reset instruction will be ignored to protect the device from accidently being reset. When sending the software instruction, the other bits are not written.

The SPI-bus is reset whenever the chip enable pin CE is inactive.



(1) When CE is inactive, the interface is reset.

Fig 10. Software reset command

Table 7. Register reset values

Bits labeled as - are not implemented. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	0	0	0	0	0	0	0	0
01h	Control_2	0	0	0	0	0	0	0	0
02h	Seconds	1	X	X	X	X	X	X	X
03h	Minutes	1	X	X	X	X	X	X	X
04h	Hours	-	-	X	X	X	X	X	X
05h	Days	-	-	X	X	X	X	X	X
06h	Weekdays	-	-	-	-	-	X	X	X
07h	Months	-	-	-	X	X	X	X	X
08h	Years	X	X	X	X	X	X	X	X
09h	Minute_alarm	1	X	X	X	X	X	X	X
0Ah	Hour_alarm	1	-	X	X	X	X	X	X
0Bh	Day_alarm	1	-	X	X	X	X	X	X
0Ch	Weekday_alarm	1	-	-	-	-	X	X	X
0Dh	Offset_register	0	0	0	0	0	0	0	0
0Eh	Timer_clkout	-	0	0	0	0	-	1	1
0Fh	Countdown_timer	X	X	X	X	X	X	X	X

After reset, the following mode is entered:

- 32.768 kHz on pin CLKOUT active
- 24 hour mode is selected
- Offset register is set to 0
- No alarms set
- Timer disabled
- No interrupts enabled

9.6 Time and date function

The majority of the registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use. An example is shown for the Minutes register in Table 8.

Table 8. BCD example

Minutes value (decimal)	Upper-digit				Digit			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
09	0	0	0	0	1	0	0	1
10	0	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
58	0	1	0	1	1	0	0	0
59	0	1	0	1	1	0	0	1

Table 9. Register Seconds (address 02h) bits description

Bit	Symbol	Value	Description
7	OS	0	clock integrity is guaranteed
		1	clock integrity is not guaranteed; oscillator has stopped or been interrupted
6 to 0	SECONDS	00 to 59[1]	this register holds the current seconds coded in BCD format

[1] Values shown in decimal.

Table 10. Register Minutes (address 03h) bits description

Bit	Symbol	Value	Description
7	-	-	unused
6 to 0	MINUTES	00 to 59[1]	this register holds the current minutes coded in BCD format

[1] Values shown in decimal.

Table 11. Register Hours (address 04h) bits description

Bit	Symbol	Value	Description
7 and 6	-	-	unused
12 hour mode[2]			
5	AMPM	0	indicates AM
		1	indicates PM
4 to 0	HOURS	01 to 12[1]	this register holds the current hours coded in BCD format for 12 hour mode
24 hour mode[2]			
5 to 0	HOURS	00 to 23[1]	this register holds the current hours coded in BCD format for 24 hour mode

[1] Values shown in decimal.

[2] Hour mode is set by the 12_24 bit in register Control_1.

Table 12. Register Days (address 05h) bits description

Bit	Symbol	Value	Description
7 and 6	-	-	unused
5 to 0	DAYS	01 to 31[1]	this register holds the current day coded in BCD format[2]

[1] Values shown in decimal.

[2] The RTC compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

Table 13. Register Weekdays (address 06h) bits description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0[1]	WEEKDAYS	0 to 6[2]	this register holds the current weekday, see Table 14

[1] These bits may be re-assigned by the user.

[2] Values shown in decimal.

Table 14. Weekday assignments

Day[1]	Upper-digit				Digit			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sunday	X	X	X	X	X	0	0	0
Monday	X	X	X	X	X	0	0	1
Tuesday	X	X	X	X	X	0	1	0
Wednesday	X	X	X	X	X	0	1	1
Thursday	X	X	X	X	X	1	0	0
Friday	X	X	X	X	X	1	0	1
Saturday	X	X	X	X	X	1	1	0

[1] The weekday assignments may be re-defined by the user.

Table 15. Register Months (address 07h) bits description

Bit	Symbol	Value	Description
7 to 5	-	-	unused
4 to 0	MONTHS	01 to 12[1]	this register holds the current month coded in BCD format, see Table 16

[1] Values shown in decimal.

Table 16. Month assignments

Month	Upper-digit				Digit			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	X	X	X	0	0	0	0	1
February	X	X	X	0	0	0	1	0
March	X	X	X	0	0	0	1	1
April	X	X	X	0	0	1	0	0
May	X	X	X	0	0	1	0	1
June	X	X	X	0	0	1	1	0
July	X	X	X	0	0	1	1	1
August	X	X	X	0	1	0	0	0
September	X	X	X	0	1	0	0	1
October	X	X	X	1	0	0	0	0
November	X	X	X	1	0	0	0	1
December	X	X	X	1	0	0	1	0

Table 17. Register Years (address 08h) bits description

Bit	Symbol	Value	Description
7 to 0	YEARS	00 to 99[1]	this register holds the current year coded in BCD format

[1] Values shown in decimal.

9.6.1 Data flow

Figure 11 shows the data flow and data dependencies starting from the 1 Hz clock tick.

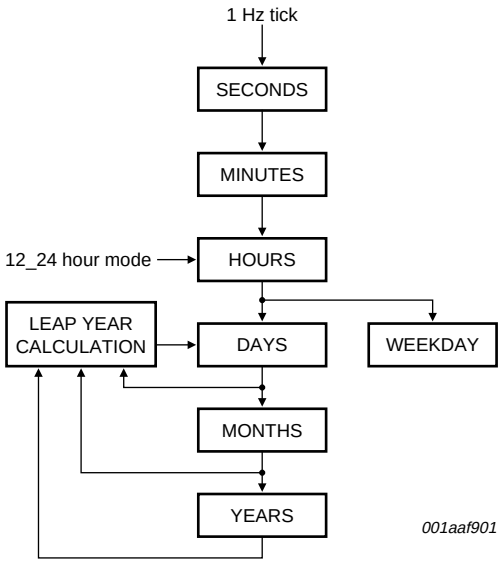


Fig 11. Data flow for the time function

In order to read the correct time it is important to read all time registers in one access i.e. seconds up to years. If the time registers are read by making individual access to the chip, then there is the risk that the time will increment between accesses.

9.7 Alarm function

When one or more of these registers are loaded with a valid minute, hour, day or weekday and its corresponding alarm enable not bit (AEN_x) is logic 0, then that information will be compared with the current minute, hour, day and weekday.

Table 18. Register Minute_alarm (address 09h) bits description

Bit	Symbol	Value	Description
7	AEN_M	0	minute alarm is enabled
		1	minute alarm is disabled
6 to 0	MINUTE_ALARM	00 to 59[1]	this register holds the minute alarm information coded in BCD format

[1] Values shown in decimal.

Table 19. Register Hour_alarm (address 0Ah) bits description

Bit	Symbol	Value	Description
7	AEN_H	0	hour alarm is enabled
		1	hour alarm is disabled
6	-	-	unused
12 hour mode			
5	AMPM	0	indicates AM
		1	indicates PM
4 to 0	HOUR_ALARM	01 to 12[1]	this register holds the hour alarm information coded in BCD format when in 12 hour mode
24 hour mode			
5 to 0	HOUR_ALARM	00 to 23[1]	this register holds the hour alarm information coded in BCD format when in 24 hour mode

[1] Values shown in decimal.

Table 20. Register Day_alarm (address 0Bh) bits description

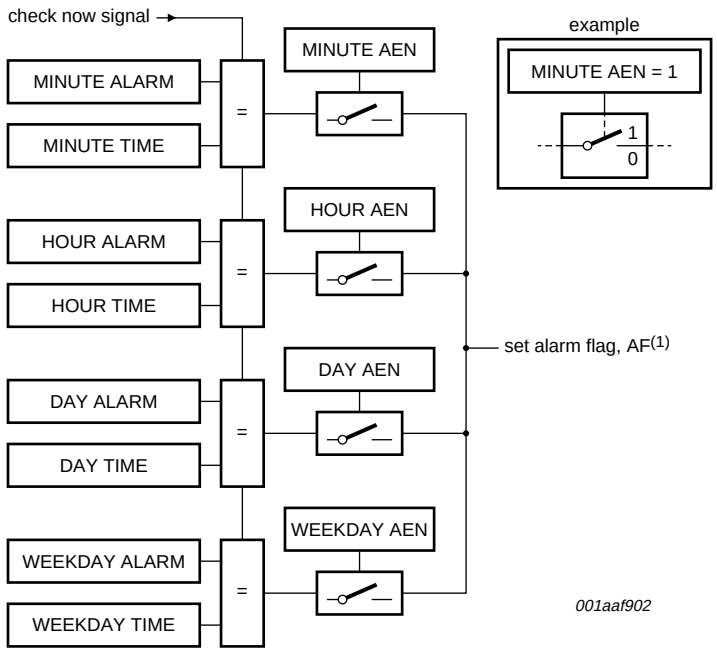
Bit	Symbol	Value	Description
7	AEN_D	0	day alarm is enabled
		1	day alarm is disabled
6	-	-	unused
5 to 0	DAY_ALARM	01 to 31[1]	this register holds the day alarm information coded in BCD format

[1] Values shown in decimal.

Table 21. Register Weekday_alarm (address 0Ch) bits description

Bit	Symbol	Value	Description
7	AEN_W	0	weekday alarm is enabled
		1	weekday alarm is disabled
3 to 6	-	-	unused
2 to 0	WEEKDAY_ ALARM	0 to 6[1]	this register holds the weekday alarm information

[1] Values shown in decimal.



(1) Only when all enabled alarm settings are matching.

Fig 12. Alarm function block diagram

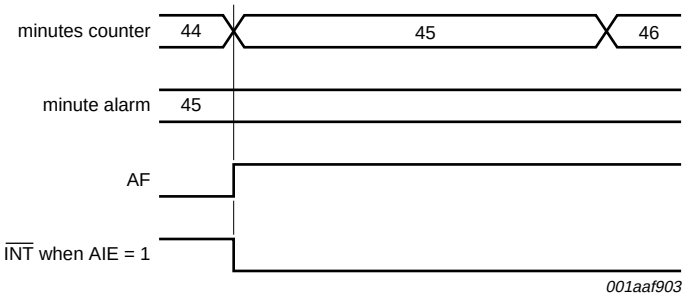
The generation of interrupts from the alarm function is described in Section 9.9.3.

9.7.1 Alarm flag

When all enabled comparisons first match, the alarm flag bit AF is set. Bit AF will remain set until cleared by software. **Once bit AF has been cleared it will only be set again when the time increments to match the alarm condition.**

Alarm registers which have bit AEN_x at logic 1 are ignored.

Table 23 shows an example for clearing bit AF but leaving bit MSF and bit TF unaffected. Clearing the flags is made by a write command; therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 13. AF timing

To prevent the timer flags being overwritten while clearing AF, a logical AND is performed during a write access. Writing a logic 1 will cause the flag to maintain its value, whereas writing a logic 0 will cause the flag to be reset.

Table 22. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	MSF	-	AF	TF	-	-

The following tables show what instruction must be sent to clear bit AF. In this example, bit MSF and bit TF are unaffected.

Table 23. Example to clear only AF (bit 3) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	1	-	0	1	-	-

9.8 Timer functions

The countdown timer has four selectable source clocks allowing for countdown periods in the range from 244 μs to 4 h 15 min. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. For periods greater than 4 hours, the alarm function can be used.

Registers 01h, 0Eh and 0Fh are used to control the timer function and output.

Table 24. Register Timer_clkout (address 0Eh) bits description

Bit	Symbol	Value	Description	Reference
7	-	-	unused	-
6 to 4	COFx	[1]	CLKOUT control	Section 9.10
3	TE	0	countdown timer is disabled	Section 9.8.2
		1	countdown timer is enabled	
2	-	-	unused	
1 to 0	CTD	00	4.096 kHz countdown timer source clock	
		01	64 Hz countdown timer source clock	
		10	1 Hz countdown timer source clock	
		11	$^1/_{60}$ Hz countdown timer source clock	

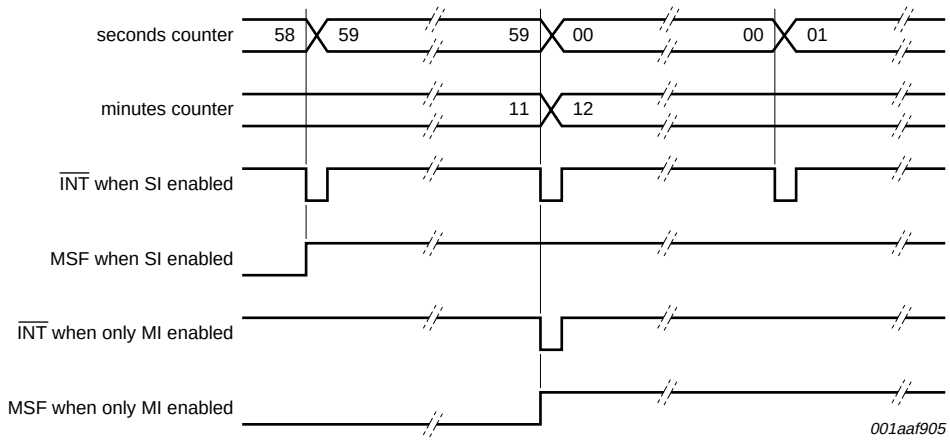
[1] Values of COF[2:0] see Table 35.

Table 25. Register Countdown_timer (address 0Ah) bits description

Bit	Symbol	Value	Description	Reference
7 to 0	COUNTDOWN_TIMER	0h to FFh	countdown value = n; $CountdownPeriod = \frac{n}{SourceClockFrequency}$	Section 9.8.2

9.8.1 Minute and second interrupt

The minute and second interrupts (bits MI and SI) are pre-defined timers for generating periodic interrupts. The timers can be enabled independently from one another. However, a minute interrupt enabled on top of a second interrupt will not be distinguishable since it will occur at the same time; see Figure 14.



In this example, TI_TP is set to logic 1 resulting in $^{1}/_{64}$ Hz wide interrupt pulse and the MSF flag is not cleared after an interrupt.

Fig 14. $\overline{\text{INT}}$ example for MI and SI

Table 26. Effect of bits MI and SI on $\overline{\text{INT}}$ generation

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	no interrupt generated
1	0	an interrupt once per minute
0	1	an interrupt once per second
1	1	an interrupt once per second

The minute and second flag (bit MSF) is set to logic 1 when either the seconds or the minutes counter increments according to the currently enabled interrupt. The flag can be read and cleared by the interface. The status of bit MSF does not affect the $\overline{\text{INT}}$ pulse generation. If the MSF flag is not cleared prior to the next coming interrupt period, an $\overline{\text{INT}}$ pulse will still be generated.

The purpose of the flag is to allow the controlling system to interrogate the PCF2123 and identify the source of the interrupt i.e. minute or second, countdown timer or alarm.

Table 27. Effect of MI and SI on MSF

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	MSF never set
1	0	MSF set when **minutes** counter increments
0	1	MSF set when **seconds** counter increments
1	1	MSF set when **seconds** counter increments

The duration of both of these timers will be affected by the register Offset_register (see Section 9.11). Only when the Offset_register has the value 00h will the periods be consistent.

9.8.2 Countdown timer function

The 8-bit countdown timer at address 0Fh is controlled by the register Timer_clkout at address 0Eh. The register Timer_clkout selects one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or $^1/_{60}$ Hz) and enables or disables the timer.

Table 28. Bits CTD0 and CTD1 for timer frequency selection and countdown timer durations

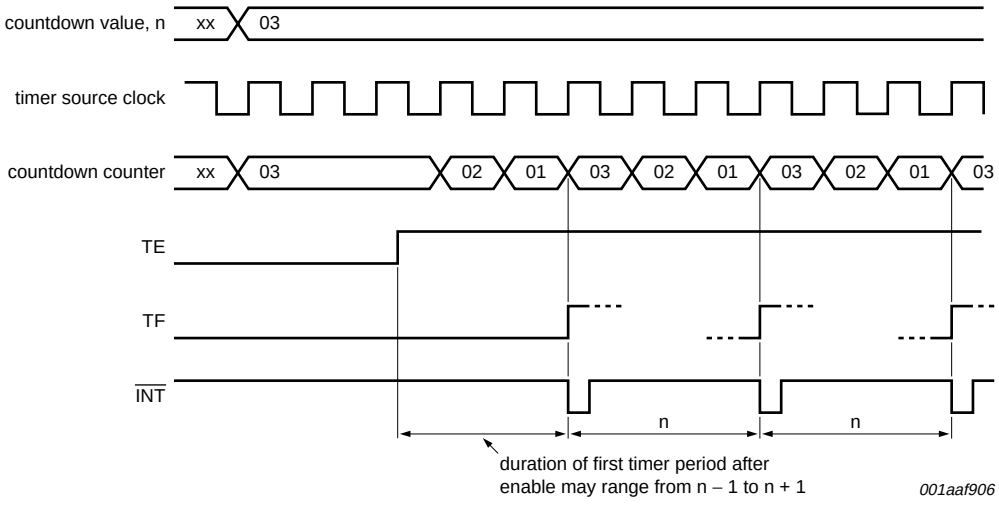
CTD[1:0]	Timer source clock frequency[1]	Delay	
		Minimum timer duration n = 1	Maximum timer duration n = 255
00	4.096 kHz	244 µs	62.256 ms
01	64 Hz	15.625 ms	3.984 s
10	1 Hz[2]	1 s	255 s
11	$^1/_{60}$ Hz[2]	60 s	4 h 15 min

[1] When not in use, CTD must be set to $^1/_{60}$ Hz for power saving.

[2] Time periods can be affected by correction pulses.

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency will result in deviation in timings. This is not applicable to interface timing.

The timer counts down from a software-loaded 8-bit binary value, n. Loading the counter with 0 stops the timer. Values from 1 to 255 are valid. When the counter reaches 1, the countdown timer flag (bit TF) will be set and the counter automatically re-loads and starts the next timer period. Reading the timer will return the current value of the countdown counter (see Figure 15).



In this example it is assumed that the timer flag is cleared before the next countdown period expires and that the pin $\overline{INT}$ is set to pulsed mode.

Fig 15. General countdown timer behavior

If a new value of n is written before the end of the current timer period, then this value will take immediate effect. NXP does not recommend changing n without first disabling the counter (by setting bit TE = 0). The update of n is asynchronous to the timer clock, therefore changing it without setting bit TE = 0 may result in a corrupted value loaded into the countdown counter which results in an undetermined countdown period for the first period. The countdown value n will, however, be correctly stored and correctly loaded on subsequent timer periods.

When the countdown timer flag is set, an interrupt signal on $\overline{INT}$ will be generated provided that this mode is enabled. See Section 9.9.2 for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period will have an uncertainty which is a result of the enable instruction being generated from the interface clock which is asynchronous from the timer source clock. Subsequent timer periods will have no such delay. The amount of delay for the first timer period will depend on the chosen source clock, see Table 29.

Table 29. First period delay for timer counter value n

Timer source clock	Minimum timer period	Maximum timer period
4.096 kHz	n	n + 1
64 Hz	n	n + 1
1 Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz
$\frac{1}{60}$ Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz

At the end of every countdown, the timer sets the countdown timer flag (bit TF). Bit TF may only be cleared by software. The asserted bit TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output may be disabled with bit TIE, see Table 6.

When reading the timer, the current countdown value is returned and **not** the initial value n. For accurate read back of the countdown value, the SPI-bus clock (SCL) must be operating at a frequency of at least twice the selected timer clock. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

Timer source clock frequency selection of 1 Hz and $\frac{1}{60}$ Hz will be affected by the Offset_register. The duration of a program period will vary according to when the offset is initiated. For example, if a 100 s timer is set using the 1 Hz clock as source, then some 100 s periods will contain correction pulses and therefor be longer or shorter depending on the setting of the Offset_register. See Section 9.11 to understand the operation of the Offset_register.

9.8.3 Timer flags

When a minute or second interrupt occurs, bit MSF is set to logic 1. Similarly, at the end of a timer countdown or alarm event, bit TF or AF are set to logic 1. These bits maintain their value until overwritten by software. If both countdown timer and minute or second interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logical AND is performed during a write access. Writing a logic 1 will cause the flag to maintain its value, whilst writing a logic 0 will cause the flag to be reset.

Three examples are given for clearing the flags. Clearing the flags is made by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

Table 30. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 31, Table 32 and Table 33 show what instruction must be sent to clear the appropriate flag.

Table 31. Example to clear only TF (bit 2) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	1	-	1	0	-	-

Table 32. Example to clear only MSF (bit 5) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	0	-	1	1	-	-

Table 33. Example to clear both TF and MSF (bit 2 and bit 5) in register Control_2

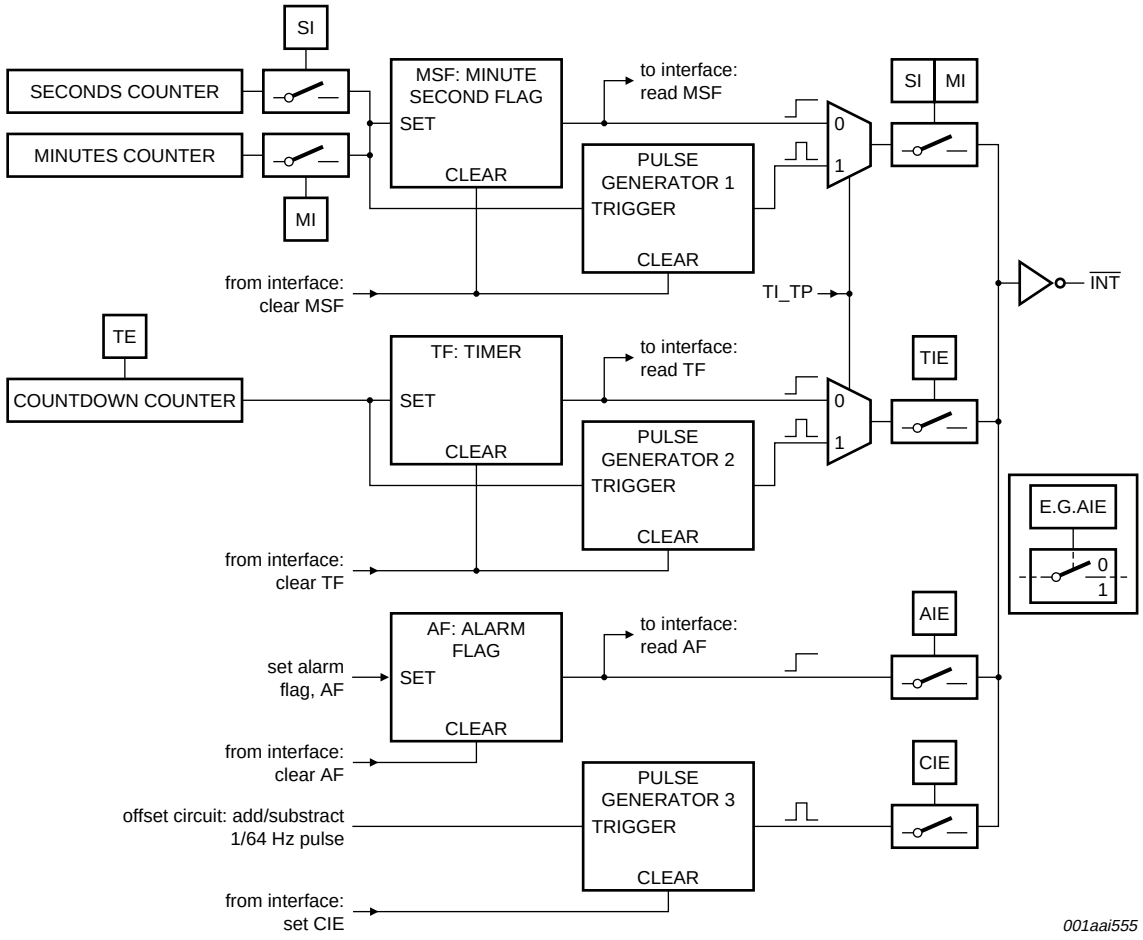
Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	0	-	1	0	-	-

Clearing the alarm flag (bit AF) operates in exactly the same way, see Section 9.7.1.

9.9 Interrupt output

An active LOW interrupt signal is available at pin $\overline{INT}$. Operation is controlled via the bits of register Control_2. Interrupts may be sourced from four places: second and minute timer, countdown timer, alarm function or offset function.

With bit TI_TP, the timer generated interrupts can be configured to either generate a pulse or to follow the status of the interrupt flags (bits TF and MSF). Correction interrupt pulses are always $^{1}/_{128}$ second long. Alarm interrupts always follow the condition of AF.



When bits SI, MI, TIE, AIE and CIE are all disabled, pin $\overline{INT}$ will remain high-impedance.

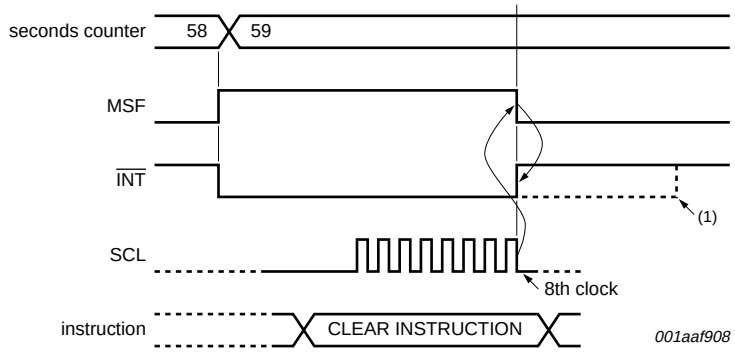
Fig 16. Interrupt scheme

Remark: Note that the interrupts from the four sources are wired-OR, meaning they will mask one another (see Figure 16).

9.9.1 Minute and second interrupts

The pulse generator for the minute and second interrupt operates from an internal 64 Hz clock and consequently generates a pulse of $^{1}/_{64}$ second in duration.

If the MSF flag is cleared before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced i.e. the system does not have to wait for the completion of the pulse before continuing; see Figure 17. Instructions for clearing MSF are given in Section 9.8.3.



(1) Indicates normal duration of $\overline{INT}$ pulse (bit TI_TP = 1)

Fig 17. Example of shortening the $\overline{INT}$ pulse by clearing the MSF flag

The timing shown for clearing bit MSF in Figure 17 is also valid for the non-pulsed interrupt mode i.e. when bit TI_TP = 0, $\overline{INT}$ may be shortened by setting both MI and SI or MSF to logic 0.

9.9.2 Countdown timer interrupts

The generation of interrupts from the countdown timer is controlled via bit TIE.

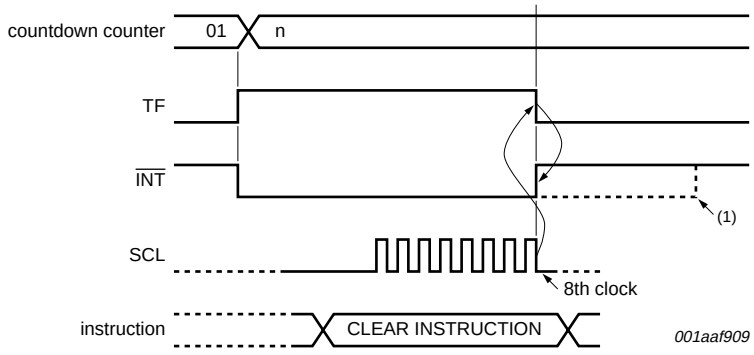
The pulse generator for the countdown timer interrupt also uses an internal clock, but this time it is dependent on the selected source clock for the countdown timer and on the countdown value n. As a consequence, the width of the interrupt pulse varies (see Table 34).

Table 34. $\overline{INT}$ operation (bit TI_TP = 1)

Source clock (Hz)	$\overline{INT}$ period (s)	
	n = 1[1]	n > 1
4096	$1/8192$	$1/4096$
64	$1/128$	$1/64$
1	$1/64$	$1/64$
$1/60$	$1/64$	$1/64$

[1] n = loaded countdown value. Timer stopped when n = 0.

If the TF flag is cleared before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced i.e. the system does not have to wait for the completion of the pulse before continuing (see Figure 18). Instructions for clearing MSF can be found in Section 9.8.3.



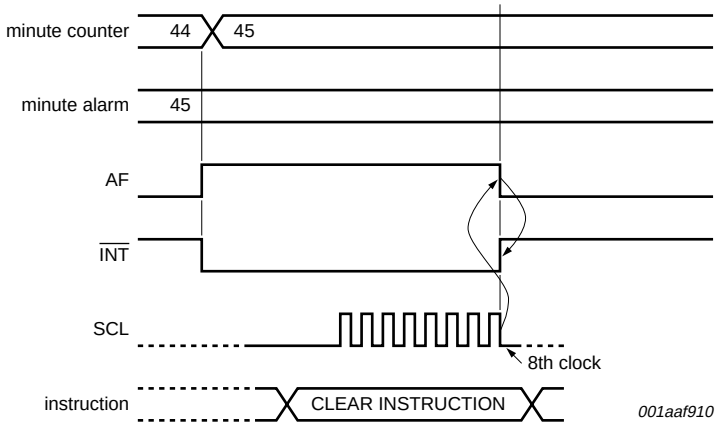
(1) Indicates normal duration of $\overline{INT}$ pulse (bit TI_TP = 1).

Fig 18. Example of shortening the $\overline{INT}$ pulse by clearing the TF flag

The timing shown for clearing bit TF in Figure 18 is also valid for the non-pulsed interrupt mode i.e. when bit TI_TP = 0, $\overline{INT}$ may be shortened by setting bit TIE to logic 0.

9.9.3 Alarm interrupts

The generation of interrupts from the alarm function is controlled via bit AIE (see Table 6). If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. Clearing bit AF will immediately clear $\overline{INT}$. No pulse generation is possible for alarm interrupts (see Figure 19).



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 19. AF timing

9.9.3.1 Correction pulse interrupts

Interrupt pulses generated by correction events can be shortened by writing a logic 1 to bit CIE in register Control_1.

9.10 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] bits in the register Timer_clkout. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLKOUT is an open-drain output and enabled at power-on. When disabled the output is high-impedance.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all will be 50 : 50 except the 32.768 kHz frequencies.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When the STOP bit is set to logic 1, the CLKOUT pin will generate a continuous LOW for those frequencies that can be stopped. For more details of the STOP bit function see Section 9.13.

Table 35. CLKOUT frequency selection

Bits COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1]	Effect of STOP bit
000	32768	60 : 40 to 40 : 60	no effect
001	16384	50 : 50	no effect
010	8192	50 : 50	no effect
011	4096	50 : 50	CLKOUT = LOW
100	2048	50 : 50	CLKOUT = LOW
101	1024	50 : 50	CLKOUT = LOW
110	1[2]	50 : 50	CLKOUT = LOW
111	CLKOUT = high-Z	-	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] 1 Hz clock pulses will be affected by offset correction pulses.

9.10.1 CLKOE pin

The CLKOE pin can be used to block the CLKOUT function and force the CLKOUT pin to an high-impedance state. The effect is the same as setting COF[2:0] = 111.

9.11 Offset register

The PCF2123 incorporates an offset register (address 0Dh) which can be used to implement several functions, such as:

- Ageing adjustment
- Temperature compensation
- Accuracy tuning

The offset is made once every two hours in the normal mode, or once every hour in the course mode. Each LSB will introduce an offset of 2.17 ppm for normal mode and 4.34 ppm for course mode. The values of 2.17 ppm and 4.34 ppm are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63 LSB to −64 LSB.

Table 36. Register Offset_register

OFFSET[6:0]	Offset value in decimal	Offset value in ppm	
		Normal mode MODE = 0	Course mode MODE = 1
0 1 1 1 1 1 1	+63	+136.71	+273.42
0 1 1 1 1 1 0	+62	+134.54	+269.08
:	:	:	:
0 0 0 0 0 1 0	+2	+4.34	+8.68
0 0 0 0 0 0 1	+1	+2.17	+4.34
0 0 0 0 0 0 0	0[1]	0	0
1 1 1 1 1 1 1	–1	–2.17	–4.34
1 1 1 1 1 1 0	–2	–4.34	–8.68
:	:	:	:
1 0 0 0 0 0 1	–63	–136.71	–273.42
1 0 0 0 0 0 0	–64	–138.88	–277.76

[1] Default mode.

The correction is made by adding or subtracting 64 Hz clock correction pulses, thereby changing the period of a single second.

Table 37. Example of converting the offset in ppm to seconds

Offset in ppm	Seconds per			
	Day	Week	Month	Year
2.17	0.187	1.31	5.69	68.2
4.34	0.375	2.62	11.4	136

In normal mode, the correction is triggered once per two hours and then correction pulses are applied once per minute until the programmed correction values has been implement.

In course mode, the correction is triggered once per hour and then correction pulses are applied once per minute up to a maximum of 60 minutes. When correction values greater than 60 are used, additional correction pulses are made in the 59th minute (see Table 38).

Table 38. Correction pulses for course mode

Correction value	Hour:Minute[1]	Correction pulses on $\overline{INT}$ per minute[2]
+1 or –1	02:00	1
	02:01 to 02:59	0
+2 or –2	02:00	1
	02:01	1
	02:02 to 02:59	0
+3 or –3	02:00	1
	02:01	1
	02:02	1
	02:03 to 02:59	0
:	:	:
+59 or –59	02:00 to 02:58	1
	02:59	0
+60 or –60	02:00 to 02:59	1
+61 or –61	02:00 to 02:58	1
	02:59	2
+62 or –62	02:00 to 02:58	1
	02:59	3
+63 or –63	02:00 to 02:58	1
	02:59	4
–64	02:00 to 02:58	1
	02:59	5

[1] Example is given in a time range from 2:00 to 2:59.

[2] Correction $\overline{INT}$ pulses are $\frac{1}{128}$ s wide. For multiple pulses they are repeated at $\frac{1}{64}$ s interval.

It is possible to monitor when correction pulses are applied. The correction interrupt enable mode (bit CIE) will generate a $\frac{1}{128}$ second pulse on $\overline{INT}$ for every correction applied. In the case where multiple correction pulses are applied, a $\frac{1}{128}$ second interrupt pulse will be generated and repeated every $\frac{1}{64}$ seconds.

Correction is applied to the 1 Hz clock. Any timer or clock output using a frequency of 1 Hz or below will also be affected by the correction pulses.

Table 39. Effect of correction pulses

Frequency (Hz)	Effect of correction
CLKOUT	
32768	no effect
16384	no effect
8192	no effect
4096	no effect
2048	no effect
1024	no effect
1	effected
Time source clock	
4096	no effect
64	no effect
1	effected
$^1/_{60}$	effected

9.12 External clock test mode

A test mode is available which allows for on-board testing. In this mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit EXT_TEST in register Control_1. Then pin CLKOUT becomes an input. The test mode replaces the internal clock signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT generates an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a minimum period of 1000 ns. The internal clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0. (STOP must be cleared before the prescaler can operate again.)

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_TEST test mode (register Control_1, bit EXT_TEST = 1).
2. Set STOP (Control_1, bit STOP = 1).
3. Clear STOP (Control_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

9.13 STOP bit function

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler (F_2 to F_{14}) to be held in reset and thus no 1 Hz ticks will be generated. The time circuits can then be set and will not increment until the STOP bit is released (see Figure 21 and Table 40).

The STOP bit function will not affect the output of 32.768 kHz, 16.384 kHz or 8.192 kHz (see Section 9.10).

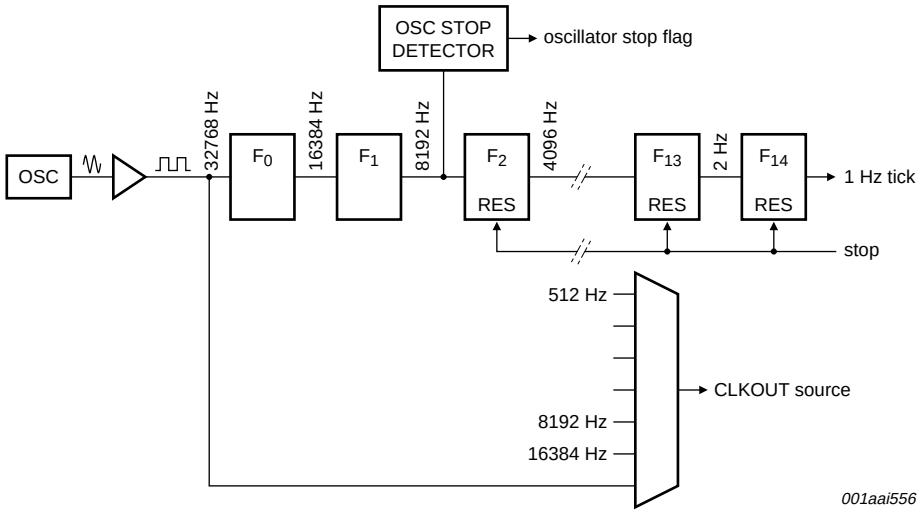


Fig 20. STOP bit

The lower two stages of the prescaler (F_0 and F_1) are not reset and because the SPI-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between 0 and one 8.192 kHz cycle (see Figure 21).

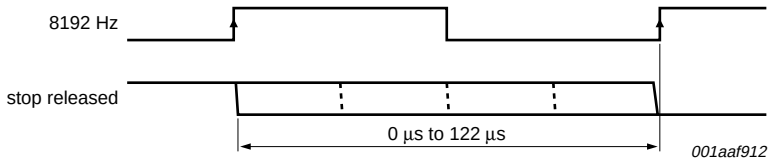
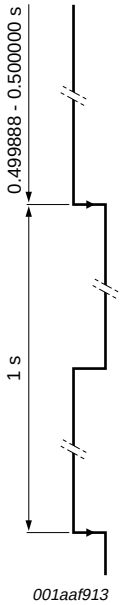


Fig 21. STOP bit release timing

The first increment of the time circuits is between 0.499888 s and 0.500000 s after STOP bit is released. The uncertainty is caused by the prescaler bits F_0 and F_1 not being reset (see Table 40).

Table 40. First increment of time circuits after STOP bit release

Bit STOP	Prescaler bits F_0F_1-F_2 to F_{14} [1]	1 Hz tick	Time hh:mm:ss	Comment
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	prescaler counting normally
STOP bit is activated by user. F_0F_1 are not reset and values cannot be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	prescaler is reset; time circuits are frozen
STOP bit is released by user				
0	XX-0 0000 0000 0000		08:00:00	prescaler is now running
	XX-1 0000 0000 0000		08:00:00	-
	XX-0 1000 0000 0000		08:00:00	-
	XX-1 1000 0000 0000		08:00:00	-
	:		:	:
	11-1 1111 1111 1110		08:00:00	-
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F_{14} increments the time circuits
	10-0 0000 0000 0001		08:00:01	-
	:		:	:
	11-1 1111 1111 1111		08:00:01	-
	00-0 0000 0000 0000		08:00:01	-
	10-0 0000 0000 0000		08:00:01	-
	:		:	-
	11-1 1111 1111 1110		08:00:01	-
	00-0 0000 0000 0001		08:00:02	0 to 1 transition of F_{14} increments the time circuits

[1] F_0 is clocked at 32.768 kHz.

9.14 3-line serial interface

Data transfer to and from the device is made via a 3-wire SPI-bus (see Table 41). The data lines for input and output are split. The data input and output lines can be connected together to facilitate a bidirectional data bus. The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the Most Significant Bit (MSB) sent first (see Figure 23).

Table 41. Serial interface

Symbol	Function	Description
CE	chip enable input	when LOW, the interface is reset; pull-down resistor included; active input may be higher than V_{DD}, but may not be wired permanently HIGH
SCL	serial clock input	when CE is LOW, this input may float; input may be higher than V_{DD}
SDI	serial data input	when CE is LOW, input may float; input may be higher than V_{DD}; input data is sampled on the rising edge of SCL
SDO	serial data output	push-pull output; drives from V_{SS} to V_{DD}; output data is changed on the falling edge of SCL; will be high-Z when not driving; may be connected directly to SDI

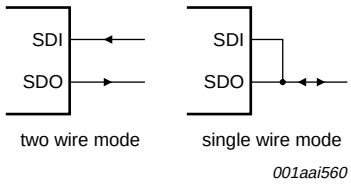


Fig 22. SDI, SDO configurations

The transmission is controlled by the active HIGH chip enable signal CE. The first byte transmitted is the command byte. Subsequent bytes will be either data to be written or data to be read. Data is sampled on the rising edge of the clock and transferred internally on the falling edge.

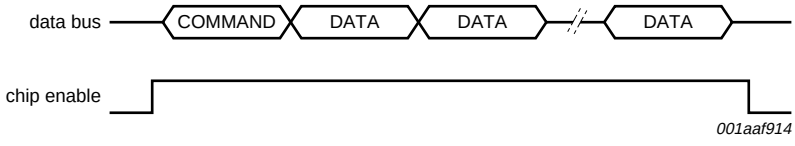


Fig 23. Data transfer overview

The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will rollover to zero after the last register is accessed. The read/$\overline{\text{write}}$ bit (R/$\overline{\text{W}}$) defines if the following bytes will be read or write information.

Table 42. Command byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		data read or data write selection
		0	write data
		1	read data
6 to 4	SA	001	subaddress; other codes will cause the device to ignore data transfer
3 to 0	RA	0h to Fh	register address range

In Figure 24, the register Seconds is set to 45 seconds and the register Minutes is set to 10 minutes.

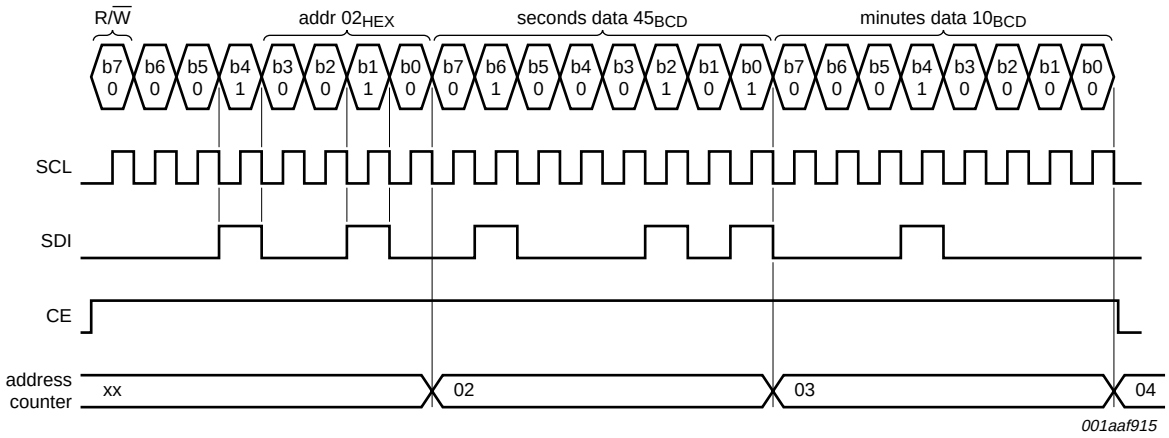


Fig 24. Serial bus write example

In Figure 25, the Months and Years registers are read. In this example, pins SDI and SDO are not connected together. For this configuration, it is important that pin SDI is never left floating. It must always be driven either HIGH or LOW. If pin SDI is left open, high I_{DD} currents may result. Short transition periods in the order of 200 ns will not cause any problems.

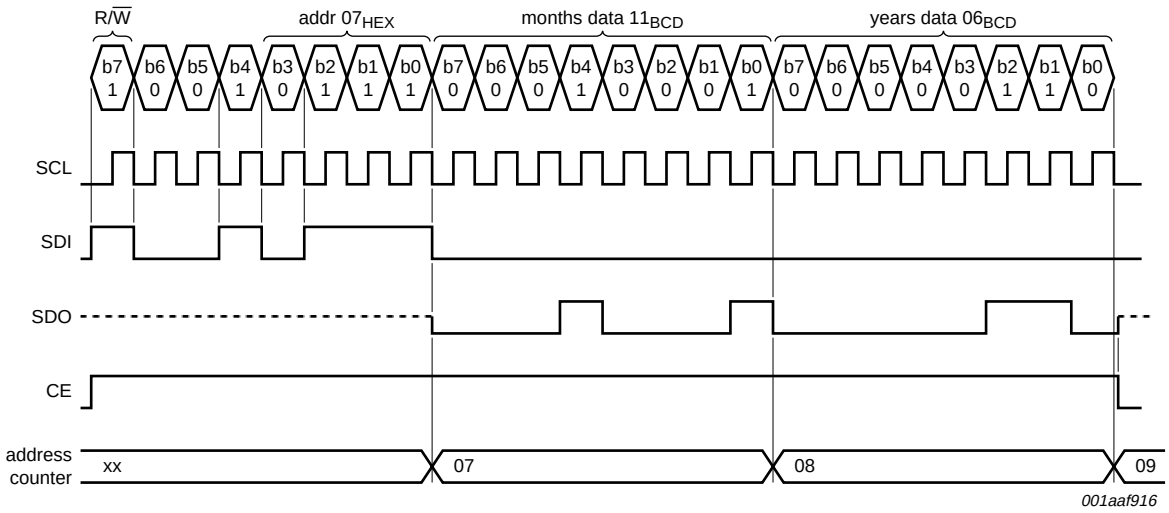
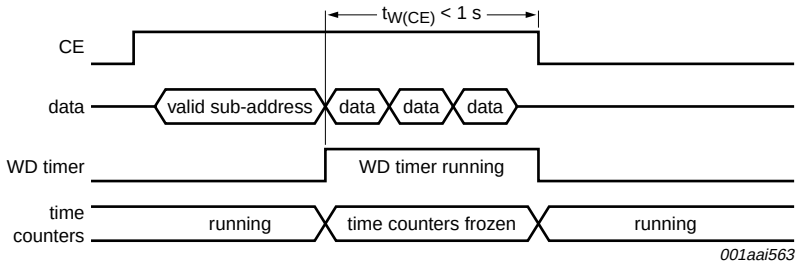


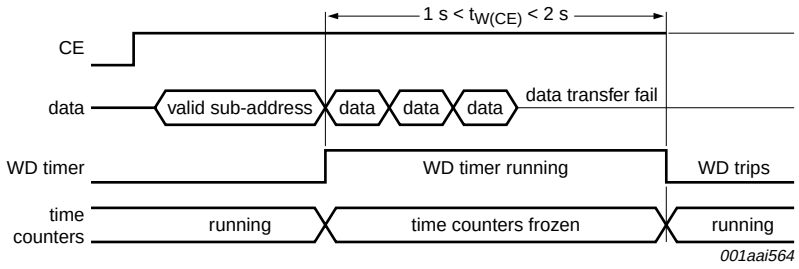
Fig 25. Serial bus read example

9.14.1 Interface watchdog timer

During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface by setting pin CE LOW, the PCF2123 has a built in watchdog timer. Should the interface be active for more than 1 s from the time a valid subaddress is transmitted, then the PCF2123 will automatically clear the interface and allow the time counting circuits to continue counting. CE must return LOW once more before a new data transfer can be executed.



a. Correct data transfer: read or write



b. Incorrect data transfer; read or write

Fig 26. Interface watchdog timer

The watchdog is implemented to prevent the excessive loss of time due to interface access failure e.g. if main power is removed from a battery backed-up system during an interface access.

Each time the watchdog period is exceeded, 1 s will be lost from the time counters. The watchdog will trigger between 1 s and 2 s after receiving a valid subaddress.

10. Limiting values

Table 43. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[1]	–0.5	+6.5	V
I_{DD}	supply current			–50	+50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
V_O	output voltage		[1]	–0.5	+6.5	V
I_I	input current			–10	+10	mA
I_O	output current			–10	+10	mA
P_{tot}	total power dissipation			-	300	mW
T_{amb}	ambient temperature			–40	+85	°C
V_{esd}	electrostatic discharge voltage	HBM	[2]	-	±3000	V
		MM	[3]	-	±300	V
I_{lu}	latch-up current		[4]	-	200	mA
T_{stg}	storage temperature		[5]	–65	+150	°C

[1] With respect to V_{SS}.

[2] Pass level; Human Body Model (HBM) according to JESD22-A114.

[3] Pass level; Machine Model (MM), according to JESD22-A115

[4] Pass level; latch-up testing, according to JESD78.

[5] According to the NXP store and transport conditions (document *SNW-SQ-623*) the devices have to be stored at a temperature of +5 °C to +45 °C and a humidity of 25 % to 75 %.

11. Static characteristics

Table 44. Static characteristics

V_{DD} = 1.1 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 15 kΩ; C_L = 7 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage	for clock data integrity; SPI-bus inactive	[1]	1.1	-	5.5	V
		T_{amb} = 25 °C		-	0.9	-	V
		SPI-bus active		1.6	-	5.5	V
I_{DD}	supply current	SPI-bus active					
		f_{SCL} = 4.5 MHz; V_{DD} = 5 V		-	250	400	µA
		f_{SCL} = 1.0 MHz; V_{DD} = 3 V		-	30	80	µA
		SPI-bus inactive; CLKOUT disabled	[2]				
		T_{amb} = 25 °C; V_{DD} = 2.0 V		-	100	-	nA
		T_{amb} = 25 °C; V_{DD} = 3.0 V		-	110	-	nA
		T_{amb} = 25 °C; V_{DD} = 5.0 V		-	120	-	nA
		SPI-bus inactive; CLKOUT disabled; T_{amb} = −40 °C to +85 °C	[2]				
		V_{DD} = 2.0 V		-	-	330	nA
		V_{DD} = 3.0 V		-	-	350	nA
		V_{DD} = 5.0 V		-	-	380	nA
		SPI-bus inactive; CLKOUT enabled at 32 kHz; T_{amb} = 25 °C					
		V_{DD} = 2.0 V		-	260	-	nA
		V_{DD} = 3.0 V		-	340	-	nA
		V_{DD} = 5.0 V		-	520	-	nA
		SPI-bus inactive; CLKOUT enabled at 32 kHz; T_{amb} = −40 °C to +85 °C					
		V_{DD} = 2.0 V		-	-	450	nA
		V_{DD} = 3.0 V		-	-	550	nA
		V_{DD} = 5.0 V		-	-	750	nA
Inputs							
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_I	input voltage	on pins CE, SDI, SCL, OSCI, CLKOE, CLKOUT		–0.5	-	5.5	V

Table 44. Static characteristics *...continued*

V_{DD} = 1.1 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 15 kΩ; C_L = 7 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_L	leakage current	$V_I = V_{DD}$ or V_{SS} on pins SDI, SCL, OSCI, CLKOE, CLKOUT		−1	0	+1	µA
		$V_I = V_{SS}$ on pin CE		−1	0	-	µA
R_{pd}	pull-down resistance	on pin CE		-	240	550	kΩ
C_i	input capacitance	-	[3]	-	-	7	pF
Outputs							
V_O	output voltage	on pins CLKOUT and $\overline{INT}$	[4]	−0.5	-	5.5	V
		on pin OSCO		−0.5	-	5.5	V
		on pin SDO		−0.5	-	V_{DD}+0.5	V
V_{OH}	HIGH-level output voltage	on pin SDO		0.8V_{DD}	-	V_{DD}	V
V_{OL}	LOW-level output voltage	on pin SDO		V_{SS}	-	0.2V_{DD}	V
		on pins CLKOUT and $\overline{INT}$; V_{DD} = 5 V; I_{OL}=1.5 mA		V_{SS}	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = 4.6 V; V_{DD} = 5 V on pin SDO		-	-	1.5	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V on pins $\overline{INT}$, SDO and CLKOUT		−1.5	-	-	mA
I_{LO}	output leakage current	$V_O = V_{DD}$ or V_{SS}		−1	0	+1	µA
$C_{L(itg)}$	integrated load capacitance	on pins OSCO and OSCI	[5]	3.3	7	14	pF

[1] For reliable oscillator start at power-on: $V_{DD} = V_{DD(min)} + 0.3$ V.

[2] Timer source clock = $^1/_{60}$ Hz, level of pins CE, SDI and SCL is V_{DD} or V_{SS}.

[3] Implicit by design.

[4] Refers to external pull-up voltage.

[5] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series. $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$

12. Dynamic characteristics

Table 45. SPI-bus characteristics

V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C. All timing values are valid within the operating supply voltage and temperature range and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions	V_{DD} = 1.6 V		V_{DD} = 2.4 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Timing characteristics (see Figure 27)											
$f_{clk(SCL)}$	SCL clock frequency		-	2.9	-	4.54	-	5.71	-	8.0	MHz
t_{SCL}	SCL time		345	-	220	-	175	-	125	-	ns
$t_{clk(H)}$	clock HIGH time		90	-	50	-	45	-	40	-	ns
$t_{clk(L)}$	clock LOW time		200	-	120	-	95	-	70	-	ns
t_r	rise time	for SCL signal	-	100	-	100	-	50	-	50	ns
t_f	fall time	for SCL signal	-	100	-	100	-	50	-	50	ns
$t_{su(CE)}$	CE set-up time		40	-	35	-	30	-	25	-	ns
$t_{h(CE)}$	CE hold time		40	-	30	-	25	-	15	-	ns
$t_{rec(CE)}$	CE recovery time		30	-	25	-	20	-	15	-	ns
$t_{w(CE)}$	CE pulse width	measured after valid subaddress is received	-	0.99	-	0.99	-	0.99	-	0.99	s
t_{su}	set-up time	set-up time for SDI data	10	-	5	-	3	-	2	-	ns
t_h	hold time	hold time for SDI data	25	-	10	-	8	-	5	-	ns
$t_{d(R)SDO}$	SDO read delay time	bus load = 50 pF	-	190	-	108	-	85	-	60	ns
$t_{dis(SDO)}$	SDO disable time	no load value; bus will be held up by bus capacitance; use RC time constant with application values	-	70	-	45	-	40	-	27	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	to avoid bus conflict	0	-	0	-	0	-	0	-	ns

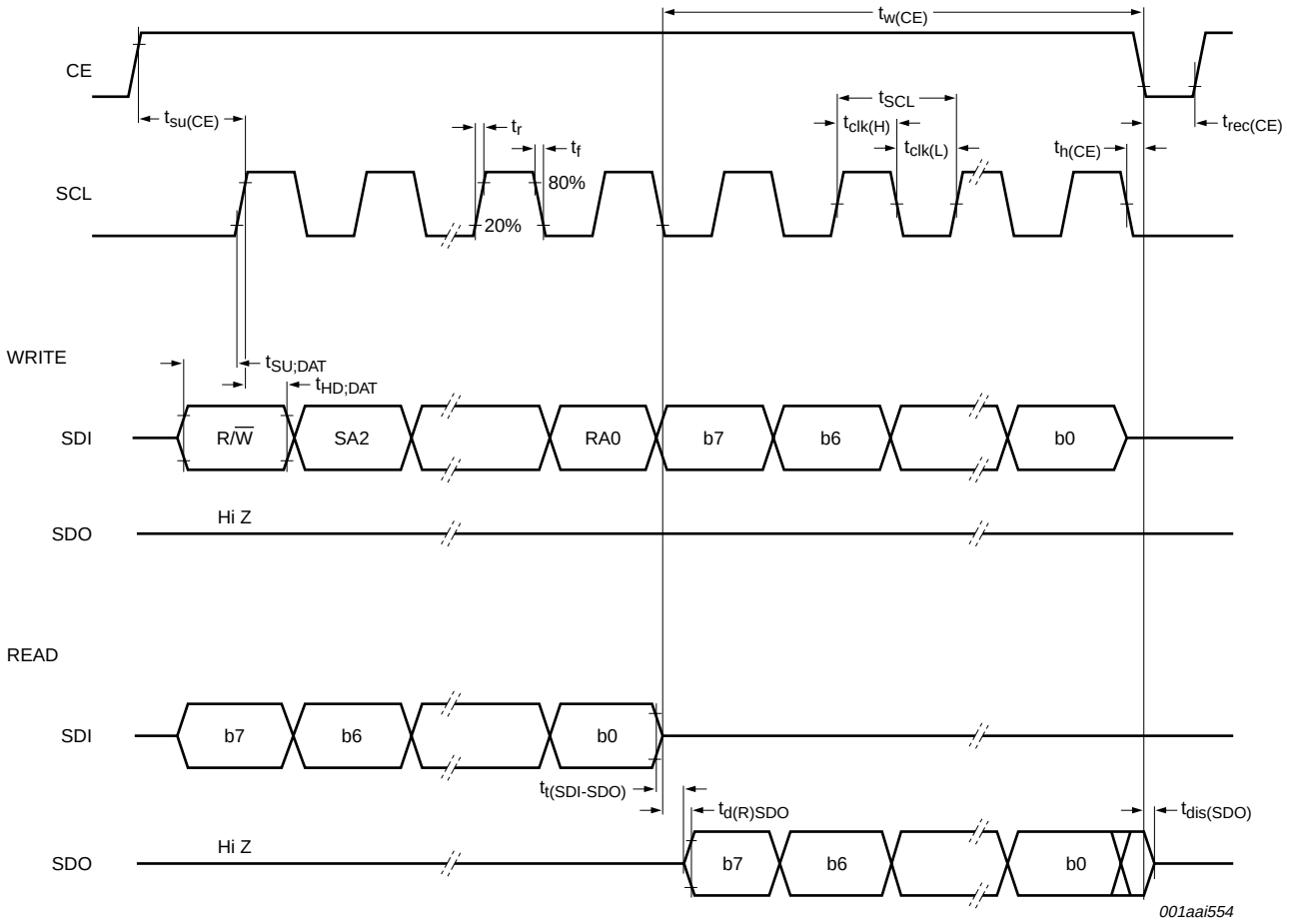
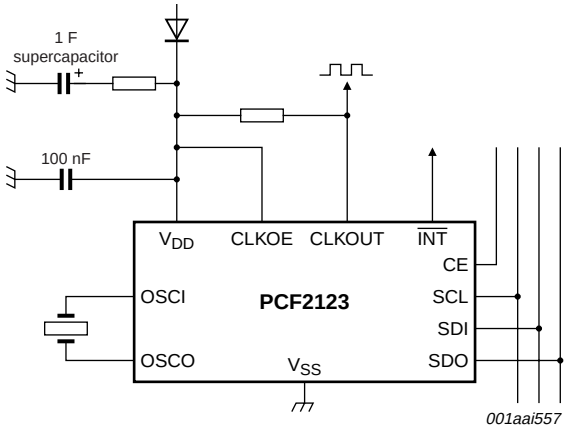


Fig 27. SPI-bus timing

13. Application information

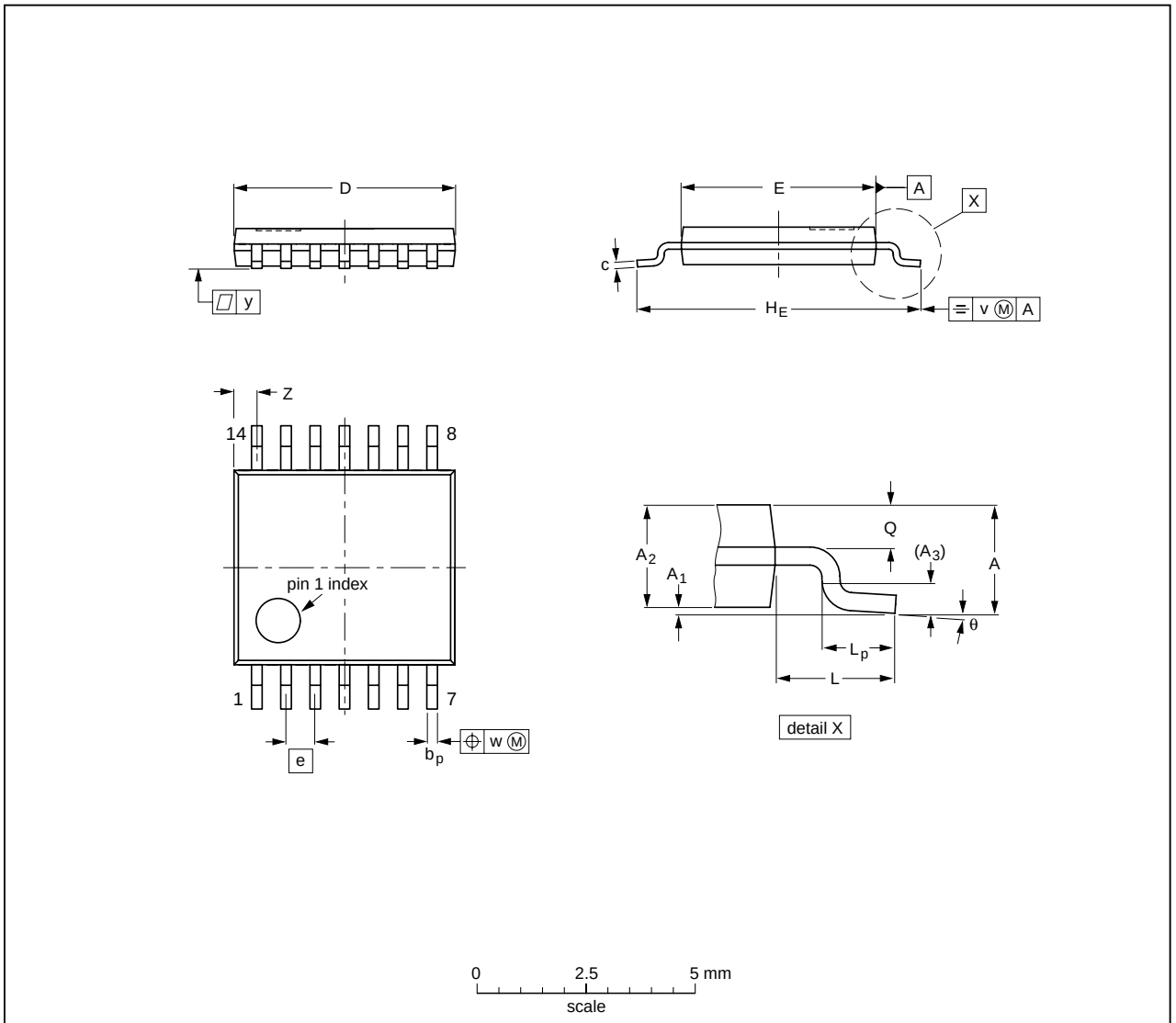


A 1 farad super capacitor combined with a low V_F diode can be used as a standby or back-up supply. With the RTC in its minimum power configuration i.e. timer off and CLKOUT off, the RTC may operate for weeks.

Fig 28. Typical application diagram

14. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

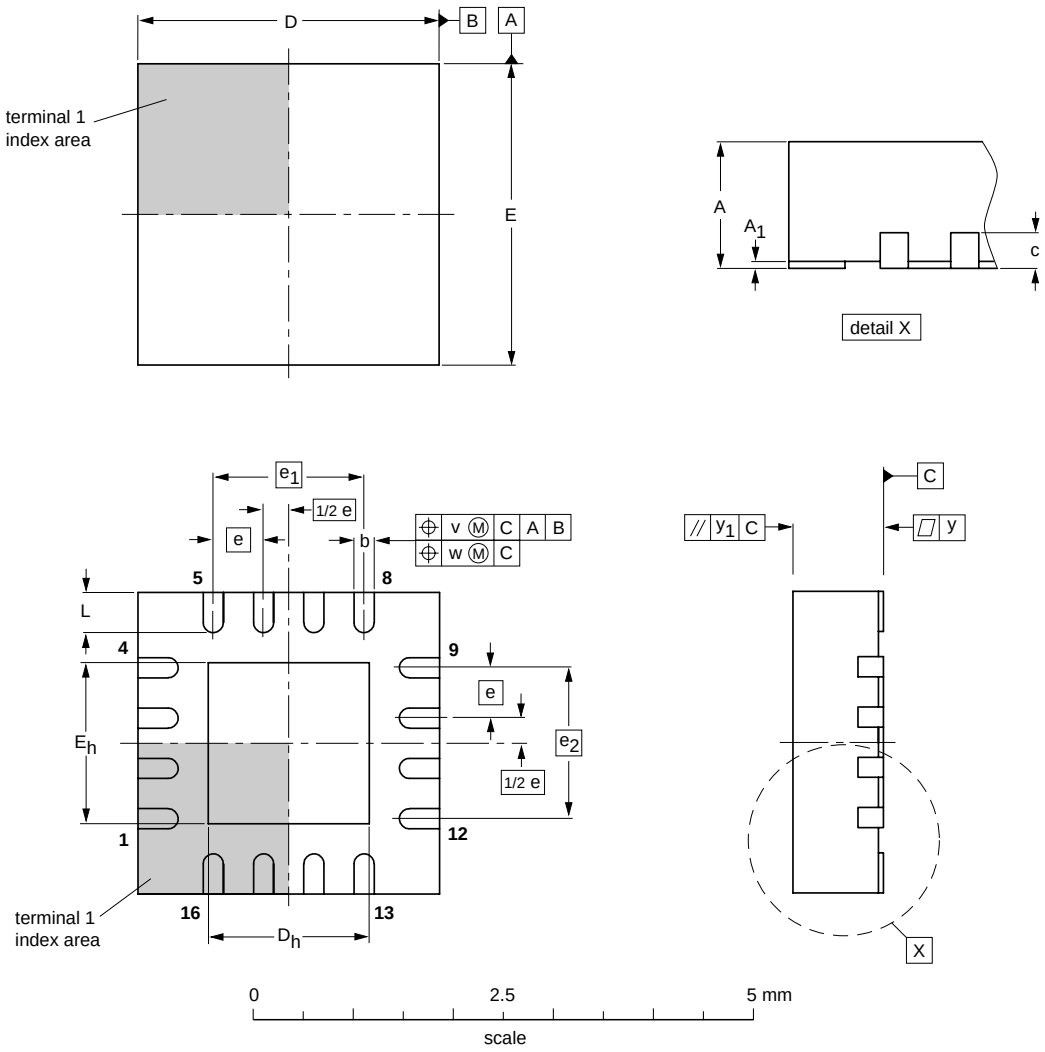
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 29. Package outline of PCF2123TS (SOT402-1)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm **SOT758-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

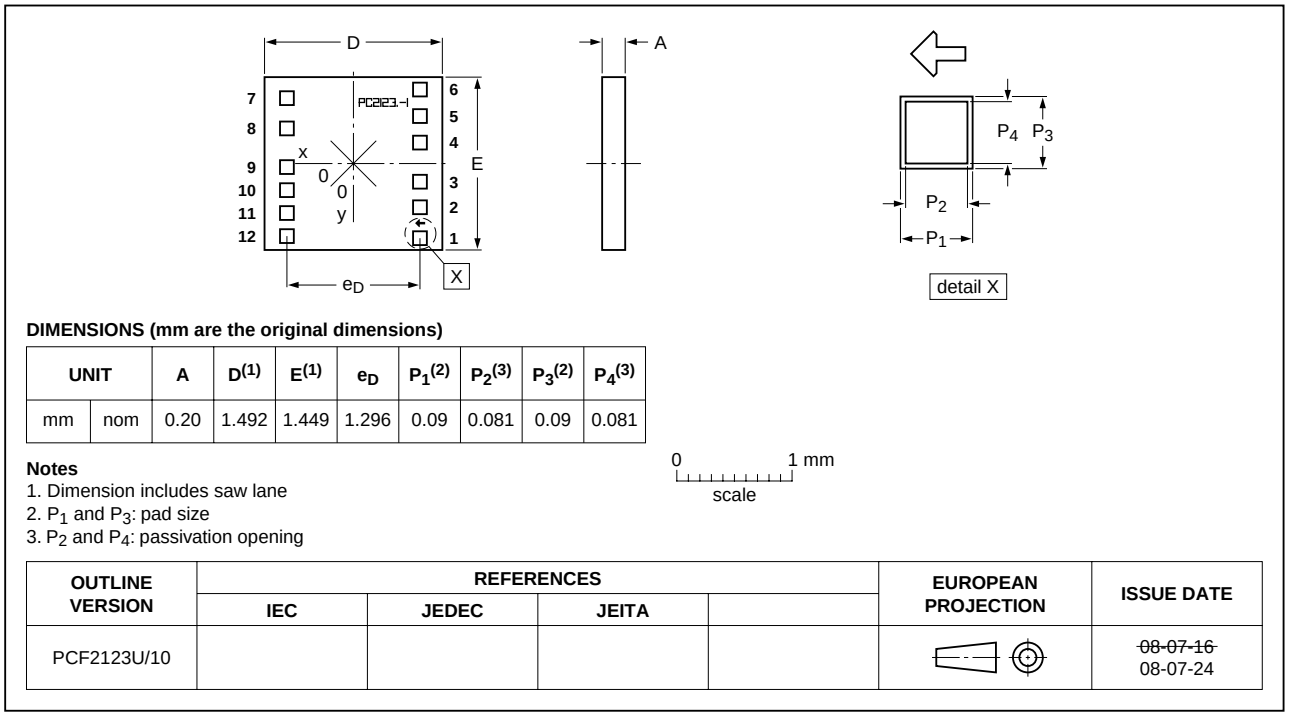
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-03-25~~ 02-10-21

Fig 30. Package outline of PCF2123BS (SOT758-1)

15. Bare die outline

Wire bond die; 12 bonding pads; 1.492 x 1.449 x 0.20 mm **PCF2123U/10**



DIMENSIONS (mm are the original dimensions)

UNIT		A	$D^{(1)}$	$E^{(1)}$	e_D	$P_1^{(2)}$	$P_2^{(3)}$	$P_3^{(2)}$	$P_4^{(3)}$
mm	nom	0.20	1.492	1.449	1.296	0.09	0.081	0.09	0.081

Notes
1. Dimension includes saw lane
2. P_1 and P_3: pad size
3. P_2 and P_4: passivation opening

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PCF2123U/10						~~08-07-16~~ 08-07-24

Fig 31. Bare die outline of PCF2123U/10

Table 46. Bonding pad locations

Symbol	Pad	Coordinates[1]	
		x	y
SDO	1	648.0	–575.0
SDI	2	648.0	–377.0
SCL	3	648.0	–179.0
CLKOE	4	648.0	171.2
CLKOUT	5	648.0	369.2
V_{DD}	6	648.0	625.7
OSCI	7	–648.0	639.0
OSCO	8	–648.0	421.9
TEST	9	–648.0	–25.9
$\overline{INT}$	10	–648.0	–223.9
CE	11	–648.0	–441.0
V_{SS}[2]	12	–648.0	–639.0
Alignment mark		693	–516.2

[1] All coordinates are referenced in µm to the center of the die (see Figure 31).

[2] The substrate (rear side of the die) is wired to V_{SS} but should not be electrically connected.

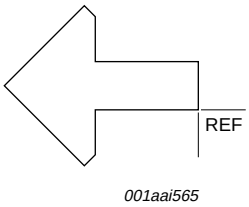


Fig 32. Alignment mark

16. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

17. Packing information

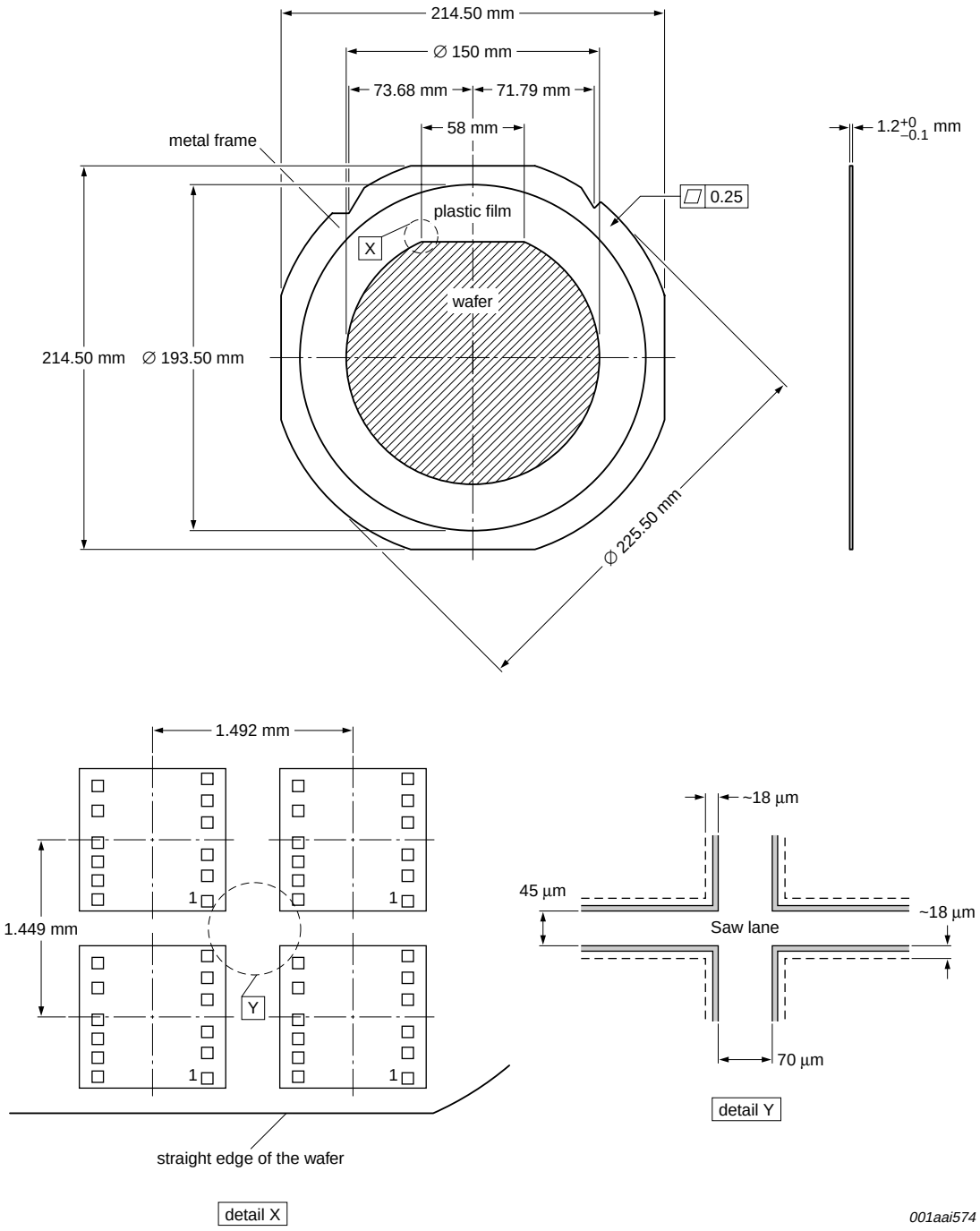


Fig 33. PCF2123U/10, sawn wafer on film frame carrier; 200 µm thickness

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 34) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 47 and 48

Table 47. SnPb eutectic process (from J-STD-020C)

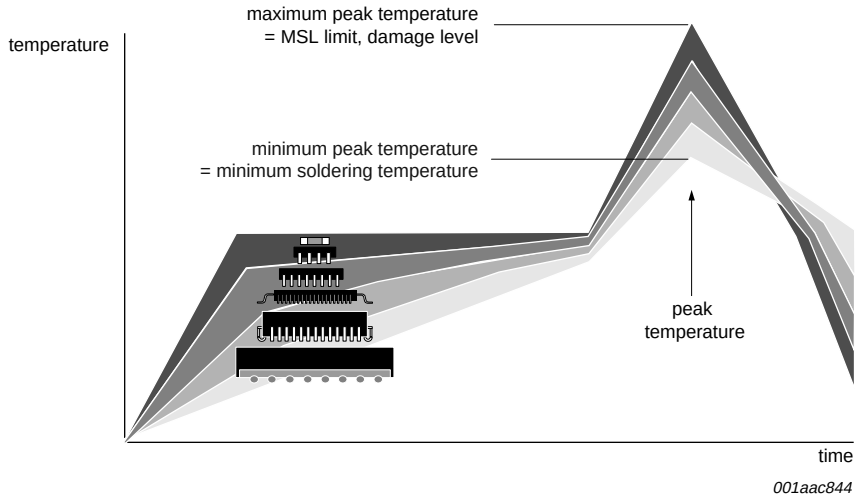
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 48. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 34.



MSL: Moisture Sensitivity Level

Fig 34. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 49. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
BCD	Binary Coded Decimal
FFC	Film Frame Carrier
HBM	Human Body Model
LSB	Least Significant Bit
MM	Machine Model
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
RTC	Real Time Clock
SMD	Surface Mount Device
SPI	Serial Peripheral Interface

20. Revision history

Table 50. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF2123_1	20081119	Product data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 19 November 2008
Document identifier: PCF2123_1