

# DATA SHEET

## **74LVC109**

Dual  $\overline{JK}$  flip-flop with set and reset;  
positive-edge trigger

Product specification  
Supersedes data of 1997 Mar 18  
IC24 Data Handbook

1998 Apr 28

Dual  $\overline{JK}$  flip-flop with set and reset; positive-edge trigger

74LVC109

## FEATURES

- Wide supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output capability: standard
- $I_{CC}$  category: flip-flops

## DESCRIPTION

The 74LVC109 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT109.

The 74LVC109 is a dual positive-edge triggered  $\overline{JK}$ -type flip-flop featuring individual J,  $\overline{K}$  inputs, clock (CP) inputs, set ( $\overline{S}_D$ ) and reset ( $\overline{R}_D$ ) inputs; also complementary Q and  $\overline{Q}$  outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and  $\overline{K}$  inputs control the state changes of the flip-flops as described in the mode select function table. The J and  $\overline{K}$  inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. The  $\overline{JK}$  design allows operation as a D-type flip-flop by tying the J and  $\overline{K}$  inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay nCP to nQ, n $\overline{Q}$ n $\overline{S}_D$ to nQ, n $\overline{Q}$ n $\overline{R}_D$ to nQ, n $\overline{Q}$	$C_L = 50$ pF; $V_{CC} = 3.3$ V	4.0 4.5 4.5	ns
$f_{max}$	Maximum clock frequency		250	MHz
$C_I$	Input capacitance		5.0	pF
$C_{PD}$	Power dissipation capacitance per flip-flop	$V_I = \text{GND to } V_{CC}^1$	27	pF

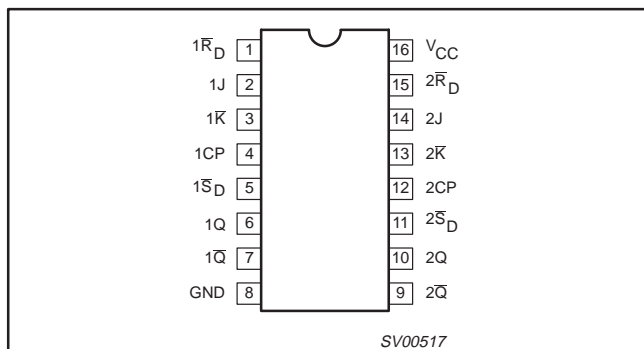
## NOTE:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic SO	$-40^\circ\text{C to } +85^\circ\text{C}$	74LVC109 D	74LVC109 D	SOT109-1
16-Pin Plastic SSOP Type II	$-40^\circ\text{C to } +85^\circ\text{C}$	74LVC109 DB	74LVC109 DB	SOT338-1
16-Pin Plastic TSSOP Type I	$-40^\circ\text{C to } +85^\circ\text{C}$	74LVC109 PW	74LVC109PW DH	SOT403-1

## PIN CONFIGURATION



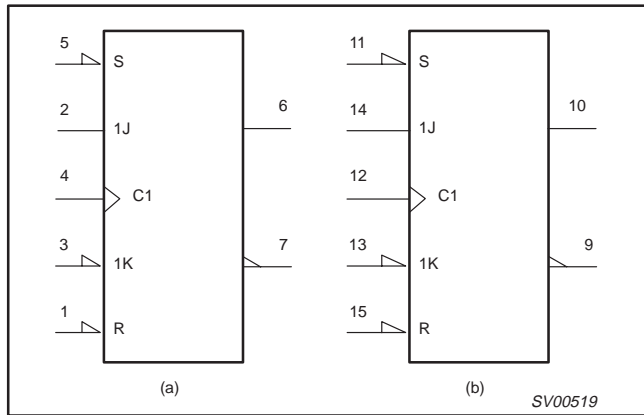
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	$1\overline{R}_D, 2\overline{R}_D$	Asynchronous reset input (active LOW)
2, 14, 3, 13	1J, 2J, 1 $\overline{K}$ , 2 $\overline{K}$	Synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	Clock input (LOW-to-HIGH, edge-triggered)
5, 11	$1\overline{S}_D, 2\overline{S}_D$	Asynchronous set inputs (active LOW)
6, 10	1Q, 2Q	True flip-flop outputs
7, 9	$1\overline{Q}, 2\overline{Q}$	Complement flip-flop outputs
8	GND	Ground (0 V)
16	$V_{CC}$	Positive supply voltage

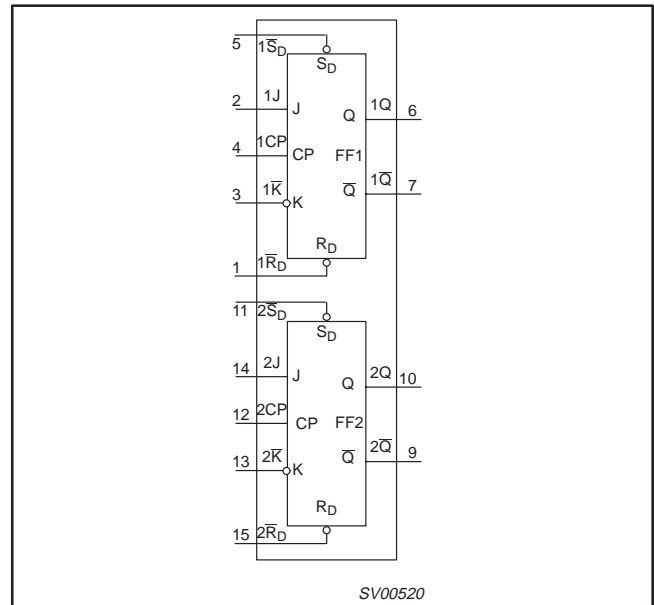
# Dual JK flip-flop with set and reset; positive-edge trigger

## 74LVC109

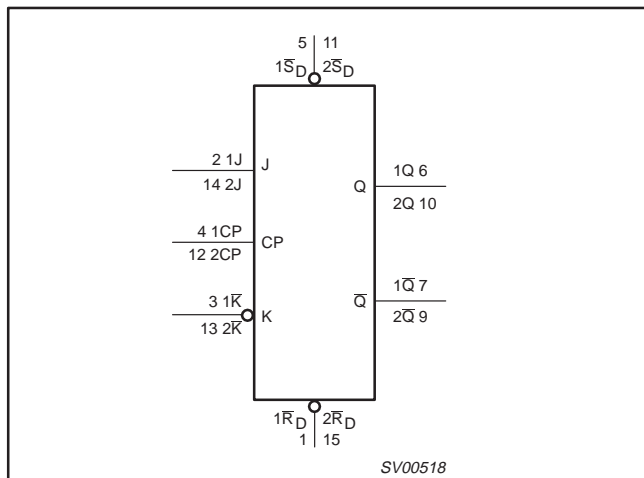
### LOGIC SYMBOL (IEEE/IEC)



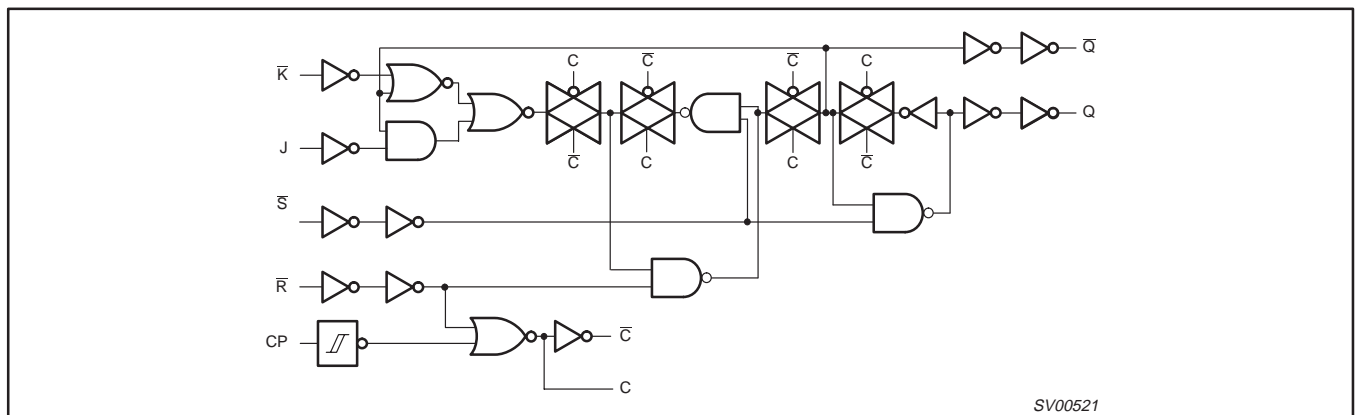
### FUNCTIONAL DIAGRAM



### LOGIC SYMBOL



### LOGIC DIAGRAM



## Dual JK flip-flop with set and reset; positive-edge trigger

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## FUNCTION TABLE

OPERATING MODES	INPUTS					OUTPUTS	
	nS <sub>D</sub>	nR <sub>D</sub>	nCP	nJ	nK	nQ	nQ̄
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	q̄	q
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	q̄

## NOTES:

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.

X = don't care

↑ = LOW-to-HIGH CP transition

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V <sub>I</sub>	DC input voltage range		0	5.5	V
V <sub>O</sub>	DC output voltage range		0	V <sub>CC</sub>	V
T <sub>amb</sub>	Operating free-air temperature range		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6V	0	10	

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +6.5	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage	Note 2	-0.5 to +5.5	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	±50	mA
V <sub>O</sub>	DC output voltage	Note 2	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>O</sub>	DC output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±50	mA
I <sub>GND</sub> , I <sub>CC</sub>	DC V <sub>CC</sub> or GND current		±100	mA
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C
P <sub>TOT</sub>	Power dissipation per package - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K	500	mW
		above +60°C derate linearly with 5.5 mW/K	500	

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## Dual JK flip-flop with set and reset; positive-edge trigger

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 1.0			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND		±0.1	±5	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	10	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	μA

**NOTE:**1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.**AC CHARACTERISTICS**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns; C<sub>L</sub> = 50 pF; R<sub>L</sub> = 500Ω; T<sub>amb</sub> = -40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT	
			V <sub>CC</sub> = 3.3V ±0.3V			V <sub>CC</sub> = 2.7V				
			MIN	TYP <sup>1</sup>	MAX	MIN	TYP NO TAG	MAX		
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nCP to nQ, nQ̄	Figures 1, 3		4.3	7.5				8.5	ns
t <sub>PLH</sub>	Propagation delay nS <sub>D</sub> to nQ nR <sub>D</sub> to nQ̄	Figures 2, 3		4.5	8.0				9.0	ns
t <sub>PHL</sub>	Propagation delay nS <sub>D</sub> to nQ̄ nR <sub>D</sub> to nQ	Figures 2, 3		5.2	9.0				10	ns
t <sub>W</sub>	Clock pulse width HIGH or LOW	Figure 1	3.3	2.0						ns
t <sub>W</sub>	Set or reset pulse width HIGH or LOW	Figure 2	3.0							ns
t <sub>rem</sub>	Removal time nS <sub>D</sub> , nR <sub>D</sub> to nCP	Figure 2	3.0							ns
t <sub>su</sub>	Set-up time nJ, nK̄ to CP	Figure 1	2.5							ns
t <sub>h</sub>	Hold time nJ, nK̄ to nCP	Figure 1	2.0							ns
f <sub>max</sub>	Maximum clock pulse frequency	Figure 1	150	225						MHz

**NOTE:**1. These typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

# Dual JK flip-flop with set and reset; positive-edge trigger

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### AC WAVEFORMS

$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

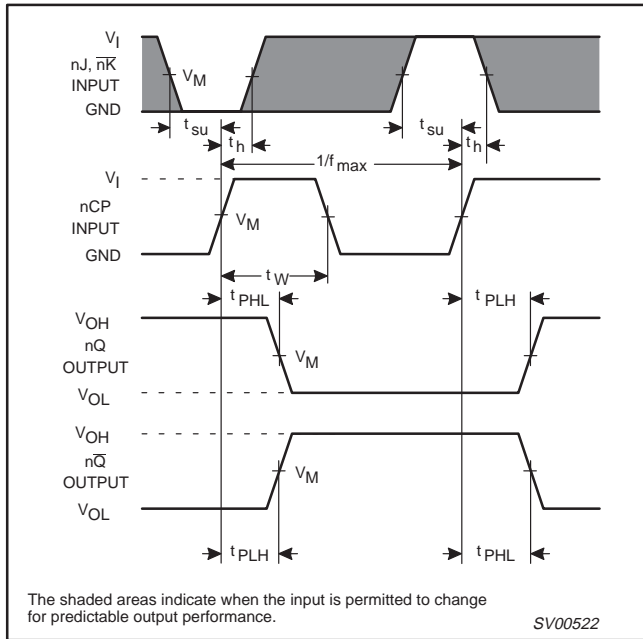


Figure 1. Clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nJ and nK to nCP set-up, the nCP to nJ, nK hold times and the maximum clock pulse frequency.

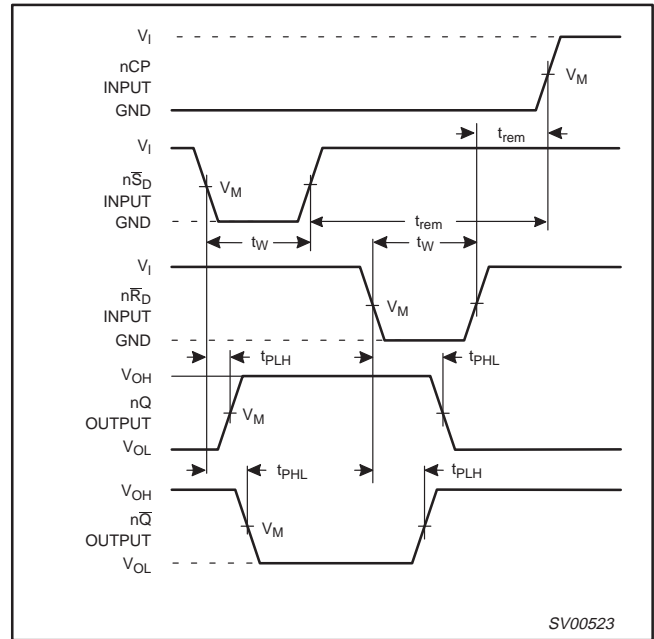


Figure 2. Set (nSD) and reset (nRD) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nRD, nSD to nCP removal time.

### TEST CIRCUIT

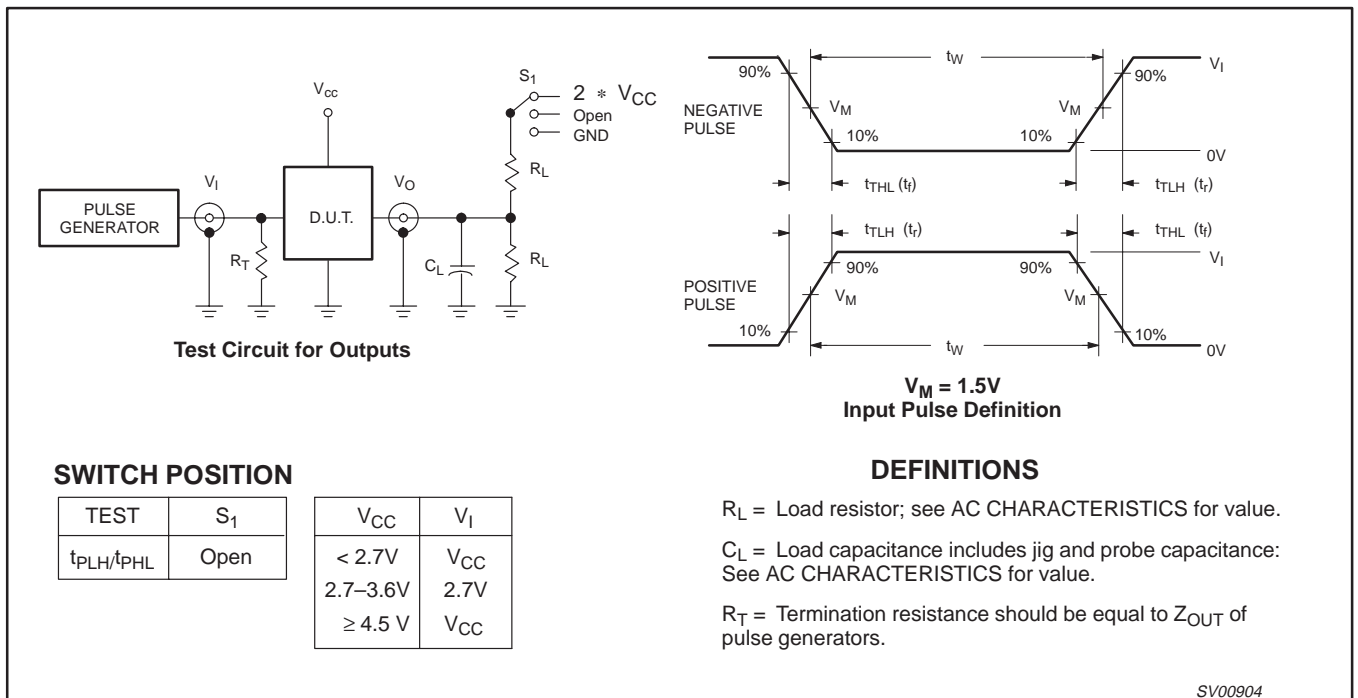


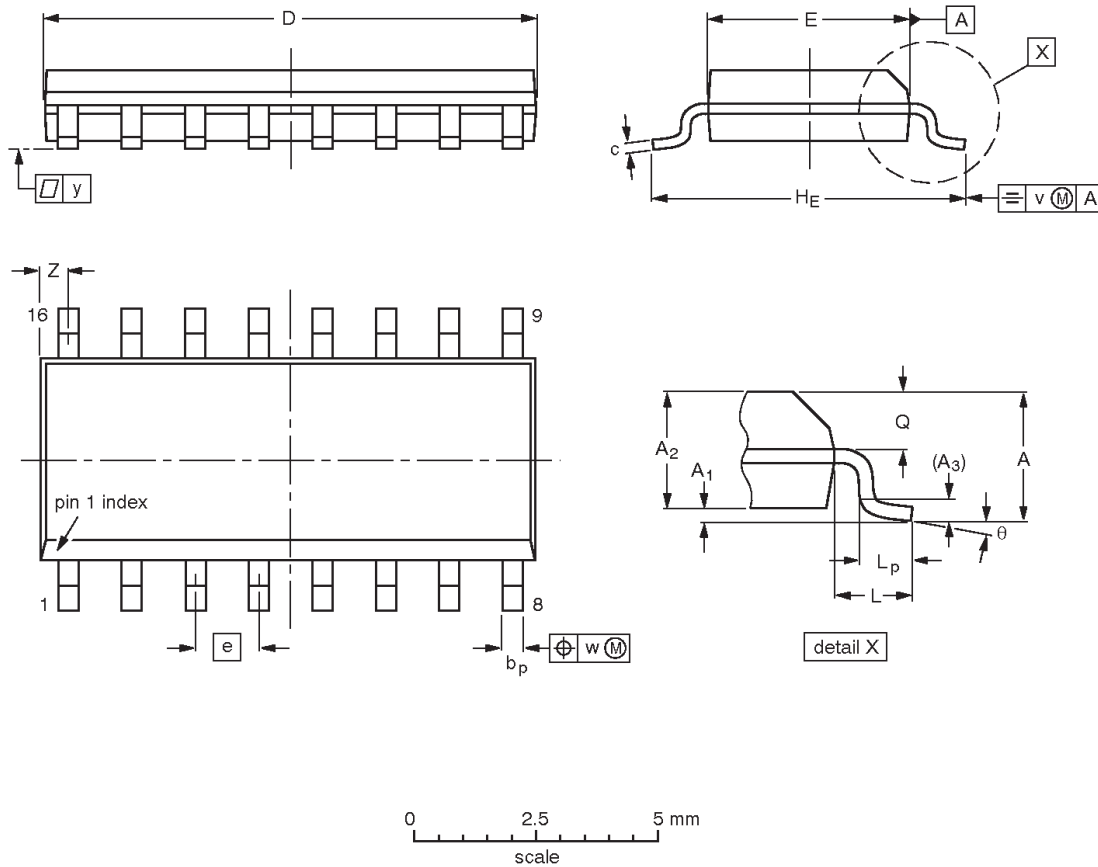
Figure 3. Load circuitry for switching times.

# Dual JK flip-flop with set and reset; positive-edge trigger

## 74LVC109

**SO16: plastic small outline package; 16 leads; body width 3.9 mm**

**SOT109-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

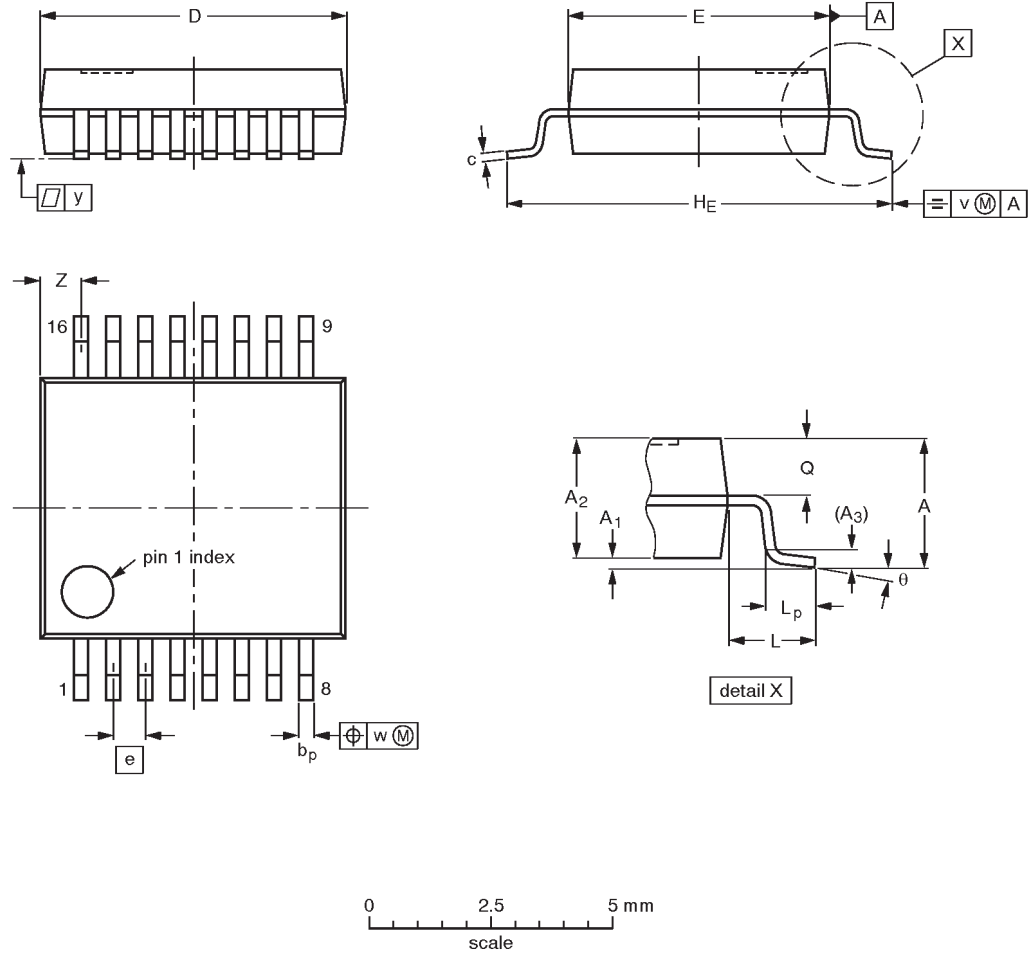
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

# Dual JK flip-flop with set and reset; positive-edge trigger

## 74LVC109

**SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm**

**SOT338-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14- 95-02-04

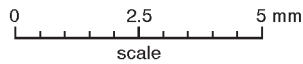
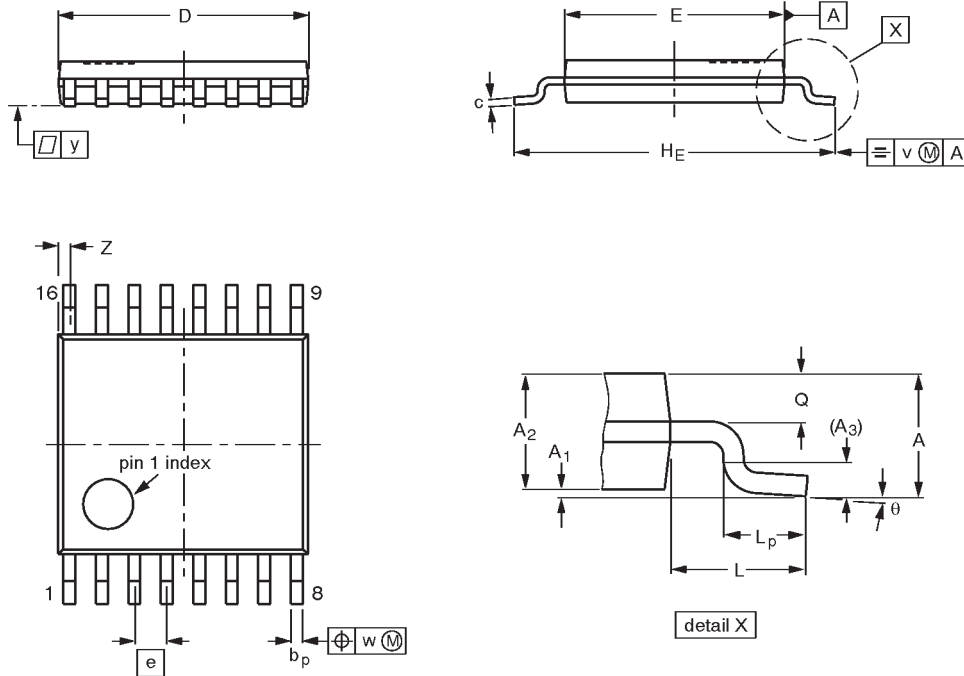


# Dual JK flip-flop with set and reset; positive-edge trigger

## 74LVC109

**TSSOP16:** plastic thin shrink small outline package; 16 leads; body width 4.4 mm

**SOT403-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

## Dual JK flip-flop with set and reset; positive-edge trigger

74LVC109

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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**811 East Arques Avenue**  
**P.O. Box 3409**  
**Sunnyvale, California 94088-3409**  
**Telephone 800-234-7381**

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