DATA SHEET

PCF85102C-2; PCF85103C-2

256 × 8-bit CMOS EEPROMs with I²C-bus interface

Product specification

2000 Feb 15

File under Integrated Circuits, IC12

Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Low power CMOS:
  - maximum operating current: 2.0 mA
  - maximum standby current 10 µA (at 6.0 V), typical 4 µA.
- Non-volatile storage of:
  - 2 kbits organized as 256 × 8-bit.
- Single supply with full operation down to 2.5 V
- On-chip voltage multiplier
- Serial input/output I²C-bus
- Write operations:
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte).
- Read operations:
  - sequential read
  - random read.
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code
- Endurance: 1000000 Erase/Write (E/W) cycles at T_{amb} = 22 °C
- 10 years non-volatile data retention time
- Standard industrial pinning (pin 7 not connected)
- Up to sixteen EEPROMs addressable in one I²C-bus using both PCF85102 and PCF85103 in combination.

2 GENERAL DESCRIPTION

The PCF85102C-2 and PCF85103C-2 (further referred to as PCF8510xC-2) are 2 kbits (256 × 8-bit) floating gate Electrically Erasable Programmable Read Only Memories (EEPROMs). Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.
The PCF8510x-2 is pin compatible to widely used industrial pinning (pin 7 not connected).

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to sixteen PCF8510xC-2 devices may be connected to the I²C-bus. This is possible with the introduction of a second device selection code. Chip select is accomplished by three address inputs (A0, A1 and A2) for each PCF8510xC-2 type.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current read	f_{SCL} = 100 kHz			
		V_{DD} = 2.5 V	–	60	µA
		V_{DD} = 6.0 V	–	200	µA
I_{DDW}	supply current E/W	f_{SCL} = 100 kHz			
		V_{DD} = 2.5 V	–	0.6	mA
		V_{DD} = 6.0 V	–	2.0	mA
I_{DDstb}	standby supply current	V_{DD} = 2.5 V	–	3.5	µA
		V_{DD} = 6.0 V	–	10	µA

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF85102C-2P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF85103C-2P			
PCF85102C-2T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCF85103C-2T			

5 DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
PCF85102-C	1	0	1	0	A2	A1	A0	R/$\overline{W}$
PCF85103-C	0	0	1	0	A2	A1	A0	R/$\overline{W}$

Note

1. The Most Significant Bit (MSB) ‘b7’ is sent first.

6 BLOCK DIAGRAM

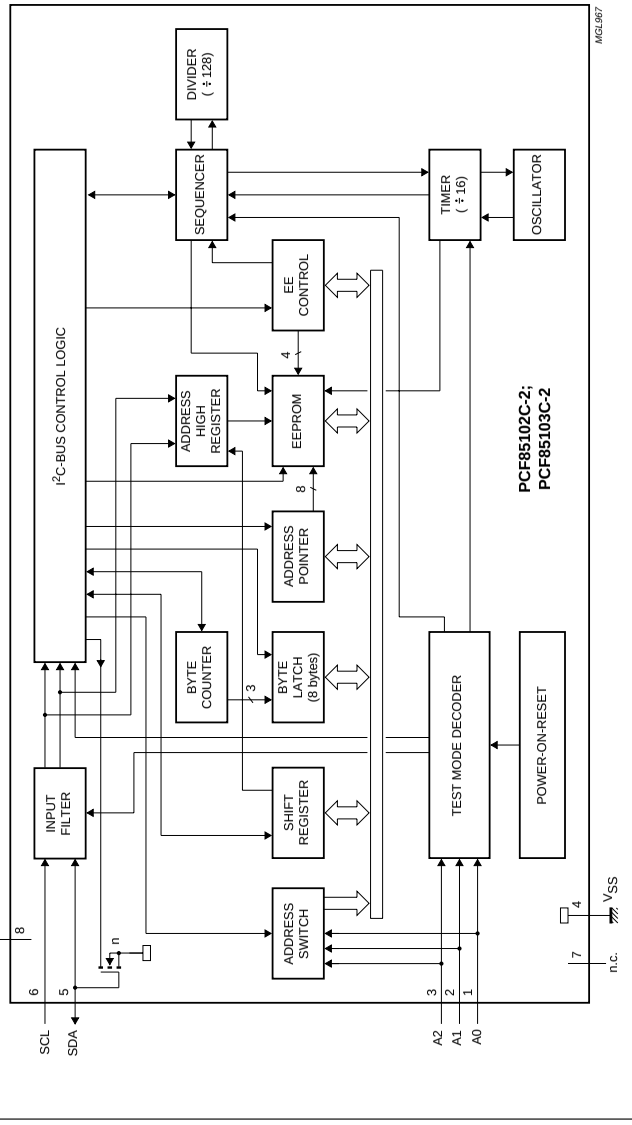


Fig.1 Block diagram.

The pin numbers in this block diagram refer to the PCF85102C-2.
For PCF85103C-2, please see Chapter 7.

7 PINNING

PCF8510xC-2 has standard industrial pinning which will be compatible for most applications.

7.1 Pin description PCF85102C-2

SYMBOL	PIN	DESCRIPTION
A0	1	address input 0
A1	2	address input 1
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I^2C-bus)
SCL	6	serial clock input (I^2C-bus)
n.c.	7	not connected
V_{DD}	8	positive supply voltage

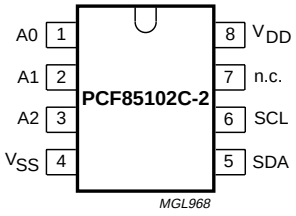


Fig.2 Pin configuration PCF85102C-2.

7.2 Pin description PCF85103C-2

SYMBOL	PIN	DESCRIPTION
WP	1	address input 0
A1	2	address input 1
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I^2C-bus)
SCL	6	serial clock input (I^2C-bus)
n.c.	7	not connected
V_{DD}	8	positive supply voltage

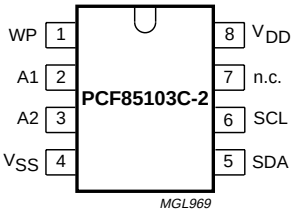


Fig.3 Pin configuration PCF85103C-2.

8 I²C-BUS PROTOCOL

The I²C-bus is designed for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

8.1 Bus conditions

The following bus conditions have been defined:

- **Bus not busy**: both data and clock lines remain HIGH.
- **Start data transfer**: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the START condition.
- **Stop data transfer**: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the STOP condition.
- **Data valid**: the state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

8.2 Data transfer

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes, transferred between the START and STOP conditions is limited to seven bytes in the E/W mode and eight bytes in the page E/W mode.

Data transfer is unlimited in the read mode.
The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications, a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF8510xC-2 operates in both modes.

By definition, a device that sends a signal is called a ‘transmitter’, and the device that receives the signal is called a ‘receiver’. The device that controls the signal is called the ‘master’. The devices that are controlled by the master are called ‘slaves’.

Each byte is followed by one acknowledge bit, which is placed on the bus at a HIGH level by the transmitter.
The master generates an extra acknowledge-related clock pulse. The slave receiver that is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull the SDA line down during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master generation of the STOP condition.

8.3 Device addressing

Following a START condition, the bus master must output the address of the slave it is accessing. The four MSBs of the slave address are the device type identifier (see Fig.4 and Fig.5). For the PCF85102C-2, this is fixed to '1010', for the PCF85103C-2 to '0010'.

The next three significant bits address a particular device or memory page (page = 256 bytes of memory). A system could have up to sixteen PCF8510xC-2 devices on the bus. This can be achieved with eight PCF85102C devices and eight PCF85103C devices, combined on one I²C-bus. The eight addresses are defined by the state of the A0, A1 and A2 inputs per type.

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read operation is selected.

Address bits must be connected to either V_{DD} or V_{SS}.

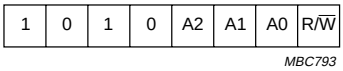


Fig.4 Slave address for PCF85102C-2.

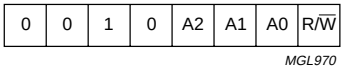


Fig.5 Slave address for PCF85103C-2.

8.3.1 Remark

The I²C-bus device select address '0010' is not exclusively reserved for device PCF85103C-2. Therefore, multiple use has to be checked in advance.

8.4 Write operations

8.4.1 Byte/word write

For a write operation, the PCF8510xC-2 requires a second address field. This address field is a word address providing access to the 256 words of memory. On receipt of the word address, the PCF8510xC-2 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. The word address is automatically incremented. The master can now terminate the transfer by generating a STOP condition or transmitting up to six more bytes of data and then terminating by generating a STOP condition.

After this STOP condition, the E/W cycle starts and the bus is free for another transmission. The duration of the E/W cycle is 10 ms per byte.

During the E/W cycle, the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

8.4.2 Page write

The PCF8510xC-2 is capable of an 8-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte, the PCF8510xC-2 will respond with an acknowledge.
The typical E/W time in this mode is 9 × 3.5 ms = 31.5 ms. Erasing a block of eight bytes in page mode takes a typical 3.5 ms and sequential writing of these eight bytes another typical 28 ms.

After the receipt of each data byte, the three low order bits of the word address are internally incremented. The five high order bits of the address remain unchanged.
The slave acknowledges the reception of each data byte with an ACK. The I²C-bus data transfer is terminated by the master after the eighth byte with a STOP condition. If the master transmits more than eight bytes prior to generating the STOP condition, no acknowledge will be given on the ninth (and following) data bytes. Also, the whole transmission will be ignored and no programming will be done. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

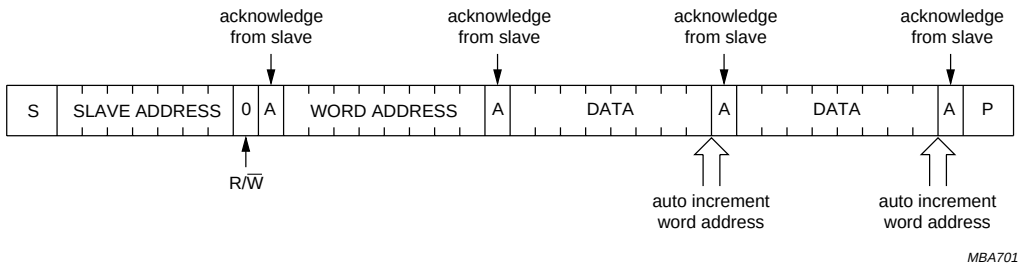


Fig.6 Auto increment memory word address; two byte write.

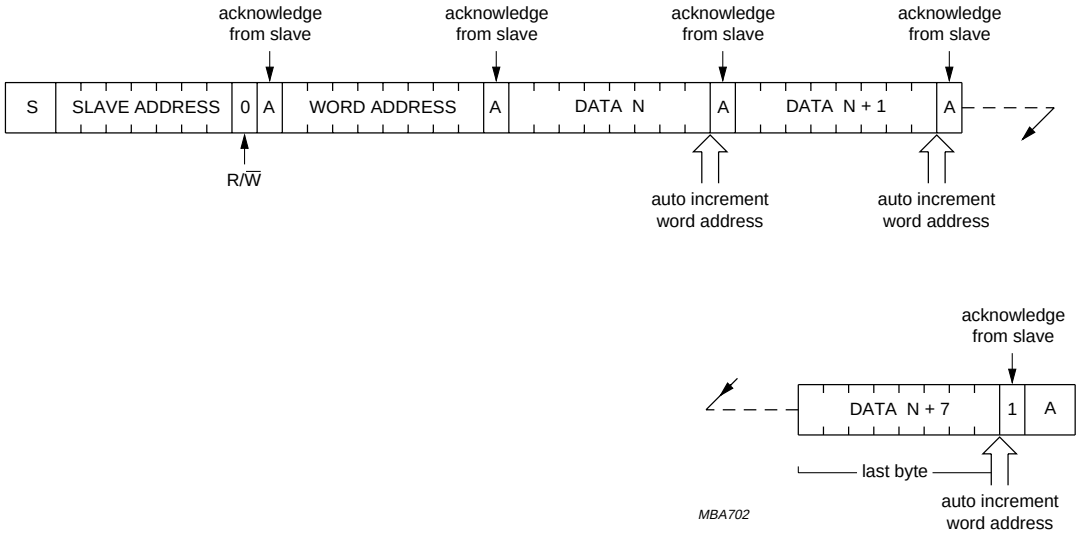


Fig.7 Page write operation; eight bytes.

8.5 Read operations

The read operations are initiated in the same way as write operations, with the exception that the LSB of the slave address is set to logic 1.

There are three basic read operations; current address read, random read and sequential read sequential read.

8.5.1 REMARK

The lower eight bits of the word address are incremented after each transmission of a data byte (read or write). The MSB of the word address, which is defined in the slave address, is not changed when the word address count overflows. Thus, the word address overflows from 255 to 0.

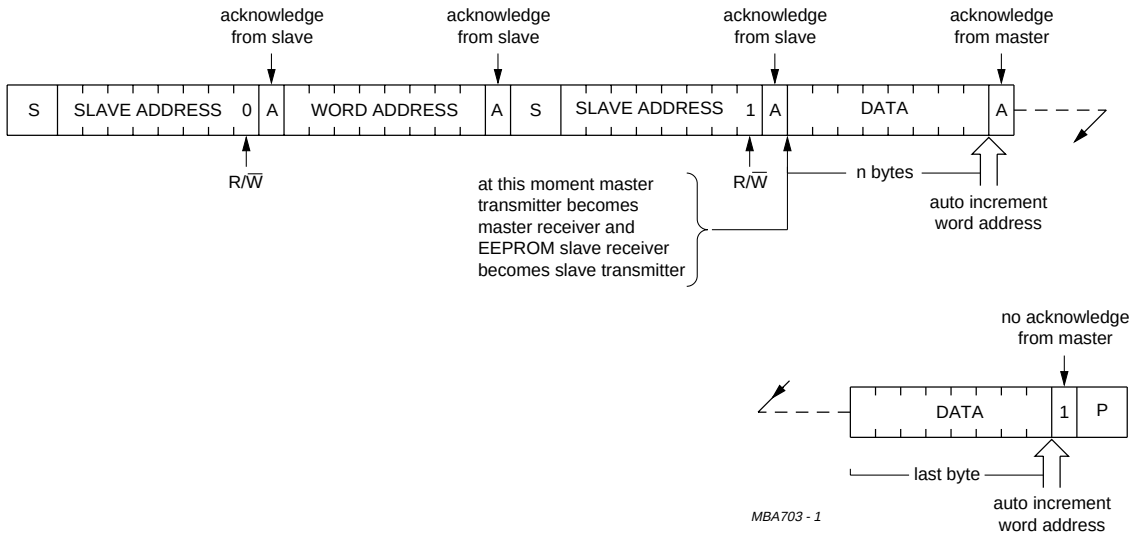


Fig.8 Master reads PCF8510xC-2 slave after setting word address (write word address; read data).

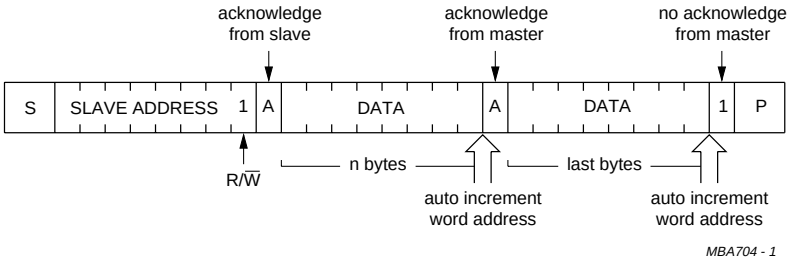


Fig.9 Master reads PCF8510xC-2 immediately after first byte (read mode).

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.3	+6.5	V
V_I	input voltage on input pins	$\|Z_i\| > 500\ \Omega$	$V_{SS} - 0.8$	+6.5	V
I_I	input current on input pins		–	1	mA
I_O	output current		–	10	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+85	°C

10 CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current read	f_{SCL} = 100 kHz			
		V_{DD} = 2.5 V	–	60	µA
		V_{DD} = 6.0 V	–	200	µA
I_{DDW}	supply current E/W	f_{SCL} = 100 kHz			
		V_{DD} = 2.5 V	–	0.6	mA
		V_{DD} = 6.0 V	–	2.0	mA
I_{DDstb}	standby supply current	V_{DD} = 2.5 V	–	3.5	µA
		V_{DD} = 6.0 V	–	10	µA
SCL input (pin 6)					
V_{IL}	LOW-level input voltage		–0.8	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	6.5	V
$\|I_{LI}\|$	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	±1	µA
f_{SCL}	clock frequency		0	100	kHz
C_i	input capacitance	$V_I = V_{SS}$	–	7	pF
SDA input/output (pin 5)					
V_{IL}	LOW-level input voltage		–0.8	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	6.5	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA; $V_{DD(min)}$	–	0.4	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	1	µA
C_i	input capacitance	$V_I = V_{SS}$	–	7	pF
Data retention time					
$t_{D(ret)}$	data retention time	T_{amb} = 55 °C	10	–	years

11 I²C-BUS CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}; see Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	clock frequency		0	100	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	–	µs
$t_{HD;STA}$	START condition hold time after which first clock pulse is generated		4.0	–	µs
t_{LOW}	LOW-level clock period		4.7	–	µs
t_{HIGH}	HIGH-level clock period		4.0	–	µs
$t_{SU;STA}$	set-up time for START condition	repeated start	4.7	–	µs
$t_{HD;DAT}$	data hold time				
	for bus compatible masters		5	–	µs
	for bus devices	note 1	0	–	ns
$t_{SU;DAT}$	data set-up time		250	–	ns
t_r	SDA and SCL rise time		–	1	µs
t_f	SDA and SCL fall time		–	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	µs

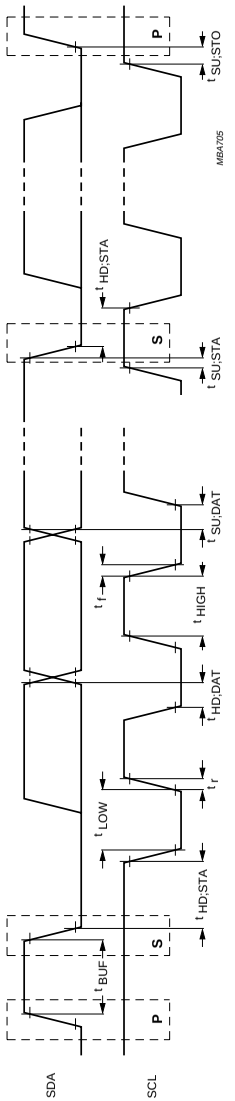
Note

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.

12 WRITE CYCLE LIMITS

Selection of the chip address is achieved by connecting the A0, A1 and A2 inputs to either V_{SS} or V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
E/W cycle timing						
$t_{E/W}$	E/W cycle time	internal oscillator	–	7	–	ms
Endurance						
$N_{E/W}$	E/W cycle per byte	T_{amb} = −40 to +85 °C	100000	–	–	cycles
		T_{amb} = 22 °C	–	1000000	–	cycles

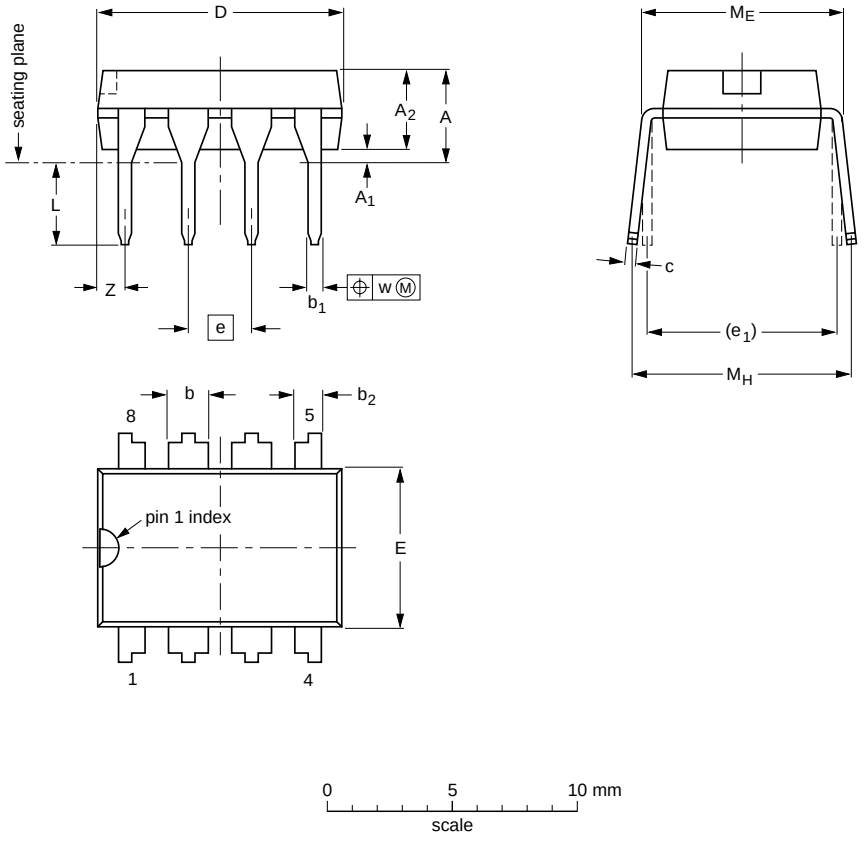


P = STOP condition; **S** = START condition.

Fig.10 Timing requirements for the I²C-bus.

13 PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

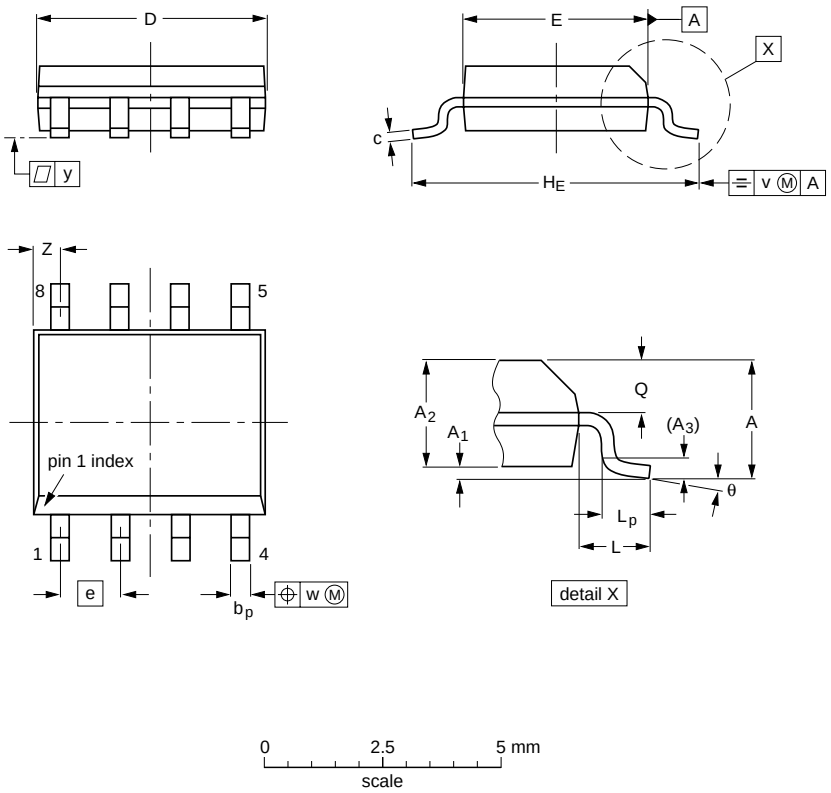
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

14 SOLDERING

14.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

14.2 Through-hole mount packages

14.2.1 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

14.3 Surface mount packages

14.3.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

14.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.4 Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

17 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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