PCF2119x

LCD controllers/drivers

Rev. 7 — 15 November 2010 Product data sheet

1. General description

The PCF2119x is a low power CMOS[1] LCD controller and driver, designed to drive a dot matrix LCD display of 2-lines by 16 characters or 1-line by 32 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2119x interfaces to most microcontrollers via a 4-bit or 8-bit bus or via the 2-wire I^2C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters.

The letter 'x' in PCF2119x characterizes the built-in character set. Various character sets can be manufactured on request. In addition 16 user defined symbols (5 × 8 dot format) are available.

2. Features and benefits

- Single-chip LCD controller and driver
- 2-line display of up to 16 characters plus 160 icons or 1-line display of up to 32 characters plus 160 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese) and user defined symbols
- Reduced current consumption while displaying icons only
- Icon blink function
- On-chip:
  - Configurable 4, 3 or 2 times voltage multiplier generating LCD supply voltage, independent of V_{DD}, programmable by instruction (external supply also possible)
  - Temperature compensation of on-chip generated V_{LCDOUT}: −0.16 %/K to −0.24 %/K (programmable by instruction)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Display Data RAM (DDRAM): 80 characters
- Character Generator ROM (CGROM): 240 characters (5 × 8)
- Character Generator RAM (CGRAM): 16 characters (5 × 8); 4 characters used to drive 160 icons, 8 characters used if icon blink feature is used in application
- 4-bit or 8-bit parallel bus and 2-wire I^2C-bus interface
- Manufactured in silicon gate CMOS process
- 18 row and 80 column outputs
- Multiplex rates 1:18 (2-line display or 1-line display), 1:9 (for 1-line display of up to 16 characters and 80 icons) and 1:2 (for icon only mode)

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20.

- Uses common 11 code instruction set (extended)
- Logic supply voltage: $V_{DD1} - V_{SS1}$ = 1.5 V to 5.5 V (chip may be driven with two battery cells)
- LCD supply voltage: $V_{LCDOUT} - V_{SS2}$ = 2.2 V to 6.5 V
- V_{LCD} generator supply voltage: $V_{DD2} - V_{SS2}$ = 2.2 V to 4 V and $V_{DD3} - V_{SS2}$ = 2.2 V to 4 V
- Direct mode to save current consumption for icon mode and multiplex drive mode 1:9 (depending on V_{DD2} value and LCD liquid properties)
- Very low current consumption (20 μA to 200 μA):
  - Icon mode: < 25 μA
  - Power-down mode: < 2 μA
- Icon mode is used to save current. When only icons are displayed, a much lower LCD operating voltage can be used and the switching frequency of the LCD outputs is reduced; in most applications it is possible to use V_{DD} as LCD supply voltage

3. Applications

- Telecom equipment
- Portable instruments
- Point-of-sale terminals

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2119AU/2DA/2	PCF2119x	bare die: 168 bumps; 7.59 × 1.71 × 0.38 mm	PCF2119x
PCF2119DU/2/2	PCF2119x	bare die: 168 bumps; 7.59 × 1.71 × 0.38 mm	PCF2119x
PCF2119FU/2/F2	PCF2119x	bare die: 168 bumps; 7.59 × 1.71 × 0.38 mm	PCF2119x
PCF2119RU/2/F2	PCF2119x	bare die: 168 bumps; 7.59 × 1.71 × 0.38 mm	PCF2119x
PCF2119RU/2DB/2[1]	PCF2119x	bare die: 168 bumps; 7.59 × 1.71 × 0.38 mm	PCF2119x
PCF2119SU/2/F2	PCF2119x	bare die: 168 bumps; 7.59 × 1.71 × 0.38 mm	PCF2119x

[1] With PI scratch protection coating, thickness 3.6 μm.

5. Marking

Table 2. Marking codes

Type number	Marking code
PCF2119AU/2DA/2	PC2119-2
PCF2119DU/2/2	PC2119-2
PCF2119FU/2/F2	PC2119-2
PCF2119RU/2/F2	PC2119-2
PCF2119RU/2DB/2	PC2119-2
PCF2119SU/2/F2	PC2119-2

6. Block diagram

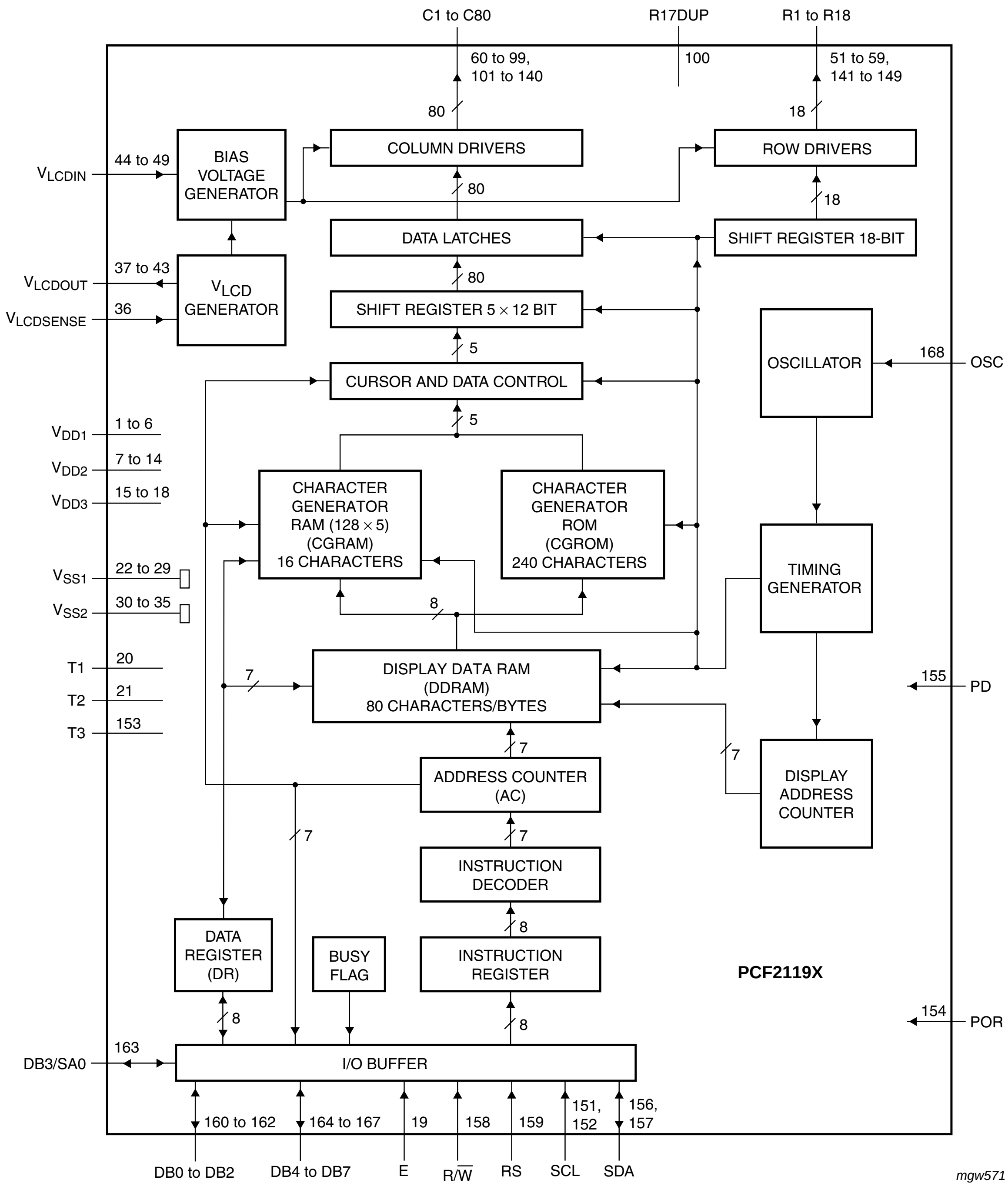
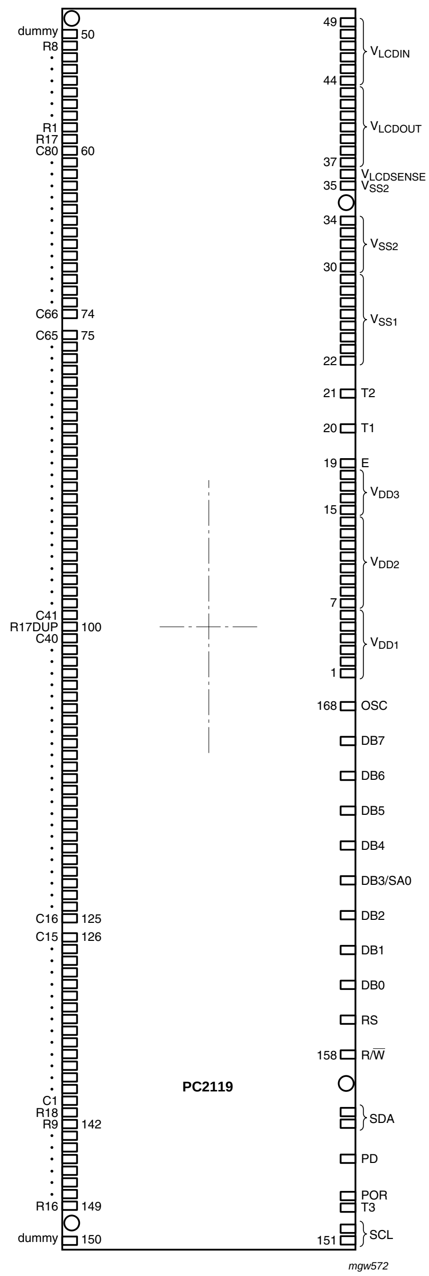


Fig 1. Block diagram

7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 50.

Fig 2. Pinning diagram of PCF2119x (bare die)

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
V_{DD1}	1 to 6		supply voltage 1 (logic)
V_{DD2}	7 to 14	[1]	supply voltage 2 (for high voltage generator)
V_{DD3}	15 to 18	[1]	supply voltage 3 (for high voltage generator)
E	19	[2]	data bus clock input • set HIGH to signal the start of a read or write operation • data is clocked in or out of the chip on the negative edge of the clock
T1 and T2	20 and 21		test pins • must be connected to V_{SS1}
V_{SS1}	22 to 29	[3]	ground supply voltage 1 • for all circuits, except of high voltage generator
V_{SS2}	30 to 35	[3]	ground supply voltage 2 • for high voltage generator
$V_{LCDSENSE}$	36		input for voltage multiplier regulation circuitry and for the bias level generation • if V_{LCD} is generated internally then this pin must be connected to V_{LCDOUT} and V_{LCDIN} • if V_{LCD} is generated externally then this pin must be connected to V_{LCDIN} only
V_{LCDOUT}	37 to 43		V_{LCD} output • if V_{LCD} is generated internally then this pin must be connected to V_{LCDIN} and to $V_{LCDSENSE}$ • if V_{LCD} is generated externally then this pin must be left open-circuit
V_{LCDIN}	44 to 49		input for LCD bias level generator • if V_{LCD} is generated internally then this pin must be connected to V_{LCDOUT} and to $V_{LCDSENSE}$ • if V_{LCD} is generated externally then this pin must be connected to $V_{LCDSENSE}$ and to the external V_{LCD} power supply
dummy	50	[4]	-
R8 to R1, R17, R17DUP, R18, R9 to R16	51 to 58, 59, 100 141, 142 to 149		LCD row driver output • R17 has two pins: R17 and R17DUP • R17 and R18 drive the icons
C80 to C41, C40 to C1	60 to 99, 101 to 140		LCD column driver output
dummy	150	[4]	-
SCL	151 and 152	[5]	I^2C-bus serial clock input
T3	153		test pin • open-circuit • not user accessible
POR	154		external Power-On Reset (POR) input

Table 3. Pin description *…continued*

Symbol	Pin	Description
PD	155	power-down mode select • for normal operation pin PD must be LOW
SDA	156 and 157 [5]	I²C-bus serial data input/output
$R/\overline{W}$	158	read/write input • pin $R/\overline{W}$ = HIGH selects the read operation • pin $R/\overline{W}$ = LOW selects the write operation • this pin has an internal pull-up resistor
RS	159	register select pin; • this pin has an internal pull-up resistor
DB0 to DB2, DB3/SA0, DB4 to DB7	160 to 162, 163, 164 to 167 [6][7]	8 bit bidirectional data bus (bit 0 to bit 7) • the 8-bit bidirectional data bus (3-state) transfers data between the microcontroller and the PCF2119x • pin DB7 may be used as the busy flag, signalling that internal operations are not yet completed • 4-bit operations the 4 higher order lines DB7 to DB4 are used, DB3 to DB0 must be left open-circuit • data bus line DB3 has an alternative function (SA0) as the I²C-bus address pin • each data line has its own internal pull-up resistor
OSC	168	oscillator or external clock input • when the on-chip oscillator is used this pin must be connected to V_{DD1}

[1] Always put $V_{DD2} = V_{DD3}$.

[2] When the I²C-bus is used, the parallel interface pin E must be LOW.

[3] The substrate (rear side of the die) is wired to V_{SS} but should not be electrically connected.

[4] On the device connected to V_{SS1}.

[5] When the parallel bus is used, the pins SCL and SDA must be connected to V_{SS1} or V_{DD1}; they must not be left open-circuit.

[6] In the I²C-bus read mode, ports DB7 to DB4 and DB2 to DB0 should be connected to V_{DD1} or left open-circuit.

[7] When the 4-bit interface is used without reading out from the PCF2119x (bit $R/\overline{W}$ is set permanently to logic 0), the unused ports DB4 to DB0 can either be set to V_{SS1} or V_{DD1} instead of leaving them open-circuit.

8. Functional description

8.1 Oscillator and timing generator

The internal logic and the LCD drive signals of the PCF2119x are timed by the frequency f_{clk} which equals either the built in oscillator frequency f_{osc} or an external clock frequency $f_{clk(ext)}$.

8.1.1 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.1.2 Internal clock

To use the on-chip oscillator, pin OSC must be connected to V_{DD1}. The on-chip oscillator provides the clock signal for the display system. No external components are required.

8.1.3 External clock

If an external clock will be used, the input is at pin OSC. The resulting display frame frequency is given by:

$$f_{fr} = \frac{f_{osc}}{3072} \quad (1)$$

Remark: Only in the power-down mode the clock is allowed to be stopped (pin OSC connected to V_{SS}), otherwise the LCD is frozen in a DC state, which is not suitable for the liquid crystals.

8.2 Reset function and Power-On Reset (POR)

The PCF2119x must be reset externally when power is turned on. If no external reset is performed, the chip might start-up in an unwanted state.

For the external reset, pin POR has to be active HIGH. The reset has to be active for at least 3 oscillator periods in order for the reset to be executed. If the internal oscillator is used, the minimum reset activity time follows from the lowest possible oscillator frequency (f_{osc} = 140 kHz, T_{osc} ~ 71 μs, 3 × T_{osc} ~ 215 μs). The internal oscillator start-up time is 200 μs (typ) up to 300 μs (max) after power-on. In case that an external oscillator is used, T_{osc} is dependent from $f_{osc(ext)}$.

Afterwards the chip executes the Clear_display instruction, which requires 165 oscillator cycles. After the reset the chip has the state shown in Table 4 and is then ready for use.

Table 4. State after reset

Step	Function	Control bit and register state	Description	Reference
1	Clear_display			Table 16
2	Entry_mode_set	bit I_D = 1	incremental cursor move direction	Table 18
		bit S = 0	no display shift	
3	Display_ctl	bit D = 0	display off	Table 19
		bit C = 0	cursor off	
		bit B = 0	cursor character blink off	
4	Function_set	bit DL = 1	8-bit interface	Table 12
		bit M = 0	1-line display	
		bit SL = 0	1:18 multiplex drive mode	
		bit H = 0	normal instruction set	
5	default address pointer to DDRAM	[1]		Table 22
6	Icon_ctl	bit IM = 0	character mode, full display	Table 25
		bit IB = 0	icon blink disabled	
7	Screen_conf	bit L = 0	default configuration	Table 23
	Disp_conf	bit P = 0; bit Q = 0	default configurations	Table 24
8	Temp_ctl	bit TC1 = 0; bit TC2 = 0	default temperature coefficient	Table 28
9	VLCD_set	register V_A = 0; register V_B = 0	V_{LCD} generator off	Table 32
10	I^2C-bus interface reset			
11	HV_gen	bit S1 = 1; bit S0 = 0	V_{LCD} generator set to 3 internal stages (4 voltage multipliers)	Table 30

[1] The Busy Flag (BF) indicates the busy state (bit BF = 1) until initialization ends. The busy state lasts 2 ms. The chip may also be initialized by software (see Table 43 and Table 44).

8.3 Power-down mode

The chip can be put into power-down mode by applying a HIGH-level to pin PD. In power-down mode all static currents are switched off (no internal oscillator, no bias level generation and all LCD outputs are internally connected to V_{SS}).

During power-down, information in the RAM and the chip state are preserved. Instruction execution during power-down is possible when pin OSC is externally clocked.

8.4 LCD supply voltage generator

The LCD supply voltage may be generated on-chip. The V_{LCD} generator is controlled by two internal 6-bit registers: V_A and V_B. Register V_A is programmed with the voltage for character mode and register V_B with the voltage for icon mode.

The nominal LCD operating voltage at room temperature is given by Equation 2:

$$V_{LCD(nom)} = V_x \times 0.08 + 1.82 \quad (2)$$

Where V_x is the integer value of the register V_A or V_B.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage (V_{oper}).

8.4.1 Programming ranges

Possible values for V_A and V_B are between 0 to 63.

Table 5. Values of V_A and V_B and the corresponding V_{LCD} values

All values at T_{ref} = 27 °C; allowed values are highlighted.

Integer values of V_A and V_B	Corresponding value of V_{LCD} in V	Integer values of V_A and V_B	Corresponding value of V_{LCD} in V	Integer values of V_A and V_B	Corresponding value of V_{LCD} in V
0	**VLCD switched off**	**22**	**3.58**	**44**	**5.34**
1	1.90	**23**	**3.66**	**45**	**5.42**
2	1.98	**24**	**3.74**	**46**	**5.50**
3	2.06	**25**	**3.82**	**47**	**5.58**
4	2.14	**26**	**3.90**	**48**	**5.66**
5	**2.22**	**27**	**3.98**	**49**	**5.74**
6	**2.30**	**28**	**4.06**	**50**	**5.82**
7	**2.38**	**29**	**4.14**	**51**	**5.90**
8	**2.46**	**30**	**4.22**	**52**	**5.98**
9	**2.54**	**31**	**4.30**	**53**	**6.06**
10	**2.62**	**32**	**4.38**	**54**	**6.14**
11	**2.70**	**33**	**4.46**	**55**	**6.22**
12	**2.78**	**34**	**4.54**	**56**	**6.30**
13	**2.86**	**35**	**4.62**	**57**	**6.38**
14	**2.94**	**36**	**4.70**	**58**	**6.46**
15	**3.02**	**37**	**4.78**	59	6.54
16	**3.10**	**38**	**4.86**	60	6.62
17	**3.18**	**39**	**4.94**	61	6.70
18	**3.26**	**40**	**5.02**	62	6.78
19	**3.34**	**41**	**5.10**	63	6.86
20	**3.42**	**42**	**5.18**		
21	**3.50**	**43**	**5.26**		

Remarks:

- Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage the temperature coefficient of V_{LCDOUT} must be taken into account.
- Values below 2.2 V are below the specified operating range of the chip and are therefore not allowed.

When the LCD supply voltage is generated on-chip, the V_{LCD} pins should be decoupled to V_{SS} with a suitable capacitor. The generated V_{LCDOUT} is independent of V_{DD} and is temperature compensated.

In Equation 2 the internal charge pump is not considered. However, if the supplied voltage to V_{DD2} and V_{DD3} is below the required V_{LCD} it is necessary to use the internal charge pump. The multiplication factor has to be set such, that V_{DD2} and V_{DD3} (which are equal) multiplied with the programmed multiplication factor exceeds the required V_{LCD} under all circumstances (i.e. at low temperatures and along with the temperature compensation - see Section 10.2.3.4). If still a higher multiplication factor is chosen, V_{LCD} will not increase (it is set by Equation 2) but the current that can be delivered will be higher. Also current consumption increases (see Section 16.6).

When the V_{LCD} generator and the direct mode are switched off, an external voltage may be supplied at connected pins V_{LCDIN} and V_{LCDOUT}. V_{LCDIN} and V_{LCDOUT} may be higher or lower than V_{DD2}.

In direct mode (see Icon_ctl instruction, Section 10.2.3.3) the internal V_{LCD} generator is turned off and the V_{LCDOUT} output voltage is directly connected to V_{DD2}. This reduces the current consumption depending on V_{DD2} value and LCD liquid properties.

The V_{LCD} generator ensures that, as long as V_{DD2} and V_{DD3} are in the valid range (2.2 V to 4 V), the required peak voltage V_{LCD} = 6.5 V can be generated at any time.

8.5 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels. Using a 5-level bias scheme for the 1:18 multiplex rate allows V_{LCD} < 5 V for most LCD liquids.

The intermediate bias levels for the different multiplex rates are shown in Table 6. These bias levels are automatically set to the given values when switching to the corresponding multiplex rate.

Table 6. Bias levels as a function of multiplex rate

Multiplex rate	Number of bias levels	Bias voltages					
		V_1	V_2	V_3	V_4	V_5	V_6
1:18	5	V_{LCD}	$\frac{3}{4}(V_{LCD} - V_{SS})$	$\frac{1}{2}(V_{LCD} - V_{SS})$	$\frac{1}{2}(V_{LCD} - V_{SS})$	$\frac{1}{4}(V_{LCD} - V_{SS})$	V_{SS}
1:9	5	V_{LCD}	$\frac{3}{4}(V_{LCD} - V_{SS})$	$\frac{1}{2}(V_{LCD} - V_{SS})$	$\frac{1}{2}(V_{LCD} - V_{SS})$	$\frac{1}{4}(V_{LCD} - V_{SS})$	V_{SS}
1:2	4	V_{LCD}	$\frac{2}{3}(V_{LCD} - V_{SS})$	$\frac{2}{3}(V_{LCD} - V_{SS})$	$\frac{1}{3}(V_{LCD} - V_{SS})$	$\frac{1}{3}(V_{LCD} - V_{SS})$	V_{SS}

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 3 and the RMS off-state voltage ($V_{off(RMS)}$) with Equation 4:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (3)$$

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (4)$$

where the values of a are

a = 2 for ¼ bias

a = 3 for ⅕ bias

and the values for n are

n = 2 for 1:2 multiplex rate

n = 9 for 1:9 multiples rate

n = 18 for 1:18 multiplex rate.

Discrimination (D) is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 5

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \quad (5)$$

8.5.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependant on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at V_{low}) and the other at 90% relative transmission (at V_{high}), see Figure 3. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{high} \quad (6)$$

$$V_{off(RMS)} \leq V_{low} \quad (7)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 3 to Equation 5) and the V_{LCD} voltage.

V_{low} and V_{high} are properties of the LCD liquid and can be provided by the module manufacturer.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

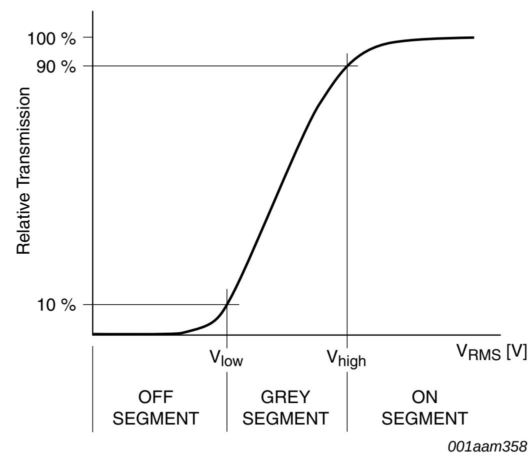
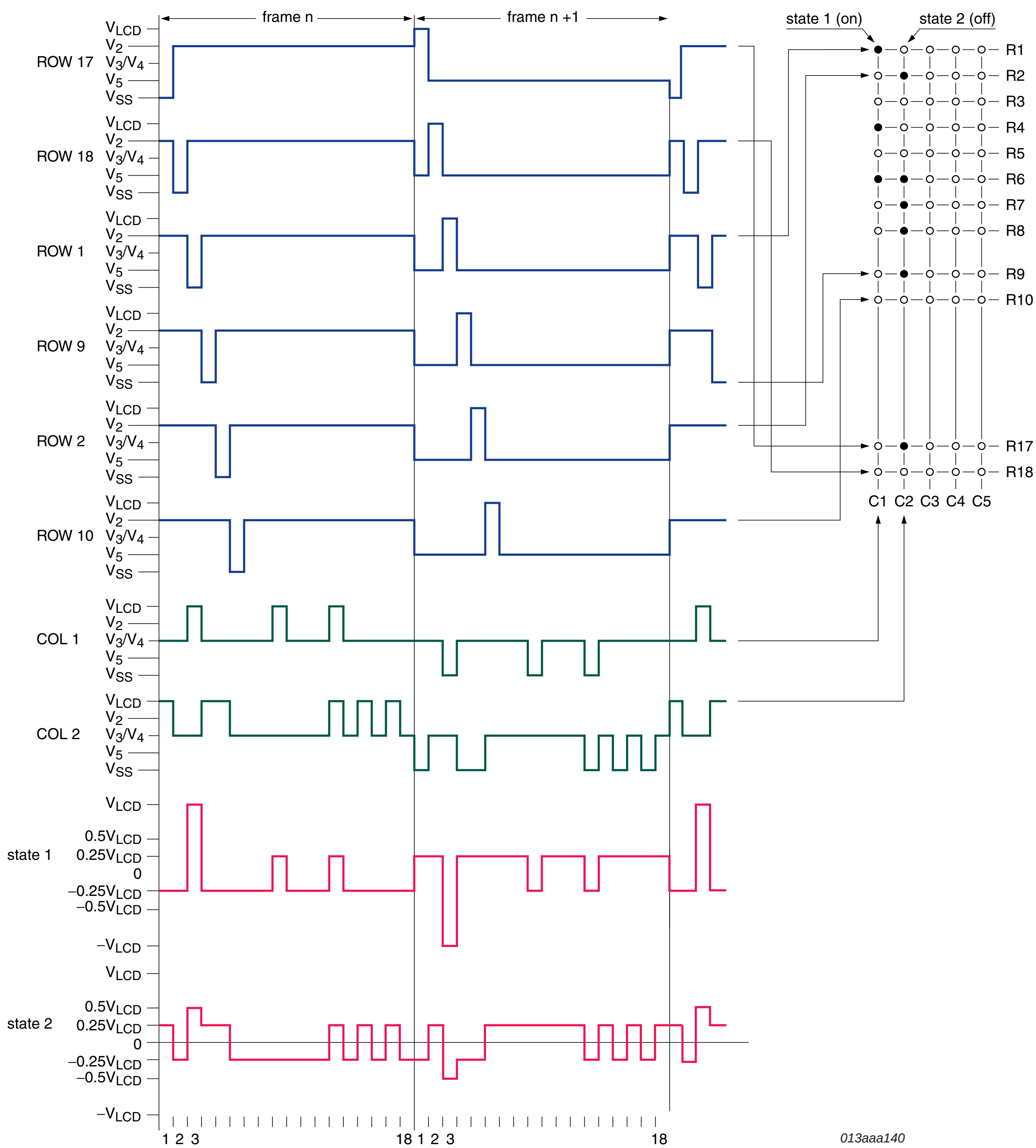


Fig 3. Electro-optical characteristic: relative transmission curve of the liquid

8.6 LCD row and column drivers

The PCF2119x contains 18 row and 80 column drivers, which drive the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows. Unused outputs should be left open.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figure 4 to Figure 6 show typical waveforms.



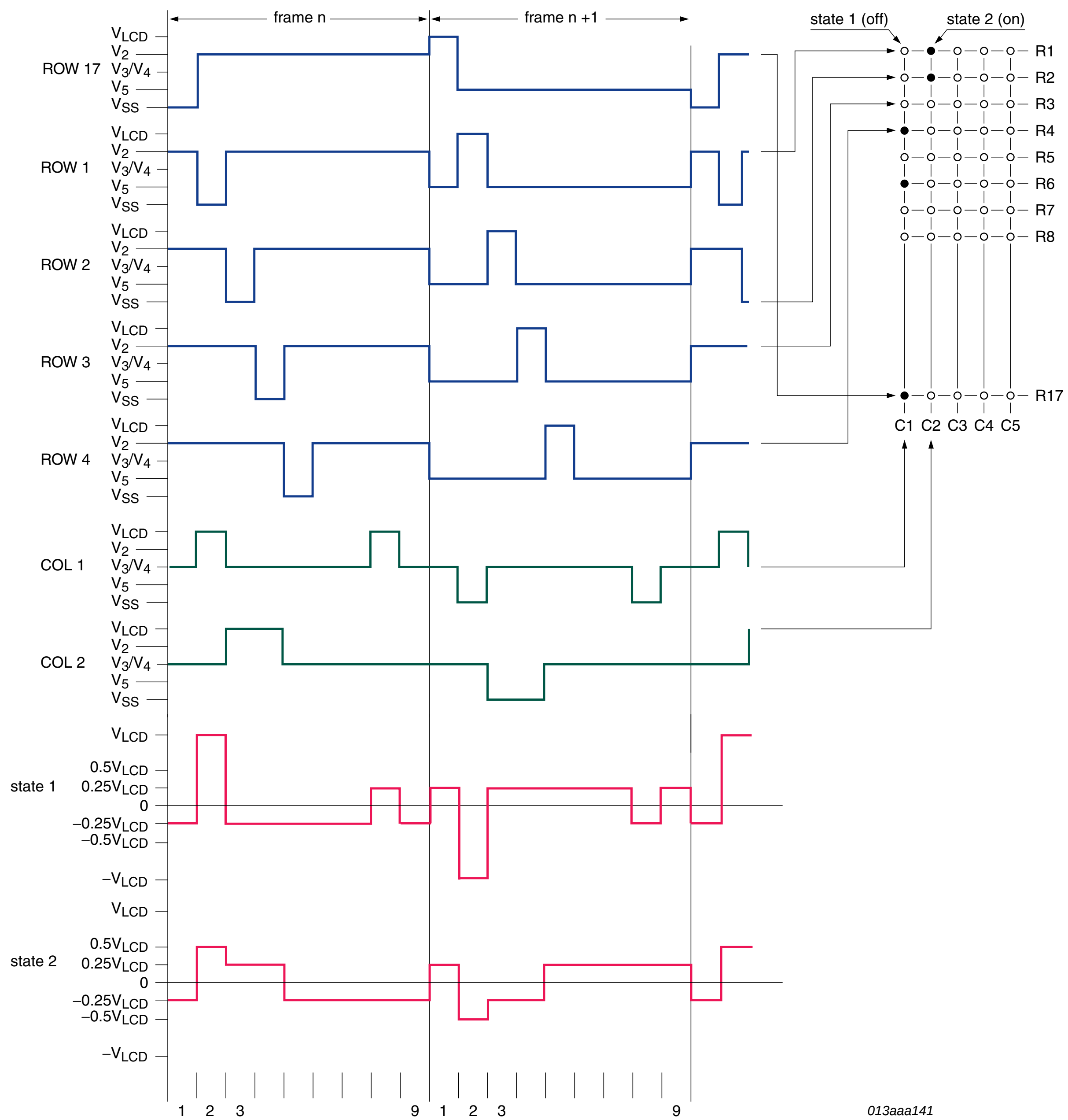
state(n) marks intersection(row(x),col(n)) of pixel(x,n)

$V_{state(n)}(t) = V_{COL(n)}(t) - V_{ROW(x)}(t)$.

$V_{state1}(t) = V_{COL1}(t) - V_{ROW1}(t)$.

$V_{state2}(t) = V_{COL2}(t) - V_{ROW1}(t)$.

Fig 4. Waveforms for the 1:18 multiplex drive mode with 5 bias levels; character mode



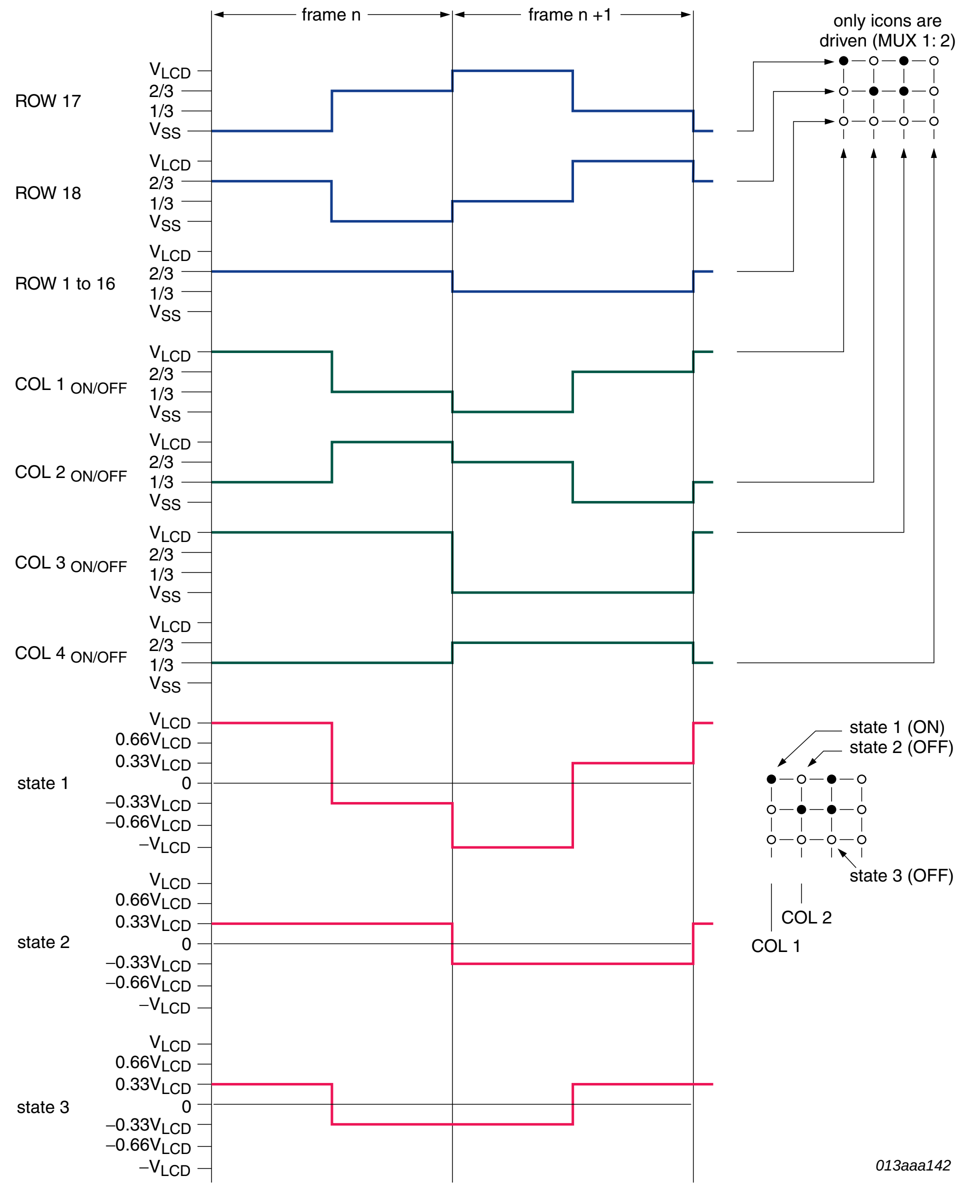
state(n) marks intersection(row(x),col(n)) of pixel(x,n)

$V_{state(n)}(t) = V_{COL(n)}(t) - V_{ROW(x)}(t)$.

$V_{state1}(t) = V_{COL1}(t) - V_{ROW1}(t)$.

$V_{state2}(t) = V_{COL2}(t) - V_{ROW1}(t)$.

Fig 5. Waveforms for the 1:9 multiplex drive mode with 5 bias levels; character mode, R9 to R16 and R18 open



state(n) marks intersection(row(x),col(n)) of pixel(x,n)

$V_{state(n)}(t) = V_{COL(n)}(t) - V_{ROW(x)}(t)$.

$V_{state1}(t) = V_{COL1}(t) - V_{ROW17}(t)$.

$V_{state2}(t) = V_{COL2}(t) - V_{ROW17}(t)$.

$V_{state3}(t) = V_{COL3}(t) - V_{ROW1\ to\ 16}(t)$.

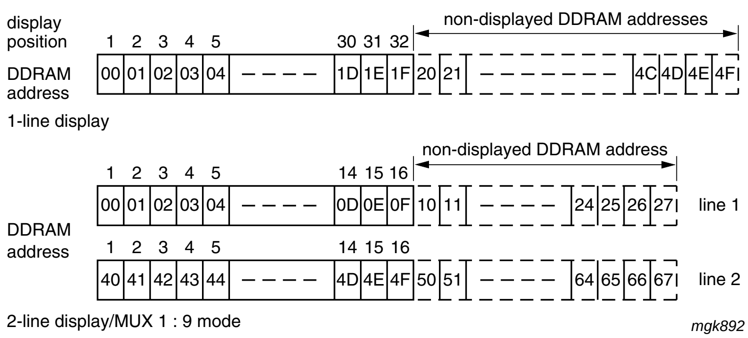
Fig 6. Waveforms for the 1:2 multiplex drive mode with 4 bias levels; icon mode

9. Display data RAM and ROM

9.1 DDRAM

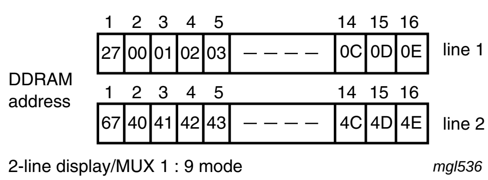
The Display Data RAM (DDRAM) stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM.

The basic RAM to display addressing scheme is shown in Figure 7, Figure 8 and Figure 9. With no display shift the characters represented by the codes in the first 32 RAM locations starting at address 00h are displayed in line 1.



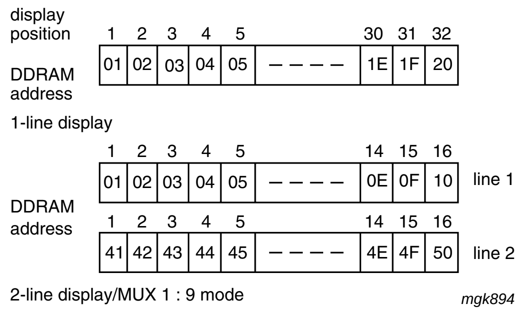
All addresses are shown in hex.

Fig 7. DDRAM to display mapping: no shift



All addresses are shown in hex.

Fig 8. DDRAM to display mapping: right shift



All addresses are shown in hex.

Fig 9. DDRAM to display mapping: left shift

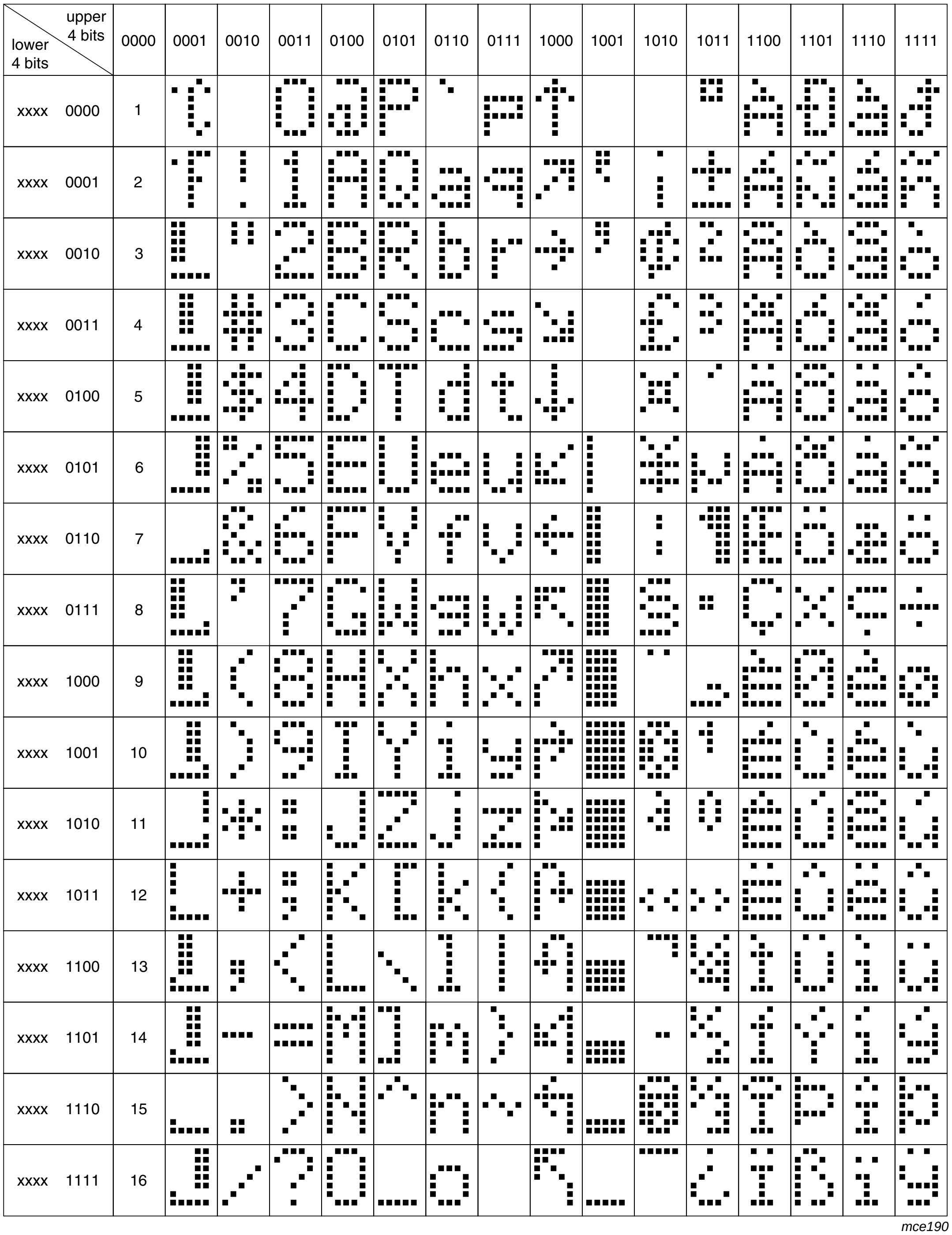
When data is written to or read from the DDRAM, wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together. The address ranges and wrap-around operations for the various modes are shown in Table 7.

Table 7. Address space and wrap-around operation

Mode	1 × 32	2 × 16	1 × 16
Address space	00h to 4Fh	00h to 27h; 40h to 67h	00h to 27h
Read/write wrap-around (moves to next line)	4Fh to 00h	27h to 40h; 67h to 00h	27h to 00h
Display shift wrap-around (stays within line)	4Fh to 00h	27h to 00h; 67h to 40h	27h to 00h

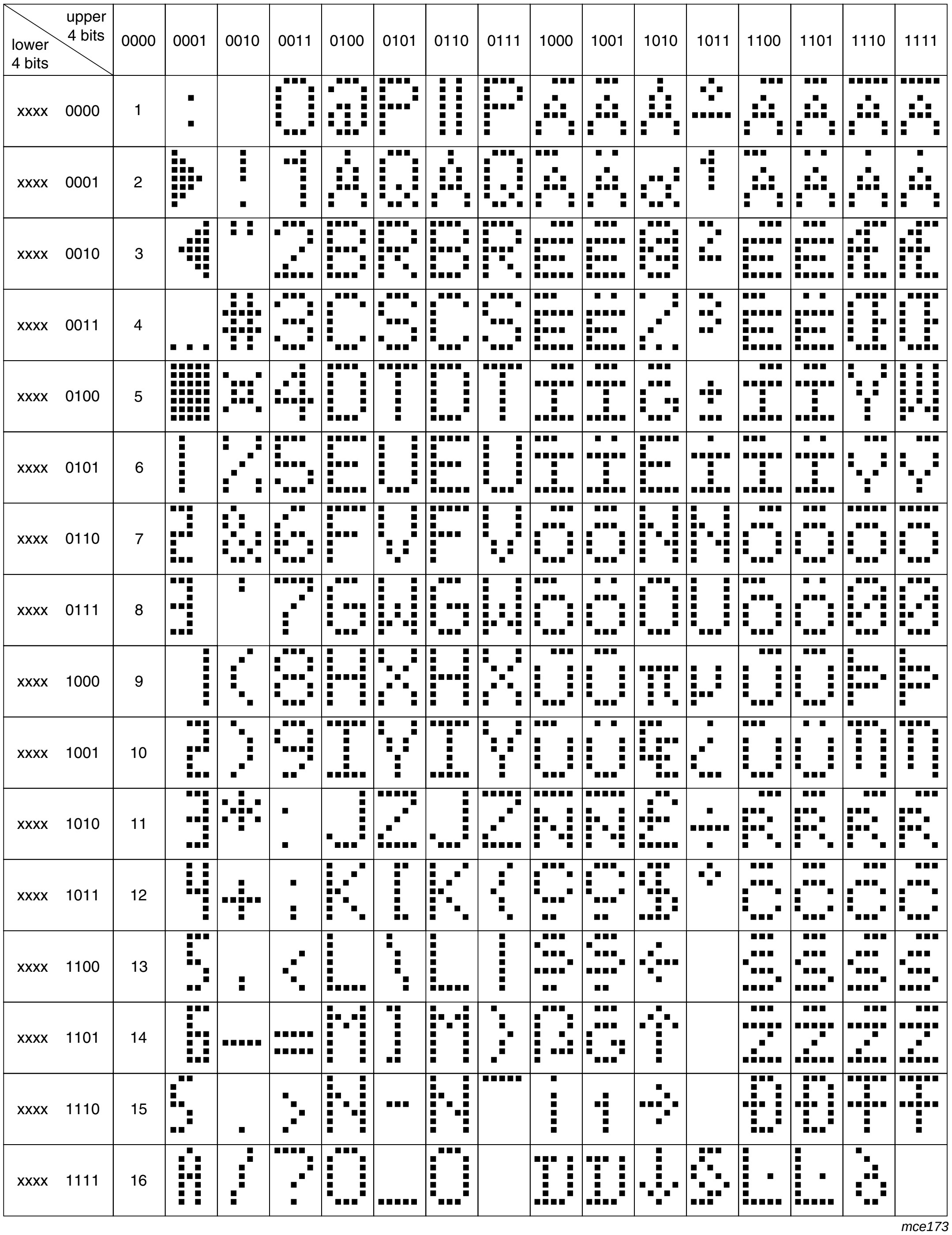
9.2 CGROM

The Character Generator ROM (CGROM) contains 240 character patterns in a 5 × 8 dot format from 8-bit character codes. Figure 10 to Figure 15 show the character sets that are currently implemented.



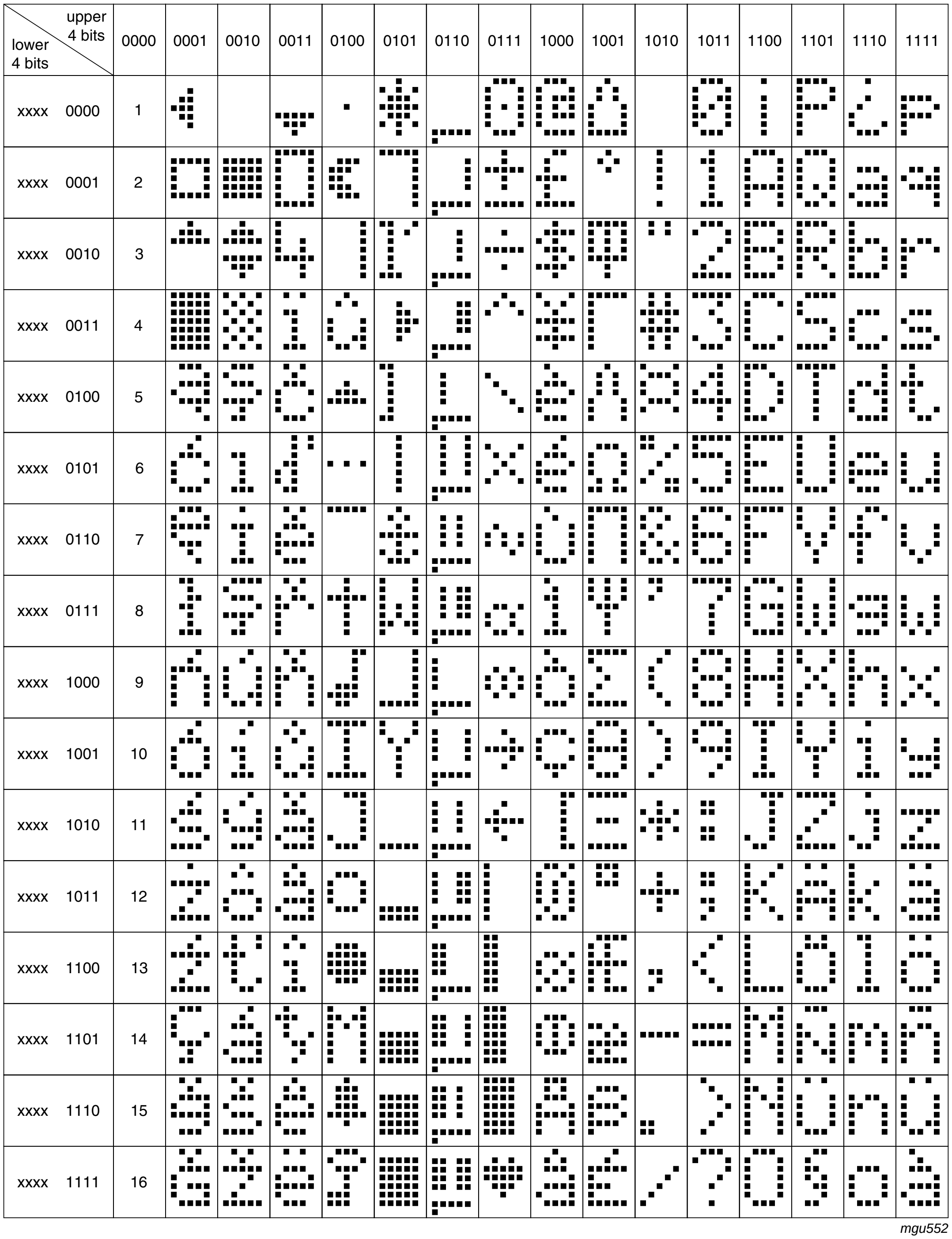
The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 10. Character set 'A' in CGROM



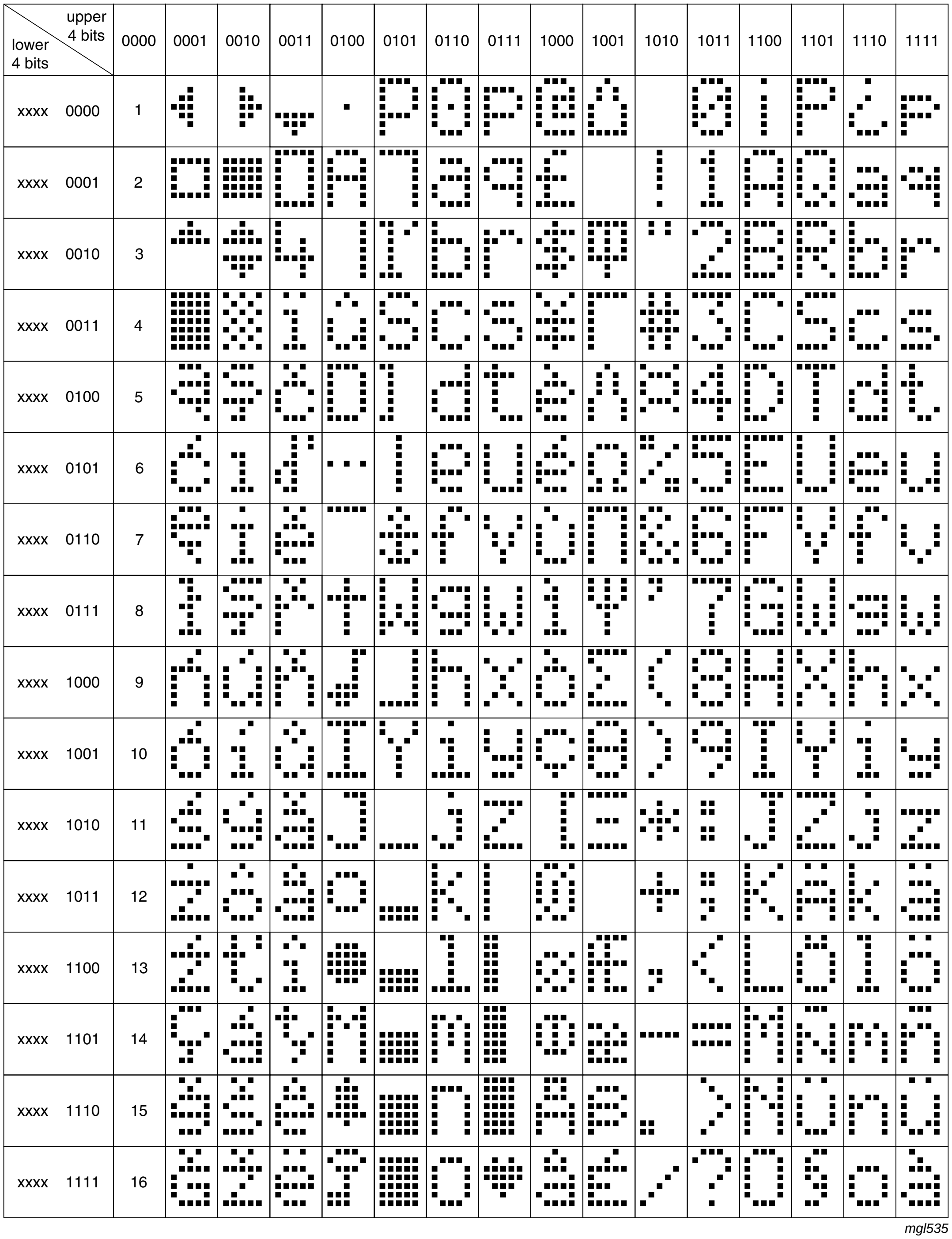
The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 11. Character set 'D' in CGROM



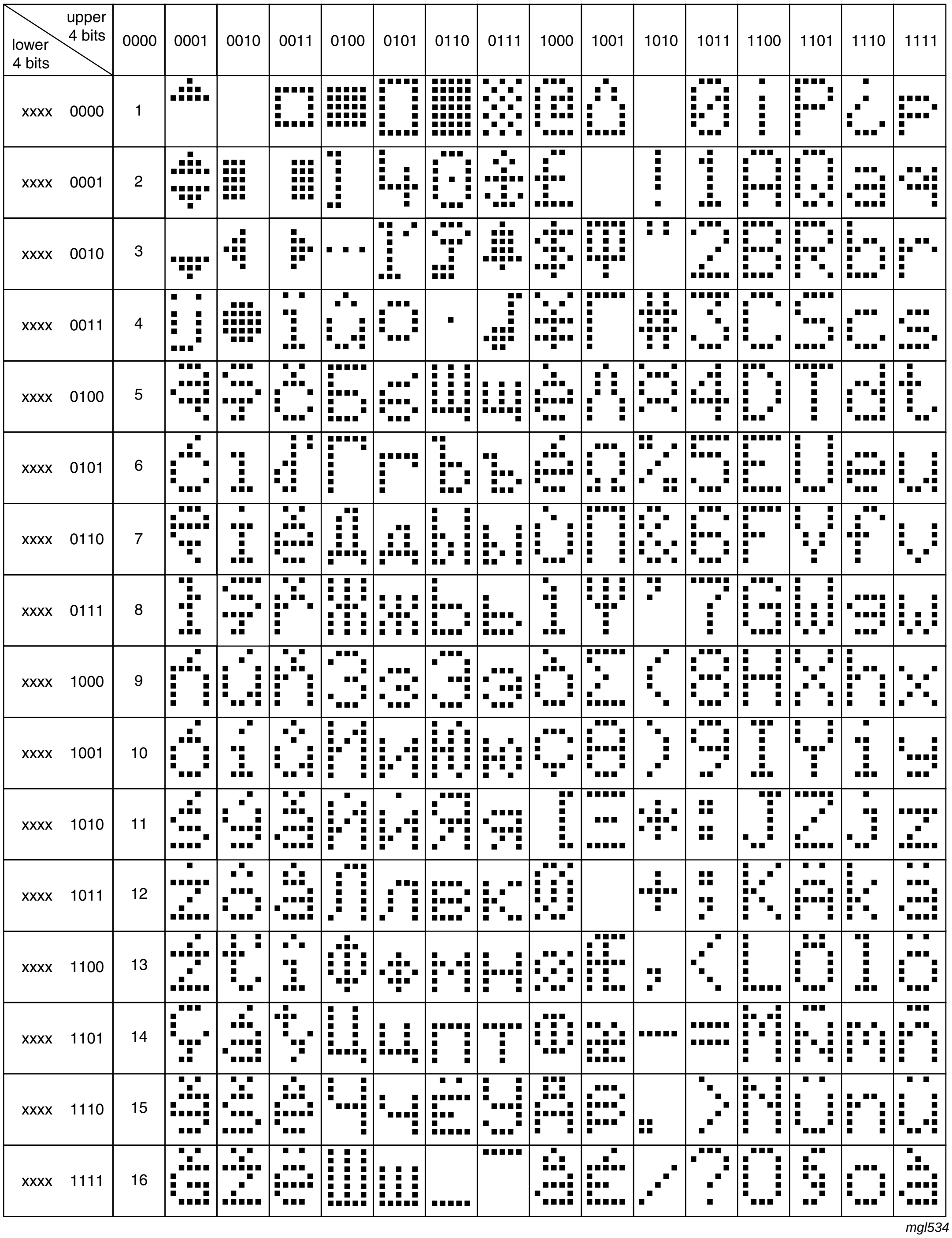
The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 12. Character set ‘F’ in CGROM



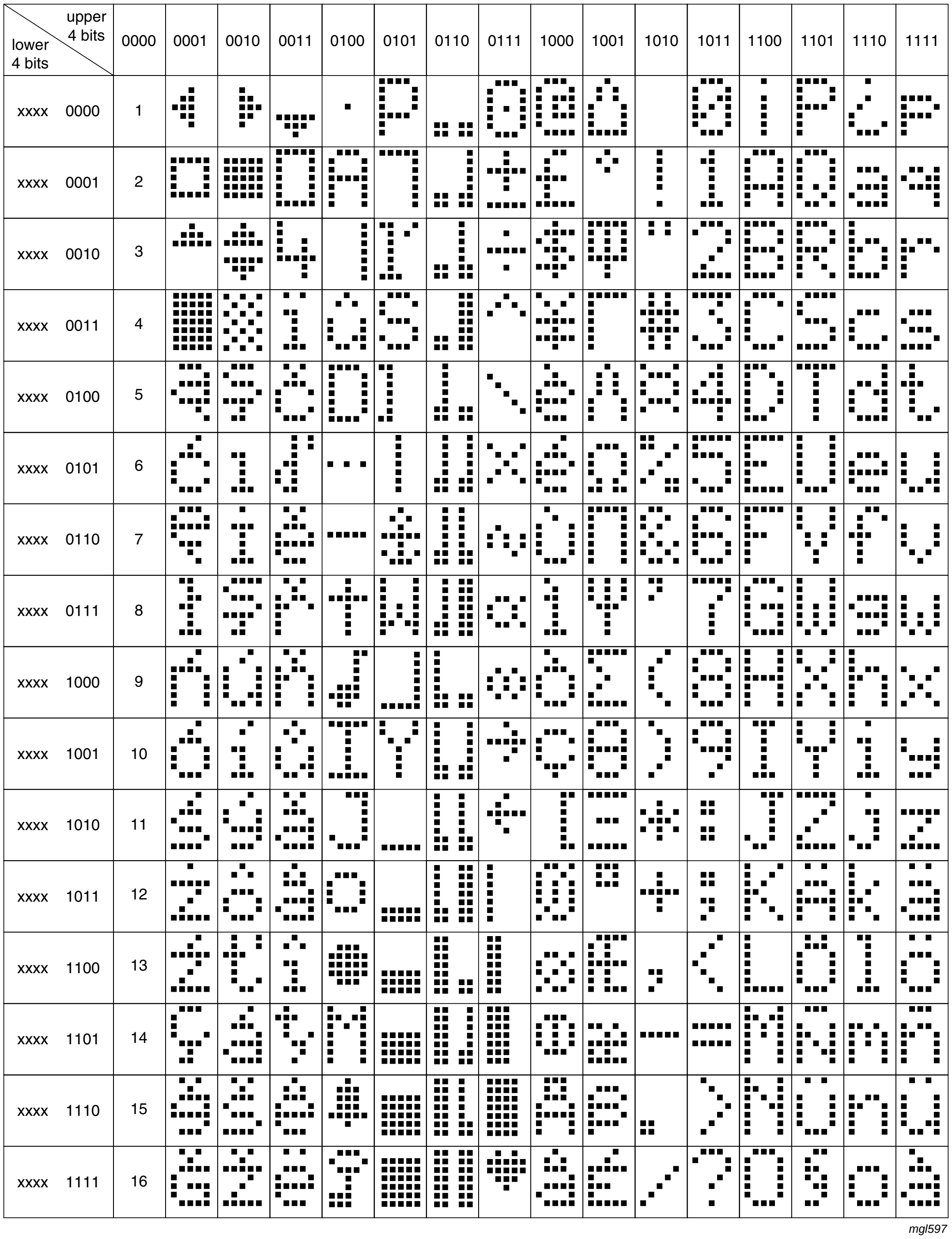
The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 13. Character set ‘R’ in CGROM



The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 14. Character set ‘S’ in CGROM



The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 15. Character set ‘V’ in CGROM

9.3 CGRAM

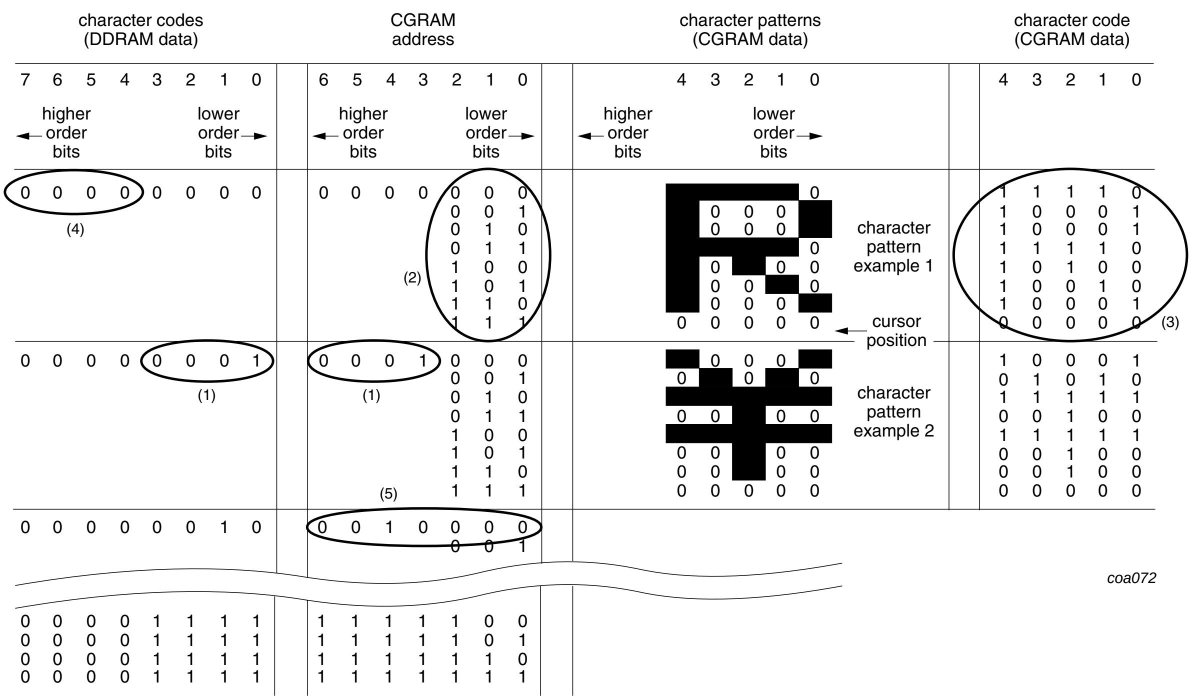
Up to 16 user defined characters may be stored in the Character Generator RAM (CGRAM). Some CGRAM characters (see Figure 22) are also used to drive icons:

- 6 CGRAM characters if icons blink and both icon rows are used in the application
- 3 CGRAM characters if no icons blink but both icon rows are used in the application
- 0 CGRAM characters if no icons are driven by the icon rows

When the icons blink option is enabled, double the number of CGRAM characters are used since both the on and off state of an icon is defined.

The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Figure 10 to Figure 15).

Figure 16 shows the addressing principle for the CGRAM.



(1) Character code bit 0 to bit 3 correspond to CGRAM address bit 3 to bit 6.

(2) CGRAM address bit 0 to bit 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th line will appear in the cursor position. Lines are numbered from 0 to 7.

(3) Character pattern column positions correspond to CGRAM data bit 0 to bit 4, as shown in Figure 10 to Figure 15.

(4) As shown in Figure 10 to Figure 15, CGRAM character patterns are selected when character code bit 4 to bit 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

(5) Only bit 0 to bit 5 of the CGRAM address are set by the Set_CGRAM command. Bit 6 can be set using the Set_DDRAM command in the valid address range or by using the auto-increment feature during CGRAM write. All bits from bit 0 to bit 6 can be read using the BF_AC instruction.

Fig 16. Relationship between CGRAM addresses, data and display patterns

9.4 Cursor control circuit

The cursor control circuit generates the cursor underline and/or cursor blink as shown in Figure 17 at the DDRAM address contained in the address counter.

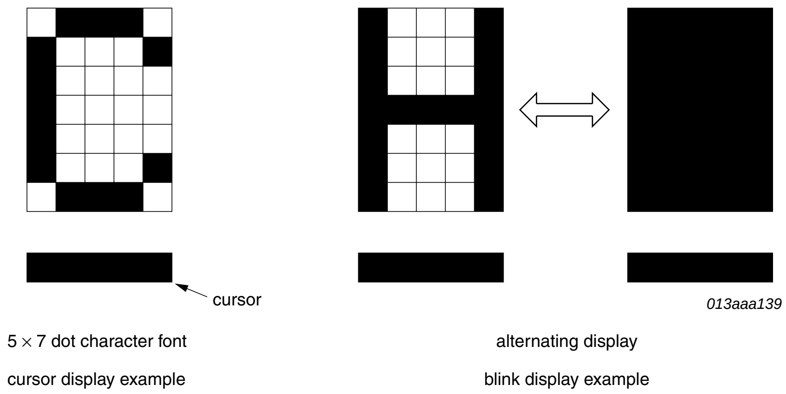


Fig 17. Cursor and blink display examples

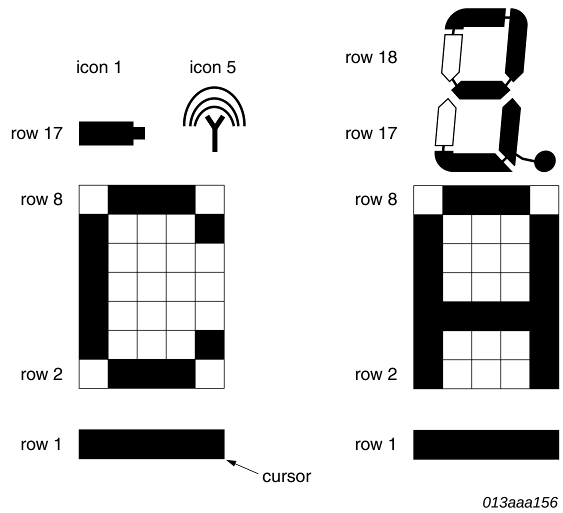


Fig 18. Example of displays with icons

10. Registers

The PCF2119x has two 8-bit registers, an instruction register and a data register. Only these two registers can be directly controlled by the microcontroller. Before an internal operation, the control information is stored temporarily in these registers, to allow interfacing to various types of microcontrollers which operate at different speeds or to allow interface to peripheral control ICs.

The instruction set for the parallel interface is shown in Table 11 together with their execution time. Details about the parallel interface can be found in Section 11.1. Examples of operations on a 4-bit bus are given in Table 38, on a 8-bit bus in Table 39, Table 40 and Table 41.

When using the I^{2}C-bus, the instruction has to be commenced with a control byte as shown in Table 8. Details about the I^{2}C-bus interface can be found in Section 11.2. An example of operations on the I^{2}C-bus is given in Table 42.

Table 8. Instruction set for I^{2}C-bus commands

Control byte								Command byte								I^{2}C-bus command
CO	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	[1]

[1] R/$\overline{W}$ is set together with the slave address (see Figure 31).

Table 9. Control byte bit description

Bit	Symbol	Value	Description
7	CO	0	last control byte
		1	another control byte follows after data/command
6	RS	0	instruction register selected
		1	data register selected
4 to 0	-	0	default logic 0

Instructions are of 4 types, those that:

1. Designate PCF2119x functions like display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others, like read ‘busy flag’ and read ‘address counter’

In normal use, type 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instructions other than the BF_AC instruction will be executed. Because the busy flag is set to logic 1 while an instruction is being executed, check to ensure it is logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 11. An instruction sent while the busy flag is logic 1 will not be executed.

The RS bit determines which register will be accessed and the R/$\overline{W}$ bit indicates if it is a read or a write operation (see Table 10).

Table 10. Register access selection

Symbol	Value	Description
RS		**register select**
	0	instruction register[1]
	1	data register[2]
R/$\overline{W}$		**read/write**
	0	write operation
	1	read operation

[1] There is only write access to the instruction register, but read access to the busy flag (BF) and the address counter (AC) of the BF_AC instruction (see Section 10.2.1.2).

[2] Write and read access.

Details of the instructions are explained in subsequent sections.

10.1 Data register

The data register temporarily stores data to be read from the DDRAM and CGRAM. Prior to being read by the Read_data instruction, data from the DDRAM or CGRAM, corresponding to the address in the instruction register, is written to the data register.

10.2 Instruction register

The instruction register stores instruction codes such as Clear_display, Curs_disp_shift, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written to but not read from by the system controller.

The instruction register is sectioned into basic, standard and extended instructions. Bit H = 1 of the Function_set instruction (see Section 10.2.1.1) sets the chip into extended instruction set mode.

Table 11. Instruction register overview

Instruction	Bits[1]										Required clock cycles[2]	Reference
	RS	R/$\overline{W}$	7	6	5	4	3	2	1	0		
Basic instructions (bit H = 0 or 1)												
NOP [3]	0	0	0	0	0	0	0	0	0	0	3	-
Function_set	0	0	0	0	1	DL	0	M	SL	H	3	Section 10.2.1.1
BF_AC	0	1	BF	AC							0	Section 10.2.1.2
Read_data	1	1	READ_DATA								3	Section 10.2.1.3
Write_data	1	0	WRITE_DATA								3	Section 10.2.1.4
Standard instructions (bit H = 0)												
Clear_display	0	0	0	0	0	0	0	0	0	1	165	Section 10.2.2.1
Return_home	0	0	0	0	0	0	0	0	1	0	3	Section 10.2.2.2
Entry_mode_set	0	0	0	0	0	0	0	1	I_D	S	3	Section 10.2.2.3
Display_ctl	0	0	0	0	0	0	1	D	C	B	3	Section 10.2.2.4
Curs_disp_shift	0	0	0	0	0	1	SC	RL	0	0	3	Section 10.2.2.5
Set_CGRAM	0	0	0	1	ACG						3	Section 10.2.2.6
Set_DDRAM	0	0	1	ADD							3	Section 10.2.2.7
Extended instructions (bit H = 1)												
Reserved [4]	0	0	0	0	0	0	0	0	0	1	-	-
Screen_conf	0	0	0	0	0	0	0	0	1	L	3	Section 10.2.3.1
Disp_conf	0	0	0	0	0	0	0	1	P	Q	3	Section 10.2.3.2
Icon_ctl	0	0	0	0	0	0	1	IM	IB	DM	3	Section 10.2.3.3
Temp_ctl	0	0	0	0	0	1	0	0	TC1	TC2	3	Section 10.2.3.4
HV_gen	0	0	0	1	0	0	0	0	S1	S0	3	Section 10.2.3.5
VLCD_set	0	0	1	V	VA or VB						3	Section 10.2.3.6

[1] The bits 0 to 7 correspond with the data bus lines DB0 to DB7.

[2] f_{osc} cycles.

[3] No operation.

[4] Do not use.

10.2.1 Basic instructions (bit H = 0 or 1)

10.2.1.1 Function_set

Table 12. Function_set bit description

Bit	Symbol	Value		Description
RS	-	0		see Table 10
R/$\overline{W}$	-	0		
7 to 5	-	001		fixed value
4	DL			**interface data length (for parallel mode only)**
		0	[1]	2 × 4 bits (DB7 to DB4)
		1	[2]	8 bits (DB7 to DB0)
3	-	0		unused
2	M		[3]	**number of display lines**
		0		1 line × 32 characters
		1	[4]	2 line × 16 characters
1	SL			**multiplex mode**
		0		1:18 multiplex drive mode, 1 × 32 or 2 × 16 character display
		1	[4][5]	1:9 multiplex drive mode, 1 × 16 character display
0	H			**instruction set control**
		0		basic instruction set plus standard instruction set
		1	[4]	basic instruction set plus extended instruction set

[1] When 4-bit width is selected, data is transmitted in two cycles using the parallel-bus. In a 4-bit application ports DB3 to DB0 should be left open-circuit (internal pull-ups).

[2] Default value after power-on in I^2C-bus mode.

[3] No impact if SL = 1.

[4] Due to the internal pull-ups on DB3 to DB0 in a 4-bit application, the first Function_set after power-on sets bits M, SL and H to logic 1. A second Function_set must be sent to set bits M, SL and H to the required values.

[5] Independent of bit M and bit L of the Screen_conf instruction (see Section 10.2.3.1). Only row 1 to row 8 and row 17 are used. All other rows must be left open-circuit. The DDRAM map is the same as in the 2 × 16 character display mode, however, the second line cannot be displayed.

10.2.1.2 BF_AC instructions

Table 13. BF_AC bit

Bit	Symbol	Value		Description
RS	-	0		see Table 10
R/$\overline{W}$	-	1		
7	BF		[1]	**read busy flag**
		0		next instruction will be executed
		1		internal operation is in progress; next instruction will not be executed until BF = 0
6 to 0	AC	0000000 to 1111111		**read address counter**

[1] It is recommended that the BF status is checked before the next write operation is started.

Busy flag: The busy flag indicates the internal status of the PCF2119x. A logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output to pin DB7 when bit RS = 0 and bit R/$\overline{W}$ = 1. Instructions should only be started after checking that the busy flag is at logic 0 or after waiting for the required number of cycles.

Address counter: The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous Set_CGRAM and Set_DDRAM instruction. After a read/write operation the address counter is automatically incremented or decremented by 1. The address counter value is output to the bus (DB6 to DB0) when bit RS = 0 and bit R/$\overline{W}$ = 1.

10.2.1.3 Read_data

Table 14. Read_data bit description

Bit	Symbol	Value	Description
RS	-	1	see Table 10
R/$\overline{W}$	-	1	
7 to 0	READ_DATA	00000000 to 11111111	**read data from CGRAM or DDRAM**

Read_data from CGRAM or DDRAM: Read_data reads binary 8-bit data from the CGRAM or DDRAM. The most recent 'set address' command (Set_CGRAM or Set_DDRAM) determines whether the CGRAM or DDRAM is to be read.

The Read_data instruction gates the content of the data register to the bus while pin E is HIGH. After pin E goes LOW again, internal operation increments (or decrements) the address counter and stores RAM data corresponding to the new address counter into the data register.

There are only three instructions that update the data register:

- Set_CGRAM
- Set_DDRAM
- Read_data from CGRAM or DDRAM

Other instructions (e.g. Write_data, Curs_disp_shift, Clear_display and Return_home) do not modify the value of the data register.

10.2.1.4 Write_data

Table 15. Write_data bit description

Bit	Symbol	Value	Description
RS	-	1	see Table 10
R/$\overline{W}$	-	0	
7 to 0	WRITE_DATA	00000000 to 11111111	**write data to CGRAM or DDRAM**

Write_data to CGRAM or DDRAM: Write_data writes binary 8-bit data to the CGRAM or the DDRAM.

The previous Set_CGRAM or Set_DDRAM command determines if data is written into CGRAM or DDRAM. After writing, the address counter automatically increments or decrements by 1, in accordance with the Entry_mode_set (see Section 10.2.2.3). Only bit 4 to bit 0 of CGRAM data are valid, bit 7 to bit 5 are ‘don’t care’.

10.2.2 Standard instructions (bit H = 0)

10.2.2.1 Clear_display

Table 16. Clear_display bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
$R/\overline{W}$	-	0	
7 to 0	-	0000 0001	fixed value

Clear_display: writes usually the character code 20h (blank pattern) into all DDRAM addresses except for the character sets ‘R’ and ‘V’ where the character code 20h is not a blank pattern.

In addition Clear_display

- sets the DDRAM address counter to logic 0
- returns the display to its original position, if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display
- sets entry mode bit I_D = 1 (increment mode); bit S of entry mode does not change

The instruction Clear_display requires extra execution time. This may be allowed by checking the busy flag bit BF or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

Remark: When using the character sets ‘R’ or ‘V’, where the character code 20h is not the blank pattern, the following alternative instruction set has to be used:

1. Switch display off (Display_ctl, bit D = 0).
2. Write a blank pattern into all DDRAM addresses (Write_data).
3. Switch display on (Display_ctl, bit D = 1).

10.2.2.2 Return_home

Table 17. Return_home bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
$R/\overline{W}$	-	0	
7 to 0	-	0000 0010	fixed value

Return_home: Sets the DDRAM address counter to logic 0 and switches a shifted display back to an unshifted state. The DDRAM content remain unchanged. The cursor or blink position goes to the left of the first display line. Bit I_D and bit S of the Entry_mode_set instruction remain unchanged.

10.2.2.3 Entry_mode_set

Table 18. Entry_mode_set bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
R/$\overline{W}$	-	0	
7 to 2	-	000001	fixed value
1	I_D		**address increment or decrement**
		0	DDRAM or CGRAM address decrements by 1, cursor moves to the left
		1	DDRAM or CGRAM address increments by 1, cursor moves to the right
0	S		**shift display to the left or right**
		0	display does not shift
		1	display shifts

Bit I_D: When bit I_D = 1 the DDRAM or CGRAM address increments by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right.

When bit I_D = 0 the DDRAM or CGRAM address decrements by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the left.

The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

Bit S: When bit S = 0, the display does not shift.

During DDRAM write, when bit S = 1 and bit I_D = 0, the entire display shifts to the right; when bit S = 1 and bit I_D = 1, the entire display shifts to the left.

Thus it appears as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM.

10.2.2.4 Display_ctl instructions

Table 19. Display_ctl bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
R/$\overline{W}$	-	0	
7 to 3		00001	fixed value
2	D		**display on or off**
		0	display is off; chip is in power-down mode
		1	display is on
1	C		**cursor on or off**
		0	cursor is off
		1	cursor is on
0	B		**character blink on or off**
		0	character blink is off
		1	character blink is on

Bit D: The display is on when bit D = 1 and off when bit D = 0. Display data in the DDRAM is not affected and can be displayed immediately by setting bit D = 1.

When the display is off (bit D = 0) the chip is in partial power-down mode:

- The LCD outputs are connected to V_{SS}
- The V_{LCD} generator and bias generator are turned off

Three oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards the oscillator can be stopped. If the oscillator is running during partial power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (pin OSC to V_{SS}).

To ensure $I_{DD} < 1\ \mu A$:

- the parallel bus ports DB7 to DB0 should be connected to V_{DD}
- pins RS and $R/\overline{W}$ should be connected to V_{DD} or left open-circuit
- pin PD should be connected to V_{DD}

Recovery from power-down mode:

- pin PD should be connected back to V_{SS}
- if necessary pin OSC should be connected back to V_{DD}
- a Display_ctl instruction with bit D = 1 should be sent

Bit C: The cursor is displayed when bit C = 1 and inhibited when bit C = 0. Even if the cursor disappears, bit I_D and bit S (see Section 10.2.2.3) remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Figure 17).

Bit B: The character indicated by the cursor blinks when bit B = 1. The character blink is displayed by switching between display characters and all dots on with a period of approximately 1 second, with $f_{blink} = \frac{f_{osc}}{52224}$

10.2.2.5 Curs_disp_shift

Table 20. Curs_disp_shift bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
$R/\overline{W}$	-	0	
7 to 4		0001	fixed value
3	SC		**cursor move or display shift**
		0	move cursor
		1	shift display
2	RL		**shift or move to the right or left**
		0	left shift or move
		1	right shift or move
1 to 0	-	00	fixed value

Bits SC and RL: Curs_disp_shift moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display.

In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The address counter content does not change if the only action performed is shift display (SC = 1) but increments or decrements with the shift cursor (SC = 0).

10.2.2.6 Set_CGRAM

Table 21. Set_CGRAM bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
R/$\overline{W}$	-	0	
7 to 6	-	01	fixed value
5 to 0	ACG	000000 to 111111	**set CGRAM address**

Set_CGRAM: Sets the CGRAM address bits ACG[5:0] into the address counter. Data can then be written to or read from the CGRAM.

Remark: The CGRAM address uses the same address register as the DDRAM address. This register consists of 7 bits. But with the Set_CGRAM command, only bit 5 to bit 0 are set. Bit 6 can be set using the Set_DDRAM command first, or by using the auto-increment feature during CGRAM write. All bits 6 to 0 can be read using the BF_AC instruction.

When writing to the lower part of the CGRAM, ensure that bit 6 of the address is not set (e.g. by an earlier DDRAM write).

10.2.2.7 Set_DDRAM

Table 22. Set_DDRAM bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
R/$\overline{W}$	-	0	
7	-	1	fixed value
6 to 0	ADD	0000000 to 1111111	**set DDRAM address**

Set_DDRAM: Sets the DDRAM address bits ADD[6:0] into the address counter. Data can then be written to or read from the DDRAM.

10.2.3 Extended instructions (bit H = 1)

10.2.3.1 Screen_conf

Table 23. Screen_conf bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
R/$\overline{W}$	-	0	
7 to 1		0000001	fixed value
0	L		**screen configuration**
		0	split screen standard connection
		1	split screen mirrored connection

Screen_conf:

- If bit L = 0, then the two halves of a split screen are connected in a standard way i.e. column 1/81, 2/82 to 80/160.
- If bit L = 1, then the two halves of a split screen are connected in a mirrored way i.e. column 1/160, 2/159 to 80/81. This allows single layer PCB or glass layout.

10.2.3.2 Disp_conf

Table 24. Disp_conf bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
R/$\overline{W}$	-	0	
7 to 2		000001	fixed value
1	P		**display column configuration**
		0	column data: left to right; column data is displayed from column 1 to column 80
		1	column data: right to left; column data is displayed from column 80 to column 1
0	Q		**display row configuration**
		0	row data: top to bottom; row data is displayed from row 1 to row 16 and icon row data in row 17 and row 18 in single line mode (SL = 1) row data is displayed from row 1 to row 8 and icon row data in row 17
		1	row data: bottom to top; row data is displayed from row 16 to row 1 and icon row data in row 18 and row 17 in single line mode (SL = 1) row data is displayed from row 8 to row 1 and icon row data in row 17

Bit P: The P bit is used to flip the display left to right by mirroring the column data, as shown in Figure 19. This allows the display to be viewed from behind instead of front and enhances the flexibility in the assembly of equipment and avoids complicated data manipulation within the controller.

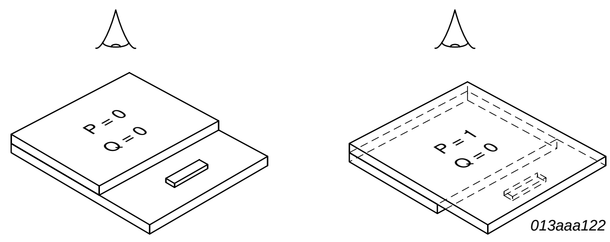


Fig 19. Use of bit P

Bit Q: The Q bit flips the display top to bottom by mirroring the row data, as shown in Figure 20.

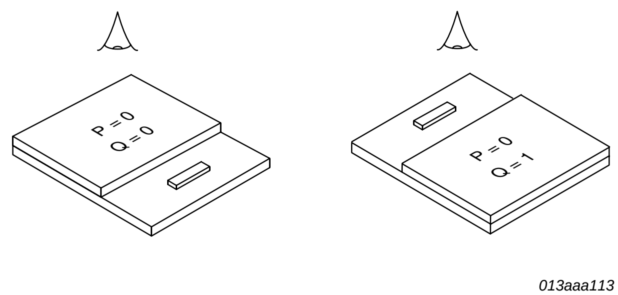


Fig 20. Use of bit Q

Combination of bit P and bit Q: A combination of P and Q allows the display to be rotated horizontally and vertically by 180 degree, as shown in Figure 21. This is useful for viewing the display from the opposite edge.

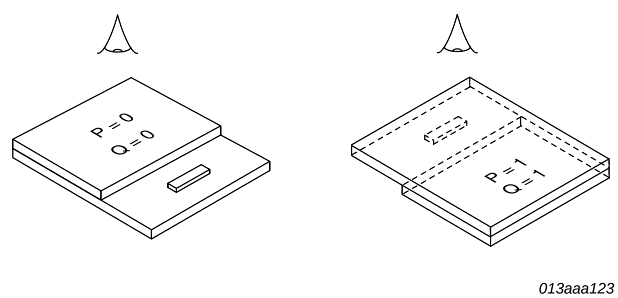


Fig 21. Use of bit P and bit Q

10.2.3.3 Icon_ctl

Table 25. Icon_ctl bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
R/$\overline{W}$	-	0	
7 to 3	-	00001	fixed value
2	IM		**icon mode**
		0	character mode, full display
		1	icon mode, only icons displayed
1	IB		**icon blink**
		0	icon blink disabled
		1	icon blink enabled
0	DM		**direct mode**
		0	off
		1	on

The PCF2119x can drive up to 160 icons. See Figure 22 and Figure 23 for CGRAM to icon mapping.

Bit IM: When bit IM = 0, the chip is in character mode. In the character mode characters and icons are driven (multiplex drive mode 1:18 or 1:9). The V_{LCD} generator, if used, produces the V_{LCDOUT} voltage programmed with register V_A.

When bit IM = 1, the chip is in icon mode. In the icon mode only the icons are driven (multiplex drive mode 1:2). The V_{LCD} generator, if used, produces the V_{LCDOUT} voltage as programmed with register V_B.

Table 26. Normal/icon mode operation

Bit IM	Mode	V_{LCDOUT}
0	character mode	generated from V_A
1	icon mode	generated from V_B

Bit IB: Icon blink control is independent of the cursor/character blink function.

When bit IB = 0, the icon blink is disabled. Icon data is stored in CGRAM character 0 to 3 ($4 \times 8 \times 5$ = 160 bits for 160 icons).

When bit IB = 1, the icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 3 ($4 \times 8 \times 5$ = 160 bits for 160 icons). These bits also define icon state when icon blink is not used (see Table 27).

Icon states for the odd phase are stored in CGRAM character 4 to 7 (another 160 bits for the 160 icons). When icon blink is disabled CGRAM characters 4 to 7 may be used as normal CGRAM characters.

Table 27. Blink effect for icons and cursor character blink

Parameter	Even phase	Odd phase
cursor character blink	block (all on)	normal (display character)
icons	state 1; CGRAM character 0 to 3	state 2; CGRAM character 4 to 7

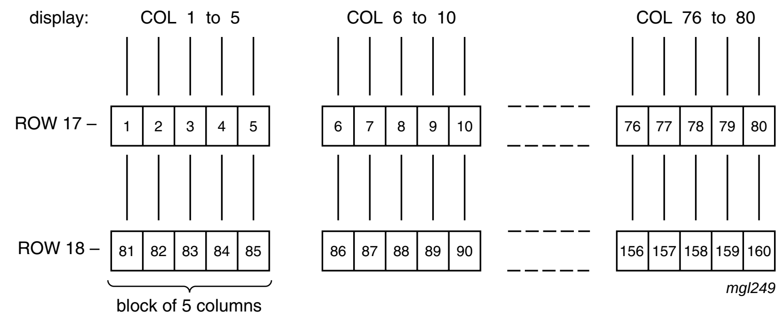


Fig 22. CGRAM to icon mapping (a)

icon no.	phase	ROW/COL	character codes 7 6 5 4 3 2 1 0 (MSB ... LSB)	CGRAM address 6 5 4 3 2 1 0 (MSB ... LSB)	CGRAM data 4 3 2 1 0 (MSB ... LSB)	icon view
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
76-80	even	17/76-80	0 0 0 0 0 0 0 1	0 0 0 1 1 1 1	1 1 1 1 1	
81-85	even	18/1-5	0 0 0 0 0 0 1 0	0 0 1 0 0 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
156-160	even	18/76-80	0 0 0 0 0 0 1 1	0 0 1 1 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
156-160	odd (blink)	18/76-80	0 0 0 0 0 1 1 1	0 1 1 1 1 1 1	0 0 1 1 0	

mgk999

CGRAM data: logic 1 of a data bit turns the icon on and logic 0 turns the icon off.

Character codes: bits 0 to 3 define the icon state when icon blink is disabled or during the even phase when icon blink is enabled. Bits 4 to 7 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled)

Fig 23. CGRAM to icon mapping (b)

Bit DM: When DM = 0, the chip is not in the direct mode. Either the internal V_{LCD} generator or an external voltage may be used to achieve V_{LCD}.

When DM = 1, the chip is in direct mode. The internal V_{LCD} generator is turned off and the output V_{LCDOUT} is directly connected V_{DD2} (i.e. the V_{LCD} generator supply voltage).

Remark: In direct mode, no external V_{LCD} is possible.

The direct mode can be used to reduce the current consumption when the required output voltage V_{LCDOUT} is close to the V_{DD2} supply voltage. This can be the case in icon mode or in MUX 1:9 (depending on LCD liquid properties).

10.2.3.4 Temp_ctl

Table 28. Temp_ctl bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
R/$\overline{W}$	-	0	
7 to 2	-	000100	
1 to 0	TC[1:0]	00 to 11	**temperature coefficient**

The bit-field TC[1:0] selects the temperature coefficient for the internally generated V_{LCDOUT} (see Table 29).

Table 29. TC[1:0] selection of V_{LCD} temperature coefficient

TC[1:0]	Typical value	Description
00	−0.16 %/K	V_{LCD} temperature coefficient 0 (default value)
10	−0.18 %/K	V_{LCD} temperature coefficient 1
01	−0.21 %/K	V_{LCD} temperature coefficient 2
11	−0.24 %/K	V_{LCD} temperature coefficient 3

10.2.3.5 HV_gen

Table 30. HV_gen bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
R/$\overline{W}$	-	0	
7 to 2	-	010000	fixed value
1 to 0	S[1:0]	00 to 11	**voltage multiplier**

A software configurable voltage multiplier is incorporated in the V_{LCD} generator and can be set via the HV_gen command. The voltage multiplier control can be used to reduce current consumption by disconnecting internal voltage multiplier stages, depending on the required V_{LCDOUT} output voltage (see Table 31).

Table 31. Voltage multiplier control bits

S[1:0]	Description
00	set V_{LCD} generator stages to 1 (2 × voltage multiplier)
01	set V_{LCD} generator stages to 2 (3 × voltage multiplier)
10	set V_{LCD} generator stages to 3 (4 × voltage multiplier)
11	do not use

10.2.3.6 VLCD_set

Table 32. VLCD_set bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 10
R/$\overline{W}$	-	0	
7	-	1	fixed value
6	V		**set register VA or VB**
		0	set register V_A
		1	set register V_B
5 to 0	V_A or V_B	000000 to 111111	**factor for calculating VLCD**

The V_{LCD} value is calculated with the Equation 2 on page 10. The multiplication factor is programmed by instruction. Two on-chip registers (V_A and V_B) hold the multiplication factor for the character mode and the icon mode, respectively. The generated V_{LCDOUT} value is independent of V_{DD}, allowing battery operation of the chip.

V_x programming:

1. Send Function_set instruction with bit H = 1.
2. Send VLCD_set instruction to write to the voltage register:
    a. Bit 7 = 1 and bit 6 = 0: bit 5 to bit 0 are the multiplication factor for V_{LCD} of character mode (V_A).
    b. Bit 7 = 1 and bit 6 = 1: bit 5 to bit 0 are the multiplication factor for V_{LCD} of icon mode (V_B).
    c. Bit 5 to bit 0 = 0 switches V_{LCD} generator off (when selected).
    d. During ‘display off’/power-down the V_{LCD} generator is also disabled.
3. Send Function_set instruction with bit H = 0 to resume normal programming.

11. Basic architecture

11.1 Parallel interface

The PCF2119x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 ports DB7 to DB0. Three further control lines E, RS and R/$\overline{W}$ are required.

In 4-bit mode data is transferred in two cycles of 4 bits each using ports DB7 to DB4 for the transaction. The higher order bits (corresponding to range of bit 7 to bit 4 in 8-bit mode) are sent in the first cycle and the lower order bits (bit 3 to bit 0 in 8-bit mode) in the second cycle. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction (see Figure 24 to Figure 26 for examples of bus protocol).

In 4-bit mode, ports DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

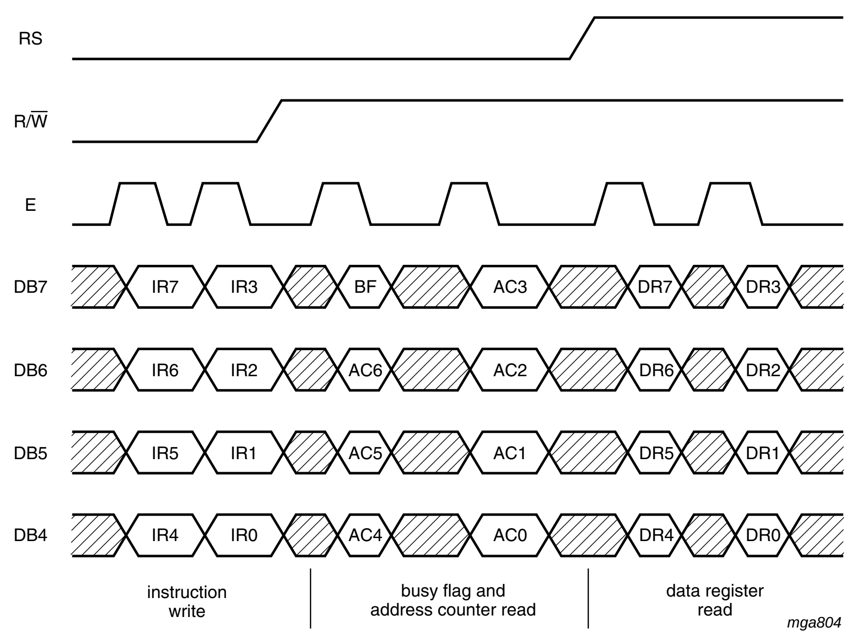
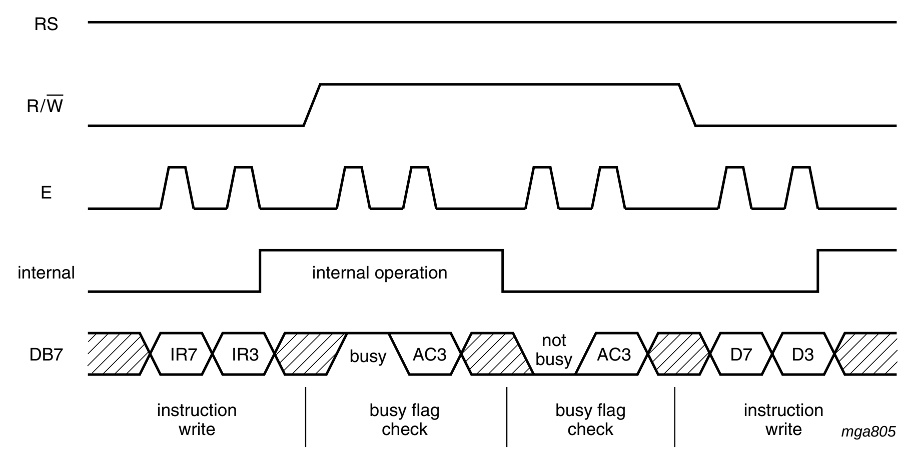


Fig 24. 4-bit transfer example



IR7, IR3: instruction 7th, 3rd bit.

AC3: address counter 3rd bit.

D7, D3: data 7th, 3rd bit.

Fig 25. An example of 4-bit data transfer timing sequence

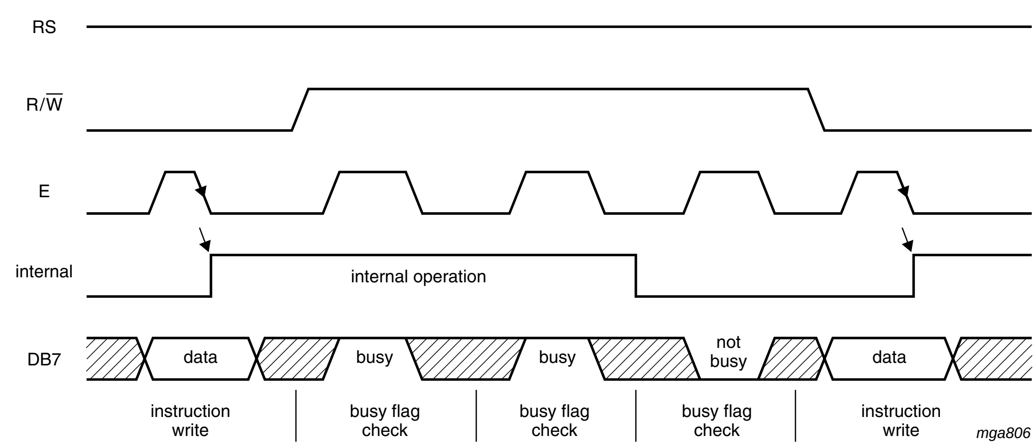


Fig 26. Example of busy flag checking timing sequence

11.2 I2C-bus interface

The I2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are the Serial Data line (SDA) and the Serial Clock Line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

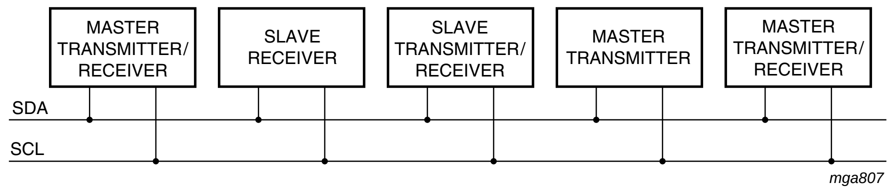


Fig 27. System configuration

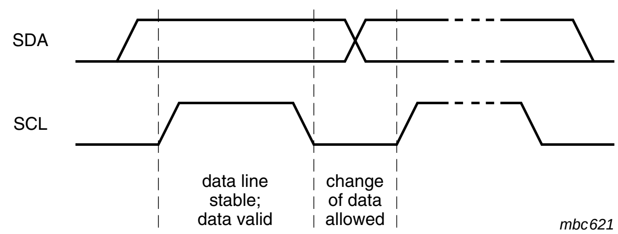


Fig 28. Bit transfer

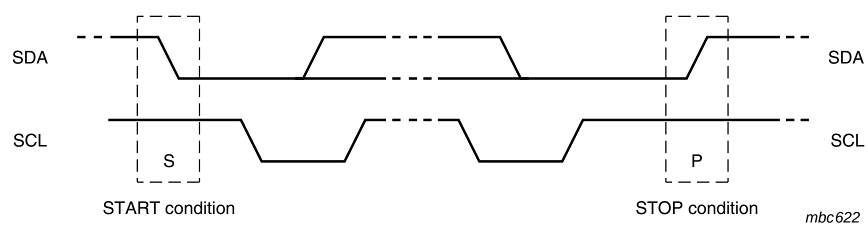


Fig 29. Definition of START and STOP conditions

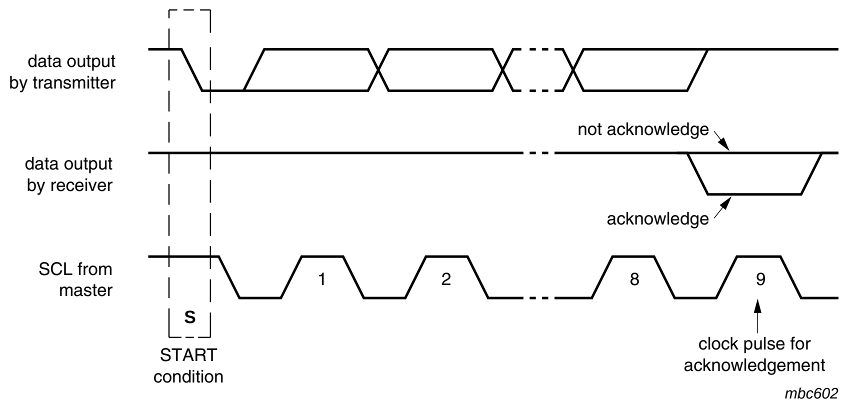


Fig 30. Acknowledgement on the I²C-bus

The I²C-bus interface of PCF2119x is 5 V tolerant.

11.2.1 I²C-bus protocol

One I²C-bus slave address is reserved for the PCF2119x (see Figure 31).

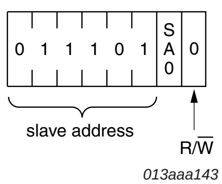


Fig 31. PCF2119x I²C-bus slave address

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure.

The I²C-bus configuration for the different PCF2119x read and write cycles is shown in Figure 32 to Figure 34.

The slow down feature of the I²C-bus protocol (receiver holds SCL line LOW during internal operations) is not used in the PCF2119x.

11.2.2 I²C-bus definitions

Definitions:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device addressed by a master.
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message.

- Arbitration: procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

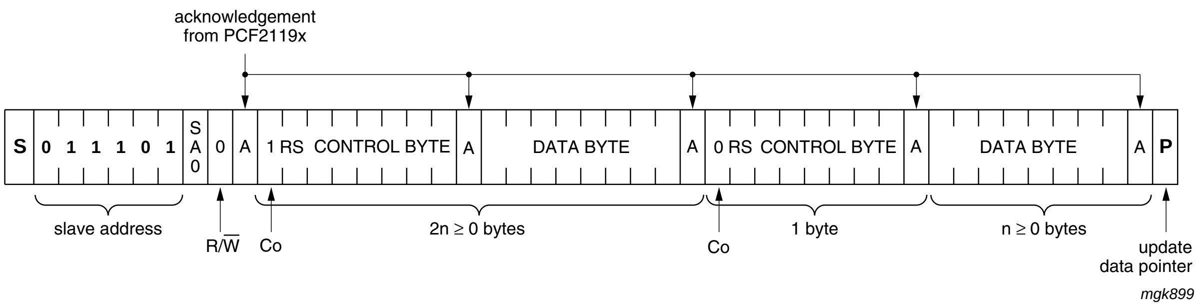
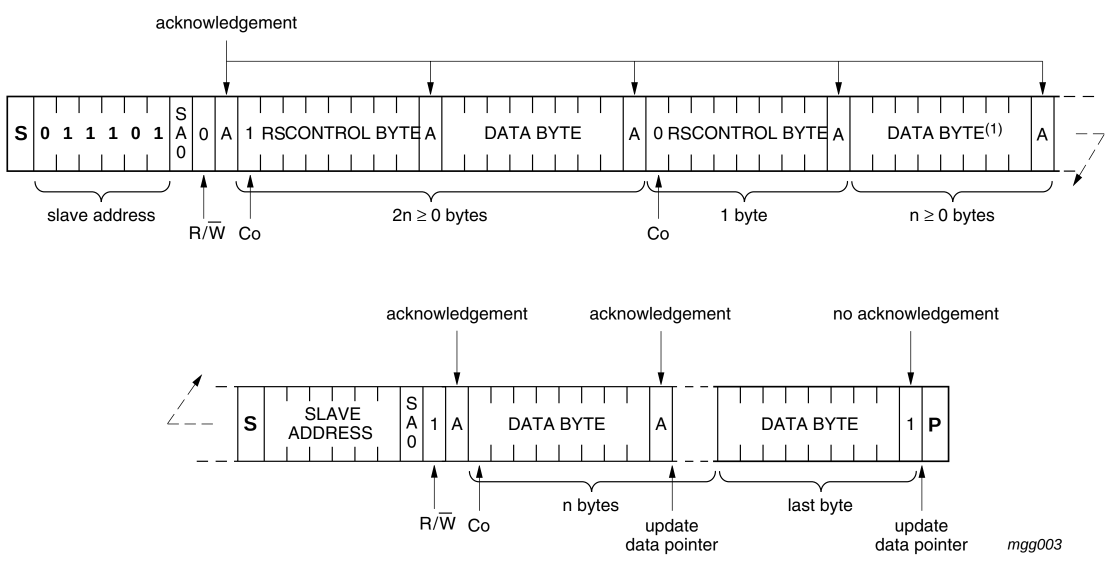


Fig 32. Master transmits to slave receiver; write mode



(1) Last data byte is a dummy byte (may be omitted).

Fig 33. Master reads after setting word address; writes word address, set RS; Read_data

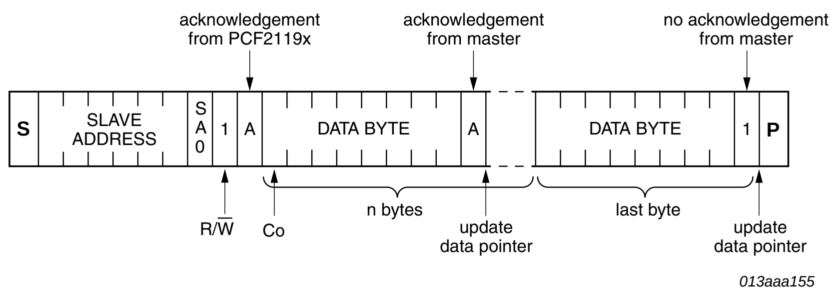
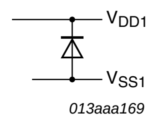
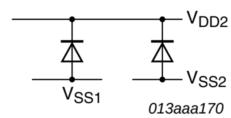
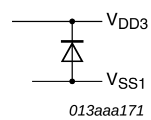
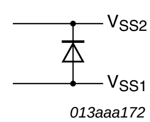
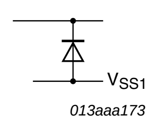
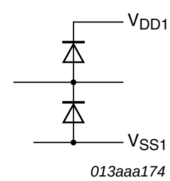
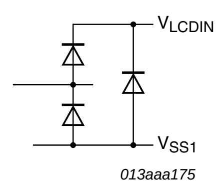


Fig 34. Master reads slave immediately after first byte; read mode (RS previously defined)

12. Internal circuitry

Table 33. Device protection circuits

Symbol	Pin	Internal circuit
V_{DD1}	1 to 6	
V_{DD2}	7 to 14	
V_{DD3}	15 to 18	
V_{SS1}	22 to 29	
V_{SS2}	30 to 35	
$V_{LCDSENSE}$	36	
V_{LCDIN}	44 to 49	
V_{LCDOUT}	37 to 43	
SCL	151 to 152	
SDA	156 to 157	
OSC	168	
PD	155	
POR	154	
T1	20	
T2	21	
T3	153	
E	19	
RS	159	
R/$\overline{W}$	158	
DB0 to DB7	160 to 167	
R1 to R18	58, 57 to 51, 142 to 149, 59, 100, 141	
C1 to C80	140 to 101, 99 to 60	

13. Limiting values

Table 34. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD1}	supply voltage 1	logic		–0.5	+6.5	V
V_{DD2}	supply voltage 2	V_{LCD} generator		–0.5	+4.5	V
V_{DD3}	supply voltage 3					
V_{LCD}	LCD supply voltage			–0.5	+7.5	V
V_I	input voltage	V_{DD} related		–0.5	+6.5	V
		V_{LCD} related		–0.5	+7.5	V
I_I	input current	DC level		–10	+10	mA
I_O	output current	DC level		–10	+10	mA
I_{DD}	supply current			–50	+50	mA
I_{SS}	ground supply current			–50	+50	mA
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P_o	output power	dissipation per output		-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±3000	V
		MM	[2]	-	±300	V
I_{lu}	latch-up current		[3]	-	200	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+85	°C

[1] Pass level; Human Body Model (HBM) according to Ref. 5 “JESD22-A114”.

[2] Pass level; Machine Model (MM), according to Ref. 6 “JESD22-A115”.

[3] Pass level; latch-up testing according to Ref. 7 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the NXP store and transport requirements (see Ref. 9 “NX3-00092”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

14. Static characteristics

Table 35. Static characteristics

V_{DD1} = 1.5 V to 5.5 V; V_{DD2} = V_{DD3} = 2.2 V to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 V to 6.5 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD1}	supply voltage 1	logic		1.5	-	5.5	V
V_{DD2}	supply voltage 2	internal V_{LCD} generation; V_{LCD} > V_{DD2} = V_{DD3}		2.2	-	4.0	V
V_{DD3}	supply voltage 3						
V_{LCD}	LCD supply voltage	pins V_{LCD}, V_{LCDIN}, V_{LCDOUT}		2.2	-	6.5	V
Ground supply current using external V_{LCD} [1]							
I_{SS}	ground supply current			-	70	120	µA
		V_{DD} = 3 V; V_{LCD} = 5 V	[2]	-	35	80	µA
		icon mode; V_{DD} = 3 V; V_{LCD} = 2.5 V	[2]	-	25	45	µA
		power-down mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS and R/$\overline{W}$ = 1; OSC = 0; PD = 1		-	0.5	5	µA
Ground supply current using internal V_{LCD} [1][3]							
I_{SS}	ground supply current			-	190	400	µA
		V_{DD} = 3 V; V_{LCD} = 5 V	[2]	-	135	400	µA
		icon mode; V_{DD} = 2.5 V; V_{LCD} = 2.5 V	[2]	-	85	-	µA
Logic							
V_I	input voltage			–0.5	-	V_{DD1} + 0.5	V
V_{IL}	LOW-level input voltage			V_{SS1}	-	0.3V_{DD1}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD1}	-	V_{DD1}	V
Oscillator input; pin OSC							
V_{IL}	LOW-level input voltage			V_{SS1}	-	V_{DD1} – 1.2	V
V_{IH}	HIGH-level input voltage			V_{DD1} – 0.1	-	V_{DD1}	V
Data bus; pins DB7 to DB0							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD1} = 5 V		1.6	4	-	mA
I_{OH}	HIGH-level output current	V_{OH} = 4 V; V_{DD1} = 5 V		–1	–8	-	mA
I_{pu}	pull-up current	V_I = V_{SS1}		0.04	0.15	1	µA
I_L	leakage current	V_I = $V_{DD1, 2, 3}$ or $V_{SS1, 2}$		–1	-	+1	µA
I^2C-bus; pins SDA and SCL							
Inputs: pins SDA and SCL							
V_I	input voltage			–0.5	-	5.5	V
V_{IL}	LOW-level input voltage			0	-	0.3V_{DD1}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD1}	-	5.5	V
I_{LI}	input leakage current	V_I = $V_{DD1, 2, 3}$ or $V_{SS1, 2}$		–1	-	+1	µA
C_i	input capacitance			-	5	-	pF

Table 35. Static characteristics *…continued*

V_{DD1} = 1.5 V to 5.5 V; V_{DD2} = V_{DD3} = 2.2 V to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output: pin SDA							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD1} > 2 V		3	-	-	mA
		V_{OL} = 0.2 V_{DD1}; V_{DD1} < 2 V		2	-	-	mA
LCD outputs							
R_O	output resistance	row output, pins R1 to R18	[4]	-	10	30	kΩ
		column output, pins C1 to C80	[4]	-	15	40	kΩ
ΔV_{bias}	bias voltage variation	on pins R1 to R18 and C1 to C80	[5]	-	20	130	mV
ΔV_{LCD}	LCD voltage variation	T_{amb} = 25 °C	[3]				
		V_{LCD} < 3 V		-	-	160	mV
		V_{LCD} < 4 V		-	-	200	mV
		V_{LCD} < 5 V		-	-	260	mV
		V_{LCD} < 6 V		-	-	340	mV

[1] LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.

[2] T_{amb} = 25 °C; f_{osc} = 200 kHz.

[3] LCD outputs are open-circuit; V_{LCD} generator is on; load current I_{LCD} = 5 μA.

[4] Resistance of output pins (R1 to R18 and C1 to C80) with a load current of 10 μA; outputs measured one at a time; external LCD supply V_{LCD} = 3 V; V_{DD1} = V_{DD2} = V_{DD3} = 3 V.

[5] LCD outputs open-circuit; external LCD supply.

15. Dynamic characteristics

Table 36. Dynamic characteristics

V_{DD1} = 1.5 V to 5.5 V; V_{DD2} = V_{DD3} = 2.2 V to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock and oscillator							
$f_{fr(LCD)}$	LCD frame frequency	internal clock; V_{DD} = 5.0 V		45	95	147	Hz
f_{osc}	oscillator frequency	not available at any pin		140	250	450	kHz
$f_{osc(ext)}$	external oscillator frequency			140	-	450	kHz
$t_{d(startup)(OSC)}$	start-up delay time on pin OSC	oscillator, after power-down	[1]	-	200	300	µs
Timing characteristics of parallel interface[2]							
Write operation (writing data from microcontroller to PCF2119x); see Figure 35							
$t_{cy(en)}$	enable cycle time			500	-	-	ns
$t_{w(en)}$	enable pulse width			220	-	-	ns
$t_{su(A)}$	address set-up time			50	-	-	ns
$t_{h(A)}$	address hold time			25	-	-	ns
$t_{su(D)}$	data input set-up time			60	-	-	ns
$t_{h(D)}$	data input hold time			25	-	-	ns
Read operation (reading data from PCF2119x to microcontroller); see Figure 36							
$t_{cy(en)}$	enable cycle time			500	-	-	ns
$t_{w(en)}$	enable pulse width			220	-	-	ns
$t_{su(A)}$	address set-up time			50	-	-	ns
$t_{h(A)}$	address hold time			25	-	-	ns
$t_{d(DV)}$	data input valid delay time	V_{DD1} > 2.2 V		-	-	150	ns
		V_{DD1} > 1.5 V		-	-	250	ns
$t_{h(D)}$	data input hold time			20	-	100	ns
Timing characteristics of I^2C-bus interface[2]; see Figure 37							
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
t_r	rise time of both SDA and SCL signals		[1][3]	15 + 0.1 C_b	-	300	ns
t_f	fall time of both SDA and SCL signals		[1][3]	15 + 0.1 C_b	-	300	ns
C_b	capacitive load for each bus line			-	-	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs

Table 36. Dynamic characteristics *...continued*

V_{DD1} = 1.5 V to 5.5 V; V_{DD2} = V_{DD3} = 2.2 V to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	-	50	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs

[1] Tested on sample base.

[2] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[3] C_b = total capacitance of one bus line in pF.

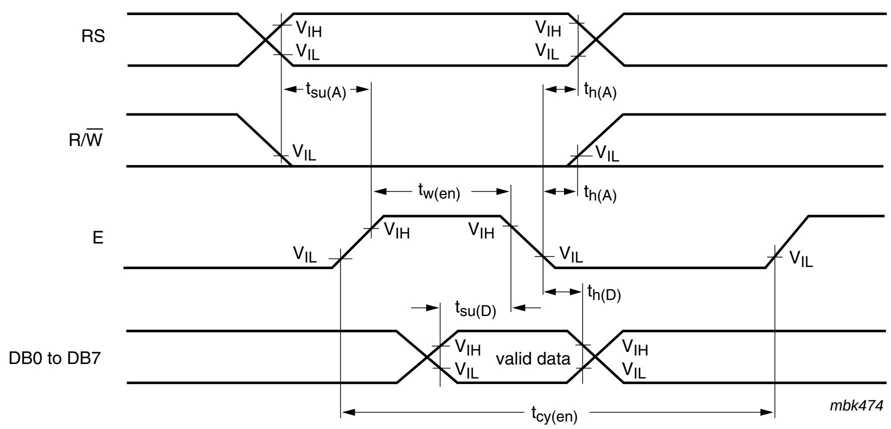


Fig 35. Parallel bus write operation sequence; writing data from microcontroller to PCF2119x

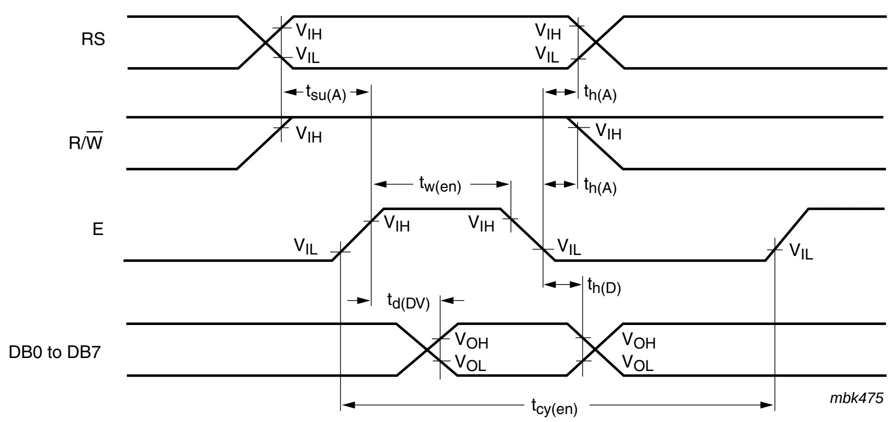


Fig 36. Parallel bus read operation sequence; writing data from PCF2119x to microcontroller

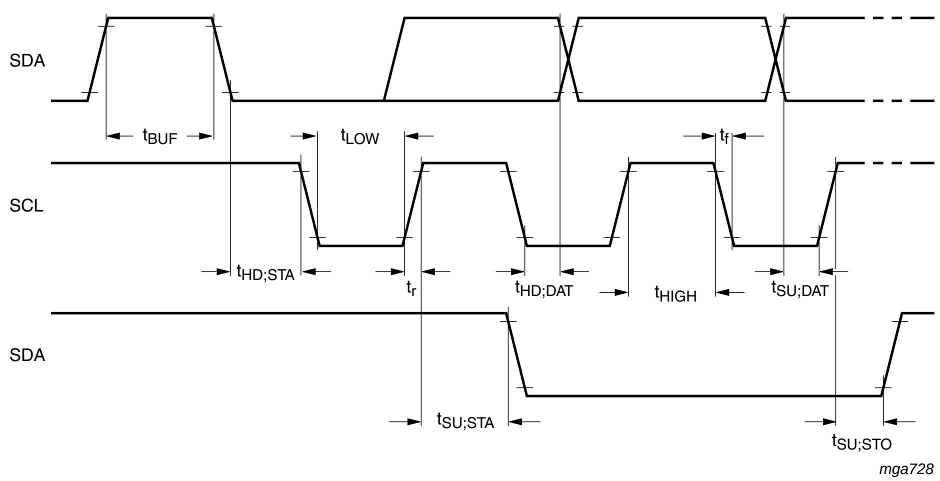


Fig 37. I²C-bus timing diagram

16. Application information

16.1 General application information

The required minimum value for the external capacitors in an application with the PCF2119x are: C_{ext} from pins V_{LCD} to V_{SS} = 100 nF and for pins V_{DD} to V_{SS} = 470 nF. Higher capacitor values are recommended for ripple reduction.

For COG applications the recommended ITO track resistance is to be minimized for the I/O and supply connections. Optimized values for these tracks are below 50 Ω for the supply and below 100 Ω for the I/O connections. Higher track resistance reduce performance and increase current consumption. To avoid accidental triggering of Power-On Reset (POR) (especially in COG applications), the supplies must be adequately decoupled. Depending on power supply quality, V_{DD1} may have to be risen above the specified minimum.

When external LCD supply voltage is supplied, V_{LCDOUT} should be left open-circuit to avoid any stray current, and V_{LCDIN} must be connected to $V_{LCDSENSE}$.

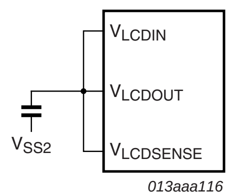
The PCF2119x I^{2}C-bus interface is compatible with systems, where the I^{2}C pull-up resistors are connected to a 5 V ±10 % supply.

16.2 Power supply connections for internal V_{LCD} generation

Drawings are showing alternative circuits.

Decoupling capacitors are not shown in the drawings.

Fig 38. Recommended V_{DD} connections for internal V_{LCD} generation



The value of the capacitor should be at least 100 nF.

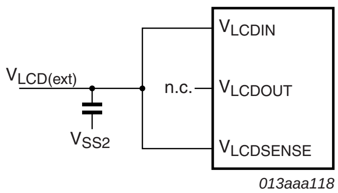
Fig 39. Recommended V_{LCD} connections for internal V_{LCD} generation

16.3 Power supply connections for external V_{LCD} generation

Drawings are showing alternative circuits.

Decoupling capacitors are not shown in the drawings.

Fig 40. Recommended V_{DD} connections for external V_{LCD} generation



The value of the capacitor should be at least 100 nF.

Fig 41. Recommended V_{LCD} connections for external V_{LCD} generation

Remark: When using an external V_{LCD}, the internal V_{LCD} generator **must never** be switched on and direct mode must be avoided otherwise damages will occur.

16.4 Information about V_{LCD} connections

V_{LCDIN} — This input is used for generating the 5 LCD bias levels. It is the power supply for the bias level buffers.

V_{LCDOUT} — This is the V_{LCD} output if V_{LCD} is generated internally. In this case pin V_{LCDOUT} must be connected to V_{LCDIN} and to $V_{LCDSENSE}$. If V_{LCD} is generated externally, V_{LCDOUT} must be left unconnected.

$V_{LCDSENSE}$ — This input is used for the voltage multiplier's regulation circuitry. When using the internal V_{LCD} generation, this pin must be connected to V_{LCDOUT} and V_{LCDIN}. When using an external V_{LCD} supply it must be connected to V_{LCDIN} only.

16.5 Reducing current consumption

Reducing current consumption can be achieved by one of the options given in Table 37.

When V_{LCD} lies outside the V_{DD} range and must be generated, it is usually more efficient to use the on-chip V_{LCD} generator than an external regulator.

Table 37. Reducing current consumption

Original mode	Alternative mode
character mode	icon mode (control bit IM)
display on	display off (control bit D)
V_{LCD} generator operating	direct mode
any mode	power-down mode (pin PD)

16.6 Charge pump characteristics

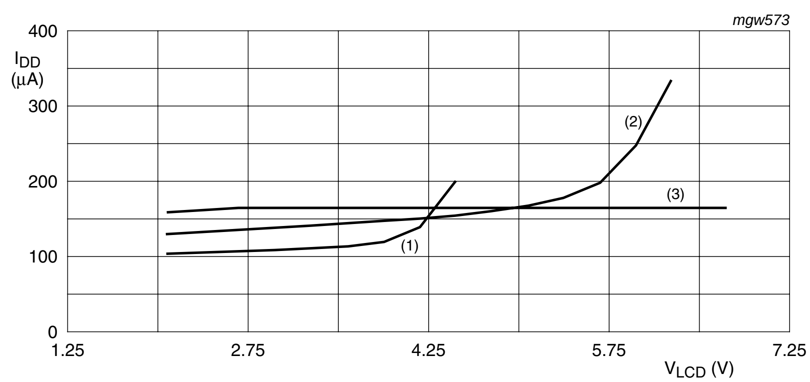
Typical graphs of the total power consumption of the PCF2119x using the internal charge pump are illustrated in Figure 42, Figure 43 and Figure 44.

The graphs were obtained under the following conditions:

- T_{amb} = 25 °C
- $V_{DD1} = V_{DD2} = V_{DD3}$ = 2.2 V (minimum), 2.7 V (typical) and 4.0 V (maximum)
- Normal mode
- f_{osc} = internal oscillator
- multiplex drive mode 1:18
- Typical current load for I_{LCD} = 10 μA.

For each multiplication factor there is a separate line. The line ends where it is not possible to get a higher voltage under its conditions (a higher multiplication factor is needed to get higher voltages).

Connecting different displays may result in different current consumption. This affects the efficiency and the optimum multiplication factor to be used to generate a certain output voltage.

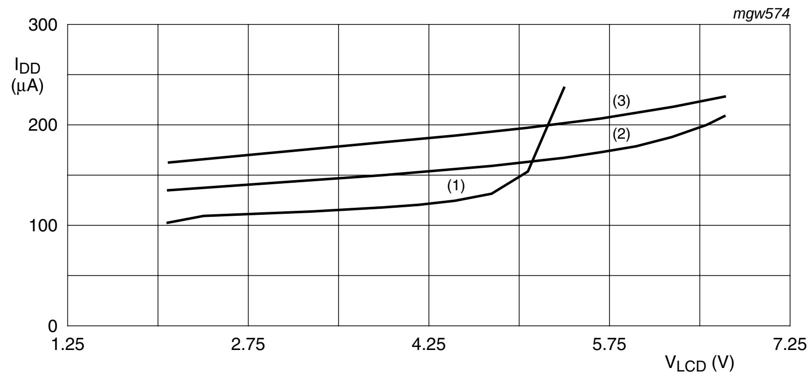


(1) 2 × multiplication factor.

(2) 3 × multiplication factor.

(3) 4 × multiplication factor.

Fig 42. Typical charge pump characteristics (a), V_{DD} = 2.2 V

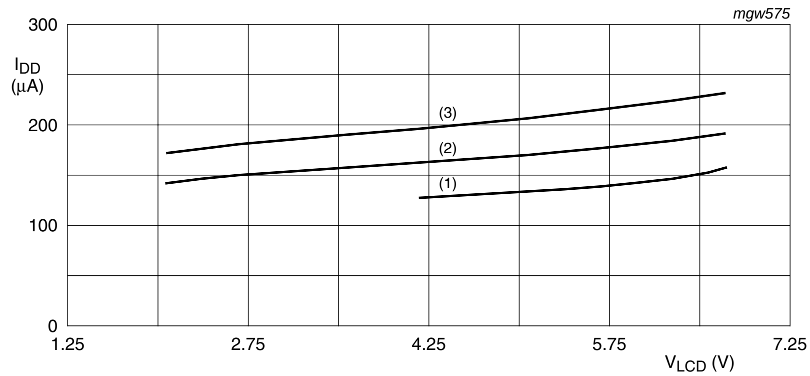


(1) 2 × multiplication factor.

(2) 3 × multiplication factor.

(3) 4 × multiplication factor.

Fig 43. Typical charge pump characteristics (b), V_{DD} = 2.7 V



(1) 2 × multiplication factor.

(2) 3 × multiplication factor.

(3) 4 × multiplication factor.

Fig 44. Typical charge pump characteristics (c), V_{DD} = 4.0 V

16.7 Interfaces

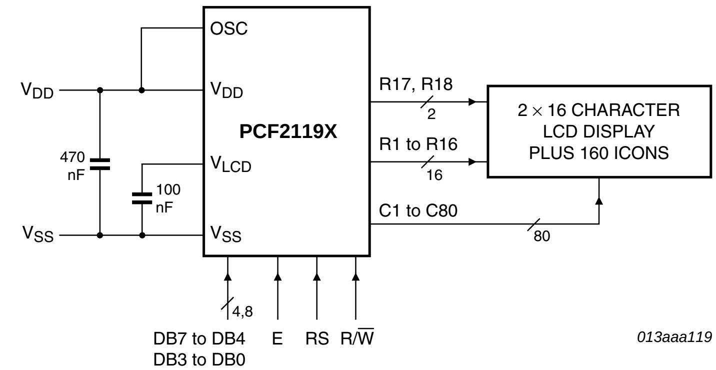


Fig 45. Typical application using parallel interface, 4 or 8 bit bus possible

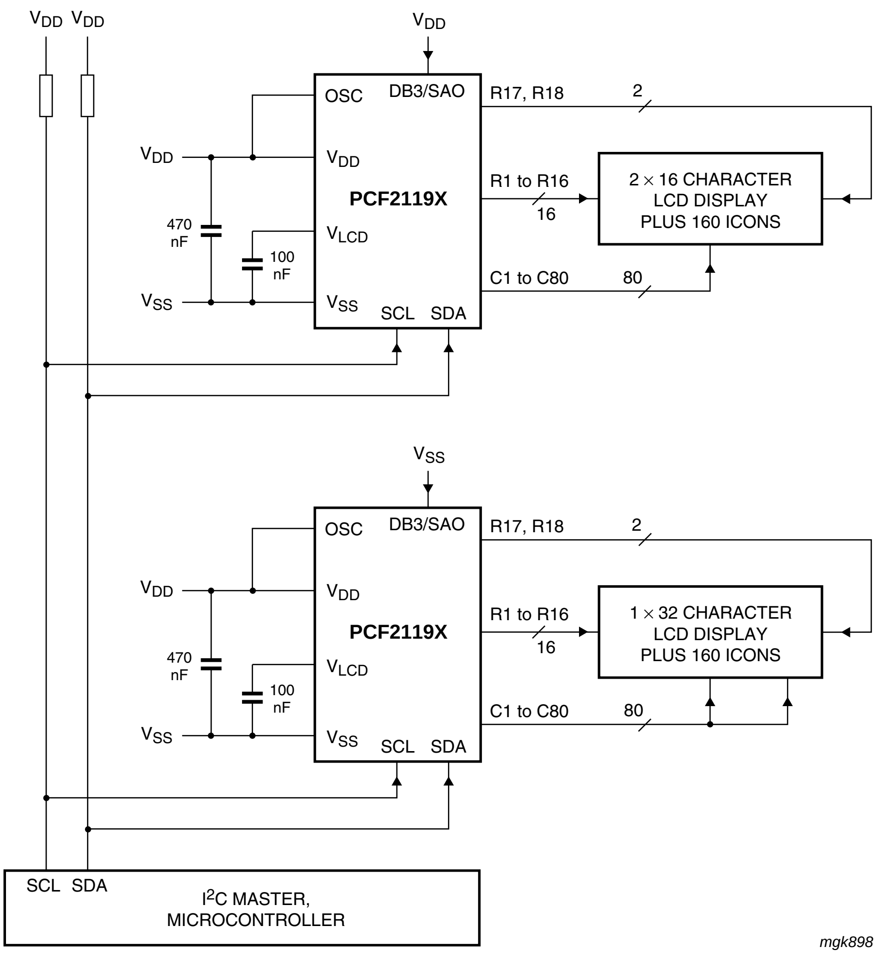


Fig 46. Application using I²C-bus interface

16.8 Connections with LCD modules

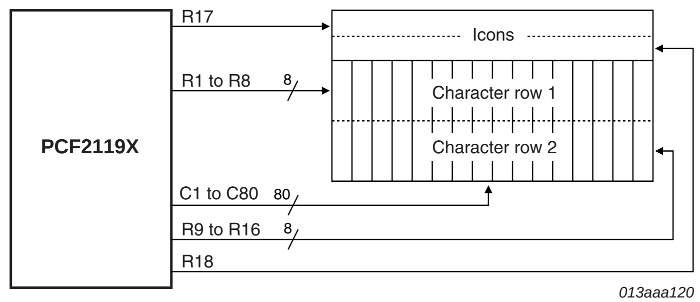


Fig 47. Connecting PCF2119x with 2 × 16 character LCD

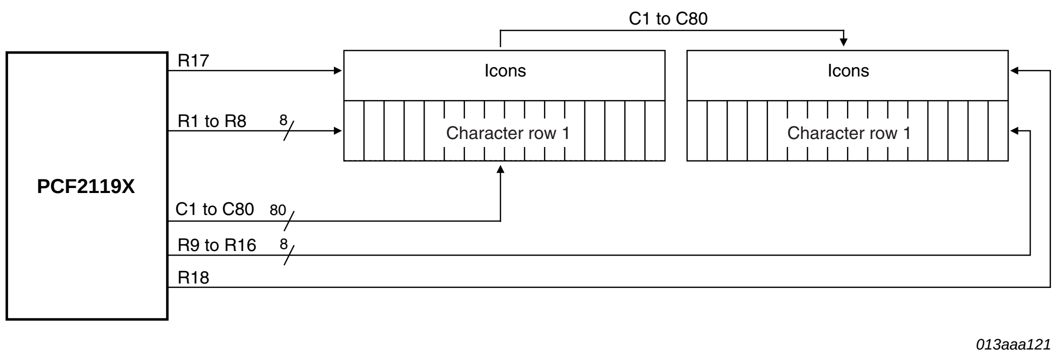


Fig 48. Connecting PCF2119x with 1 × 32 character LCD

16.9 4-bit operation, 1-line display using external reset

The program must set functions prior to a 4-bit operation (see Table 38). When power is turned on, 8-bit operation is automatically selected and the PCF2119x attempts to perform the first write as an 8-bit operation. Since nothing is connected to ports DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 38 step 3). Thus, DB4 to DB7 of the Function_set are written twice.

Table 38. 4-bit operation, 1-line display example; using external reset (character set 'A')

Step	Instruction						Display	Operation
	RS	R/W	DB7	DB6	DB5	DB4		
1	power supply on							initialized by the external reset; no display appears
2	Function_set							sets to 4-bit operation; in this instance operation is handled as 8-bit by initialization and only this instruction completes with one write
	0	0	0	0	1	0		
3	Function_set							sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$; 4-bit operation starts from this point and resetting is needed
	0	0	0	0	1	0		
	0	0	0	0	0	0		
4	Display_ctl							turns display and cursor on; entire display is blank after initialization
	0	0	0	0	0	0	_	
	0	0	1	1	1	0		
5	Entry_mode_set							sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
	0	0	0	0	0	0	_	
	0	0	0	1	1	0		
6	Write_data to CGRAM/DDRAM							writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	1	0	1	**P**_	
	1	0	0	0	0	0		

16.10 8-bit operation, 1-line display using external reset

Table 39 and Table 40 show an example of a 1-line display in 8-bit operation. The PCF2119x functions must be set by the Function_set instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and the DDRAM contents remain unchanged, display data entered first can be displayed when the Return_home operation is performed.

Table 39. 8-bit operation, 1-line display example; using external reset (character set 'A')

Step	Instruction										Display	Operation
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	power supply on											initialized by the external reset; no display appears
2	Function_set											sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
	0	0	0	0	1	1	0	0	0	0		
3	Display_ctl											turns on display and cursor; entire display is blank after initialization
	0	0	0	0	0	0	1	1	1	0	_	

Table 39. 8-bit operation, 1-line display example; using external reset (character set 'A') *…continued*

Step	Instruction										Display	Operation
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
4	Entry_mode_set											sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DDRAM/CGRAM; display is not shifted
	0	0	0	0	0	0	0	1	1	0	_	
5	Write_data to CGRAM/DDRAM											writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	1	0	1	0	0	0	0	**P_**	
6	Write_data to CGRAM/DDRAM											writes 'H'
	1	0	0	1	0	0	1	0	0	0	**PH_**	
7 to 10			:								**PHILIP_**	writes 'ILIP'
11	Write_data to CGRAM/DDRAM											writes 'S'
	1	0	0	1	0	1	0	0	1	1	**PHILIPS_**	
12	Entry_mode_set											sets mode for display shift at the time of write
	0	0	0	0	0	0	0	1	1	1	**PHILIPS_**	
13	Write_data to CGRAM/DDRAM											writes space
	1	0	0	0	1	0	0	0	0	0	**HILIPS _**	
14	Write_data to CGRAM/DDRAM											writes 'M'
	1	0	0	1	0	0	1	1	0	1	**ILIPS M_**	
15 to 19			:								MICROK_	writes 'ICROK'
20	Write_data to CGRAM/DDRAM											writes 'O'
	1	0	0	1	0	0	1	1	1	1	**MICROKO_**	
21	Curs_disp_shift											shifts only the cursor position to the left
	0	0	0	0	0	1	0	0	0	0	**MICROKO**	
22	Curs_disp_shift											shifts only the cursor position to the left
	0	0	0	0	0	1	0	0	0	0	**MICROKO**	
23	Write_data to CGRAM/DDRAM											writes 'C' correction; display moves to the left
	1	0	0	1	0	0	0	0	1	1	**ICROCO**	
24	Curs_disp_shift											shifts the display and cursor to the right
	0	0	0	0	0	1	1	1	0	0	**MICROCO**	
25	Curs_disp_shift											shifts only the cursor to the right
	0	0	0	0	0	1	0	1	0	0	**MICROCO_**	
26	Write_data to CGRAM/DDRAM											writes 'M'
	1	0	0	1	0	0	1	1	0	1	**ICROCOM_**	
27	Return_home											returns both display and cursor to the original position (address 0)
	0	0	0	0	0	0	0	0	1	0	**PHILIPS M**	

Table 40. 8-bit operation, 1-line display and icon example; using external reset (character set 'A')

Step	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Display	Operation
1	power supply on											initialized by the external reset; no display appears
2	Function_set											sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
	0	0	0	0	1	1	0	0	0	0		
3	Display_ctl											turns on display and cursor; entire display is blank after initialization
	0	0	0	0	0	0	1	1	1	0	_	
4	Entry_mode_set											sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
	0	0	0	0	0	0	0	1	1	0	_	
5	Set_CGRAM											sets the CGRAM address to position of character 0; the CGRAM is selected
	0	0	0	1	0	0	0	0	0	0	_	
6	Write_data to CGRAM/DDRAM											writes data to CGRAM for icon even phase; icons appears
	1	0	0	0	0	0	1	0	1	0	_	
7	:										_	
8	Set_CGRAM											sets the CGRAM address to position of character 4; the CGRAM is selected
	0	0	0	1	1	1	0	0	0	0	_	
9	Write_data to CGRAM/DDRAM											writes data to CGRAM for icon odd phase
	1	0	0	0	0	0	1	0	1	0	_	
10	:										_	
11	Function_set											sets bit H = 1
	0	0	0	0	1	1	0	0	0	1	_	
12	Icon_ctl											icons blink
	0	0	0	0	0	0	1	0	1	0	_	
13	Function_set											sets bit H = 0
	0	0	0	0	1	1	0	0	0	1	_	
14	Set_DDRAM											sets the DDRAM address to the first position; DDRAM is selected
	0	0	1	0	0	0	0	0	0	0		
15	Write_data to CGRAM/DDRAM											writes 'P'; the cursor is incremented by 1 and shifted to the right
	1	0	0	1	0	1	0	0	0	0	**P_**	
16	Write_data to CGRAM/DDRAM											writes 'H'
	1	0	0	1	0	0	1	0	0	0	**PH_**	
17 to 21	:										**PHILIPS_**	writes 'ILIPS'
22	Return_home											returns both display and cursor to the original position (address 0)
	0	0	0	0	0	0	0	0	1	0	**PHILIPS**	

16.11 8-bit operation, 2-line display

For a 2-line display the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the 8th character is completed (see Table 41). It should be noted that both lines of the display are always shifted together; data does not shift from one line to the other.

Table 41. 8-bit operation, 2-line display example; using external reset (character set 'A')

Step	Instruction										Display	Operation
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	power supply on											initialized by the external reset; no display appears
2	Function_set											sets to 8-bit operation; selects 2-line display and V_{LCD} generator off
	0	0	0	0	1	1	0	1	0	0		
3	display mode on/off control											turns on display and cursor; entire display is blank after initialization
	0	0	0	0	0	0	1	1	1	0	_	
4	Entry_mode_set											sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted
	0	0	0	0	0	0	0	1	1	0	_	
5	Write_data to CGRAM/DDRAM											writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	1	0	1	0	0	0	0	**P_**	
6 to 10	:										**PHILIP_**	writes 'HILIP'
11	Write_data to CGRAM/DDRAM											writes 'S'
	1	0	0	1	0	1	0	0	1	1	**PHILIPS_**	
12	Set_DDRAM											sets DDRAM address to position the cursor at the head of the 2nd line
	0	0	1	1	0	0	0	0	0	0	**PHILIPS** _	
13	Write_data to CGRAM/ DDRAM											writes 'M'
	1	0	0	1	0	0	1	1	0	1	**PHILIPS** **M_**	
14 to 18	:										**PHILIPS** **MICROC_**	writes 'ICROC'
19	Write_data to CGRAM/DDRAM											writes 'O'
	1	0	0	1	0	0	1	1	1	1	**PHILIPS** **MICROCO_**	
20	Write_data to CGRAM/DDRAM											sets mode for display shift at the time of write
	0	0	0	0	0	0	0	1	1	1	**PHILIPS** **MICROCO_**	
21	Write_data to CGRAM/DDRAM											writes 'M'; display is shifted to the left; the first and second lines shift together
	1	0	0	1	0	0	1	1	0	1	**HILIPS** **ICROCOM_**	

Table 41. 8-bit operation, 2-line display example; using external reset (character set 'A') *…continued*

Step	Instruction										Display	Operation
	RS	$R/\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
22					:						:	
23	Return_home											returns both display and cursor to the original position (address 0)
	0	0	0	0	0	0	0	0	1	0	**PHILIPS MICROCOM**	

16.12 I²C-bus operation, 1-line display

A control byte is required with most commands (see Table 42).

Table 42. Example of I²C-bus operation; 1-line display (using external reset, assuming pin SA0 = V_{SS})[1]

Step	I²C-bus byte									Display	Operation
1	I²C-bus start										initialized; no display appears
2	slave address for write										during the acknowledge cycle SDA will be pulled-down by the PCF2119x
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	$R/\overline{W}$	Ack		
	0	1	1	1	0	1	0	0	1		
3	send a control byte for Function_set										control byte sets RS for following data bytes
	CO	RS	0	0	0	0	0	0	Ack		
	0	0	0	0	0	0	0	0	1		
4	Function_set										selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	1	X	0	0	0	0	1		
5	Display_ctl										turns on display and cursor; entire display shows character code 20h (blank in ASCII-like character sets)
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	_	
	0	0	0	0	1	1	1	0	1		
6	Entry_mode_set										sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	_	
	0	0	0	0	0	1	1	0	1		
7	I²C-bus start									_	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write										
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	$R/\overline{W}$	Ack	_	
	0	1	1	1	0	1	0	0	1		
9	send a control byte for Write_data										
	CO	RS	0	0	0	0	0	0	Ack	_	
	0	1	0	0	0	0	0	0	1		
10	Write_data to DDRAM										writes 'P'; the DDRAM has been selected at power-on; the cursor is incremented by 1 and shifted to the right
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	**P_**	
	0	1	0	1	0	0	0	0	1		
11	Write_data to DDRAM										writes 'H'
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	**PH_**	
	0	1	0	0	1	0	0	0	1		
12 to 15					:					**PHILIP_**	writes 'ILIP'

Table 42. Example of I²C-bus operation; 1-line display (using external reset, assuming pin SA0 = V_{SS})[1] *…continued*

Step	I²C-bus byte									Display	Operation
16	Write_data to DDRAM										writes ‘S’
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	**PHILIPS_**	
	0	1	0	1	0	0	1	1	1		
17	optional I²C-bus STOP									**PHILIPS_**	
18	I²C-bus start									**PHILIPS_**	
19	slave address for write										
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack	**PHILIPS_**	
	0	1	1	1	0	1	0	0	1		
20	control byte										
	CO	RS	0	0	0	0	0	0	Ack	**PHILIPS_**	
	1	0	0	0	0	0	0	0	1		
21	Return_home										sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the data register
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	**PHILIPS**	
	0	0	0	0	0	0	1	0	1		
22	I²C-bus start									**PHILIPS**	
23	slave address for read										during the acknowledge cycle the content of the data register is loaded into the internal I²C-bus interface to be shifted out; in the previous instruction neither a ‘set address’ nor a Read_data has been performed; therefore the content of the data register was unknown; bit R/$\overline{W}$ has to be set to logic 1 while still in I²C-write mode
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack	**PHILIPS**	
	0	1	1	1	0	1	0	1	1		
24	control byte for read										DDRAM content will be read from following instructions
	CO	RS	0	0	0	0	0	0	Ack	**PHILIPS**	
	0	1	1	0	0	0	0	0	1		
25	Read_data: 8 × SCL + master acknowledge[2]										8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	**PHILIPS**	
	X	X	X	X	X	X	X	X	0		
26	Read_data: 8 × SCL + master acknowledge[2]										8 × SCL; code of letter ‘H’ is read first; during master acknowledge code of ‘I’ is loaded into the I²C-bus interface
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	**PHILIPS**	
	0	1	0	0	1	0	0	0	0		
27	Read_data: 8 × SCL + no master acknowledge[2]										no master acknowledge; after the content of the I²C-bus interface register is shifted out no internal action is performed; no new data is loaded to the interface register, data register is not updated, address counter is not incremented and cursor is not shifted
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	**PHILIPS**	
	0	1	0	0	1	0	0	1	1		
28	I²C-bus STOP									**PHILIPS**	

[1] X = don’t care.

[2] SDA is left at high-impedance by the microcontroller during the read acknowledge.

16.13 Initialization

Table 43. Initialization by instruction, 8-bit interface ([1])

Step	Instruction										Description
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	power-on or unknown state										
2	wait 2 ms										after internal reset has been applied
3	Function_set										interface is 8 bits long; BF cannot be checked before this instruction
	0	0	0	0	1	1	X	X	X	X	
4	wait 2 ms										
5	Function_set										interface is 8 bits long; BF cannot be checked before this instruction
	0	0	0	0	1	1	X	X	X	X	
6	wait more than 40 μs										
7	Function_set										interface is 8 bits long; BF cannot be checked before this instruction
	0	0	0	0	1	1	X	X	X	X	
BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 11)											
8	Function_set (interface is 8 bits long)										specify number of display lines
	0	0	0	0	1	1	0	M	0	H	
9	Display_ctl										display off
	0	0	0	0	0	0	1	0	0	0	
10	Clear_display										
	0	0	0	0	0	0	0	0	0	1	
11	Entry_mode_set										
	0	0	0	0	0	0	0	1	I_D	S	
12	initialization ends										

[1] X = don't care.

Table 44. Initialization by instruction, 4-bit interface; not applicable for I²C-bus operation

Step	Instruction						Description
	RS	R/W̄	DB7	DB6	DB5	DB4	
1	power-on or unknown state						
2	wait 2 ms after internal reset has been applied						
3	Function_set						interface is 8 bits long; BF cannot be checked before this instruction
	0	0	0	0	1	1	
4	wait 2 ms						
5	Function_set						interface is 8 bits long; BF cannot be checked before this instruction
	0	0	0	0	1	1	
6	wait more than 40 μs						
7	Function_set						interface is 8 bits long; BF cannot be checked before this instruction
	0	0	0	0	1	1	
BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 11)							
8	Function_set						
	0	0	0	0	1	0	set interface to 4 bit long interface is 8 bit long
9	Function_set						
	0	0	0	0	1	0	set interface to 4 bits long
	0	0	0	M	0	H	specify number of display line
10	Display_ctl						
	0	0	0	0	0	0	
	0	0	1	0	0	0	display off
11	Clear_display						
	0	0	0	0	0	0	
	0	0	0	0	0	1	
12	Entry_mode_set						
	0	0	0	0	0	0	
	0	0	0	1	I_D	S	
				:			
13	Initialization ends						

16.14 User defined characters and symbols

Up to 16 user defined characters may be stored in the CGRAM. The content of the CGRAM is lost during power-down, therefore the CGRAM has to be rewritten after every power-on.

0	0	1	1	0
0	1	0	0	1
0	1	0	0	0
1	1	1	1	0
1	1	1	1	0
0	1	0	0	0
0	1	0	0	1
0	0	1	1	0

013aaa144

Fig 49. User defined euro currency sign

Below some source code is printed, which shows how a user defined character is defined - in this case the euro currency sign. The display used is a 2 lines by 16 characters display and the interface is the I^2C-bus:

```
// Write a user defined character into the CGRAM
startI2C();
// PCF2119 slave address for write, SA0 is connected to Vdd
SendI2CAddress(0x70);
// MSB (Continuation bit Co) = 0, more than one byte may follow. Bit6, RS=0, next byte
// is command byte
i2c_write(0x00);
// 2 lines x 16, 1/18 duty, basic instruction set. Next byte will be another command.
i2c_write(0x24);
// Set CGRAM address to 0
i2c_write(0x40);
// Repeated Start condition
startI2C();
SendI2CAddress(0x70);
// RS=1, next byte is a data byte
i2c_write(0x40);

// Here the data bytes to define the character
// Behind the write commands the 5x8 dot matrix is shown, the 1 represents a on pixel.
// The Euro currency character can be recognized by the 0/1 pattern (see Figure 49)
i2c_write(0x06); // 00110
i2c_write(0x09); // 01001
i2c_write(0x08); // 01000
i2c_write(0x1E); // 11110
i2c_write(0x1E); // 11110
i2c_write(0x08); // 01000
i2c_write(0x09); // 01001
```

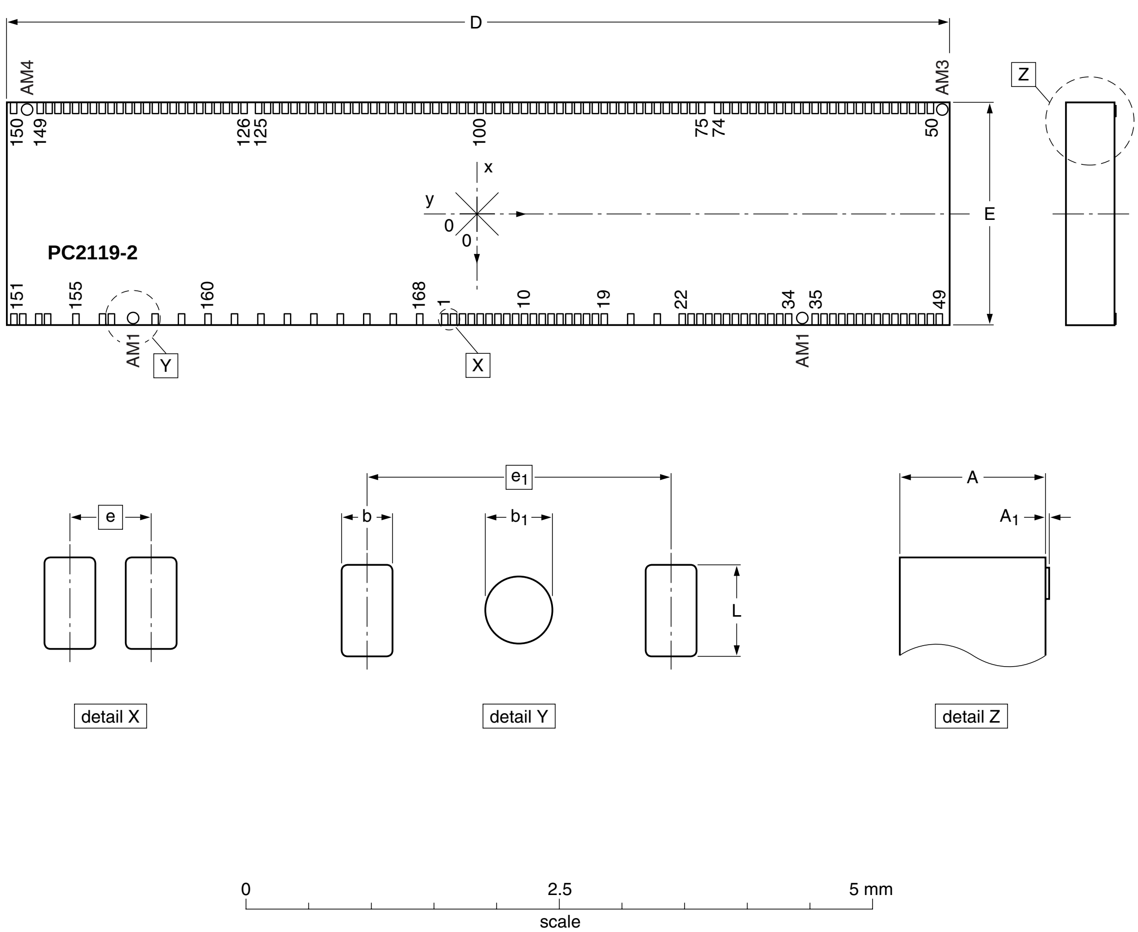
```
i2c_write(0x06); // 00110
i2c_stop();
// Until here the definition of the character and writing it into the CGRAM. Now it
// still needs to be displayed. See below.

// PCF2119, setting of proper display modes
startI2C();
// PCF2119 slave address for write, SA0 is connected to Vdd
SendI2CAddress(0x70);
// MSB (Continuation bit Co) = 0, more than one byte may follow. Bit6, RS=0, next byte
// is command byte
i2c_write(0x00);
// 2 lines x 16, 1/18 duty, extended instruction set. Next byte will be another
// command.
i2c_write(0x25);
// Set display configuration to right to left, column 80 to 1. Row data displ. top to
// bottom,1 to 16.
i2c_write(0x06);
// Set to character mode, full display, icon blink disabled
i2c_write(0x08);
// Set voltage multiplier to 2
i2c_write(0x40);
// Set Vlcd and store in register VA
i2c_write(0xA0);
// Change from extended instruction set to basic instruction set
i2c_write(0x24);
// Display control: set display on, cursor off, no blink
i2c_write(0x0C);
// Entry mode set, increase DDRAM after access, no shift
i2c_write(0x06);
// Return home, set DDRAM address 0 in address counter
i2c_write(0x02);
// Clear entire display, set DDRAM address to 0 in address counter
i2c_write(0x01);

// Repeated Start condition because RS needs to be changed from 0 to 1
startI2C();
SendI2CAddress(0x70);
// RS=1, next byte is data
i2c_write(0x40);
// Write the character at address 0, which is the previously defined Euro currency
// character
i2c_write(0x00);
i2c_stop();
```

17. Bare die outline

Bare die: 168 bumps; 7.59 x 1.71 x 0.38 mm **PCF2119X**



Dimensions

Unit		A(1)	A_1(1)	b(1)	b_1(1)	D	E	e(1)	e_1(1)	L(1)
mm	max		0.0225							
	nom	0.380	0.0175	0.050	0.100	7.59	1.71	0.070	0.350	0.090
	min		0.0125							

Note

1. Dimension not drawn to scale

pcf2119x_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF2119X						~~09-07-16~~ 09-08-03

Fig 50. Bare die outline of PCF2119x

Table 45. Pin location

All X and Y coordinates are referenced to the center of the chip (dimensions in μm).

Symbol	Pin	X	Y	Description
V_{DD1}	1	+745	−274	logic supply voltage 1
V_{DD1}	2	+745	−204	
V_{DD1}	3	+745	−134	
V_{DD1}	4	+745	−64	
V_{DD1}	5	+745	+6	
V_{DD1}	6	+745	+76	
V_{DD2}	7	+745	+146	V_{LCD} generator supply voltage 2
V_{DD2}	8	+745	+216	
V_{DD2}	9	+745	+286	
V_{DD2}	10	+745	+356	
V_{DD2}	11	+745	+426	
V_{DD2}	12	+745	+496	
V_{DD2}	13	+745	+566	
V_{DD2}	14	+745	+636	
V_{DD3}	15	+745	+706	
V_{DD3}	16	+745	+776	
V_{DD3}	17	+745	+846	
V_{DD3}	18	+745	+916	
E	19	+745	+986	data bus clock input
T1	20	+745	+1196	test pin 1
T2	21	+745	+1406	test pin 2
V_{SS1}	22	+745	+1616	ground 1
V_{SS1}	23	+745	+1686	
V_{SS1}	24	+745	+1756	
V_{SS1}	25	+745	+1826	
V_{SS1}	26	+745	+1896	
V_{SS1}	27	+745	+1966	
V_{SS1}	28	+745	+2036	
V_{SS1}	29	+745	+2106	
V_{SS2}	30	+745	+2176	ground 2
V_{SS2}	31	+745	+2246	
V_{SS2}	32	+745	+2316	
V_{SS2}	33	+745	+2386	
V_{SS2}	34	+745	+2456	
V_{SS2}	35	+745	+2666	
$V_{LCDSENSE}$	36	+745	+2736	input for voltage multiplier regulation
V_{LCDOUT}	37	+745	+2806	V_{LCD} output
V_{LCDOUT}	38	+745	+2876	
V_{LCDOUT}	39	+745	+2946	
V_{LCDOUT}	40	+745	+3016	

Table 45. Pin location *…continued*

All X and Y coordinates are referenced to the center of the chip (dimensions in μm).

Symbol	Pin	X	Y	Description
V_{LCDOUT}	41	+745	+3086	V_{LCD} output
V_{LCDOUT}	42	+745	+3156	
V_{LCDOUT}	43	+745	+3226	
V_{LCDIN}	44	+745	+3296	input for generation of LCD bias levels
V_{LCDIN}	45	+745	+3366	
V_{LCDIN}	46	+745	+3436	
V_{LCDIN}	47	+745	+3506	
V_{LCDIN}	48	+745	+3576	
V_{LCDIN}	49	+745	+3646	
dummy (V_{SS1})	50	−745	+3576	dummy
R8	51	−745	+3506	LCD row driver output
R7	52	−745	+3436	
R6	53	−745	+3366	
R5	54	−745	+3296	
R4	55	−745	+3226	
R3	56	−745	+3156	
R2	57	−745	+3086	
R1	58	−745	+3016	
R17	59	−745	+2946	
C80	60	−745	+2876	LCD column driver output
C79	61	−745	+2806	
C78	62	−745	+2736	
C77	63	−745	+2666	
C76	64	−745	+2596	
C75	65	−745	+2526	
C74	66	−745	+2456	
C73	67	−745	+2386	
C72	68	−745	+2316	
C71	69	−745	+2246	
C70	70	−745	+2176	
C69	71	−745	+2106	
C68	72	−745	+2036	
C67	73	−745	+1966	
C66	74	−745	+1896	
C65	75	−745	+1756	
C64	76	−745	+1686	
C63	77	−745	+1616	
C62	78	−745	+1546	
C61	79	−745	+1476	
C60	80	−745	+1406	

Table 45. Pin location *…continued*

All X and Y coordinates are referenced to the center of the chip (dimensions in μm).

Symbol	Pin	X	Y	Description
C59	81	–745	+1336	LCD column driver output
C58	82	–745	+1266	
C57	83	–745	+1196	
C56	84	–745	+1126	
C55	85	–745	+1056	
C54	86	–745	+986	
C53	87	–745	+916	
C52	88	–745	+846	
C51	89	–745	+776	
C50	90	–745	+706	
C49	91	–745	+636	
C48	92	–745	+566	
C47	93	–745	+496	
C46	94	–745	+426	
C45	95	–745	+356	
C44	96	–745	+286	
C43	97	–745	+216	
C42	98	–745	+146	
C41	99	–745	+76	
R17DUP	100	–745	+6	LCD row driver output
C40	101	–745	–64	LCD column driver output
C39	102	–745	–134	
C38	103	–745	–204	
C37	104	–745	–274	
C36	105	–745	–344	
C35	106	–745	–414	
C34	107	–745	–484	
C33	108	–745	–554	
C32	109	–745	–624	
C31	110	–745	–694	
C30	111	–745	–764	
C29	112	–745	–834	
C28	113	–745	–904	
C27	114	–745	–974	
C26	115	–745	–1044	
C25	116	–745	–1114	
C24	117	–745	–1184	
C23	118	–745	–1254	
C22	119	–745	–1324	
C21	120	–745	–1394	

Table 45. Pin location *…continued*

All X and Y coordinates are referenced to the center of the chip (dimensions in μm).

Symbol	Pin	X	Y	Description
C20	121	–745	–1464	LCD column driver output
C19	122	–745	–1534	
C18	123	–745	–1604	
C17	124	–745	–1674	
C16	125	–745	–1744	
C15	126	–745	–1884	
C14	127	–745	–1954	
C13	128	–745	–2024	
C12	129	–745	–2094	
C11	130	–745	–2164	
C10	131	–745	–2234	
C9	132	–745	–2304	
C8	133	–745	–2374	
C7	134	–745	–2444	
C6	135	–745	–2514	
C5	136	–745	–2584	
C4	137	–745	–2654	
C3	138	–745	–2724	
C2	139	–745	–2794	
C1	140	–745	–2864	
R18	141	–745	–2934	LCD row driver output
R9	142	–745	–3004	
R10	143	–745	–3074	
R11	144	–745	–3144	
R12	145	–745	–3214	
R13	146	–745	–3284	
R14	147	–745	–3354	
R15	148	–745	–3424	
R16	149	–745	–3494	
dummy (V_{SS1})	150	–745	–3704	dummy
SCL	151	+745	–3704	I²C-bus serial clock input
SCL	152	+745	–3634	
T3	153	+745	–3494	test pin 3
POR	154	+745	–3424	external Power-On Reset (POR) input
PD	155	+745	–3214	power-down mode select input
SDA	156	+745	–3004	I²C-bus serial data input/output
SDA	157	+745	–2934	
R/$\overline{W}$	158	+745	–2584	read/write input
RS	159	+745	–2374	register select input
DB0	160	+745	–2164	8-bit bidirectional data bus; bit 0

Table 45. Pin location *…continued*

All X and Y coordinates are referenced to the center of the chip (dimensions in μm).

Symbol	Pin	X	Y	Description
DB1	161	+745	−1954	8-bit bidirectional data bus; bit 1
DB2	162	+745	−1744	8-bit bidirectional data bus; bit 2
DB3/SA0	163	+745	−1534	8-bit bidirectional data bus; bit 3
DB4	164	+745	−1324	8-bit bidirectional data bus; bit 4
DB5	165	+745	−1114	8-bit bidirectional data bus; bit 5
DB6	166	+745	−904	8-bit bidirectional data bus; bit 6
DB7	167	+745	−694	8-bit bidirectional data bus; bit 7
OSC	168	+745	−484	oscillator or external clock input

Table 46. Alignment mark location

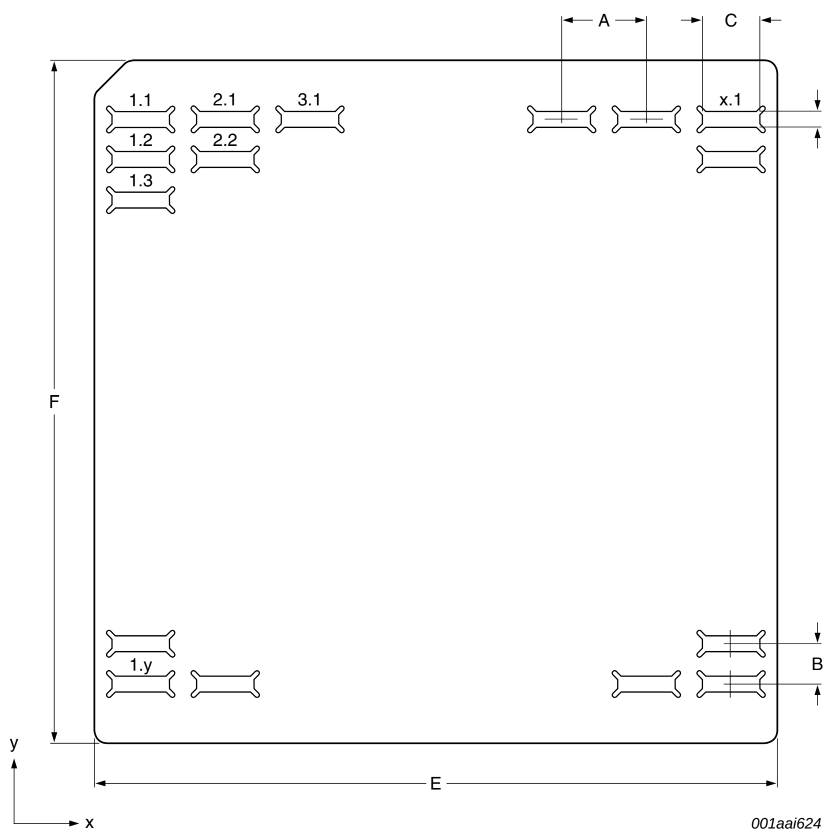
All X and Y coordinates are referenced to the center of the chip (dimensions in μm).

Symbol	Pin	X	Y
AM1	-	+745	−2689
AM2	-	+745	+2561
AM3	-	−745	+3681
AM4	-	−745	−3599

18. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

19. Packing information

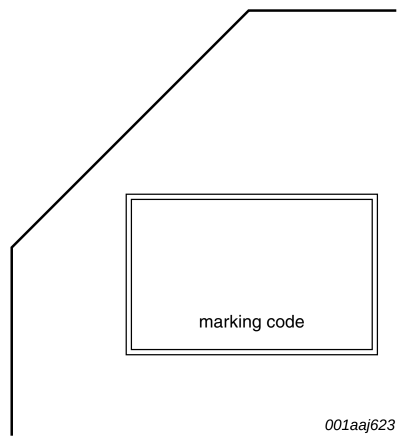


For dimensions see Table 47.

Fig 51. Tray details

Table 47. Tray dimensions

Dimension	Description	Value
A	pocket pitch x direction	10.16 mm
B	pocket pitch y direction	4.45 mm
C	pocket width x direction	7.74 mm
D	pocket width y direction	1.91 mm
E	tray width x direction	50.8 mm
F	tray width y direction	50.8 mm
x	pockets in x direction	4
y	pockets in y direction	10



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pin location diagram for the orientating and position of the type name on the die surface.

Fig 52. Tray alignment

20. Abbreviations

Table 48. Abbreviations

Acronym	Description
CGRAM	Character Generator RAM
CGROM	Character Generator ROM
CMOS	Complementary Metal Oxide Semiconductor
COG	Chip-On-Glass
DC	Direct Current
DDRAM	Display Data RAM
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MUX	Multiplexer
PCB	Printed-Circuit Board
POR	Power-On Reset
RAM	Random Access Memory
RMS	Root Mean Square
ROM	Read Only Memory
SCL	Serial Clock Line
SDA	Serial Data Line

21. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10706 —** Handling bare die

[3] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[4] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[5] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[6] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[7] **JESD78 —** IC Latch-Up Test

[8] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[9] **NX3-00092 —** NXP store and transport requirements

[10] **UM10204 —** I^2C-bus specification and user manual

22. Revision history

Table 49. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF2119X v.7	20101115	Product data sheet	-	PCF2119X v.6
Modifications:	• Removed product type PCF2119VU/2/F2			
PCF2119X v.6	20100908	Product data sheet	-	PCF2119X_5
PCF2119X_5	20090813	Product data sheet	-	PCF2119X_4
PCF2119X_4	20030130	Product specification	-	PCF2119X_3
PCF2119X_3	20020116	Product specification	-	PCF2119X_2
PCF2119X_2	19990302	Product specification	-	PCF2119X_1
PCF2119X_1	19971121	Objective specification	-	-

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Bare die — All die are tested on compliance with their related technical specifications as stated in this data sheet up to the point of wafer sawing and are handled in accordance with the NXP Semiconductors storage and transportation conditions. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post-packing tests performed on individual die or wafers.

NXP Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, NXP Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

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23.4 Trademarks

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I^{2}C-bus — logo is a trademark of NXP B.V.

24. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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