

# DATA SHEET

## **PCF84C00** 8-bit microcontroller with I<sup>2</sup>C-bus interface

Product specification  
Supersedes data of May 1996  
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1996 Nov 25

# 8-bit microcontroller with I<sup>2</sup>C-bus interface

## PCF84C00

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## PCF84C00

**1 FEATURES**

- Manufactured in silicon gate CMOS process
- 8-bit CPU, RAM, I/O in a single 28-lead or 56-lead package
- ‘Piggy-back’ and ROM-less versions, external program memory
- 256 × 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs, one of which is also the external interrupt input
- Three single-level vectored interrupts:
  - external
  - timer/event counter
  - I<sup>2</sup>C-bus
- I<sup>2</sup>C-bus interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2.5 to 5.5 V)
- Stop and Idle modes
- Power-on reset circuit
- Operating temperature range: –40 to +85 °C.

**3 ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF84C00B	–	Non-standard 28-lead ‘piggy-back’ package with 28-pin EPROM socket on top. Bottom ‘footprint’ and pinning as DIP 28, version SOT117-1. The SOT117-1 information provided in Chapter “Package Outlines” is correct in these respects, but <b>not</b> for the physical size of the PCF84C00B, which is larger than the SOT117-1 package.	–
PCF84C00T	VSO56	Plastic very small outline package; 56 leads.	SOT 190-1

**2 GENERAL DESCRIPTION**

This data sheet details the specific properties of the PCF84C00. The shared properties of the PCF84CxxxA family of microcontrollers are described in the “PCF84CxxxA family” data sheet, which should be read in conjunction with this publication.

The PCF84C00 has 20 quasi-bidirectional I/O lines, an I<sup>2</sup>C-bus serial interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits.

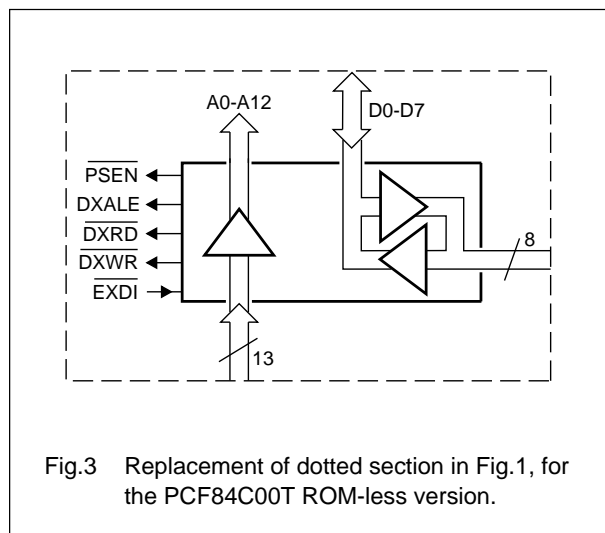
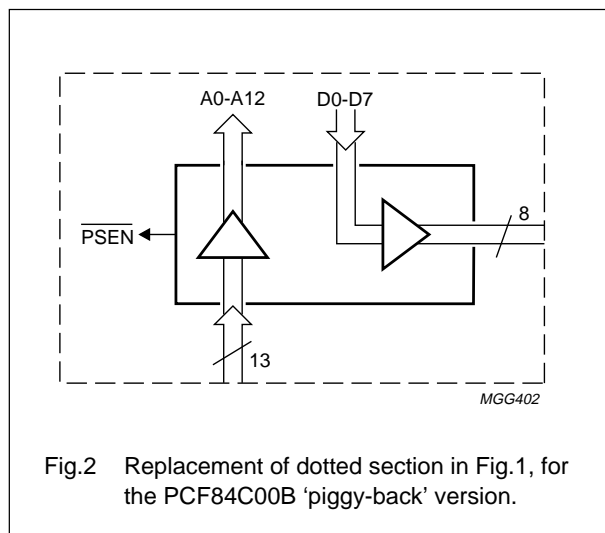
This efficient controller also performs well as an arithmetic processor. It has facilities for both binary and BCD arithmetic plus bit-handling capabilities.

The instruction set is similar to the MAB8048 and is a sub-set of that listed in the “PCF84CxxxA family” data sheet.



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## 5 PINNING

Table 1 PCF84C00B (see Fig.4)

SYMBOL	PIN	TYPE	DESCRIPTION
P2.2	1	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
SDA/P2.3	2	I/O	bidirectional data line of the I <sup>2</sup> C-bus interface; or 1 bit of Port 2: 4-bit quasi-bidirectional I/O line
SCLK	3	I/O	bidirectional clock line of the I <sup>2</sup> C-bus interface
P0.0 to P0.7	4 to 11	I/O	8 bits of Port 0: 8-bit quasi-bidirectional I/O port
INT/T0	12	I	Interrupt/Test 0: external interrupt input (negative edge triggered)/test input pin. When used as a test input, this pin is directly tested by conditional branch instructions JT0 and JNT0.
T1	13	I	Test 1: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 may also be selected as an input to the 8-bit timer/event counter via the STRT CNT instruction.
V <sub>SS</sub>	14	P	ground: circuit earth potential
XTAL1	15	I	oscillator input: input from a crystal which determines the internal oscillator frequency or an external clock generator
XTAL2	16	I/O	oscillator output: output of the inverting amplifier
RESET	17	I/O	reset input: used to initialize the microcontroller (active HIGH); also output of power-on-reset circuit
P1.0 to P1.7	18 to 25	I/O	8 bits of Port 1: 8-bit quasi-bidirectional I/O port
P2.0 to P2.1	26, 27	I/O	2 bits of Port 2: 4-bit quasi-bidirectional I/O port
V <sub>DD</sub>	28	P	power supply: 2.5 V to 5.5 V

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**Table 2** PCF84C00T (see Fig.5)

SYMBOL	PIN	TYPE	DESCRIPTION
P2.2	1	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
SDA/P2.3	2	I/O	bidirectional data line of the I <sup>2</sup> C-bus interface; or 1 bit of Port 2: 4-bit quasi-bidirectional I/O port
SCLK	3	I/O	bidirectional clock line of the I <sup>2</sup> C-bus interface
P0.0 to P0.1	4, 5	I/O	2 bits of Port 0: 8-bit quasi-bidirectional I/O port
DXALE	6	O	Address latch enable: on the falling edge of DXALE, the Dx address can be latched in an external latch. This signal occurs only during execution of the MOV Dx, A, MOV A, Dx, ANL Dx, A and ORL Dx, A instructions, with x = 0 to 255. It is active during TS10 of cycle 1 and the first half of TS1 of cycle 2.
n.c.	7	–	not connected
P0.2 to P0.7	8 to 13	I/O	6 bits of Port 0: 8-bit quasi-bidirectional I/O port
$\overline{\text{INT}}/\text{T0}$	14	I	Interrupt/Test 0: external interrupt input (negative edge triggered)/test input pin. When used as a test input, this pin is directly tested by conditional branch instructions JT0 and JNT0; note 1.
T1	15	I	Test 1: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 may also be selected as an input to the 8-bit timer/event counter via the STRT CNT instruction.
D0 to D2	16 to 18	I/O	3 bits of 8-bit data bus: for external memory and peripherals. The specified Stop mode supply current is valid only if external pull-ups are connected to all data lines.
A12	19	O	1 bit of 13-bit address bus: for external memory and peripherals
$\overline{\text{DXWR}}$	20	O	Write strobe (active LOW): on the rising edge, data on D0-D7 may be written to external registers. This signal occurs only during MOV Dx, A, ANL Dx, A and ORL Dx, A instructions, with x = 0 to 255. It is active during TS7 of cycle 2.
n.c.	21	–	not connected
A11 to A6	22 to 27	O	6 bits of 13-bit address bus: for external memory and peripherals
V <sub>SS</sub>	28	P	ground: circuit earth potential
A5 to A0	29 to 34	O	6 bits of 13-bit address bus: for external memory and peripherals
$\overline{\text{DXRD}}$	35	O	Read strobe (active LOW): when this signal is active, external registers emulating Dx registers can be read by the data bus. This signal occurs only during execution of MOV A, Dx, ANL Dx, A and ORL Dx, A instructions, with x = 0 to 255. It is active during TS3 and TS4 of cycle 2.
D3 to D7	36 to 40	I/O	5 bits of 8-bit data bus: for external memory and peripherals. The specified Stop mode supply current is valid only if external pull-ups are connected to all data lines.
$\overline{\text{PSEN}}$	41	O	Program store enable (active LOW): $\overline{\text{PSEN}}$ is used to enable external program memory and is active during TS9 and TS10 of each machine cycle and TS1 of each following cycle. $\overline{\text{PSEN}}$ is HIGH during the Stop mode.
XTAL1	42	I	oscillator input: input from a crystal which determines the internal oscillator frequency or an external clock generator
XTAL2	43	I/O	oscillator output: output of the inverting amplifier

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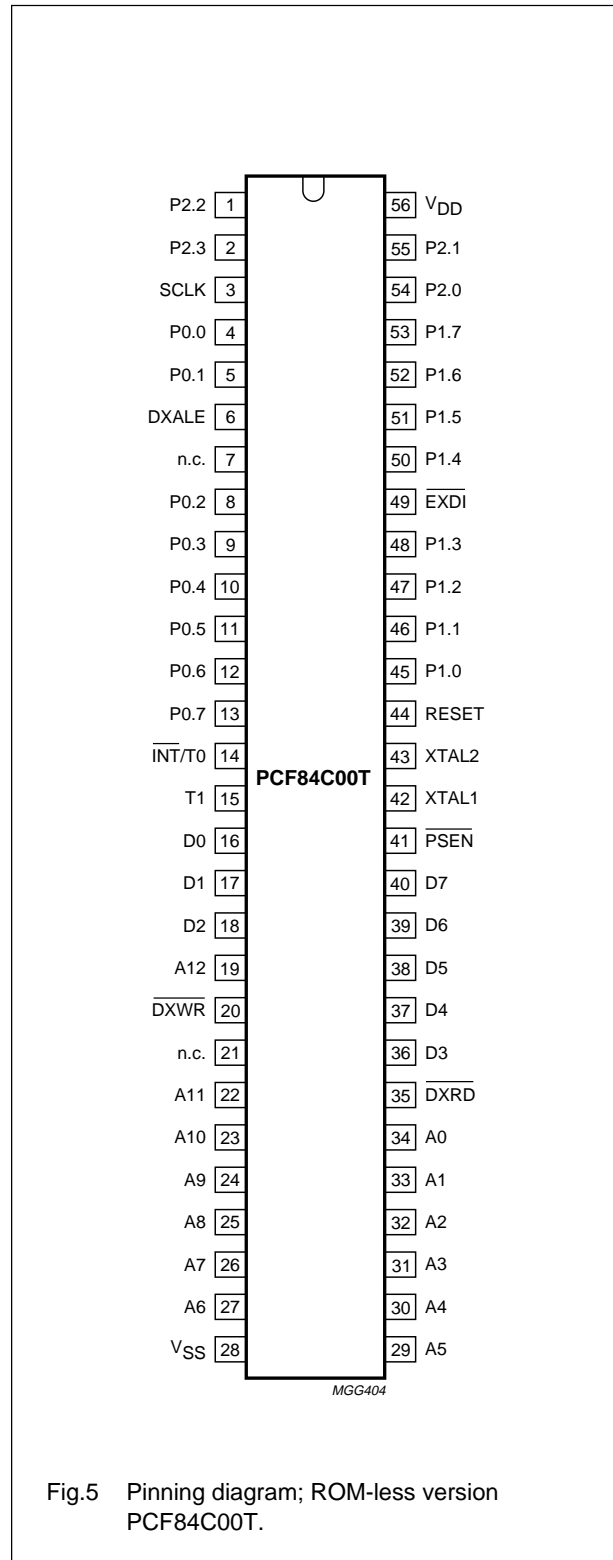
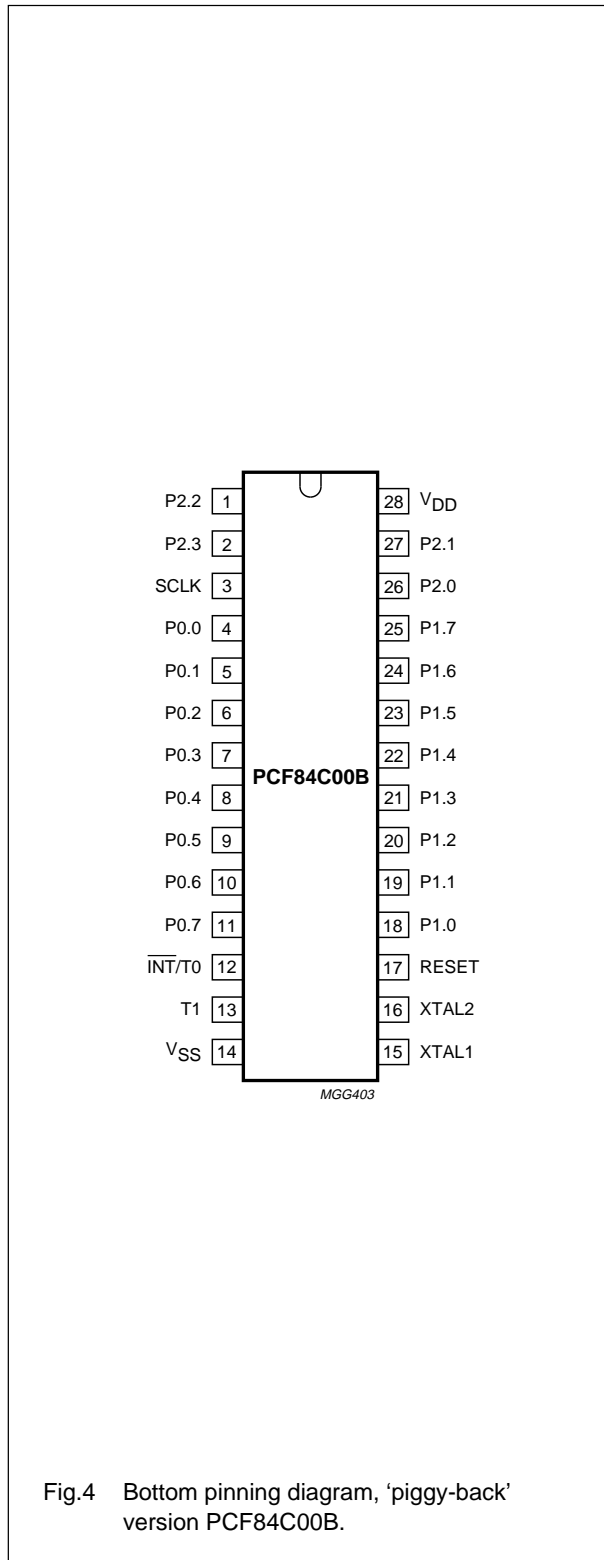
SYMBOL	PIN	TYPE	DESCRIPTION
RESET	44	I/O	reset input: used to initialize the microcontroller (active HIGH); also output of power-on-reset circuit
P1.0 to P1.3	45 to 48	I/O	4 bits of Port 1: 8-bit quasi-bidirectional I/O port
$\overline{\text{EXDI}}$	49	I	External derivative interrupt (active LOW): $\overline{\text{EXDI}}$ is 'OR-ed' with the internal serial interrupt and can be used to initiate an interrupt from external hardware emulating derivative functions. $\overline{\text{EXDI}}$ is pulled HIGH internally. The derivative interrupt is polled during time slot TS6 (note 1), and is only accepted if an EN SI instruction has been executed and the device is not already executing an interrupt routine. Derivative interrupts are not latched in the PCF84C00.
P1.4 to P1.7	50 to 53	I/O	4 bits of Port 1: 8-bit quasi-bidirectional I/O port
P2.0 to P2.1	54, 55	I/O	2 bits of Port 2: 4-bit quasi-bidirectional I/O port
V <sub>DD</sub>	56	P	power supply: 2.5 V to 5.5 V

**Note**

1. The interrupt signal must remain active until the vector address (05 H) is present on the address bus.

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## PCF84C00

**6 FUNCTIONAL DESCRIPTION****6.1 'Piggy-back' version PCF84C00B**

The PCF84C00B package has standard pinning on the bottom to facilitate insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the height of a standard DIP package. The PCF84C00B can address up to 8 kbytes of external ROM/RAM, and has 256 bytes of internal data RAM.

**6.2 ROM-less version PCF84C00T**

The PCF84C00T microcontroller contains no on-chip ROM, but has all address and data lines brought out to access an external ROM or EPROM. Consequently, this version has more pins (see Fig.5) than the devices in the PCF84Cxxx family with on-chip or 'piggy-back' ROM. The PCF84C00T can address up to 8 kbytes of external program memory, and has 256 bytes of internal data RAM.

**6.3 Data memory**

Data memory consists of 256 bytes of Random-Access Memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer.

**6.4 I/O facilities**

Each device has 23 I/O lines arranged as follows:

- Port 0; 8-bit parallel port (P0.0-P0.7)
- Port 1; 8-bit parallel port (P1.0-P1.7)
- Port 2; 4-bit parallel port (P2.0-P2.3)
- SCLK ; I<sup>2</sup>C-bus (serial I/O) clock line

- $\overline{\text{INT}}/\text{T0}$ ; External interrupt and test input. When used as a test input, it can be directly tested by conditional branch instructions JT0 and JNT0.
- T1; Test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

**6.5 Reset**

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and I<sup>2</sup>C-bus)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to divide by 32
- Resets the timer flag
- Sets all ports except P2.3 to input mode
- Sets the I<sup>2</sup>C-bus interface to slave receiver mode and disables the I<sup>2</sup>C-bus interface
- Cancels Idle and Stop mode.

A negative-going signal on the RESET input/output:

- Sets P2.3/SDA and SCLK to HIGH after a maximum of 30 clock pulses
- Sets the I<sup>2</sup>C-bus interface to slave receiver mode and disables the I<sup>2</sup>C-bus interface after a maximum of 30 clock pulses
- Starts program execution after 1866 clock pulses.

**7 LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DD</sub>	supply voltage		-0.8	+8	V
V <sub>I</sub>	all input voltages		-0.5	V <sub>DD</sub> +0.5	V
I <sub>I</sub>	DC input current		-10	+10	mA
I <sub>O</sub>	DC output current		-10	+10	mA
P <sub>tot</sub>	total power dissipation		-	125	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C

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SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T <sub>amb</sub>	operating ambient temperature range	P <sub>tot(max)</sub> = 100 mW	-40	+70	°C
		P <sub>tot(max)</sub> = 30 mW	-40	+85	°C
T <sub>j</sub>	operating junction temperature		-	90	°C

## 8 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices. See "Data Handbook IC14 Section: Handling MOS devices".

## 9 DC CHARACTERISTICS

V<sub>DD</sub> = 2.5 to 5.5 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 to +85 °C; all voltages with respect to V<sub>SS</sub>; unless otherwise specified.

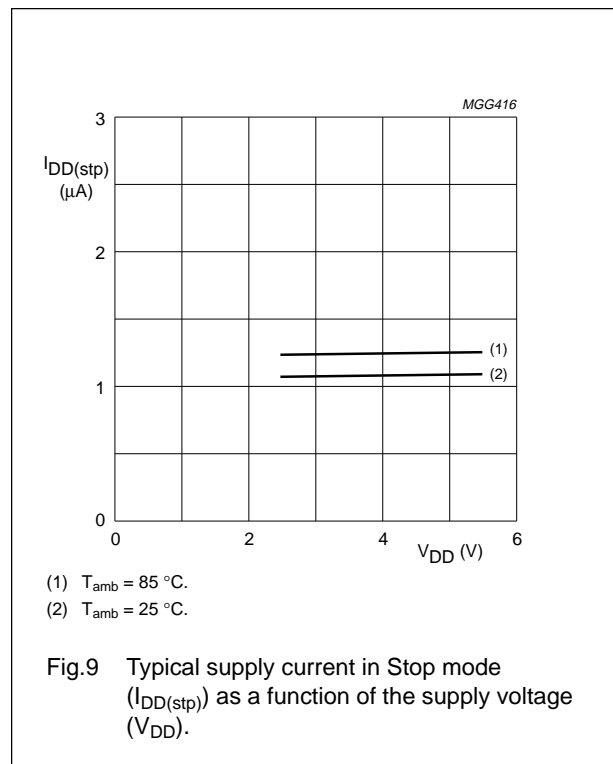
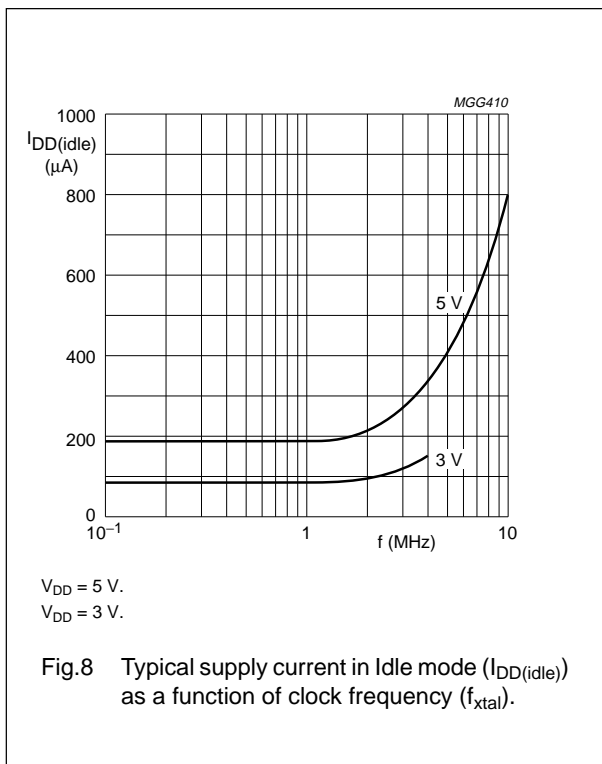
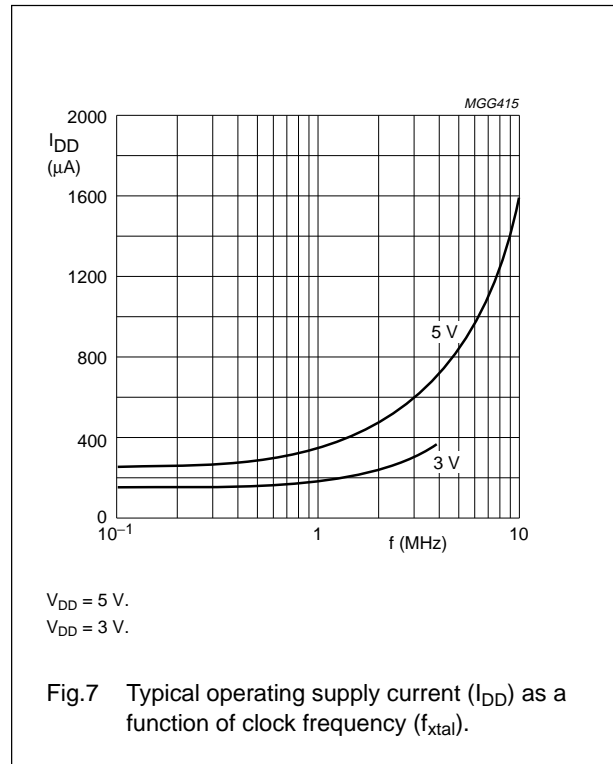
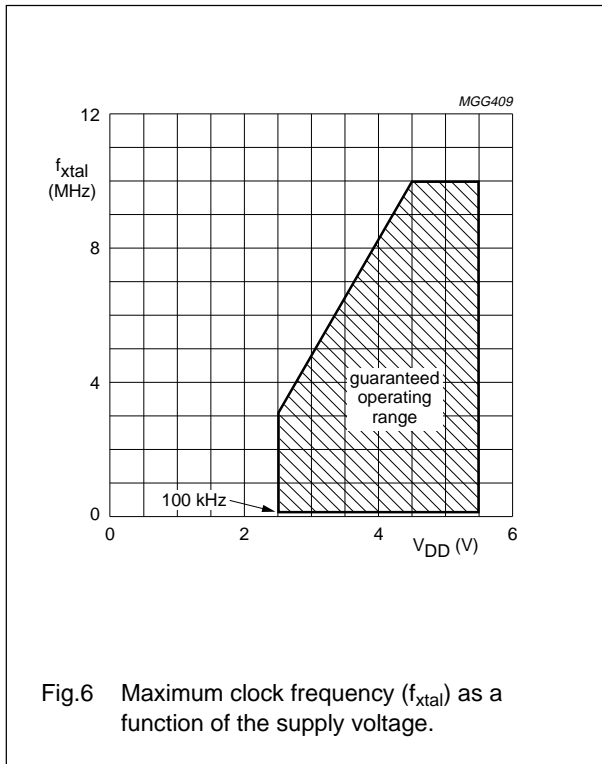
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	operating supply voltage	see Fig.6	2.5	-	5.5	V
I <sub>DD</sub>	operating supply current	note 1; see Fig.7 V <sub>DD</sub> = 5 V; f <sub>xtal</sub> = 10 MHz	-	1.6	3.2	mA
		V <sub>DD</sub> = 5 V; f <sub>xtal</sub> = 6 MHz	-	1	2	mA
		V <sub>DD</sub> = 3 V; f <sub>xtal</sub> = 3.58 MHz	-	0.3	0.6	mA
I <sub>DD(idle)</sub>	supply current (Idle mode)	note 1; see Fig.8 V <sub>DD</sub> = 5 V; f <sub>xtal</sub> = 10 MHz	-	0.8	1.6	mA
		V <sub>DD</sub> = 5 V; f <sub>xtal</sub> = 6 MHz	-	0.5	1	mA
		V <sub>DD</sub> = 3 V; f <sub>xtal</sub> = 3.58 MHz	-	0.15	0.4	mA
I <sub>DD(stp)</sub>	supply current (Stop mode)	notes 1 and 2; see Fig.9 V <sub>DD</sub> = 2.5 V; T <sub>amb</sub> = 25 °C	-	1.2	2.5	μA
		V <sub>DD</sub> = 2.5 V; T <sub>amb</sub> = 85 °C	-	-	10	μA
<b>Inputs</b>						
V <sub>IL</sub>	LOW level input voltage		0	-	0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH level input voltage		0.7V <sub>DD</sub>	-	V <sub>DD</sub>	V
I <sub>LI</sub>	input leakage current	V <sub>SS</sub> < V <sub>I</sub> < V <sub>DD</sub>	-1	-	+1	μA
<b>Outputs</b>						
I <sub>OL</sub>	LOW level output sink current	V <sub>DD</sub> = 5 V ±10%; V <sub>O</sub> = 0.4 V (except P2.3/SDA, SCLK and Port 1); see Fig.10	1.6	3	-	mA
		P2.3/SDA, SCLK; see Figs 11 and 12	3	-	-	mA
I <sub>OH</sub>	HIGH level pull-up output source current	V <sub>DD</sub> = 5 V ±10%; V <sub>O</sub> = 0.7V <sub>DD</sub>	-40	-	-	μA
		V <sub>DD</sub> = 5 V ±10%; V <sub>O</sub> = V <sub>ss</sub>	-	-	-400	μA
I <sub>OH</sub>	HIGH level push-pull output source current	V <sub>DD</sub> = 5 V ±10%; V <sub>O</sub> = V <sub>DD</sub> - 0.4 V; see Fig.13	-1.6	-3	-	mA

### Notes

- V<sub>IL</sub> = V<sub>SS</sub>; V<sub>IH</sub> = V<sub>DD</sub>; open drain outputs connected to V<sub>SS</sub>; all other outputs, including XTAL2, open (typical values at 25 °C with crystal connected between XTAL1 and XTAL2).
- V<sub>IL</sub> = V<sub>SS</sub>; V<sub>IH</sub> = V<sub>DD</sub>; RESET and T1 at V<sub>SS</sub>; INT/T0 at V<sub>DD</sub>; crystal connected between XTAL1 and XTAL2; open drain outputs connected to V<sub>SS</sub>; all other outputs open.

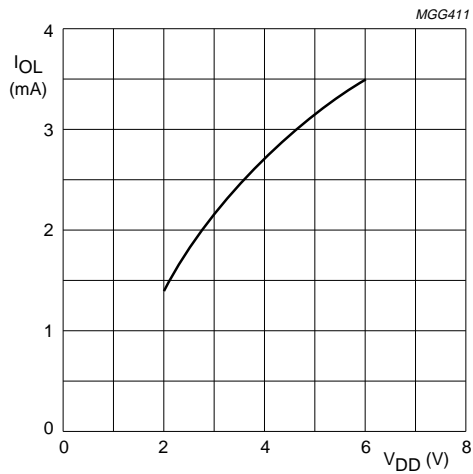
8-bit microcontroller with I<sup>2</sup>C-bus interface

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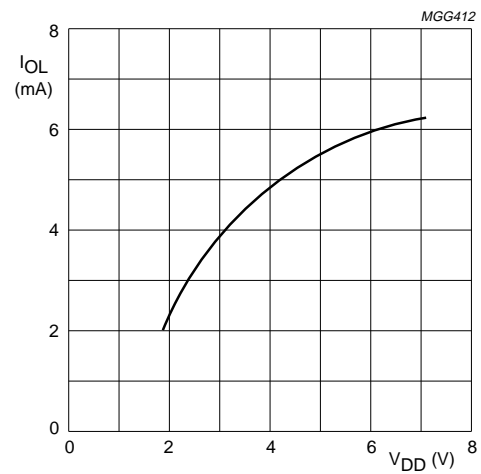
8-bit microcontroller with I<sup>2</sup>C-bus interface

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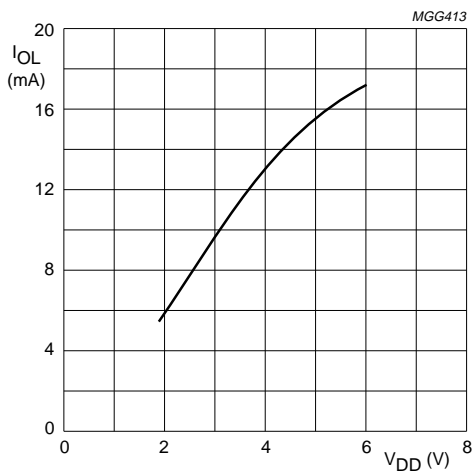
V<sub>O</sub> = 0.4 V.

Fig. 10 Typical output sink current (I<sub>OL</sub>), outputs P0.0 to P0.7 and P2.0 to P2.2, as a function of the supply voltage (V<sub>DD</sub>).



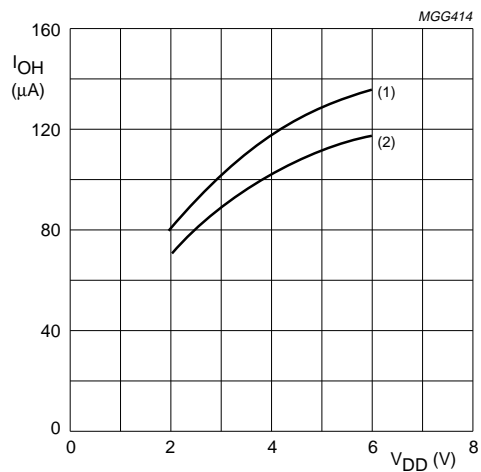
V<sub>O</sub> = 0.4 V.

Fig. 11 Typical output sink current (I<sub>OL</sub>), outputs P2.3/SDA and SCLK, as a function of the supply voltage (V<sub>DD</sub>).



V<sub>O</sub> = 1.2 V.

Fig. 12 Typical output sink current (I<sub>OL</sub>), outputs P1.0 to P1.7, as a function of the supply voltage (V<sub>DD</sub>).



(1) V<sub>O</sub> = V<sub>SS</sub>.  
(2) V<sub>O</sub> = 0.7V<sub>DD</sub>.

Fig. 13 Typical push-pull output source current (I<sub>OH</sub>) as a function of the supply voltage (V<sub>DD</sub>).

8-bit microcontroller with I<sup>2</sup>C-bus interface

## PCF84C00

**10 AC CHARACTERISTICS**

$V_{DD} = 2.5$  to  $5.5$  V;  $V_{SS} = 0$  V;  $T_{amb} = -40$  to  $+85$  °C; all voltages with respect to  $V_{SS}$ ; unless otherwise specified.

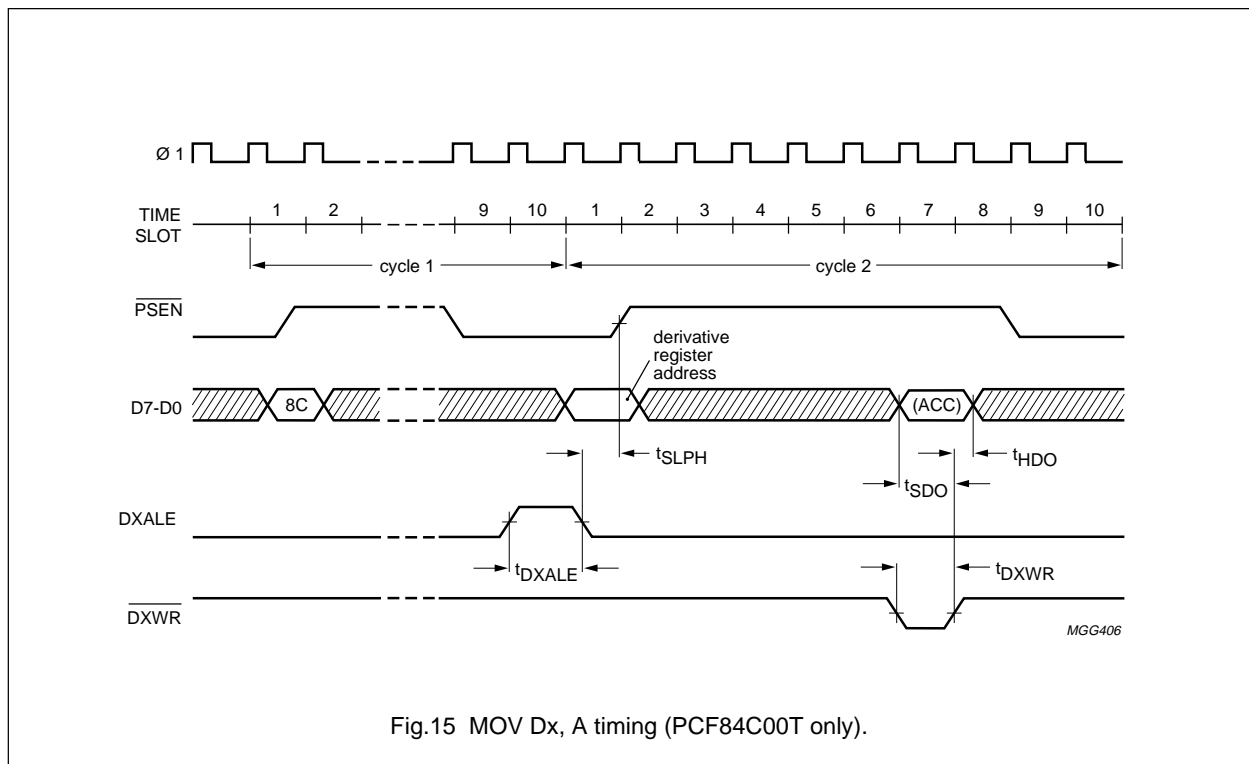
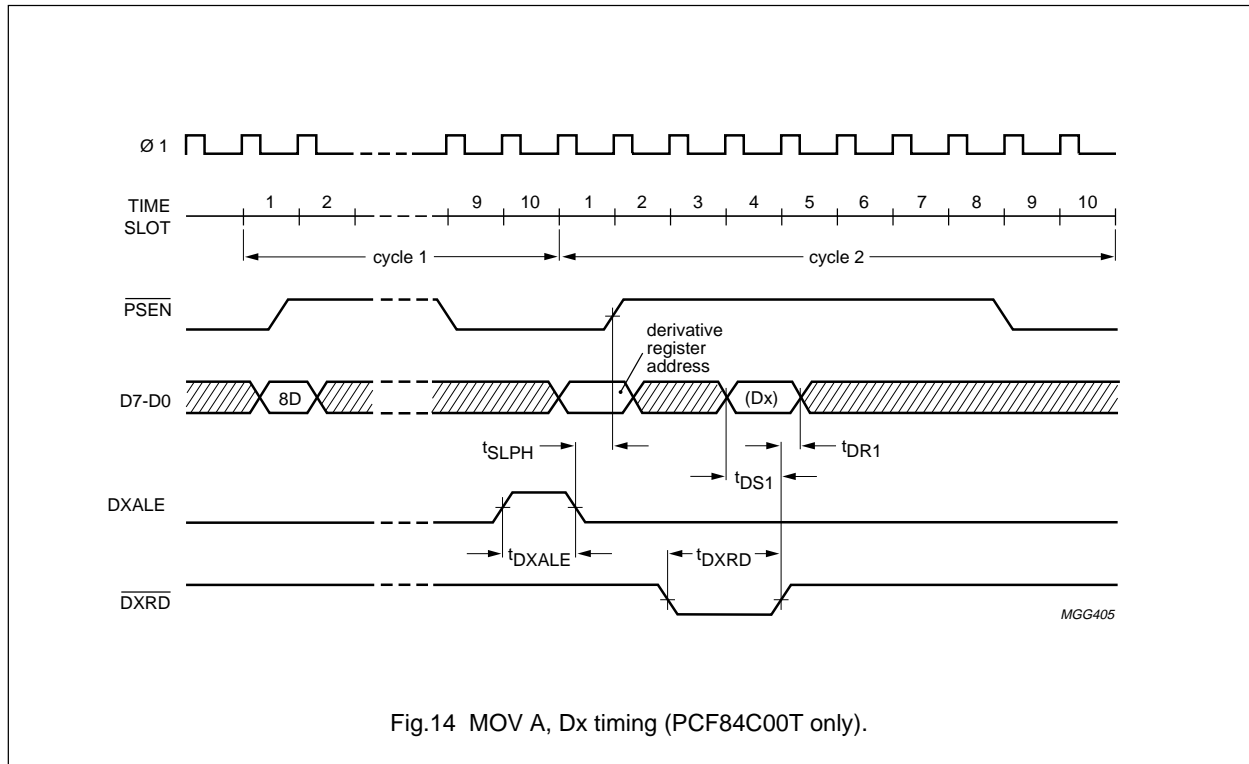
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP. <sup>(2)</sup>	MAX.	UNIT
$t_r$	rise time all outputs	note 1	–	30	–	ns
$t_f$	fall time all outputs	note 1	–	30	–	ns
$T_{cy}$	cycle time	30CP; note 2	3	–	30	μs
<b>PCF84C00/non-standard pins:</b>						
$t_{CC}$	control pulse width	Fig.16	–	9CP	–	μs
$t_{AS}$	address to $\overline{PSEN}$ set-up	Fig.16	–	1.5CP	–	μs
$t_{DS}$	data to $\overline{PSEN}$ set-up	Fig.16	–	2CP	–	μs
$t_{DR}$	data hold time	Fig.16	0	–	–	ns
$t_{SDO}$	data out to $\overline{DWXR}$ set-up	Fig.17	–	2CP	–	μs
$t_{HDO}$	data out to $\overline{DXWR}$ hold	Fig.17	–	1CP	–	μs
$t_{SLPH}$	time from $\overline{DXALE}$ to $\overline{PSEN}$	Figs 14, 15 and 17	–	1.5CP	–	μs
$t_{DS1}$	data-in to $\overline{DXRD}$ set-up	Figs 14, 15 and 17	–	2.5CP	–	μs
$t_{DR1}$	data-in to $\overline{DXRD}$ hold	Figs 14 and 17	0	–	–	ns
$t_{DXALE}$	HIGH time of $\overline{DXALE}$	Figs 14, 15 and 17	–	4.5CP	–	μs
$t_{DXRD}$	LOW time of $\overline{DXRD}$	Figs 14 and 17	–	6CP	–	μs
$t_{DXWR}$	LOW time of $\overline{DXWR}$	Figs 15 and 17	–	3CP	–	μs

**Notes**

- At  $V_{DD} = 5$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF.
- 1 time slot (TS) = 3CP, 1 clock pulse (CP) =  $1/f_{xtal}$ .

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PCF84C00

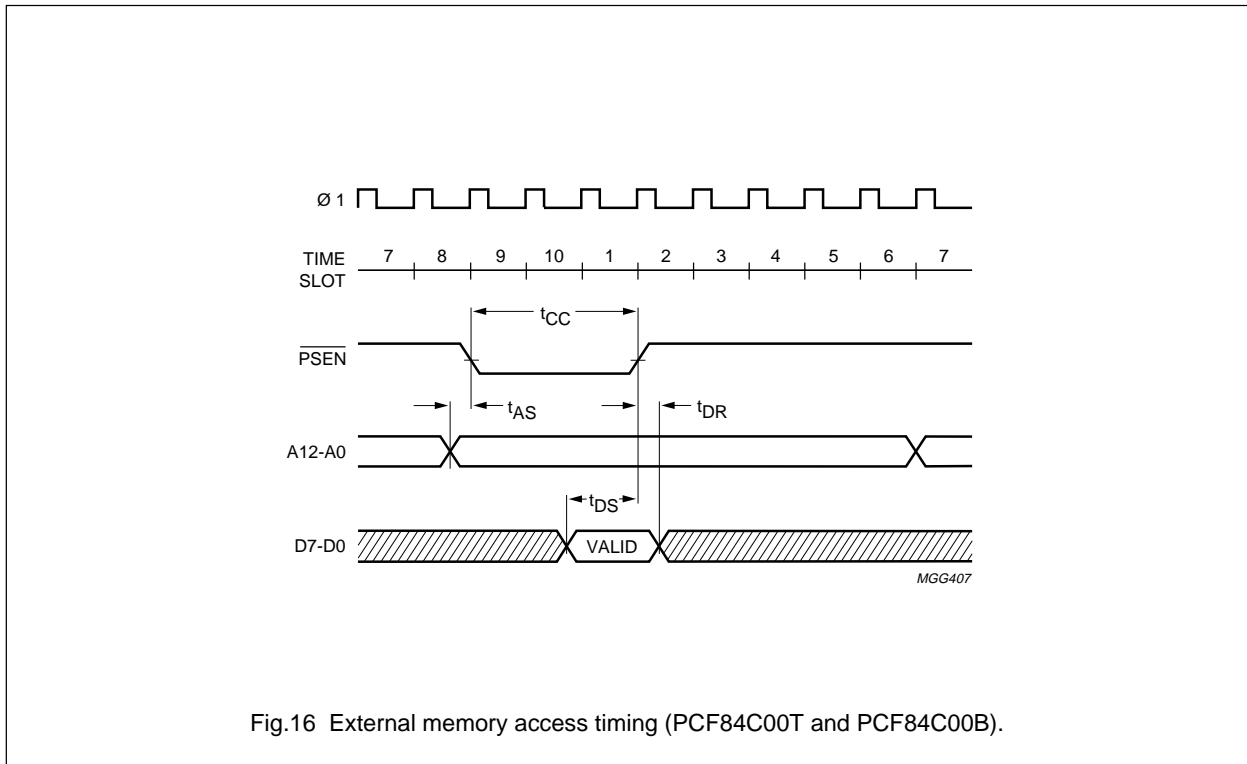


Fig.16 External memory access timing (PCF84C00T and PCF84C00B).

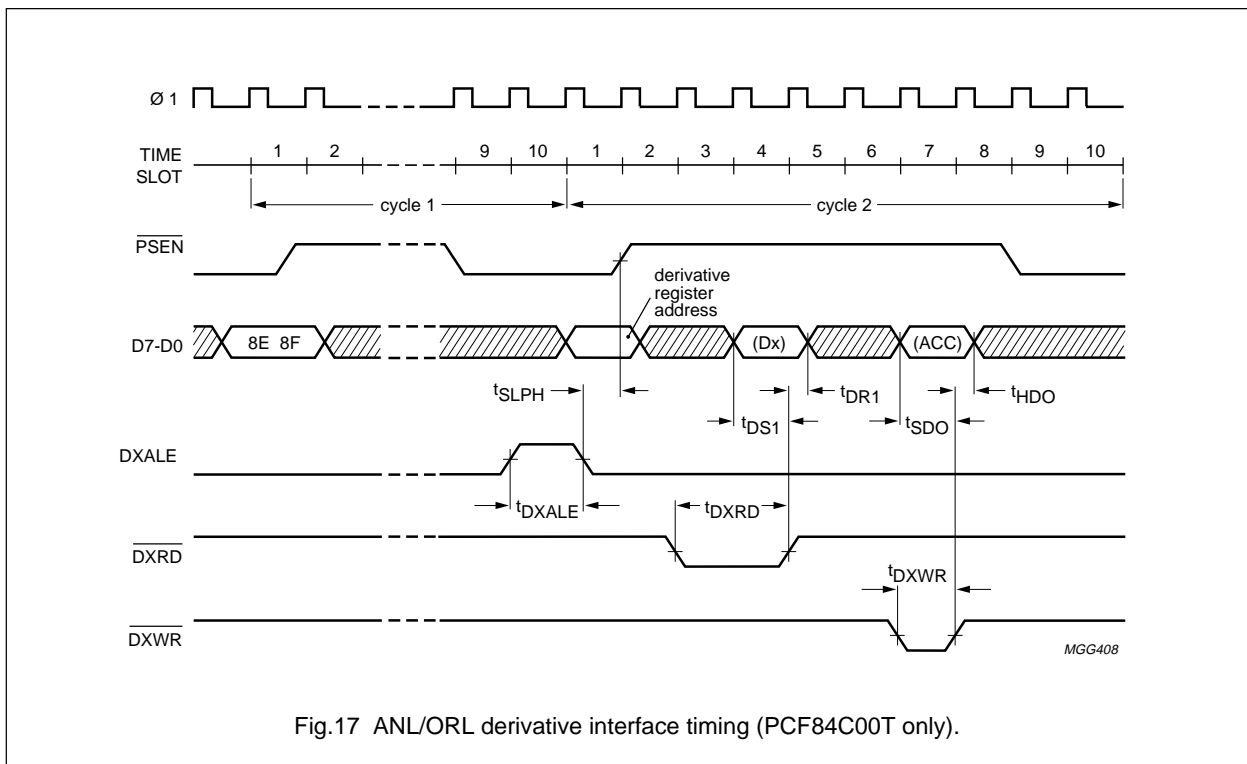


Fig.17 ANL/ORL derivative interface timing (PCF84C00T only).

8-bit microcontroller with I<sup>2</sup>C-bus interface

## PCF84C00

**Table 3** I<sup>2</sup>C-bus timing

SYMBOL	PARAMETER	INPUT (see Fig.18)	OUTPUT (see Fig.19; note 1)
<b>SCLK</b>			
t <sub>HD,STA</sub>	START condition hold time	$\geq \frac{14}{f_{xtal}}$	$\frac{DF + 9}{2 \times f_{xtal}}$
t <sub>LOW</sub>	SCLK LOW time	$\geq \frac{17}{f_{xtal}}$	$\frac{DF - 3}{2 \times f_{xtal}}$ ; note 2
t <sub>HIGH</sub>	SCLK HIGH time	$\geq \frac{17}{f_{xtal}}$	$\frac{DF + 3}{2 \times f_{xtal}}$ ; note 2
t <sub>RC</sub>	SCLK rise time	≤1 μs	≤1 μs; note 3
t <sub>FC</sub>	SCLK fall time	≤0.3 μs	≤0.1 μs; note 4
<b>SDA</b>			
t <sub>BUF</sub>	bus free time	$\geq \frac{14}{f_{xtal}}$	≥ 4.7 μs; note 5
t <sub>SU,DAT</sub>	data set-up time	≥250 ns	$\geq \frac{15}{f_{xtal}}$ ; note 6
t <sub>HD,DAT</sub>	data hold time	≥ 0	$\geq \frac{9}{f_{xtal}}$
t <sub>RD</sub>	SDA/P2.3 rise time	≤1 μs	≤1 μs; note 3
t <sub>FD</sub>	SDA/P2.3 fall time	≤0.3 μs	≤0.1 μs; note 4
t <sub>SU,STO</sub>	STOP condition set-up time	$\geq \frac{14}{f_{xtal}}$	$\frac{DF - 3}{2 \times f_{xtal}}$

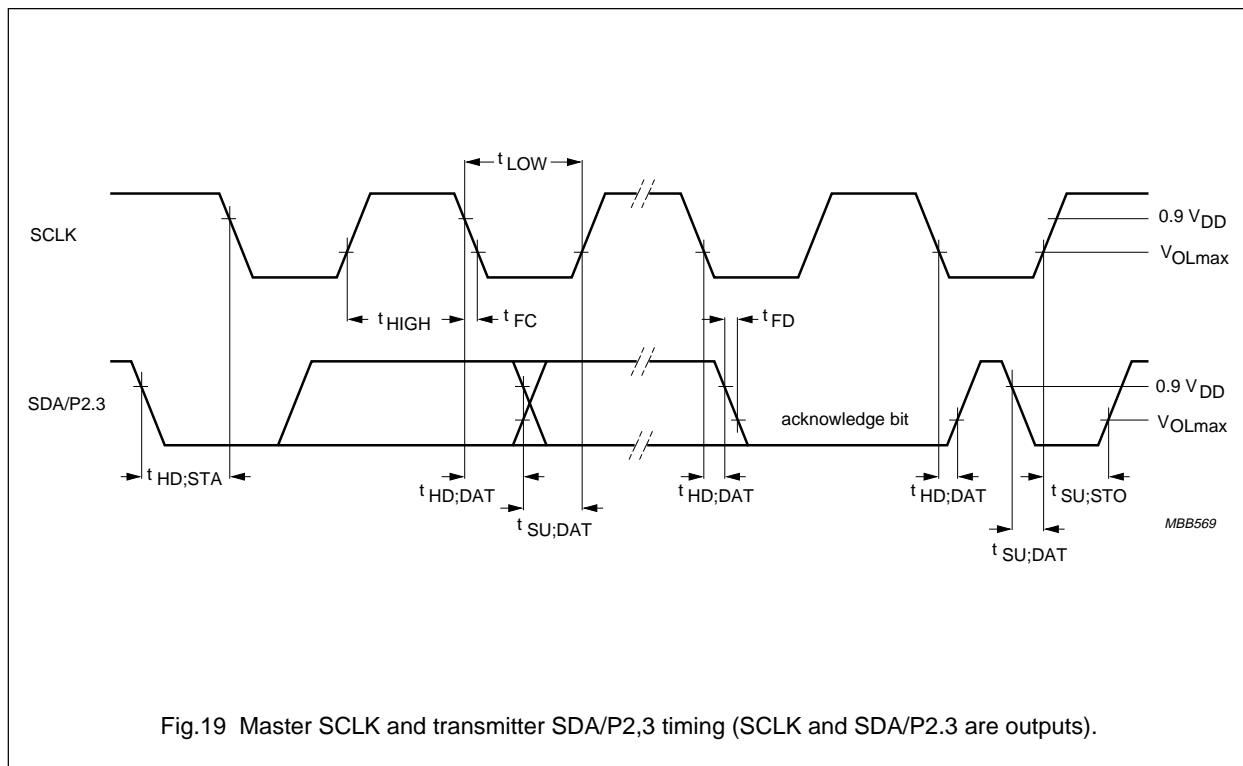
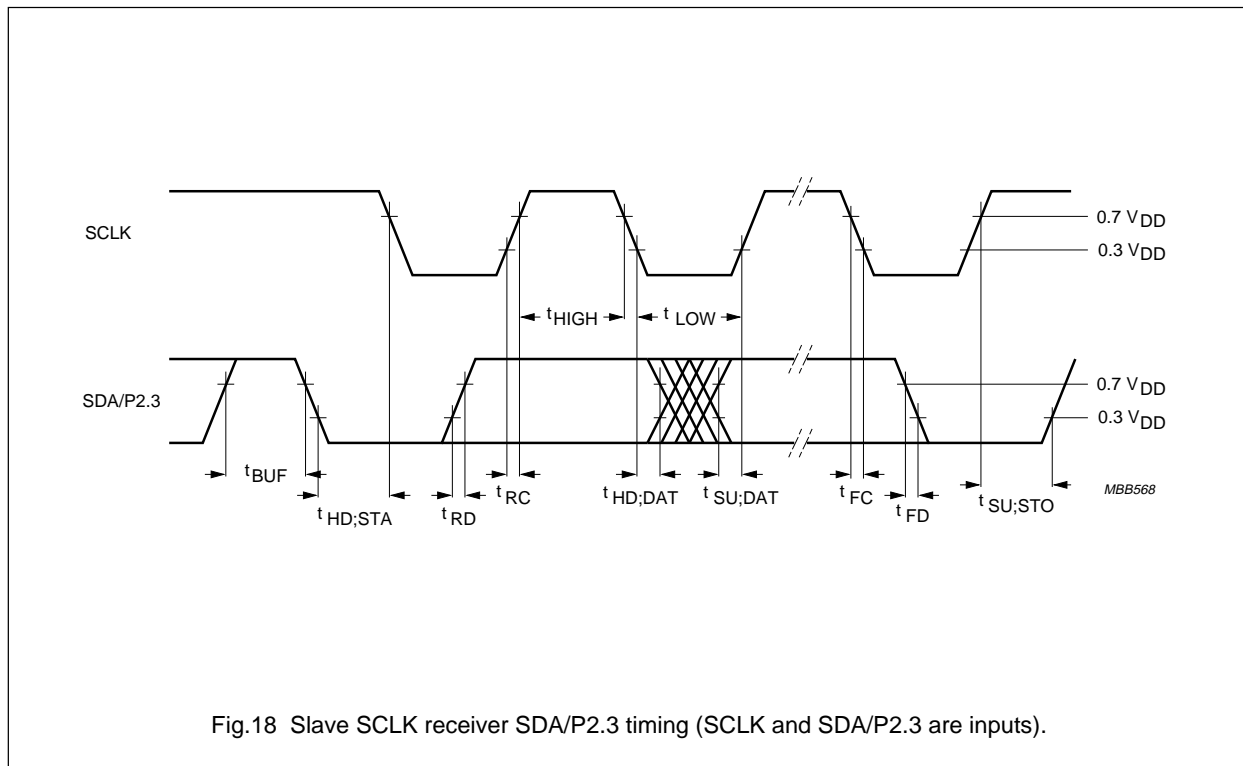
**Notes**

- DF stands for Division Factor: the divisor of f<sub>xtal</sub> (see the "PCF84CxxxA family" data sheet).
- Values given for ASC = 0; for ASC =1: t<sub>HIGH</sub> =  $\frac{3(DF + 1)}{4 \times f_{xtal}}$  ; t<sub>LOW</sub> =  $\frac{DF - 3}{4 \times f_{xtal}}$
- Determined by I<sup>2</sup>C-bus capacitance (C<sub>b</sub>) and external pull-up resistor.
- At maximum allowed I<sup>2</sup>C-bus capacitance C<sub>b</sub> = 400 pF.
- Determined by program.
- If t<sub>LOW</sub> <  $\frac{24}{f_{xtal}}$ , t<sub>SU,DAT</sub> ≥  $\frac{t_{LOW} - 9}{f_{xtal}}$ , independent of ASC.



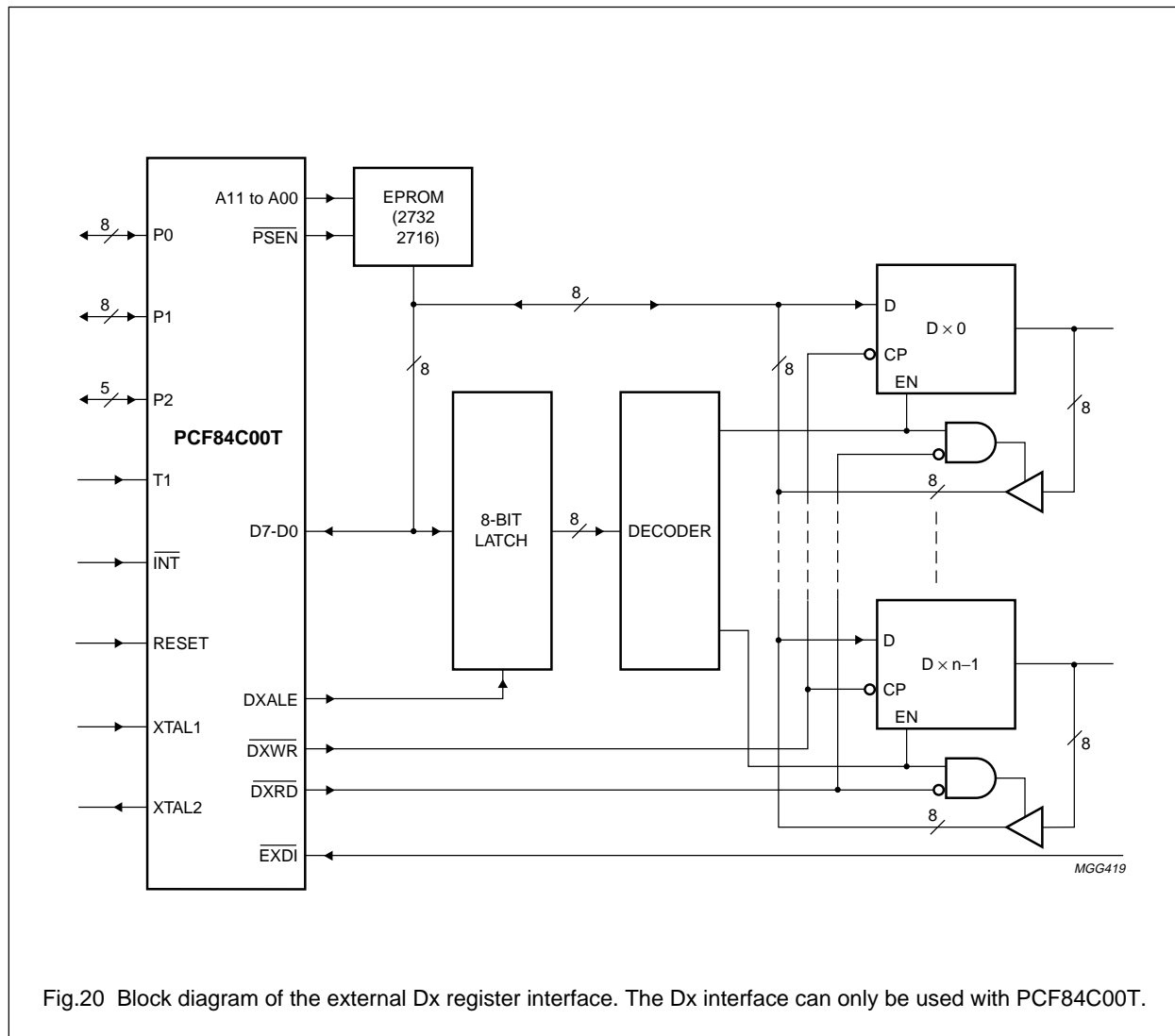
8-bit microcontroller with I<sup>2</sup>C-bus interface

PCF84C00



8-bit microcontroller with I<sup>2</sup>C-bus interface

## PCF84C00



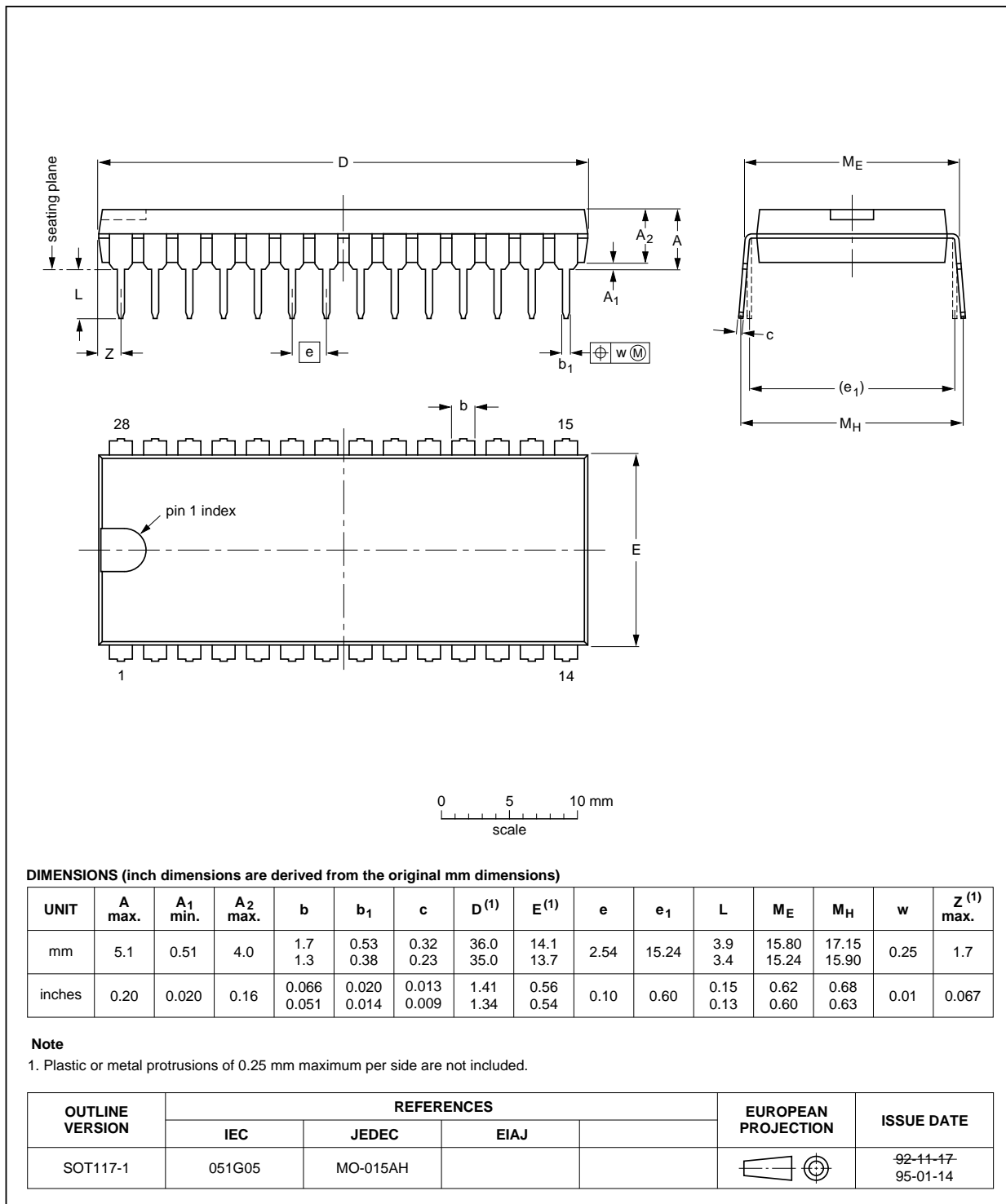
8-bit microcontroller with I<sup>2</sup>C-bus interface

PCF84C00

11 PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1

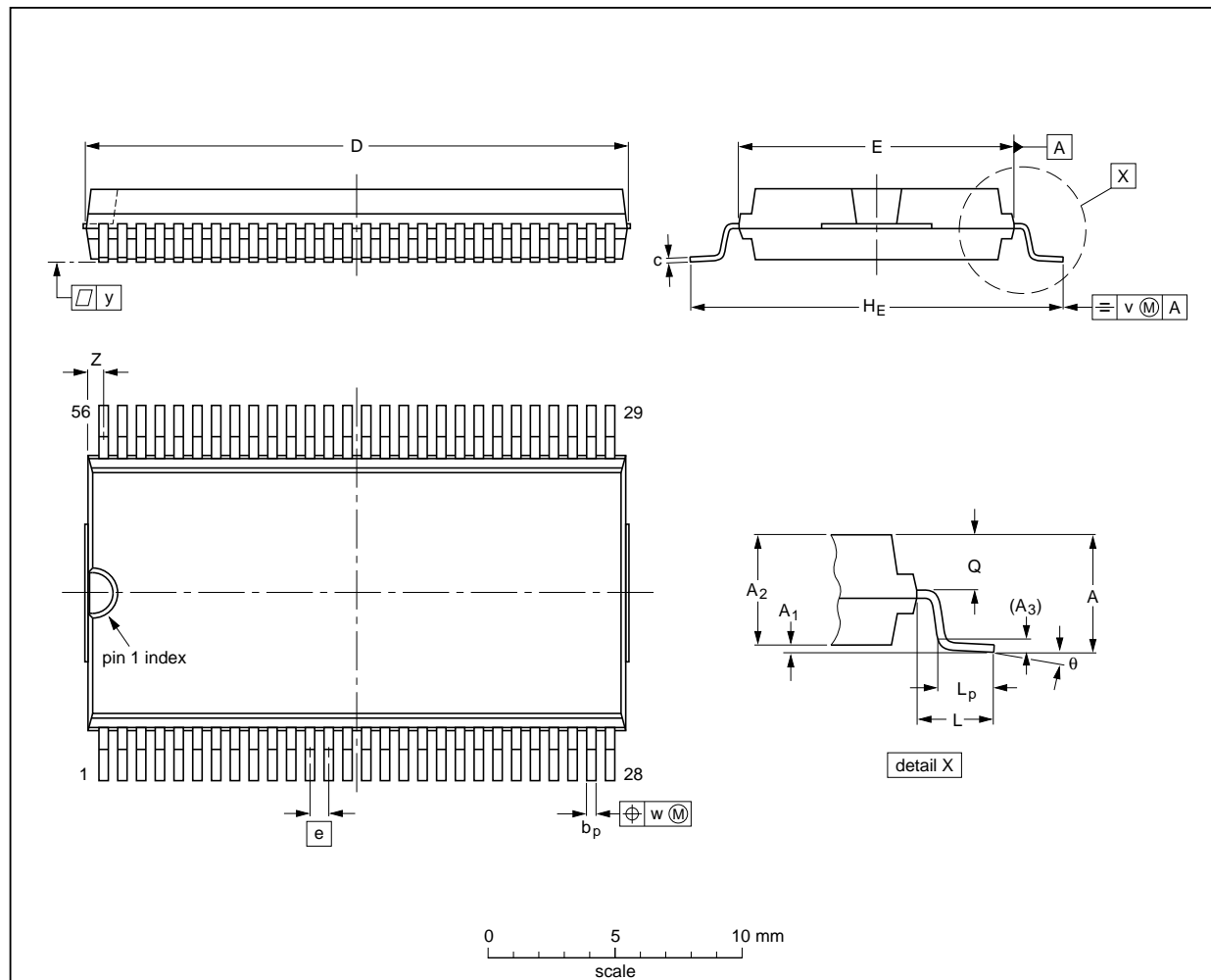


8-bit microcontroller with I<sup>2</sup>C-bus interface

PCF84C00

VSO56: plastic very small outline package; 56 leads

SOT190-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7° 0°
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.03	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

**Note**

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIA/J			
SOT190-1						92-11-17 96-04-02

8-bit microcontroller with I<sup>2</sup>C-bus interface

## PCF84C00

**12 SOLDERING****12.1 Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

**12.2 DIP****12.2.1 SOLDERING BY DIPPING OR BY WAVE**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**12.2.2 REPAIRING SOLDERED JOINTS**

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**12.3 SO and VSO****12.3.1 REFLOW SOLDERING**

Reflow soldering techniques are suitable for all SO and VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

**12.3.2 WAVE SOLDERING**

Wave soldering techniques can be used for all SO and VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**12.3.3 REPAIRING SOLDERED JOINTS**

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

8-bit microcontroller with I<sup>2</sup>C-bus interface

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**13 DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**14 LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

**15 PURCHASE OF PHILIPS I<sup>2</sup>C COMPONENTS**

Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

8-bit microcontroller with I<sup>2</sup>C-bus interface

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**NOTES**

# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 689 211, Fax. +359 2 689 102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 1949

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580/xxx

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.  
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

**Indonesia:** see Singapore

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,  
Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,  
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 247 9145, Fax. +7 095 247 9144

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 1231,  
Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 3 301 6312, Fax. +34 3 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 632 2000, Fax. +46 8 632 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2686, Fax. +41 1 481 7730

**Taiwan:** PHILIPS TAIWAN Ltd., 23-30F, 66,  
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,  
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 625 344, Fax. +381 11 635 777

**For all other countries apply to:** Philips Semiconductors, Marketing & Sales Communications,  
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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