DATA SHEET

AP172-317LF: Linear Power Amplifier

Features

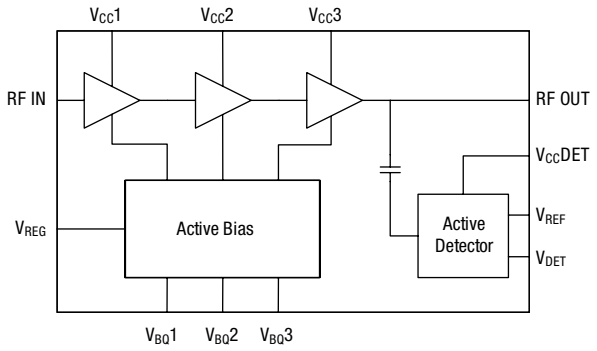
- High linearity @ 24 dBm
- High gain 33 dB
- 802.11b/g compliant
- 1800–2500 MHz operation
- Built-in level detector
- 27 dBm $P_{1\ dB}$ @ 2.4 GHz
- Uses single DC bias supply
- Low-cost plastic package
- Available on tape and reel
- Available lead (Pb)-free and RoHS-compliant

Description

The AP172-317LF is a linear, high-gain, medium-power amplifier designed for low voltage operation in a 2.4–2.5 GHz band having linear and high-efficiency performance with 802.11b/g signals and built-in level detection circuit. The device is manufactured on an advanced InGap HBT process and housed in a 16-pin 4 x 4 mm micro lead package.

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.

Simplified Block Diagram



Absolute Maximum Ratings

Characteristic	Value
RF input power	20 dBm
Supply current	600 mA
Supply voltage	5 V
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +125 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

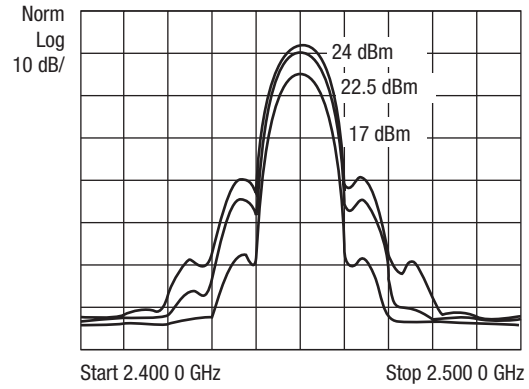
Electrical Specifications at 25 ºC (0, 3 V)

Z_0 = 50 Ω, unless otherwise noted

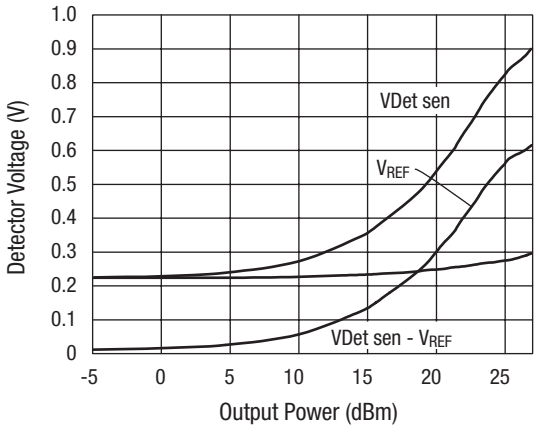
Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Frequency range		MHz	1800		2500	dB
Small signal gain	F = 2.45 GHz	$\lvert S_{21} \rvert$	31	33		dB
Output power at 1 dB compression	F = 2.45 GHz	$P_{1\ dB}$	26	27		dBm
Linear output power[1]	F = 2.45 GHz, I_C = 240 mA	P_{OUT}	23	24.5		dBm
First side lobe[1]	F = 2.45 GHz, I_C = 220 mA, P_{OUT} = 23 dBm			-35		dBc
Second side lobe[1]	F = 2.45 GHz, I_C = 220 mA, P_{OUT} = 23 dBm			-54		dBc
Operating voltage	Amplifier DC voltage	V_D	2.5	3.3	4.5	V
Reverse isolation		Isol.		30		dB
Current consumption	P_{OUT} = 24.0 dBm P_{OUT} = 22.5 dBm P_{OUT} = 17 dBm Quiescent	 Iq0		240 220 140 70		mA mA mA mA
Detector supply voltage	V_{CC}Det		2	2.5	4	V
Detector supply current	V_{CC}Det = 2.5 V	I_{CC}Det		2		mA
Detector output voltage	V_{CC}Det = 2.5 V P_{OUT} = 22.5 dBm	VDet sen - V_{REF}		0.43		V

V_{CC} = 3.3 V, I_C = 70 mA (unless otherwise specified)
1. Specifications are defined for the evaluation board with the 802.11b signal at 11 Mbit/s and having cosine (0.95) filtering.

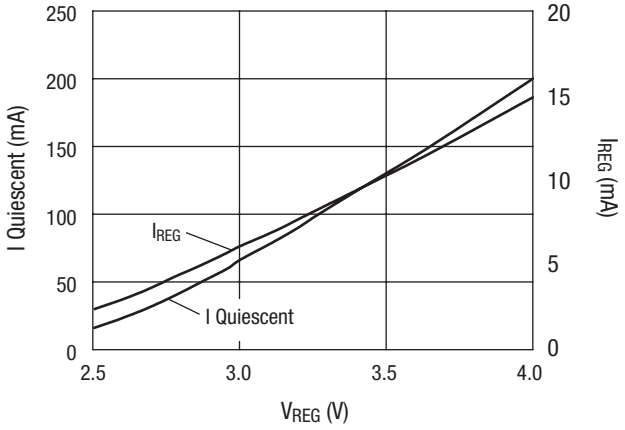
Typical Performance Data



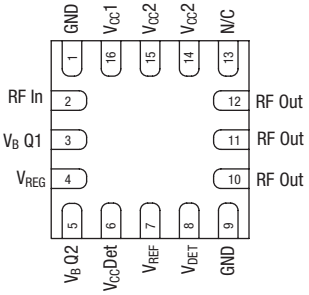
Spectrum of Output Signals at Different Power Levels



Built-In Detector Responses at V_{CC}Det = 2.5 V



Pin Out



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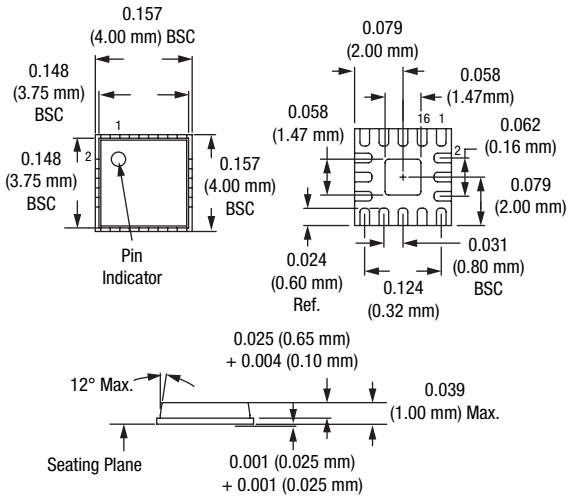


Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

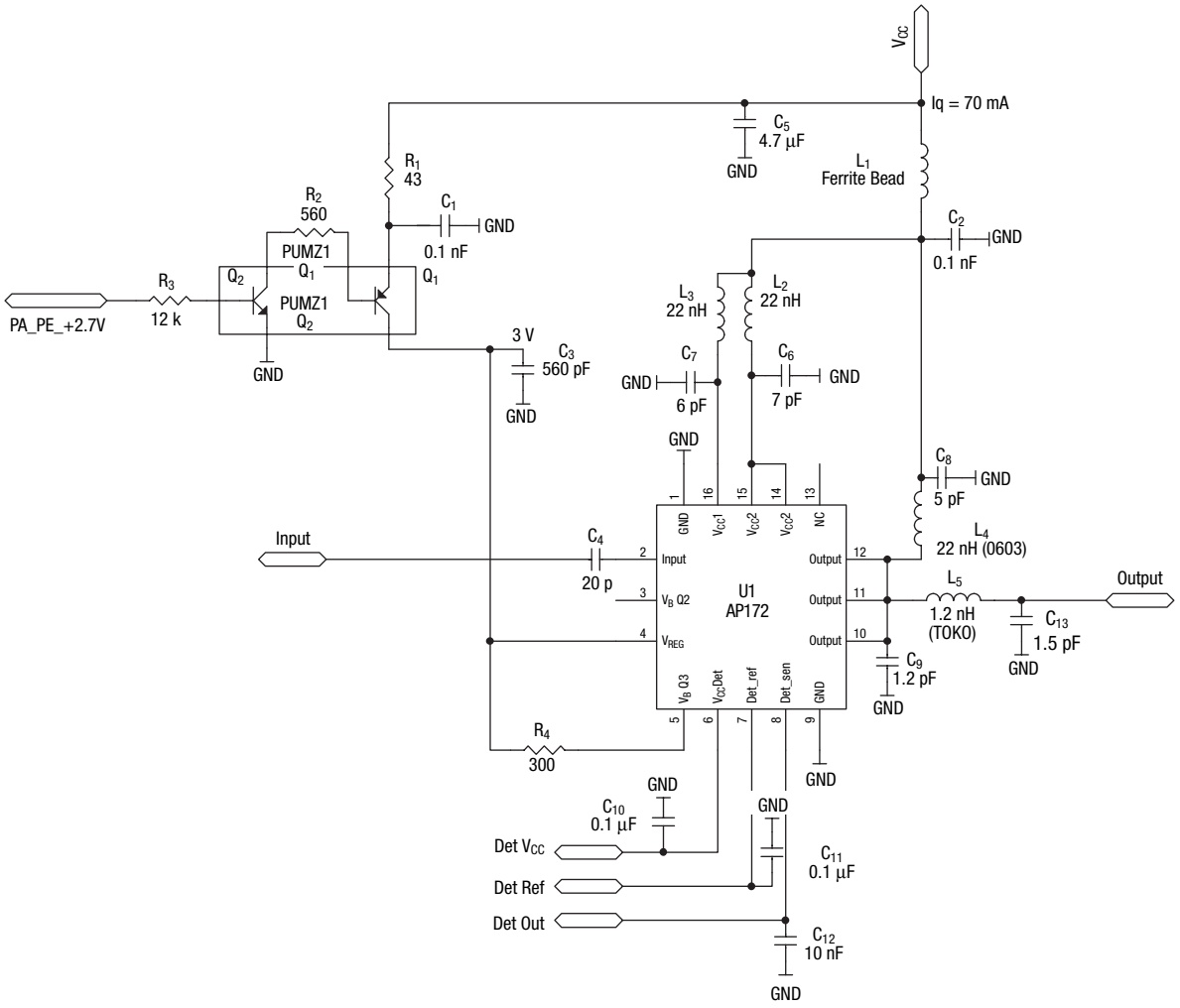
Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

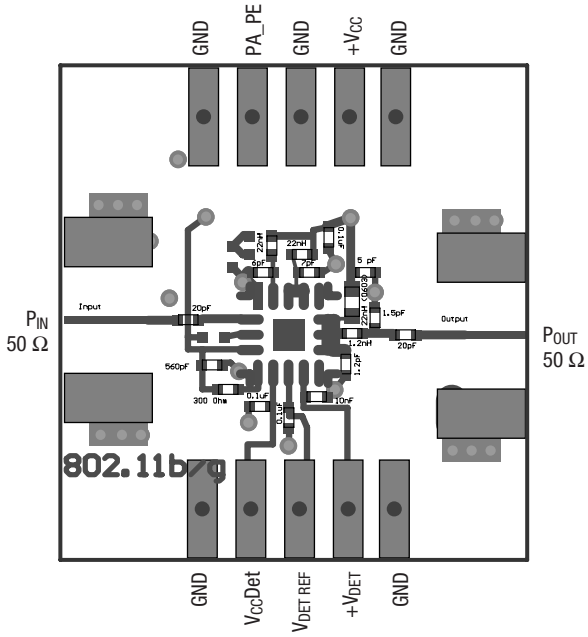
Pin Description

Pin Number	Pin Name	Description
2	J_1, J_2	RF input – RF input, 50 Ω (nominal). An external DC block is required
1, 9	GND	Equipotential point – Internal circuit common, which must be connected to the pcb ground or common via the lowest possible impedance.
3	V_B Q1	Bias adjust – 2nd stage – Quiescent current of the second amplifier stage as measured at $V_{CC}2$ can be increased by adding a resistor between this pin and V_{REG}. This pin may be left open if the nominal value of collector current for the second stage is acceptable. This pin should not be connected to ground.
4	V_{REG}	Regulated voltage input – The voltage applied to this pin supplies the active bias stages for the power amplifier stages. The nominal applied voltage is equal to V_{CC}. The power amplifier stages are disabled if this pin is open.
5	V_B Q2	Bias adjust – output stage – Quiescent current of the output amplifier stage as measured at $V_{CC}2$ can be increased by adding a resistor between this pin and V_{REG}. This pin may be left open if the nominal value of collector current for the output stage is acceptable. This pin should not be connected to ground.
6	V_{CC} DET	Active detector supply voltage – The voltage applied to this pin powers the active detector circuit. The nominal applied value is equal to V_{CC}. The active detector circuit is disabled if this pin is connected to ground.
7	V_{REF}	Active detector reference voltage output – The DC voltage produced at this pin can be used to track the temperature drift of the voltage from V_{DET}. This voltage can be used to temperature compensate the voltage from V_{DET}.
8	V_{DET}	Active detector output voltage – Detected output voltage which varies proportionally to the output power from the RF Out pins.
10, 11, 12	RF Out	RF output – RF outputs, internally connected to share signal currents. An internally-generated DC voltage is present at this pin, so a DC blocking capacitor should be included in the output circuit.
13	NC	No internal connection
14, 15	$V_{CC}2$	Collector supply voltage 2 – The voltage applied to these pins supplies the collector of the 2nd amplifier stage. These pins are internally connected to share current.
16	$V_{CC}1$	Collector supply voltage 1 – The voltage applied to this pin supplies the collector of the input amplifier stage.

Evaluation Board Schematic



Evaluation Board Layout (Top View)



Evaluation Board Layout (Bottom View)