HD74LV2GT74A

Single D–type Flip Flops with Preset and Clear / CMOS Logic Level Shifter

REJ03D0146–0200Z
(Previous ADE-205-681A (Z))
Rev.2.00
Oct.17.2003

Description

The HD74LV2GT74A has independent data, preset, clear, and clock inputs Q and $\overline{Q}$ outputs in an 8 pin package. The input data is transferred to the output at the rising edge of clock pulse CLK. The input protection circuitry on this device allows over voltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0 V CMOS Logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

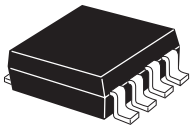
Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- TTL compatible input level.
  Supply voltage range : 3.0 to 5.5 V
  Operating temperature range : –40 to +85°C
- Logic-level translate function
  3.0 V CMOS logic → 5.0 V CMOS logic (@V_{CC} = 5.0 V)
  1.8 V or 2.5 V CMOS logic → 3.3 V CMOS logic (@V_{CC} = 3.3 V)
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
  All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Output current ±6 mA (@V_{CC} = 3.0 V to 3.6 V), ±12 mA (@V_{CC} = 4.5 V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Ordering Information

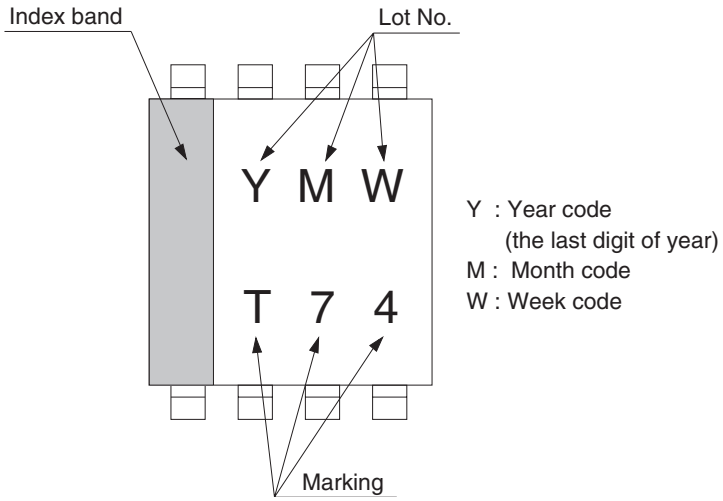
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV2GT74AUSE	SSOP-8 pin	TTP-8DBV	US	E (3,000 pcs/reel)

Outline and Article Indication

• HD74LV2GT74A



SSOP–8



Function Table

Inputs				Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H *1	H *1
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	↓	X	Q_0	$\overline{Q}_0$

H : High level

L : Low level

X : Immaterial

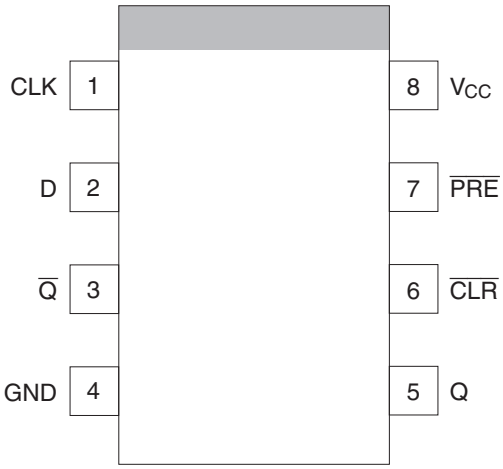
↑ : Low to high transition

↓ : High to low transition

Q_0 : The level of Q immediately before the input conditions shown in the above table are determined.

Note : 1. Q and $\overline{Q}$ will remain high as long as preset and clear are low, but Q and $\overline{Q}$ are unpredictable, if preset and clear go high simultaneously.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range [*1]	V_I	–0.5 to 7.0	V	
Output voltage range [*1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output : H or L
		–0.5 to 7.0		V_{CC} : OFF
Input clamp current	I_{IK}	–20	mA	V_I < 0
Output clamp current	I_{OK}	±50	mA	V_O < 0 or V_O > V_{CC}
Continuous output current	I_O	±25	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at Ta = 25°C (in still air) [*3]	P_T	200	mW	
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

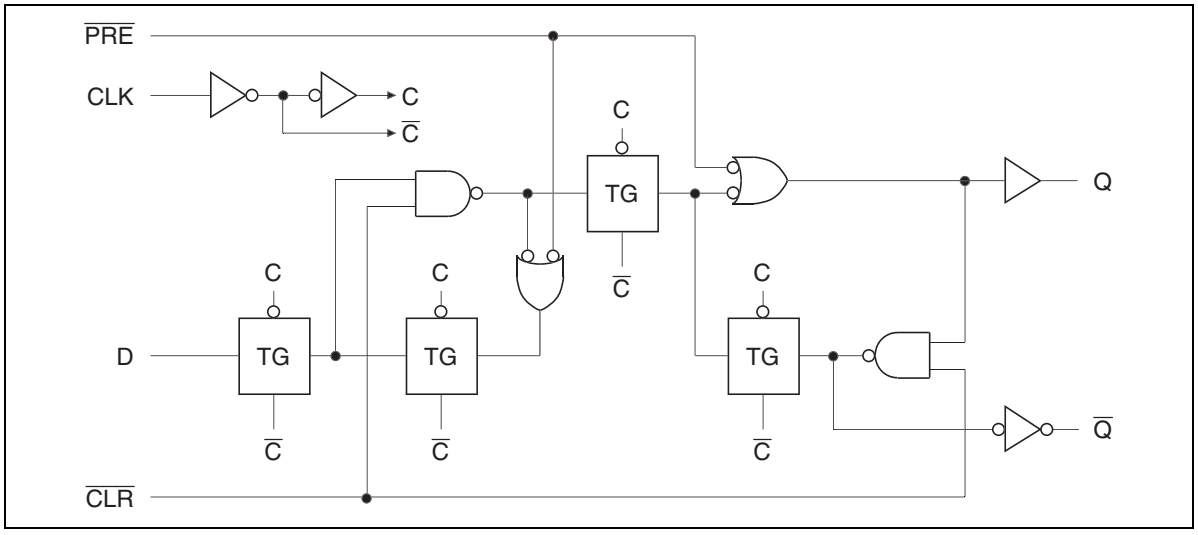
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	3.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	–40 to +85	°C
Input rise / fall time	t_r, t_f	0 to 100 (V_{CC} = 3.0 to 3.6 V)	ns
		0 to 20 (V_{CC} = 4.5 to 5.5 V)	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Electrical Characteristic

- Ta = –40 to 85°C

Item	Symbol	V_{CC} (V) *	Min	Typ	Max	Unit	Test condition
Input voltage	V_{IH}	3.0 to 3.6	1.5	—	—	V	
		4.5 to 5.5	2.0	—	—		
	V_{IL}	3.0 to 3.6	—	—	0.6		
		4.5 to 5.5	—	—	0.8		
Hysteresis voltage	V_H	3.3	—	0.10	—	V	$V_T^+ – V_T^-$
		5.0	—	0.15	—		
Output voltage	V_{OH}	Min to Max	V_{CC}–0.1	—	—	V	I_{OH} = –50 µA
		3.0	2.48	—	—		I_{OH} = –6 mA
		4.5	3.8	—	—		I_{OH} = –12 mA
	V_{OL}	Min to Max	—	—	0.1		I_{OL} = 50 µA
		3.0	—	—	0.44		I_{OL} = 6 mA
		4.5	—	—	0.55		I_{OL} = 12 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	µA	V_{IN} = 5.5 V or GND
Quiescent supply current	I_{CC}	5.5	—	—	10	µA	V_{IN} = V_{CC} or GND, I_O = 0
	ΔI_{CC}	5.5	—	—	1.5	mA	One input V_{IN} = 3.4 V, other input V_{CC} or GND
Output leakage current	I_{OFF}	0	—	—	5	µA	V_O = 5.5 V
Input capacitance	C_{IN}	5.0	—	2.5	—	pF	V_{IN} = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- V_{CC} = 3.3 ± 0.3 V

Item	Symbol	T_a = 25°C			T_a = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{max}	80	140	—	70	—	MHz	C_L = 15 pF		
		50	90	—	45	—		C_L = 50 pF		
Propagation delay time	t_{PLH} t_{PHL}	—	7.0	12.5	1.0	14.5	ns	C_L = 15 pF	$\overline{PRE}$/$\overline{CLR}$	Q or $\overline{Q}$
		—	8.0	12.0	1.0	14.0			CLK	
		—	9.0	16.0	1.0	18.0		C_L = 50 pF	$\overline{PRE}$/$\overline{CLR}$	Q or $\overline{Q}$
		—	10.0	15.5	1.0	17.5			CLK	
Setup time	t_{su}	6.0	—	—	7.0	—	ns		D	
		5.0	—	—	5.0	—			$\overline{PRE}$ or $\overline{CLR}$ inactive	
Hold time	t_h	0.5	—	—	0.5	—	ns			
Pulse width	t_w	6.0	—	—	7.0	—	ns		$\overline{PRE}$ or $\overline{CLR}$ "L"	
		6.0	—	—	7.0	—			CLK "H" or "L"	

- V_{CC} = 5.0 ± 0.5 V

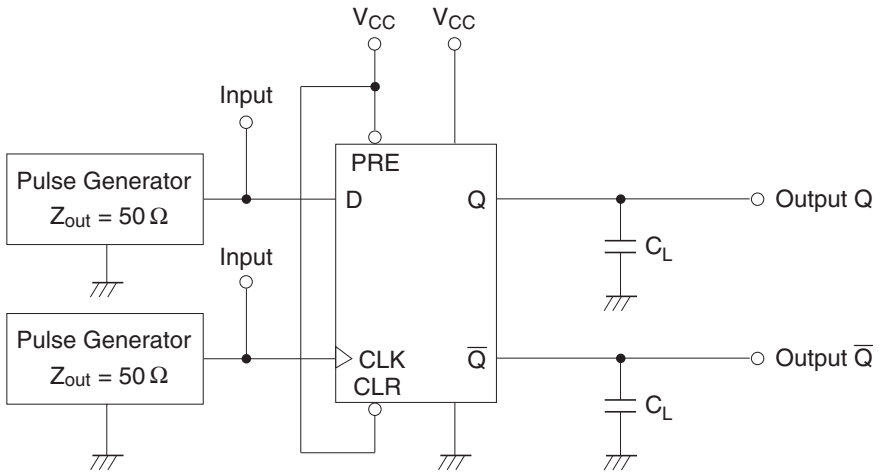
Item	Symbol	T_a = 25°C			T_a = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{max}	130	180	—	110	—	MHz	C_L = 15 pF		
		90	140	—	75	—		C_L = 50 pF		
Propagation delay time	t_{PLH} t_{PHL}	—	5.0	7.7	1.0	9.0	ns	C_L = 15 pF	$\overline{PRE}$/$\overline{CLR}$	Q or $\overline{Q}$
		—	5.6	7.3	1.0	8.5			CLK	
		—	6.6	9.7	1.0	11.0		C_L = 50 pF	$\overline{PRE}$/$\overline{CLR}$	Q or $\overline{Q}$
		—	7.2	9.3	1.0	10.5			CLK	
Setup time	t_{su}	5.0	—	—	5.0	—	ns		D	
		3.0	—	—	3.0	—			$\overline{PRE}$ or $\overline{CLR}$ inactive	
Hold time	t_h	0.5	—	—	0.5	—	ns			
Pulse width	t_w	5.0	—	—	5.0	—	ns		$\overline{PRE}$ or $\overline{CLR}$ "L"	
		5.0	—	—	5.0	—			CLK "H" or "L"	

Operating Characteristics

- C_L = 50 pF

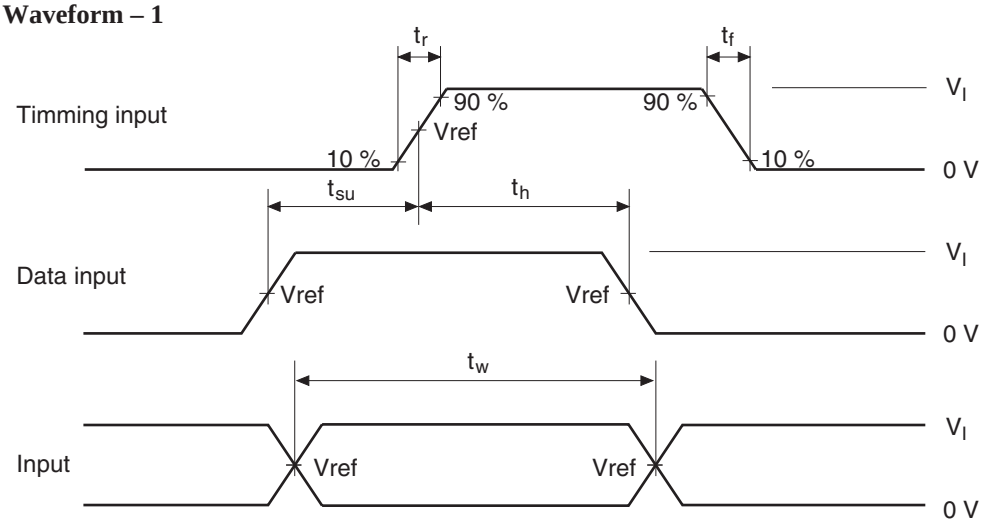
Item	Symbol	V_{CC} (V)	T_a = 25°C Min	Typ	Max	Unit	Test Conditions
Power dissipation capacitance	C_{PD}	5.0	—	14.0	—	pF	f = 10 MHz

Test Circuit

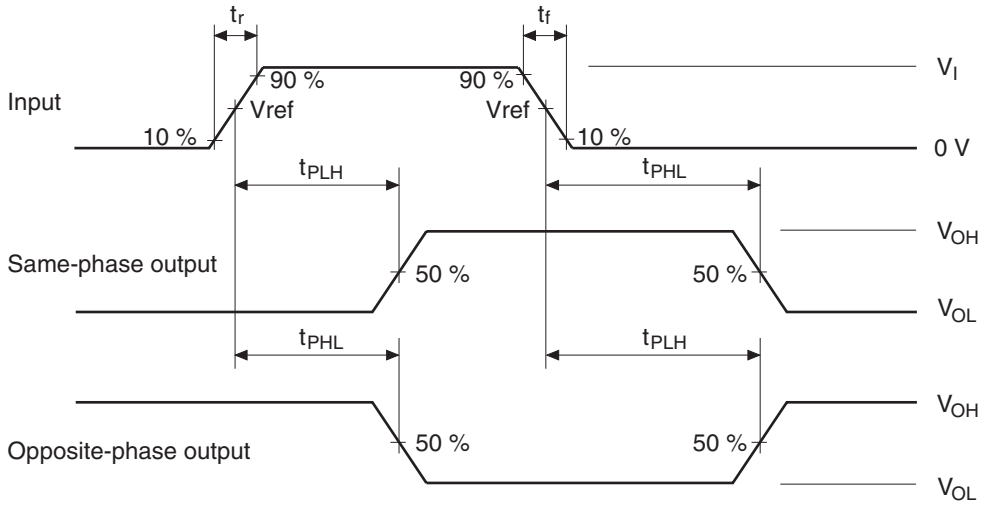


Notes: 1. C_L includes probe and jig capacitance.

• **Waveform – 1**



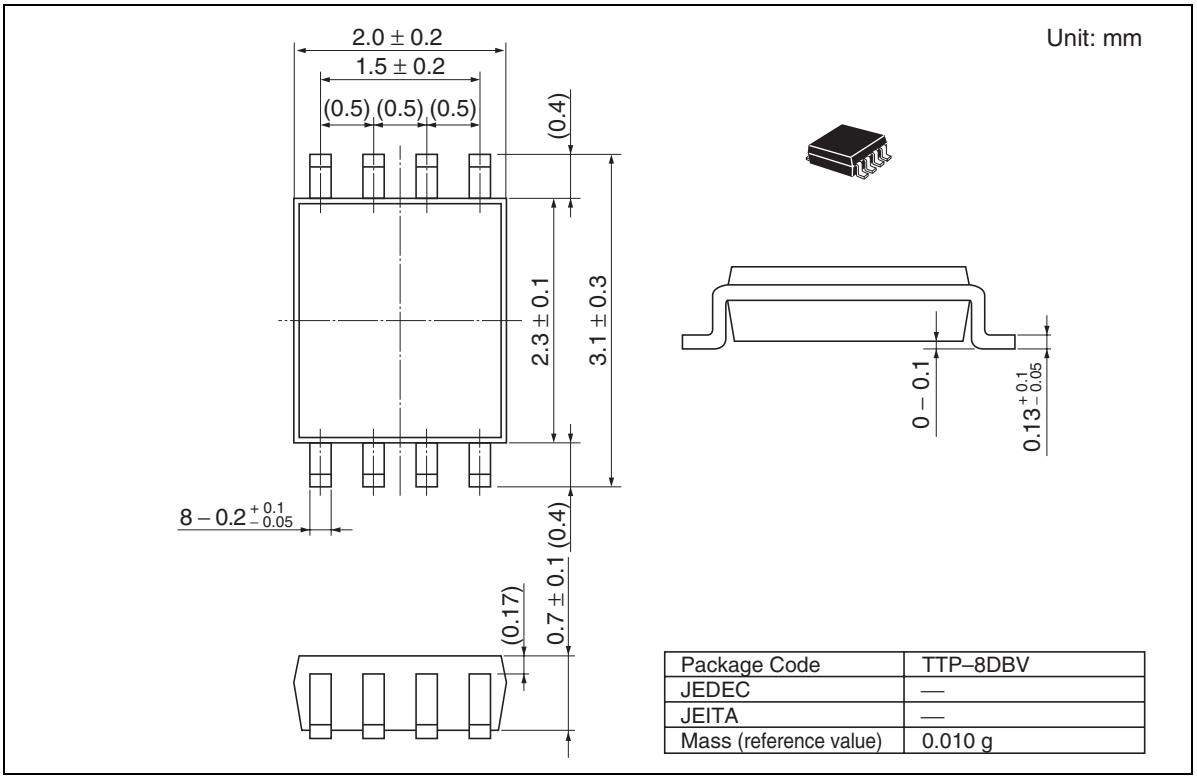
• **Waveform – 2**



V_{CC} (V)	INPUTS		Vref
	V_I	t_r / t_f	
3.3±0.3	2.5 V	≤ 3.0 ns	50%
5.0±0.5	3 V	≤ 3.0 ns	1.5 V

Notes: 1. Input waveform : PRR ≤ 1 MHz, Zo = 50 Ω.
2. The output are measured one at a time with one transition per measurement.

Package Dimensions



Package Code	TTP–8DBV
JEDEC	—
JEITA	—
Mass (reference value)	0.010 g

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