Z84C90

KIO Serial/Parallel Counter Timer

Product Specification

PS011802-0902

ZiLOG Worldwide Headquarters • 532 Race Street • San Jose, CA 95126-3432
Telephone: 408.558.8500 • Fax: 408.558.8300 • http://www.ZiLOG.com

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ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126-3432
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

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KIO Serial/Parallel Counter/Timer Product Specification

Features

Table 1. Z84C90 KIO Serial/Parallel/Counter/Timer Packages

Part Number	Package	Frequency (MHz)
Z84C9008ASC	100-pin LQFP	8
Z84C9010ASC	100-pin LQFP	10
Z84C9008VEC	84-pin PLCC	8
Z84C9008VSC	84-pin PLCC	8
Z84C9010VSC	84-pin PLCC	10
Z84C9012VSC	84-pin PLCC	12

General Description

ZiLOG's Z84C90 Serial/Parallel/Counter/Timer KIO is a multi-channel, multipurpose I/O device designed to provide the end-user with a cost-effective and powerful solution to meet peripheral needs. The Z84C90 combines the features of one Z84C30 CTC, one Z84C20 PIO, a Z84C4x SIO, a 8-bit, bit-programmable I/O port, and a crystal-oscillator into a single package (84-pin PLCC or 100-pin LQFP). Using fifteen internal registers for data and programming information, the KIO can easily be configured to any given system environment. Although the optimum performance is obtained with a Z84C00 CPU, the KIO can just as easily be used with any other CPU.

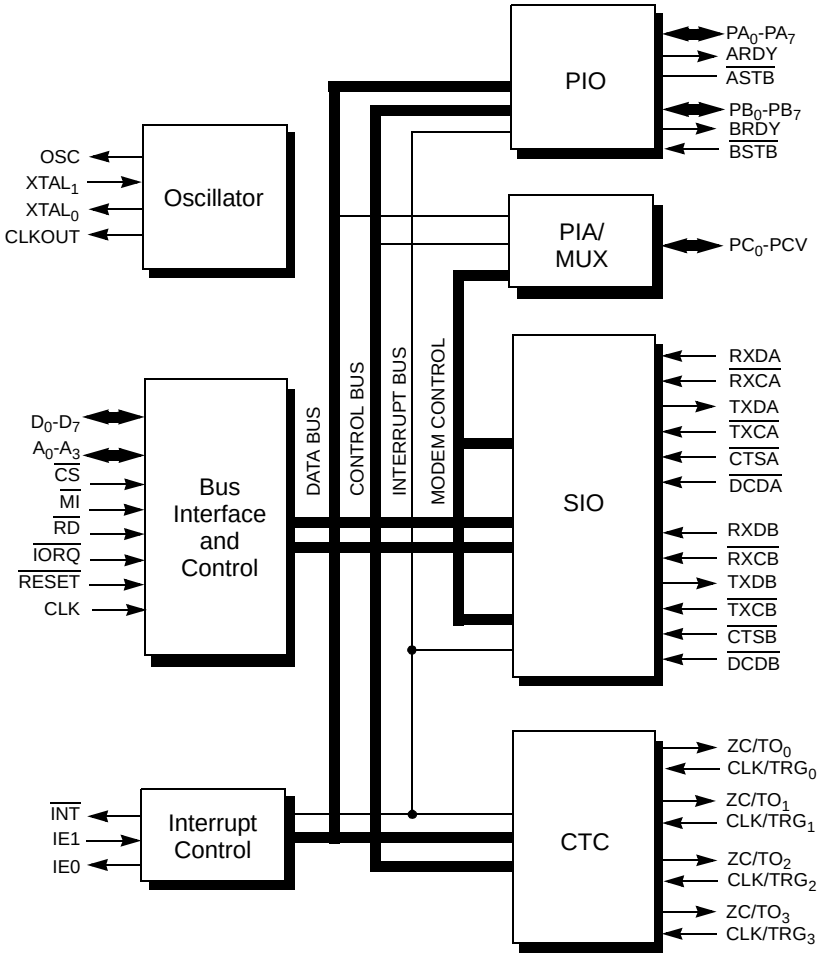

Figure 1. KIO Block Diagram

Absolute Maximum Ratings

Voltage on V_{CC} with respect to V_{SS}	–0.3V to +7.0V
Voltages on all inputs with respect to V_{SS}	–0.3V to V_{CC} +0.3V
Operating Ambient Temperature	See Ordering Information
Storage Temperature	–65 C to +150 C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Types

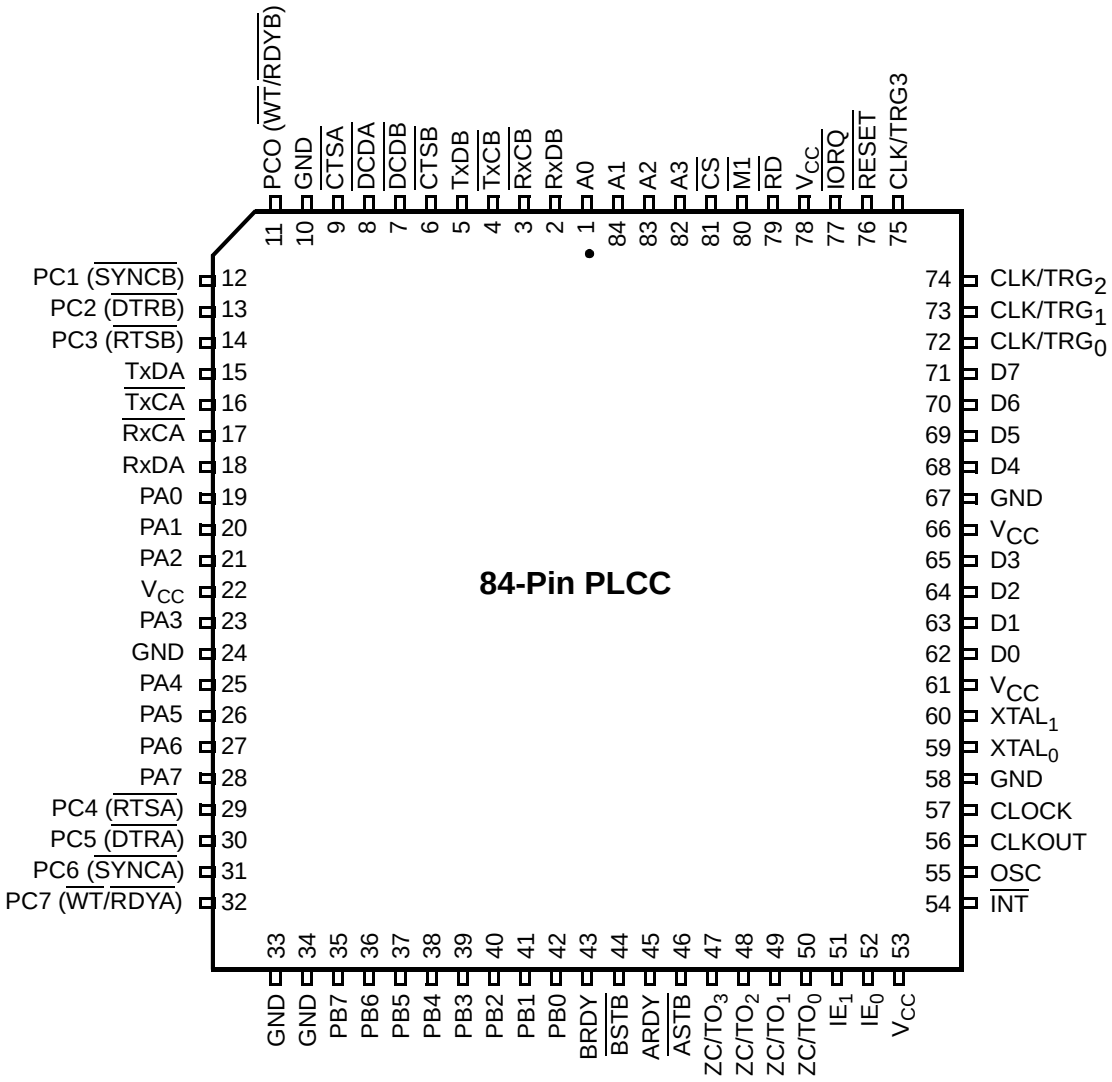

Figure 2. Z84C90 84-Pin PLCC Configuration

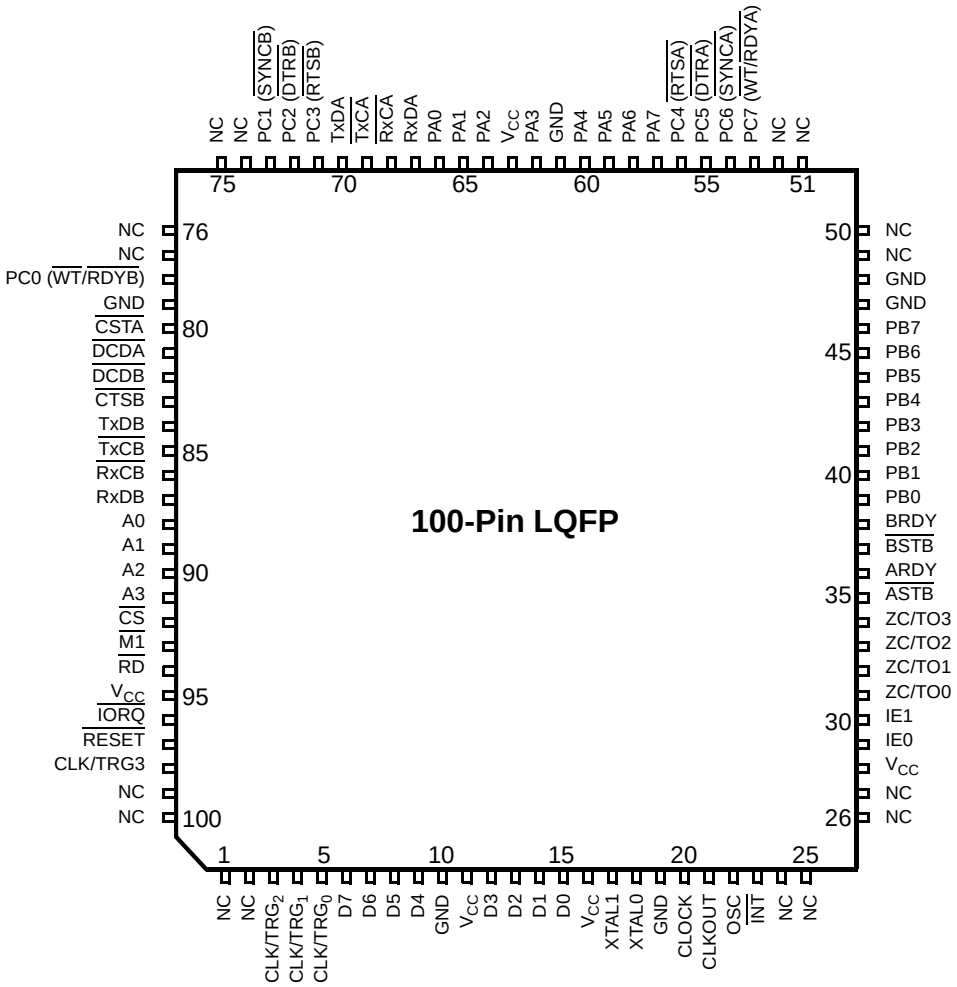

Figure 3. 100-Pin LQFP Configuration

Pin Descriptions

A0–A3. Address bus (inputs). Used to select the port/register for each bus cycle.

ARDY, BRDY. Port Ready (outputs, Active High). These signals indicate that the port is ready for a data transfer. In Mode 0, the signal indicates that the port has data available to the peripheral device. In Mode 1, the signal indicates that the port is ready to accept data from the peripheral device. In Mode 2, ARDY indicates that Port A has data available for the peripheral device, but that the data is not be placed onto PA0–PA7 until the $\overline{\text{ASTB}}$ signal is Active. BRDY indicates that Port A is able to accept data from a peripheral device.

Note: Port B does not support Mode 2 operation and can only be used in Mode 3 when Port A is programmed for Mode 2. BRDY is not associated with Port B when it is operating in Mode 3.

$\overline{\text{ASTB}}$, $\overline{\text{BSTB}}$. Port Strobe (inputs, Active Low). These signals indicate that the peripheral device has performed a transfer. In Mode 0, the signal indicates that the peripheral device has accepted the data present on the port pins. In Mode 1, the signal causes the data on the port pins to be latched onto Port A. In Mode 2, $\overline{\text{ASTB}}$ Low causes the data in the output data latch of Port A to be placed onto the Port A pins. $\overline{\text{BSTB}}$ Low causes the data present on the Port A pins to be latched into the Port A input data latch. The end of the current transaction is noted by the rising edge of these signals.

Note: Port B does not support Mode 2 operation, and can only be used in Mode 3 when Port A is programmed for Mode 2. $\overline{\text{BSTB}}$ is not associated with Port B when it is operating in Mode 3.

CLK/TRG0–CLK/TRG3. External Clock/Timer Trigger (inputs, user-selectable Active High or Low). These four pins correspond to the four counter/timer channels of the KIO. In Counter mode, each active edge causes the downcounter to decrement. In Timer mode, an active edge starts the timer.

CLKOUT. Clock Out (output). This output is a divide-by-two of the oscillator (XTAL) input.

CLOCK. System Clock (input). This clock must be the same as (or a derivative of) the CPU clock. If the CLKOUT is to be used as the system clock, then these two pins must be connected together.

$\overline{\text{CS}}$. Chip Select (input, Active Low). Used to activate the internal register decoding mechanism and allow the KIO to perform a data transfer to/from the CPU.

$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$. Clear to Send (inputs, Active Low). These signals are modem control signals for the serial channels. When programmed for Auto Enable, a Low on these pins enables their respective transmitters. If not programmed as Auto Enable, these pins may be used as general-purpose input signals.

D_0–D_7. Data Bus (bidirectional, Active High, 3-stated). Used for data exchanges between the CPU and the KIO for programming and data transfer. The KIO also monitors the data bus for RETI instructions to maintain its Interrupt Under Service (IUS) status.

$\overline{\text{DCDA}}$, **$\overline{\text{DCDB}}$**. Data Carrier Detect (inputs, Active Low). These signals are modem control signals for the serial channels. When programmed for Auto Enable, a Low on these pins enables their respective receivers. If not programmed as Auto Enable, these pins may be used as general-purpose input signals.

$\overline{\text{DTRA}}$, **$\overline{\text{DTRB}}$**. Data Terminal Ready (outputs, Active Low). These signals are modem control signals for the serial channels. They follow the state programmed into their respective serial channels, and are multiplexed with Port C, bits 5 and 2, respectively.

IEI. Interrupt Enable In (input, Active High). This signal is used with Interrupt Enable Out (IEO) to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no higher-priority device is requesting an interrupt.

IEO. Interrupt Enable Out (output, Active High). This signal is used with Interrupt Enable In (IEI) to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that this device is requesting an interrupt, and that no higher-priority device, is not requesting an interrupt. A Low blocks any lower-priority devices from requesting an interrupt.

$\overline{\text{IORQ}}$. Input/Output Request (input, Active Low). $\overline{\text{IORQ}}$ is used with $\overline{\text{RD}}$, A_0–A_3, and $\overline{\text{CS}}$ to transfer data between the KIO and the CPU. When $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, and $\overline{\text{CS}}$ are Active Low, the device selected by A_0–A_3 transfers data to the CPU. When $\overline{\text{IORQ}}$ and $\overline{\text{CS}}$ are Active Low, but $\overline{\text{RD}}$ is Active High, the device selected by A_0–A_3 is written into by the CPU. When $\overline{\text{IORQ}}$ and $\overline{\text{M1}}$ are both Active Low, the KIO may respond with an interrupt vector from its highest-priority interrupting device.

$\overline{\text{M1}}$. Machine Cycle 1 (input, Active Low). When $\overline{\text{M1}}$ and $\overline{\text{RD}}$ are Low, the Z80 CPU fetches an instruction from memory; the KIO decodes this cycle to determine if the RETI instruction sequence is being executed. When $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ are both active, the KIO decodes the cycle to be an interrupt acknowledge, and may respond with a vector from its highest-priority interrupting device.

OSC. Oscillator (output). This output is a reference clock for the oscillator.

PA0–PA7. Port A Bus (bidirectional, tristated). One of the 8-bit ports of the PIO. PA_0 is the least-significant bit of the bus.

PB0–PB7. Port B Bus (bidirectional, tristated). One of the 8-bit ports of the PIO. PB_0 is the least-significant bit of the bus. This port can also supply 1.5mA at 1.5V to drive Darlington transistors.

PC0–PC7. Port C Bus (bidirectional, tristated). PC_0 is the least-significant bit of the bus. These pins are multiplexed between the 8-bit PIA and additional modem control signals for the serial channels.

$\overline{\text{RD}}$. Read (input, Active Low). When $\overline{\text{RD}}$ is active, a memory or I/O read operation is in progress. $\overline{\text{RD}}$ is used with A_0–A_3, $\overline{\text{CS}}$ and $\overline{\text{IORQ}}$ to transfer data between the KIO and CPU.

$\overline{\text{RESET}}$. Reset (input, Active Low). A Low on this pin forces the KIO into a Reset condition. This signal must be active for a minimum of three Clock cycles. The KIO resets so that the PIO ports operate in Mode 1

- With handshakes inactive and interrupts disabled
- PIA port in Input mode and active
- CTC channel counting terminated and interrupts disabled

- SIO channels disabled
- Marking with interrupts disabled.

All control registers must be rewritten after a hardware reset.

$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$. Request to Send (outputs, Active Low). These signals are modem control signals for their serial channels. They follow the inverse state programmed into their respective serial channels, and are multiplexed with Port C, bits 4 and 3, respectively.

$\overline{\text{RxCA}}$, $\overline{\text{RxCB}}$. Receive Clock (inputs, Active Low). These clocks are used to assemble the data in the receiver shift register for their serial channels. Data is sampled on the rising edge of the clock.

RxDA, RxDB. Receive Data (inputs, Active High). These pins are the input data pins to the receive shift register for their serial channels.

$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$. Synchronization (bidirectional, Active Low). In the Asynchronous mode of operation, these pins act much like the $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ pins. Transitions affect the Sync/Hunt status bit for their respective serial channels, but serve no other purpose. These pins are multiplexed with Port C, bits 6 and 1, respectively.

$\overline{\text{TxCA}}$, $\overline{\text{TxCB}}$. Transmit Clock (inputs, Active Low). These clocks are used to transmit data from the transmit shift register for their serial channels. Data is transmitted on the falling edge of the clock.

TxDA, TxDB. Transmit Data (outputs, Active High). These pins are the output data pins from the transmitter for their serial channels.

$\overline{\text{WT}}$/$\overline{\text{RDYA}}$, $\overline{\text{WT}}$/$\overline{\text{RDYB}}$. Wait/Ready (outputs, open-drain when programmed as Wait; tristated when programmed as Ready). These pins may be programmed as Ready lines for a DMA controller or Wait lines for interfacing to a CPU. As a Ready line, these pins indicate (when Active Low) that the transmitter or the receiver requests a transfer between the serial channel and the DMA. As a Wait line, these pins dictate (when Low) that the CPU must wait until the transmitter or receiver can complete the requested transaction. These pins are multiplexed with Port C, bit 7 and 0, respectively.

XTALI. Crystal/Clock Connection. (input).

XTALO. Crystal Connection. (output).

ZC/TO0–ZC/TO3. Zero count/Time-out (outputs, Active High). These four pins are outputs from the four counter/timer channels of the KIO. Each pin pulses High when its corresponding downcounter reaches 0.

Table 2. KIO Registers

Address	A3	A2	A1	A0
Register 0: PIO Port A Data	0	0	0	0
Register 1: PIO Port A Command	0	0	0	1
Register 2: PIO Port B Data	0	0	1	0
Register 3: PIO Port B Command	0	0	1	1
Register 4: CTC Channel 0	0	1	0	0
Register 5: CTC Channel 1	0	1	0	1
Register 6:	0	1	1	0
Register 7:	0	1	1	1
Register 8: SIO Port A Data	1	0	0	0
Register 9: SIO Port A Command/Status	1	0	0	1
Register 10: SIO Channel B Data	1	0	1	0
Register 11: SIO Channel B Command/Status	1	0	1	1
Register 12: PIA Port C Data	1	1	0	0
Register 13: PIA Port C Command	1	1	0	1
Register 14: KIO Command	1	1	1	0
Register 15: Reserved	1	1	1	1

Note: Additionally, $\overline{IORQ}$ and $\overline{CS}$ must be Low. Registers are written to or read from by the CPU, applying a 1 or a 0 respectively on the $\overline{RD}$ pin.

Standard Test Conditions

The DC Characteristics and Capacitance sections below apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature ranges are:

- S = 0° C to +70° C
- E = –40° C to +100° C

Voltage Supply Range: +5.0V ± 10%

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

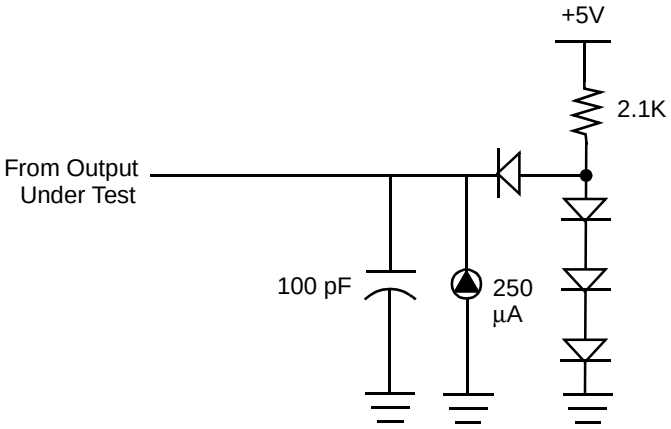

Figure 4. Test Load Diagram

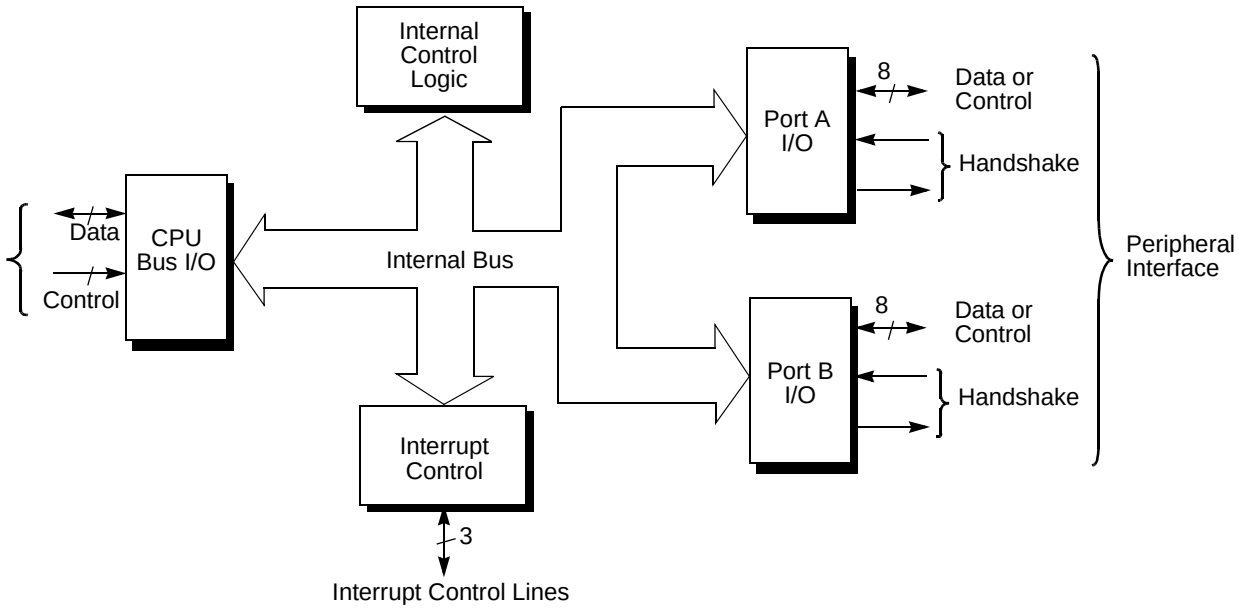

Figure 5. PIO Block Diagram

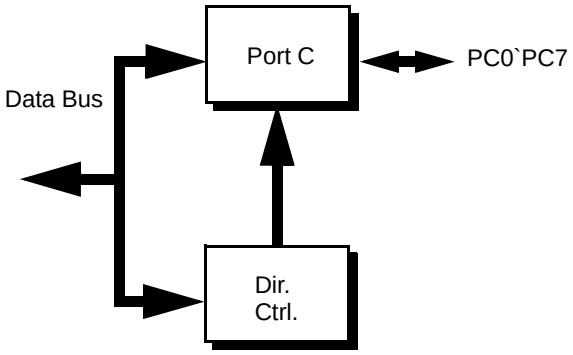

Figure 6. PIA Block Diagram

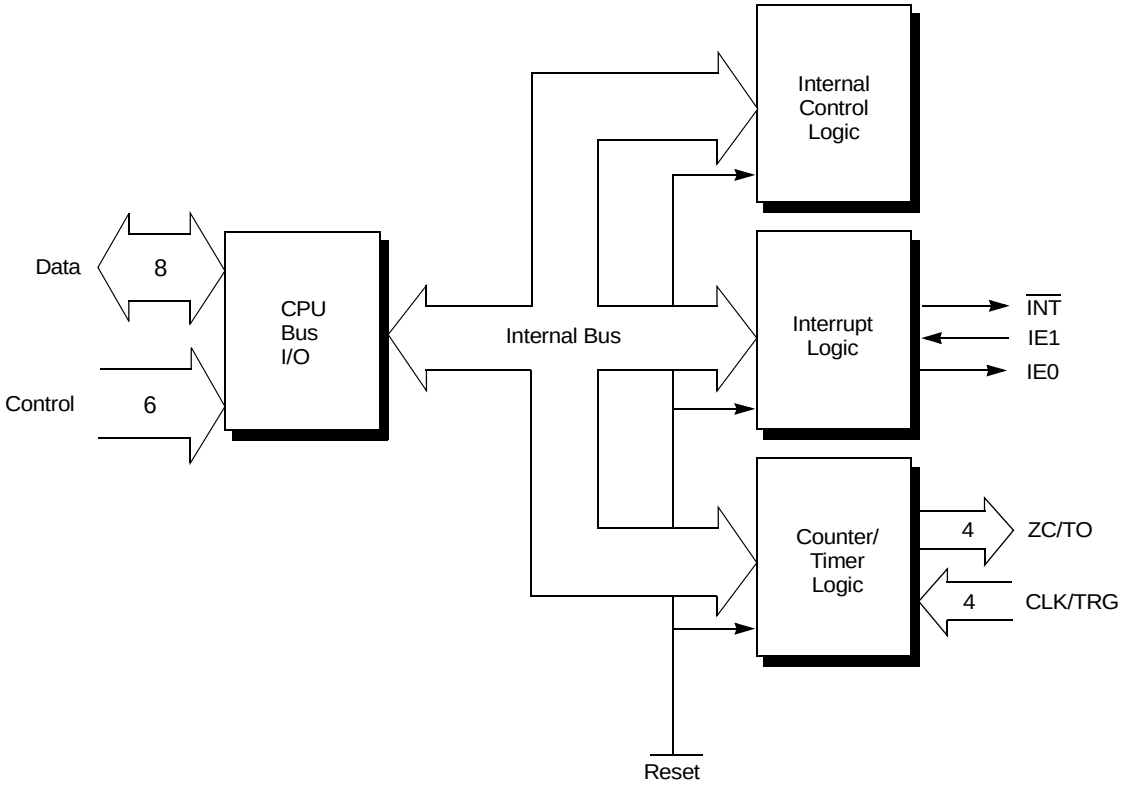

Figure 7. CTC Block Diagram

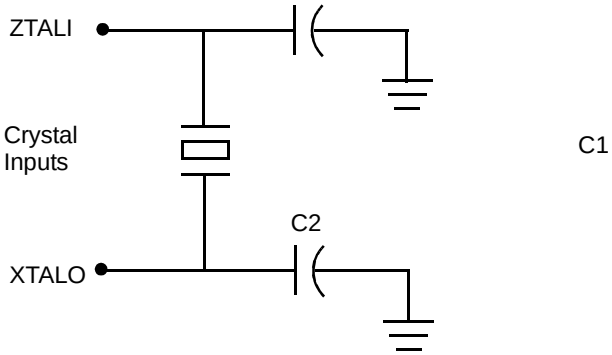

Figure 8. Crystal Connection

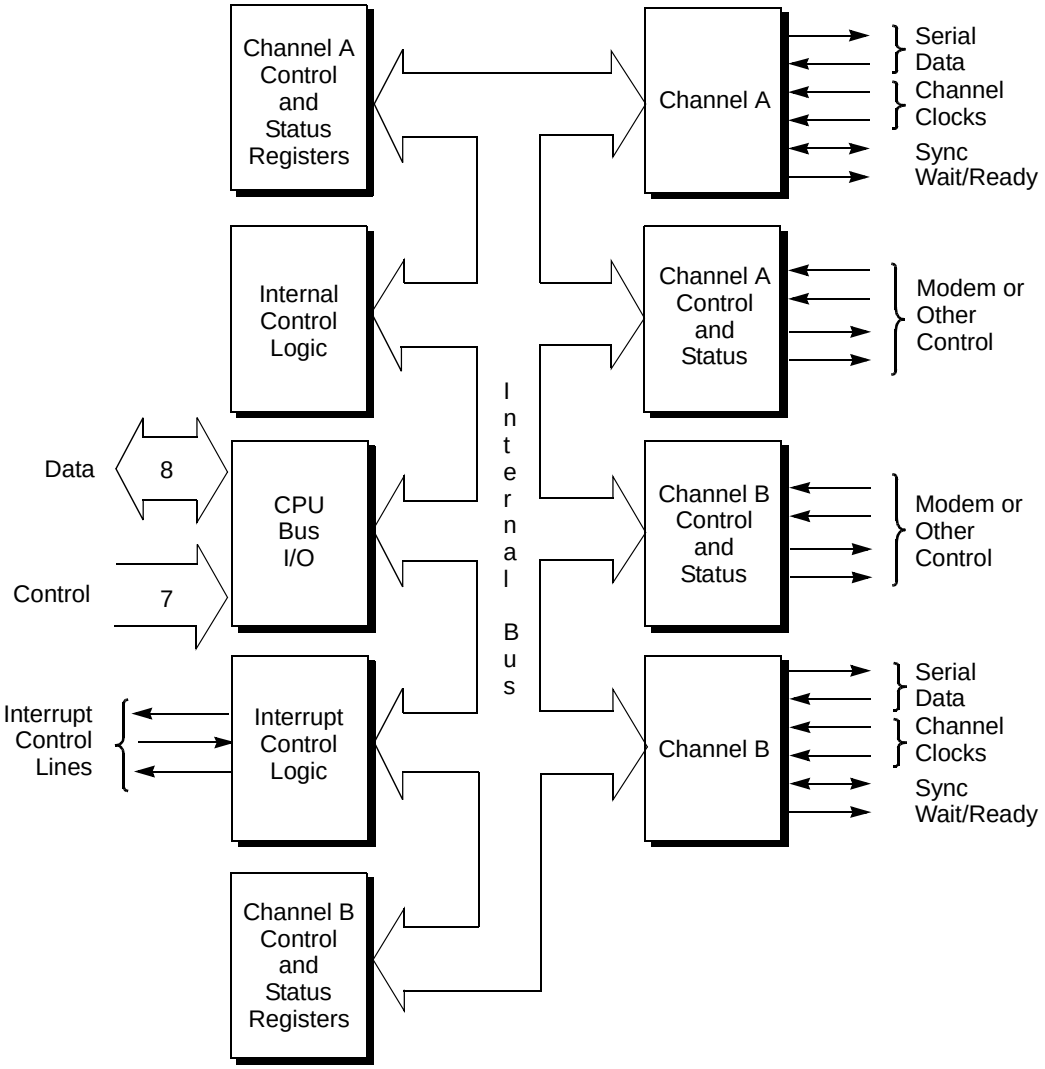

Figure 9. SIO Block Diagram

DC Characteristics

V_{cc} = 5.0V +/– 10% unless otherwise specified.

Table 3. DC Characteristics of the Z84C90

Symbol	Item	Min	Max	Unit	Condition
V_{ILC}	Clock Input Low Voltage	–0.3	+0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC}–0.6	V_{cc}+0.3		
V_{IL}	Input Low Voltage	–0.3	+0.8	V	
V_{IH}	Input High Voltage	2.2	V_{cc}	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 2.0mA
V_{OH1}	Output High Voltage 1	2.4		V	I_{OH} = 1.6mA
V_{OH2}	Output High Voltage 2	V_{CC}–0.8		V	I_{OH} = 250mA
I_{LI}	Input Leakage Current		±10.0	mA	V_{in} = 0.4~V_{cc}
I_{OL}	3-State Leakage Current		±10.0	mA	V_{in} = 0.4~V_{cc}
$I_{L(SY)}$	$\overline{SYNC}$ Pin Leakage Current	+10	–40	mA	V_{in} = 0.4~V_{cc}
I_{OHD}	Darlington Drive Current (Port B and ZC/T00~3)	–1.5		mA	V_{OH} = 1.5V R_{EXT} = 390 Ohms
I_{CC}	Power Supply Current* 8 MHz 10MHz 12.5MHz		 15 15 15	 mA mA	 V_{CC} = 5 V V_{IH} = V_{cc}–.2V V_{IL} = .2V

*Measurement made with output floating over specified temperature and voltage ranges.

Table 4. Capacitance

Symbol	Parameter	Minimum	Maximum	Unit
C_{CLOCK}	Clock Capacitance		10	cF
CI_N	Input Capacitance		10	cF
C_{OUT}	Output Capacitance		15	cF

T_A = 25°C, f = 1MHz

AC Characteristics

Table 5. AC Characteristics of the Z84C90

			8MHz		10MHz[1]		12MHz		
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**U/M**
Bus Interface Timing									
1	TcC	Clock Cycle Time	125	DC	100	DC	80	DC	ns
2	TwCh	Clock Pulse Width (High)	55	DC	42	DC	32	DC	ns
3	TwCl	Clock Pulse Width (Low)	55	DC	42	DC	32	DC	ns
4	TfC	Clock Fall Time		10		10		10	ns
5	TrC	Clock Rise Time		10		10		10	ns
6	TsA(Rlf)	Address, $\overline{CS}$ Setup to $\overline{RD}$, $\overline{IORQ}$ Fall	50		40		30		ns
7	TsRl(Cr)	$\overline{RD}$, $\overline{IORQ}$ to Clock Rise Setup	50		50		40		ns
8	Th	Hold Time for Specified Setup	15		15		15		ns
9	TdCr(DO)	CLOCK Rise to Data Out Delay		100		80		65	ns
10	TdRlr(DOz)	$\overline{RD}$, $\overline{IORQ}$ Rise to Data Out Float Delay		75		60		55	ns
11	ThRDr(D)	$\overline{M1}$,$\overline{RD}$,$\overline{IORQ}$ Rise to Data Float	15		15		15		ns
12	TsD(Cr)	Data in to Clock Rise Setup	30		25		22		ns
13	TdIOI(DO)	$\overline{IORQ}$ Fall to Data Out Delay (INTACK Cycle)[2]		95		95		95	ns
14	ThIOr(D)	$\overline{IORQ}$ Rise to Data Float (INTACK)	15		15		15		ns
15	THIOr(A)	$\overline{IORQ}$ Rise to Address Hold	15		15		15		ns
16	TsM1f(Cr)	$\overline{M1}$ Fall to Clock Rise Setup	40		40		40		ns
17	TsM1r(Cf)	$\overline{M1}$ Rise to Clock Fall Setup (M1 Cycle)	-15		-15		15		ns
18	TdM1f(IEOf)	$\overline{M1}$ Fall to IEO Fall Delay (Interrupt Immediately preceding M1 Fall)[3]		•		•		•	ns
19	TsIEI(IOf)	IEI to $\overline{IORQ}$ Fall Setup[3]		•		•		•	ns
20	TdIEIf(IEOf)	IEI Fall to IEO Fall Delay[3]		160		150		125	ns
21	TdIEIf(IEOr)	IEI Rise to IEO Rise Delay (after ED Decode)[3]		160		150		125	ns

Table 5. AC Characteristics of the Z84C90 (Continued)

			8MHz		10MHz[1]		12MHz		
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**U/M**
22	TsIEI(Cf)	IEI to Clock Fall Setup (for 4D Decode)	50		40		30		ns
23	TsIOr(Cf)	$\overline{IORQ}$ Rise to Clock Fall Setup (to activate $\overline{RDY}$ on next clock)	100		100				ns
PIO Timing									
24	TdCf(RDYr)	Clock Fall to $\overline{RDY}$ Rise Delay		100		100			ns
25	TdCf(RDYf)	Clock Fall to $\overline{RDY}$ Fall Delay		100		100			ns
26	TwSTB	$\overline{STB}$ Pulse Width	100		80				ns
27	TsSTBr(Cf)	$\overline{STB}$ Rise to Clock Fall Setup (to activate $\overline{RDY}$ on next clock cycle)	100		100				ns
28	TdIOf(PD)	$\overline{IORQ}$ Fall to Port Data Valid (Mode 0)		140		120			ns
29	TsPD(STBr)	Port A,B Data to $\overline{STB}$ Rise Setup Time (Mode 1)	140		75				ns
30	TdSTBI(PD)	$\overline{STB}$ Fall to Port A,B Data Valid Delay (Mode 2)		150		120			ns
31	TdSTBr(PDz)	$\overline{STB}$ Rise to Port Data Float Delay (Mode 2)		140		120			ns
32	TdPD(INTf)	Port Data Match to $\overline{INT}$ Fall Delay (Mode 3)		250		200			ns
33	TdSTBr(INTf)	$\overline{STB}$ Rise to $\overline{INT}$ Fall Delay		290		220			ns
34	TsPD(RIf)	PIA Port Data to $\overline{RD}$, $\overline{IORQ}$ Fall Setup	TBD		TBD				–
35	TdCr(PD)	Clock Rise to Port Data Valid Delay		80		80			ns
CTC Timing									
36	TdCr(INTf)	Clock Rise to $\overline{INT}$ Rise Delay	TcC+100		TcC+80				ns
37	TsCTRr(Cr)c	CLK/TRG Rise to Clock Rise Setup (for immediate count, Counter mode)	90		90				ns
38	TsCTRr(Cr)t	CLK/TRG Rise to Clock Rise Setup (for enabling prescaler on following Clock Rise, Timer mode)	90		90				ns

Table 5. AC Characteristics of the Z84C90 (Continued)

			8MHz		10MHz[1]		12MHz		
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**U/M**
39	TdCTRr(INTf)	CLK/TRG Rise to INT Fall Delay TsCTRr(Cr) satisfied TsCTRr(Cr) not satisfied	(36)+(38) (1)+(36)+(38)		(36)+(38) (1)+(36)+(38)				
40	TcCTR	CLK/TRG Cycle Time[4]	(2TcC)	DC	(2TcC)	DC			ns
41	TwCTRh	CLK/TRG Width High	90	DC	90	DC			ns
42	TwCTRl	CLK/TRG Width Low	90	DC	90	DC			ns
43	TrCTR	CLK/TRG Rise Time		30		30			ns
44	TfCTR	CLK/TRG Fall Time		30		30			ns
45	TdCr(ZCr)	Clock Rise to ZC/TO Rise Delay		80		80			ns
46	TdCf(ZCf)	Clock Fall to ZC/TO Fall Delay		80		80			ns
SIO Timing									
47	TdIOf(W/Rf)	$\overline{IORQ}$ Fall to $\overline{WT}$/$\overline{RDY}$ Fall Delay (Wait Mode)		130		110			ns
48	TdCr(W/Rf)	Clock Rise to $\overline{WT}$/$\overline{RDY}$ Delay (Ready Mode)		85		85			ns
49	TdCf(W/Rz)	Clock Fall to $\overline{WT}$/$\overline{RDY}$ Float Delay (Wait Mode)		90		80			ns
50	TwPh	Pulse Width High	150		120				ns
51	TwPl	Pulse Width Low	150		120				ns
52	TcTxC	$\overline{TxC}$ Cycle Time	250	DC	200	DC			ns
53	TwTxCh	$\overline{TxC}$ Width High	85	DC	80	DC			ns
54	TwTxCl	$\overline{TxC}$ Width Low	85	DC	80	DC			ns
55	TrTxC	$\overline{TxC}$ Rise Time		60		60			ns
56	TfTxC	$\overline{TxC}$ Fall Time		60		60			ns
57	TdTxCf(TxD)	$\overline{TxC}$ Fall to TxD Delay (x1 mode)		160		120			ns
58	TdTxCf(W/Rf)	$\overline{TxC}$ Fall to $\overline{WT}$/$\overline{RDY}$ Fall Delay (Ready Mode)[5]	5	9	5	9			ns
59	TdTxCf(INTf)	$\overline{TxC}$ Fall to $\overline{INT}$ Fall Delay[5]	5	9	5	9			ns
60	TcRxC	$\overline{RxC}$ Cycle Time	250	DC	200	DC			ns
61	TwRxCh	$\overline{RxC}$ Width High	85	DC	80	DC			ns
62	TwRxCl	$\overline{RxC}$ Width Low	85	DC	80	DC			ns

Table 5. AC Characteristics of the Z84C90 (Continued)

			8MHz		10MHz[1]		12MHz		
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**U/M**
63	TrRxC	$\overline{RxC}$ Rise Time		60		60			ns
64	TfRxC	$\overline{RxC}$ Fall Time		60		60			ns
65	TsRxD(RxCr)	RxD to $\overline{RxC}$ Rise Setup	0		0				ns
66	ThRxCr(RxD)	$\overline{RxC}$ Rise to RxD Hold Time	80		60				ns
67	TdRxCr(W/Rf)	$\overline{RxC}$ Rise to $\overline{W}$/$\overline{RDY}$ Fall Delay (Ready Mode)[5]	10	13	10	13			ns
68	TdRxCf(INTf)	$\overline{RxC}$ to $\overline{INT}$ Fall Delay[5]	10	13	10	13			ns
69	TdRxCr (SYNCf)	$\overline{RxC}$ Rise to $\overline{SYNC}$ Fall Delay (Output Mode)	4	7	4	7			ns
70	TsSYNCf (RxCr)	$\overline{SYNC}$ Fall to $\overline{RxC}$ Rise Setup (External Sync Mode)	-100		-100				ns
71	TdCf(IEOr)	Clock Fall to IEO Rise Delay		90		75			ns
72	TdCf(IEOf)	Clock Fall to IEO Fall Delay		110		90			ns
73	ThDI(M1r,Rdr)	Data Hold Time to $\overline{M1}$ Rise or $\overline{RD}$ Rise	0		0				ns
74	TsM1/RD(C)	Setup time for M1 and RD to clock Rising (with Data Valid)	20		20				

Notes:
1. Maximum SIO data rate is f(CLOCK) divided by 5.
2. For a Z80 CPU above 8 MHz, one Wait state is required to meet this parameter.
3. These daisy chain parameters include contributions from the PIO, SIO, and CTC cells, and vary slightly depending on how these are ordered by the KIO command register. See Table 5.
4. Counter mode only; when using a cycle time less than 3 TcC, parameter #37 must be met.
5. units are TcC.

Table 6.Daisy Chain Parameters

			8 MHz		10 MHz		12 MHz		
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**U/M**
18[1]	TdM1(IEO)	(PIO at #1)		160		150		125	ns
		(CTC at #1)		180		150		125	ns
		(SIO at #1)		230		200		200	ns

Table 6.Daisy Chain Parameters (Continued)

			8 MHz		10 MHz		12 MHz		
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**U/M**
19[2]	TsIEI (IO)	(PIO at #3)	170		140		115		ns
		(CTC at #3)	170		160		130		ns
		(SIO at #3)	180		160		130		ns
20[3]	TdIEI(IEOf)			160		150		125	ns
21[4]	TdIEI(IEOr)			160		150		125	ns

Notes: to calculate Z80 KIO daisy-chain timing, use the Z80 PIO, CTC, and SIO with I/O buffers on the chain. The following are calculation formulas:

1. Parameter 18: M1 falling to IEO delay TdM1(IEO) = TdM1(IO)#1 + TdIEI(IEO)#2 + TdIEI(IEO)#3 + Output Buffer Delay).
2. Parameter 19: IEI to IORQ falling setup time TsIEI(IO) = TdIEI(IEO)#1 + TdIEI(IEO)#2 + TdIEI(IEO)#3 + Input Buffer Delay).
3. Parameter 20: IEI falling delay = TdIEI(IEOf) - TdIEI(IEOf)PIO + TdIEI(IEOf)CTC + TdIEI(IEOf)SIO + (Input buffer Delay) + (Output Buffer Delay).
4. Parameter 21: IEI rising to IEO rising delay (after ED decode) - TdIEI(IEOr) = TdIEI(IEOr)PIO + TdIEI(IEOr)CTC + TdIEI(IEOr)SIO + ((Input buffer Delay) + (Output Buffer Delay).

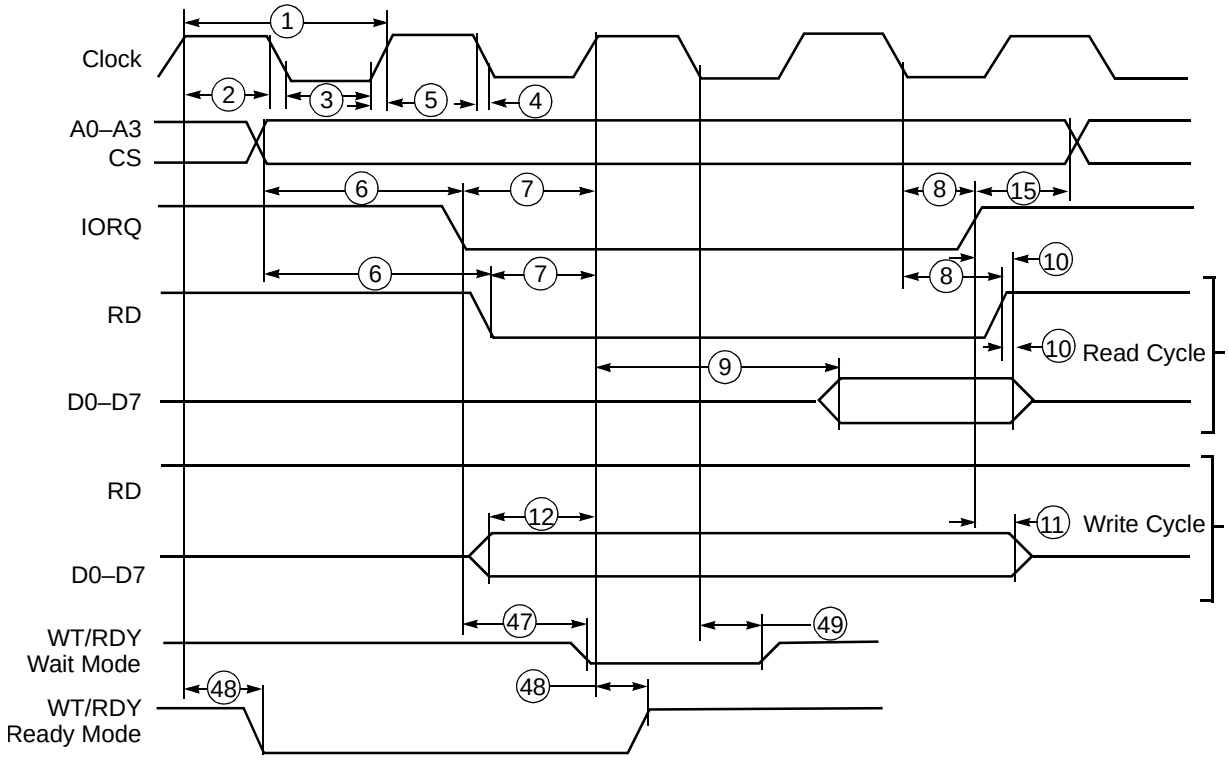

Figure 10. I/O Read/Write Timing (M1 = 1)

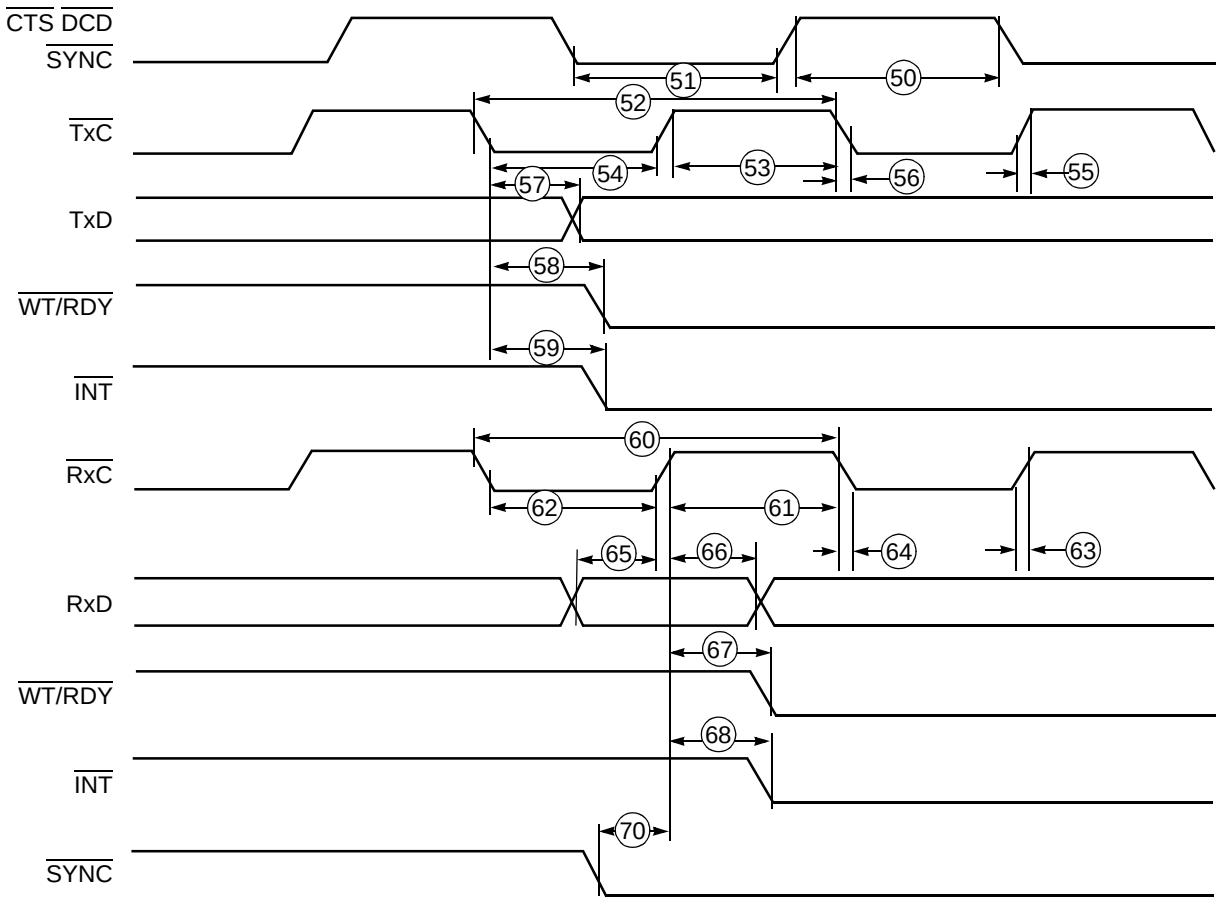

Figure 11. Serial I/O Timing

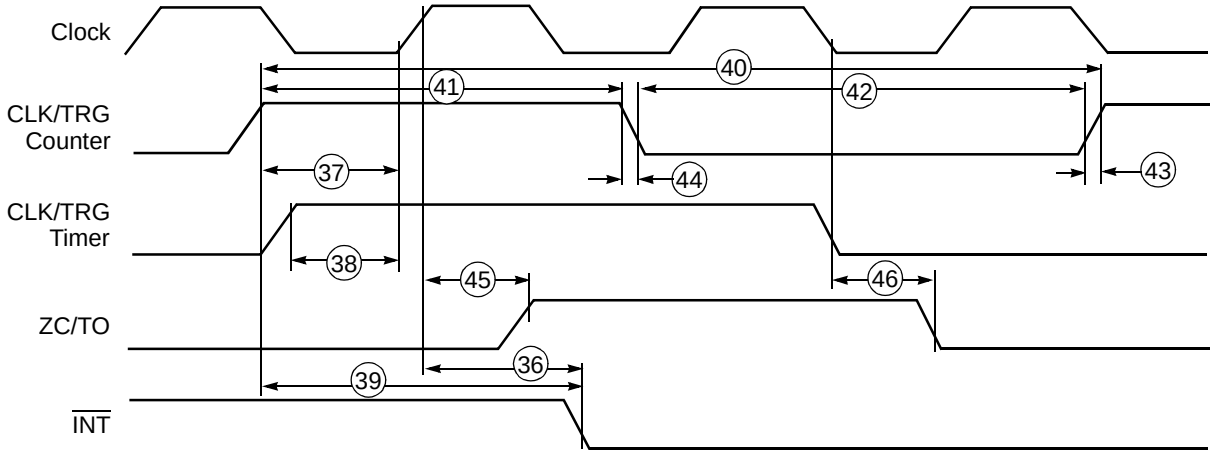

Figure 12. Counter/Timer Timing

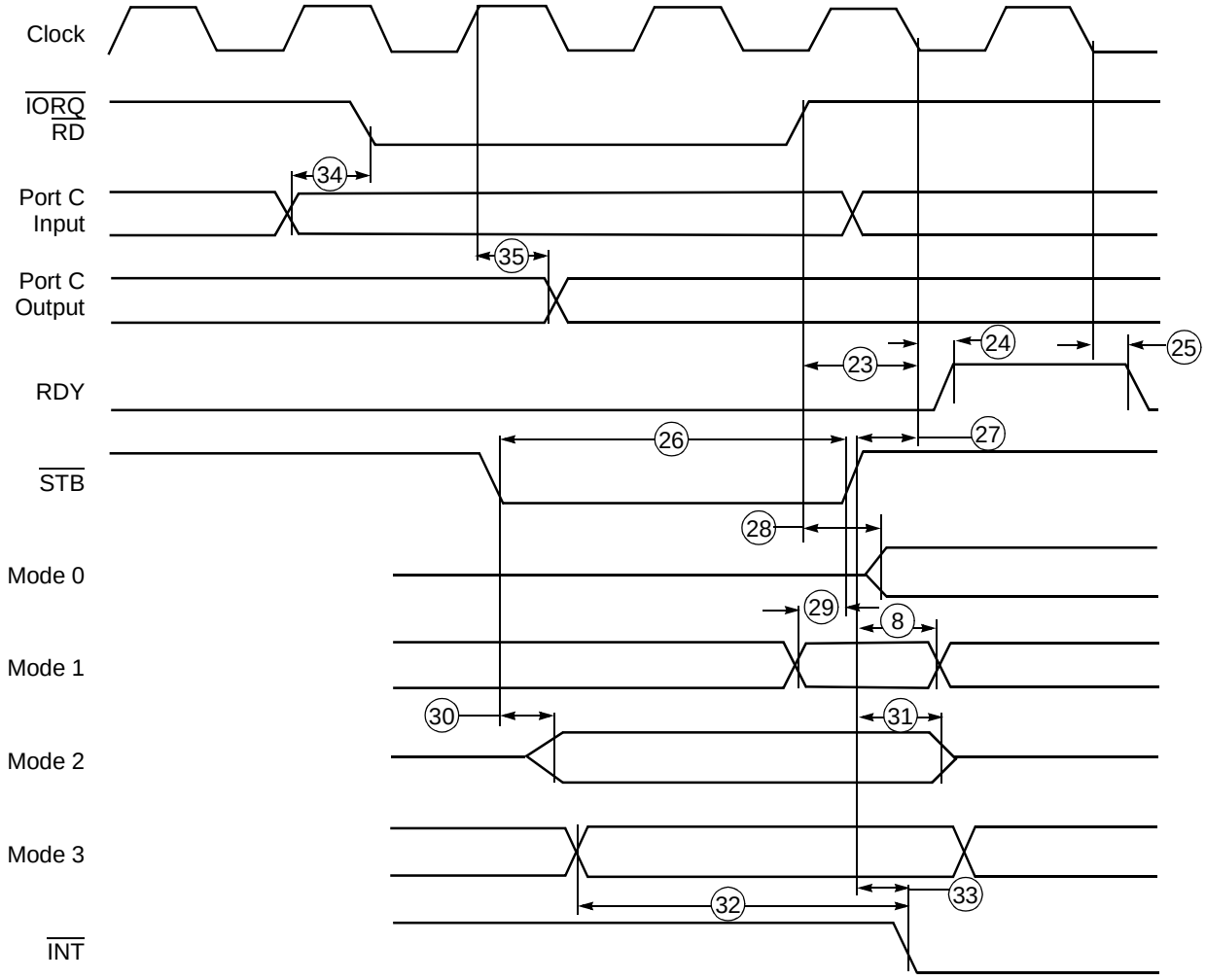

Figure 13. Port I/O Read/Write Timing

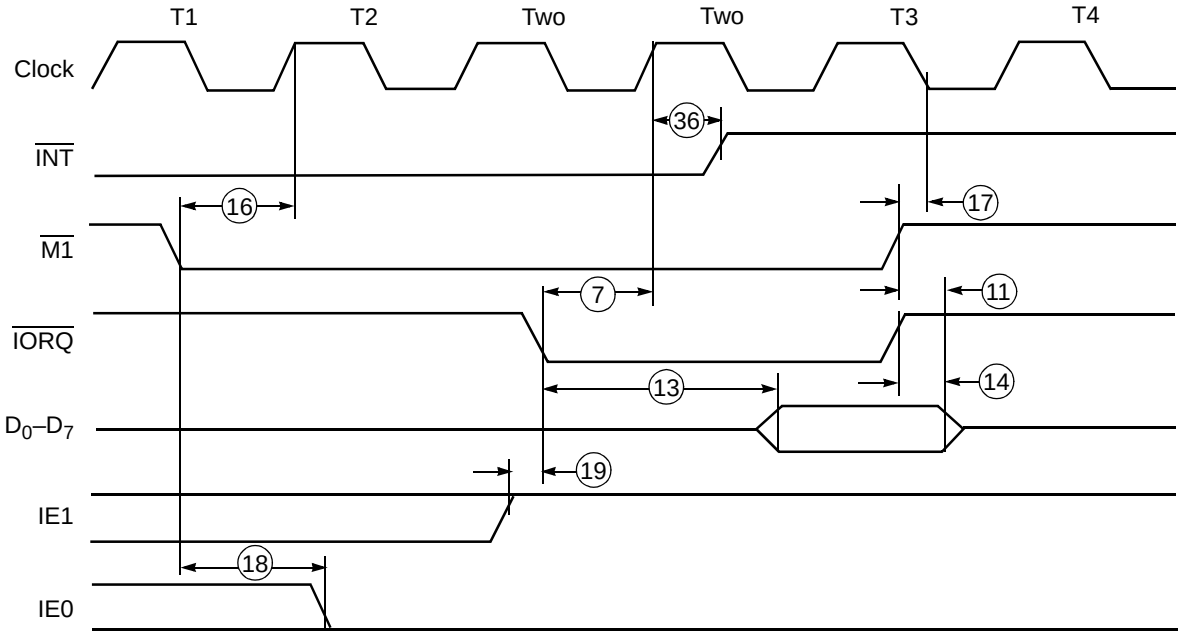

Figure 14. Interrupt Acknowledge Cycle

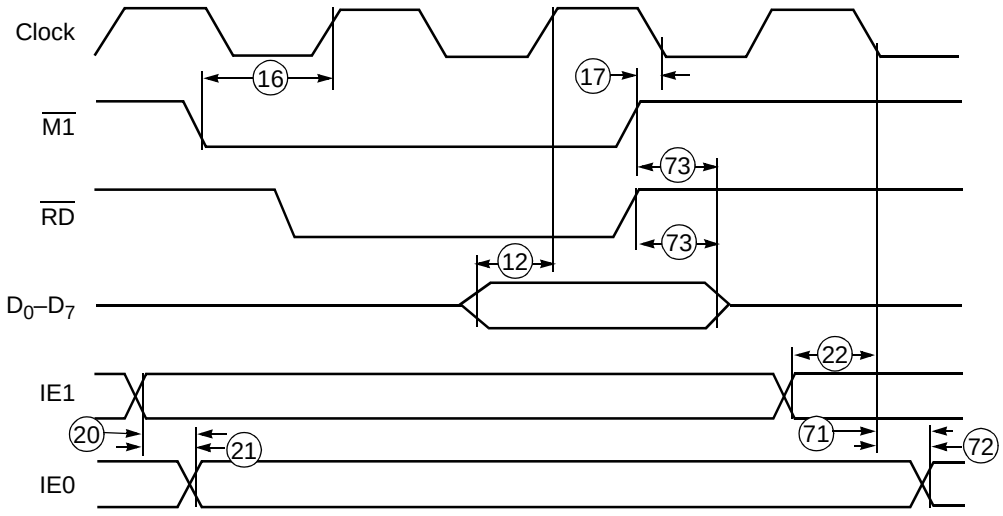

Figure 15. Op Code Fetch Cycle

Precautions & Limitations

The following describe the limitations of Revision A of the Z84C90 KIO.

Problem:

Daisy-chain. If the KIO has an Interrupt Pending during and Interrupt Acknowledge cycle, KIO misses the status of the IE1 pin. This produces vector contention if there is a higher interrupting device. It works fine if only one device is in the system.

Work Around:

There is no problem if the application has only one peripheral in the daisy chain. For two or more peripherals in the system, a "hardware workaround circuit" is needed. Please contact your local Zilog representatives to get more detailed information.

Problem:

Reset. KIO requires the $\overline{M1}$ signal to exit from Reset state. If the $\overline{M1}$ signal is not received, the KIO can not be programmed. This is not a problem for users of the Z80 CPU.

Workaround:

If the CPU is other than a Z80, an $\overline{M1}$ signal is needed to exit RESET status. Otherwise, the KIO can not be programmed.

Problem:

Port C. When Port C is used as Parallel I/O (not as SIO's modem signals) and there is a status change on PC1 or PC6, the status of $\overline{SYNCA}$ or $\overline{SYNCB}$ (SIO cell) also changes.

Work Around:

Before using Port C as a parallel port, set the SIO modem signal mode back to Port C. This procedure avoids the problem.

Problem:

Interrupt Acknowledge cycle. The KIO modifies the contents of the KIO control register (specifically, the KIO modifies the daisy-chain configuration) if the $\overline{CE}$ pin is active during the Interrupt Acknowledge cycle (with other conditions satisfied).

Work Around:

This problem could happen under the following narrowly defined conditions:

- $\overline{CE}$ signal is active throughout the Interrupt Acknowledge cycle.
- The address on the bus, A3–A0, is “110b”.
- During this time, bit D3 is 1.
- At the end of the Interrupt Acknowledge cycle, M1 goes inactive prior to the $\overline{IORQ}$ signal.
- At the time period of $\overline{CE}$ active, $\overline{IORQ}$ active, and $\overline{M1}$ returns to the inactive state; all during the rising edge of the clock.

This problem is not the case with the Z80 CPU. However, other CPUs could be affected. One of the possible workarounds is to add the condition *$\overline{M1}$ not active* to generate a $\overline{CE}$ signal.