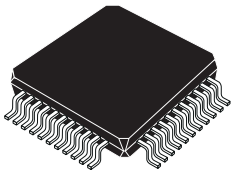
TDA7501

Line driver for digital car radio Signal processor (DSPLD)

Features

- Inputs:
  - Quasi differential stereo input for CD
  - Differential stereo inputs for phone, navigation, FM, AM
  - Single-ended input for cassette- four independent input multiplexer and gain stages
  - Envelope-detector for AM noise-blanking
  - Mixing of phone and navigation
  - DC connection to DSP
  - Dual MPX inputs
- Outputs:
  - 6 Output channels with independent volume control
  - 4 Main output channels with additional input selector for phone and/or navigation or CD
  - Outputs level up to 4V rms
  - AC connection from DSP
- Digital control:
  - SPI bus or I^2C bus interface (selectable)
  - Direct mute for the output stages and/or high impedance mpx mute



LQFP44

Description

The line driver handles all analog input and output signals for the digital car radio signal processor TDA7501. The device contains four independent input multiplexers to select the sources for the DSP's four AD converters. Four additional gain stages allow an adaptation to run the ADCs in best S/N condition.

The six outputs have independent volume stages with a large dynamic range. Using a 12V supply the outputs are able to drive up to 4Vrms .

Order codes

Part number	Package	Packing
TDA7501	LQFP44 (10 x 10 x 1.4 mm)	Tray
TDA7501TR	LQFP44 (10 x 10 x 1.4 mm)	Tape and Reel

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1 Block diagram and pin connections

Figure 1. Block diagram

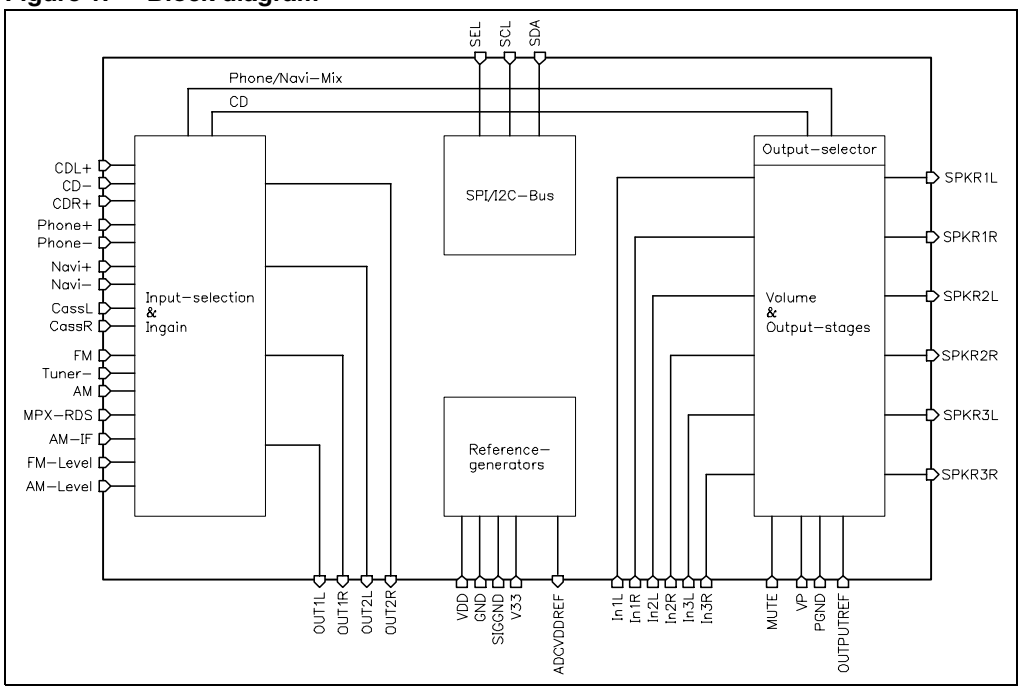
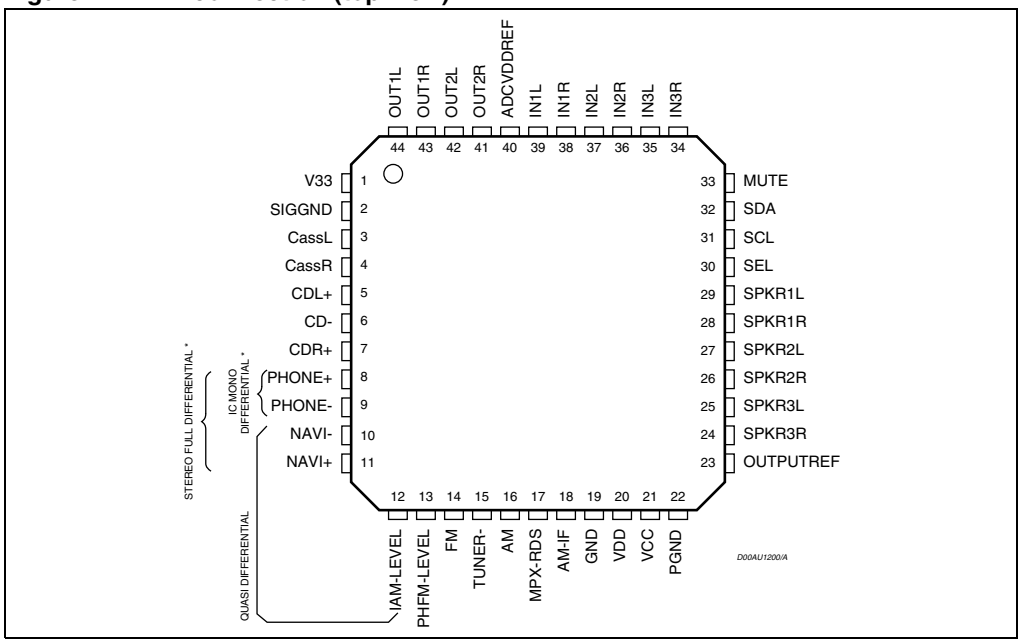


Figure 2. Pin connection (top view)



2 Electrical specifications

Table 1. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{dd}	Supply voltage		7.5	8.3	10	V
V_P	Output supply voltage			12		V
I_{S8}	Supply current V_{dd}	V_{dd} = 8.3V		27		mA
I_{S12}	Supply current V_P	V_P = 12V		5		mA
SVRR	Ripple rejection @ 1kHz			60		dB

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DDmax}	Operating supply voltage V_{DD}	10.5	V
V_{Smax}	Operating supply voltage V_s	13.0	V
Ta_{mb}	Operating temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins Max.	65	°C/W

ESD:

All pins are protected against ESD according to the MIL883 standard.

Table 4. Electrical characteristcs
(V_{DD} = V_S = 8.3V; V_{33} = 3.3V T_{amb} = 25°C; R_L = 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General						
V_{CL}	Input clipping level			2.3		V_{RMS}
S_{IN}	Input separation		80	100		dB
$G_{IN\ MIN}$	Min. input gain - input part			0		dB
$G_{IN\ MAX}$	Max. input gain - input part			15		dB
	Max. input gain - output part	Volume 0dB		12		dB
G_{STEP}	Step resolution			1		dB
V_{DC}	DC steps	Adjacent gain steps		0.5		mV
		GMIN to GMAX		5		mV
d_{IN}	Distortion	V_{OUT} = 0.7V_{RMS} all stages 0dB		0.002	0.08	%

Table 4. Electrical characteristcs (continued)
(V_{DD} = V_S = 8.3V; V_{33} = 3.3V T_{amb} = 25°C; R_L = 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DCout}	Output DC-voltage	pins 41..44		1.65		V
R_{out}	Output impedance OUT1L, 1R	pins 43..44		300		W
	Output impedance OUT2L, 2R	pins 41..42		3		kΩ
Quasi differential CD stereo input (non inverting)						
R_{in}	Input resistance (see Fig. 2)	Differential	70	100	130	kΩ
CMRR	Common mode rejection ratio	V_{CM} = $1V_{RMS}$ @ 1kHz	45	70		dB
		V_{CM} = $1V_{RMS}$ @ 10kHz	45	60		dB
V_N	Output noise	20Hz - 20kHz; unweighted		2.0		µV
Differential phone/navigation/FM/AM input (inverting)						
R_{in}	Input resistance (see Fig. 3)		35	50	65	kΩ
CMRR	Common mode rejection ratio	V_{CM} = $1V_{RMS}$ @ 1kHz	40	70		dB
		V_{CM} = $1V_{RMS}$ @ 10kHz	40	60		dB
V_N	Output noise	20Hz - 20kHz; unweighted		2.0		µV
AM IF input						
R_{in}	Input resistance		35	50	65	kΩ
Cassette input (non inverting)						
R_{in}	Input resistance		70	100	130	kΩ
V_N	Output noise	20Hz - 20kHz; unweighted		2.0		µV
AM/FM level input						
R_{in}	Input resistance		70	100	130	kΩ
V_{min}	Minimum input voltage		-0.4			V
Vmax	Maximum input voltage				7.0	V
Dual MPX control (pin tuner-)						
$V_{CTRLMPX1}$	Control voltage for MPX 1+2	MPX1 -> MPX1 + MPX2		1.5		V
$V_{CTRLMPX2}$	Control voltage for MPX2	MPX1 + MPX1 -> MPX2		4.0		V
$V_{CTRLMPX3}$	Control voltage for MPX 1+2	MPX2 -> MPX1 + MPX2		3.5		V
$V_{CTRLMPX4}$	Control voltage for MPX1	MPX1 + MPX2 -> MPX2		1.0		V
Speaker outputs RLOAD = 10KW (AC)						
R_{in}	Input impedance		35	50	65	kΩ
G_{MAX}	Max. gain	external reference mode		33		dB

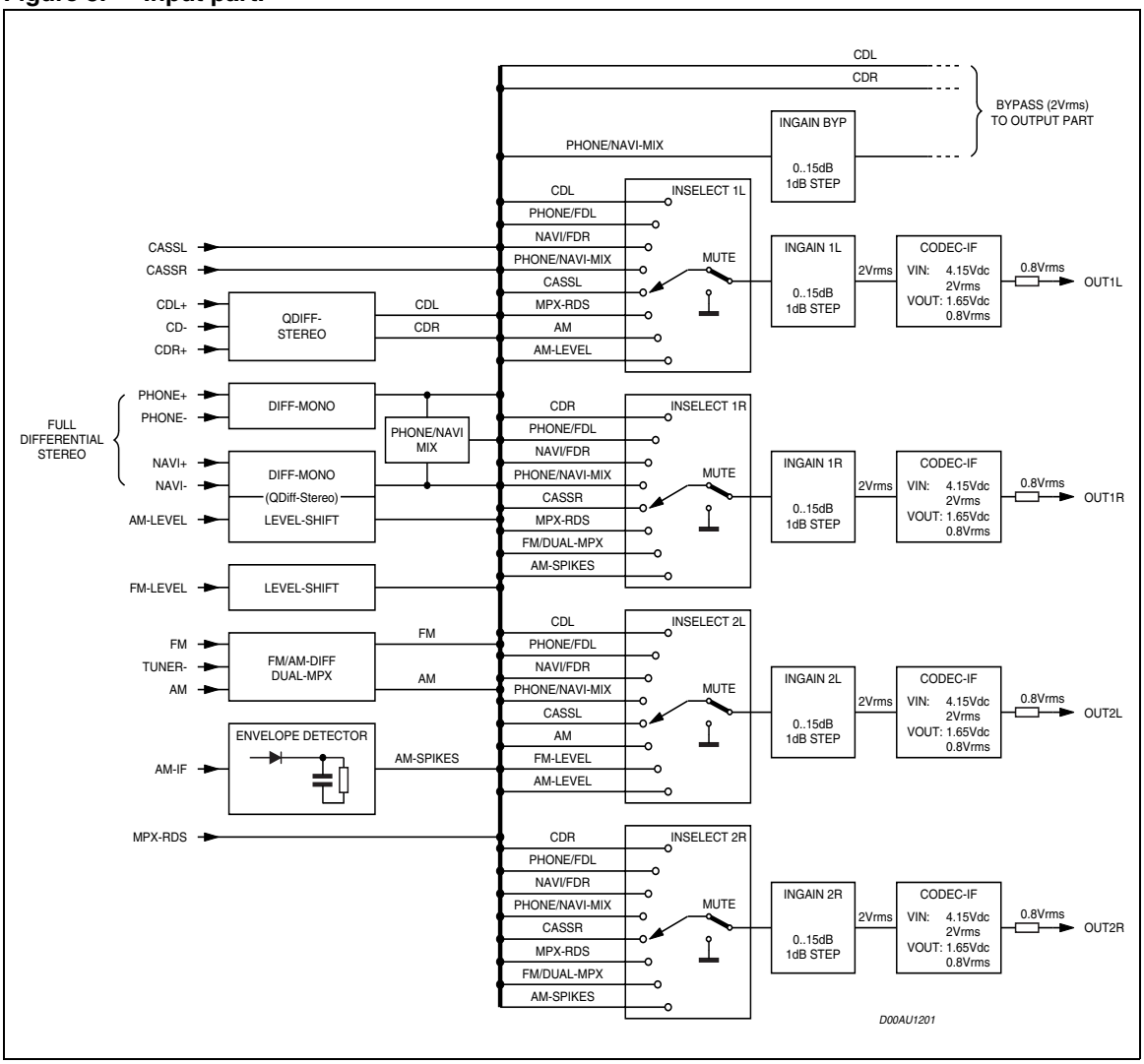
Table 4. Electrical characteristcs (continued)
(V_{DD} = V_S = 8.3V; V_{33} = 3.3V T_{amb} = 25°C; R_L = 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ATT_{MAX}	Max. attenuation	internal reference mode		-73		dB
ATT_{STEP}	Step resolution			1		dB
ATT_{MUTE}	Output mute attenuation		80	100		dB
E_E	Attenuation set error	from +15 to -40dB			2	dB
V_{DC}	DC steps	Adjacent attenuation steps		0.3	3	mV
V_{DCOUT}	Output DC voltage	internal reference mode		4.15		V
		external reference mode		outref		V
V_{CLIP}	Output clipping level	d = 0.3%, V_{CC} = V_{DD} = 8.3V gain = 0dB gain = 6dB		2.3 2.8		V_{RMS} V_{RMS}
		d = 0.3%, V_{CC} = 12V V_{DD} = 8.3V gain = 6dB		4		V_{RMS}
R_L	Output load resistance	AC coupled	5			kΩ
C_L	Output load capacitance				10	nF
R_{OUT}	Output impedance			40	120	W
V_N	Output noise	BW = 20Hz-20kHz muted0dB muted 6dB gain = 0dB gain = 6dB		3.0 7.5 10 13		µV µV µV µV
S/N	Signal to noise ratio	BW = 20Hz-20kHz V_O = $2V_{RMS}$ V_O = $4V_{RMS}$		106 110		dB dB
d_{out}	Distortion	V_{OUT} = $1V_{RMS}$; all stages 0dB		0.005	0.08	%
S_C	Channel separation left/right		80	100		dB
X	Crosstalk		80	100		dB
ADCVDDREF (CODEC reference)						
I_{maxadc}	Max. output current	pin 40			5	mA
BUS INPUTS						
V_{low}	Voltage for logic "0	"inputs SEL, SCL,SDA,MUTE			0.8	V
V_{high}	Voltage for logic "1	"inputs SEL, SCL,SDA,MUTE	2.4			V
V_{th_SPI}	SPI_mode threshold voltage	i	0		V_{DD}-1.8	V

3 Description of the input part

On the input side, the TDA7501 (see *Figure 3*) connects the external audio and tuner signals to the four AD converters of the digital car radio signal processor TDA7500. The audio signals are adjusted by the input gain stage to the internal reference signal with 2V rms referred to 4.15V (=V33 ·1.2575). The following CODEC interface attenuates the $2V_{RMS}$ to 0.8Vrms referred to the CODEC's reference voltage of 1.65V which allows a DC coupling to the TDA7500.

Figure 3. Input part.



3.1 Input Stages

The device offers several input stages for the different signals which have to be handled by the system. A quasi differential input (see *Figure 4*) can be used for (external) CD changer. The two mono differential inputs allow the connection of phone & navigation (see *Figure 5*) or it could be used as fully differential stereo input. Additionally a single-ended stereo input is available for Cassette applications. The lower part of the input section is dedicated to the tuner signals. Another quasi differential input (see *Figure 6*) is used to connect AM and FM referred to the tuner reference (Tuner). This concept supports also double tuner systems. Also two seperate level inputs are present which are followed by level-shifters to allow the use of the TDA7500's ADCs. For AM noise blanking an envelope detector driven by the AM IF is also available.

Figure 4. Quasi differential input-stage.

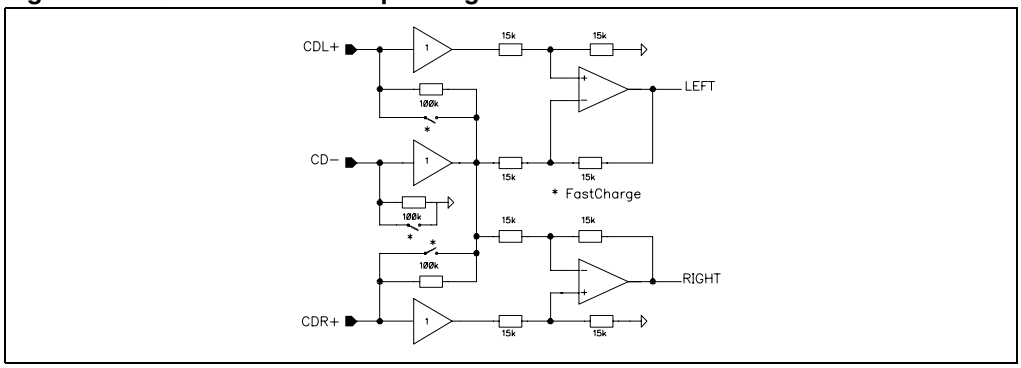


Figure 5. Mono differential input-stage.

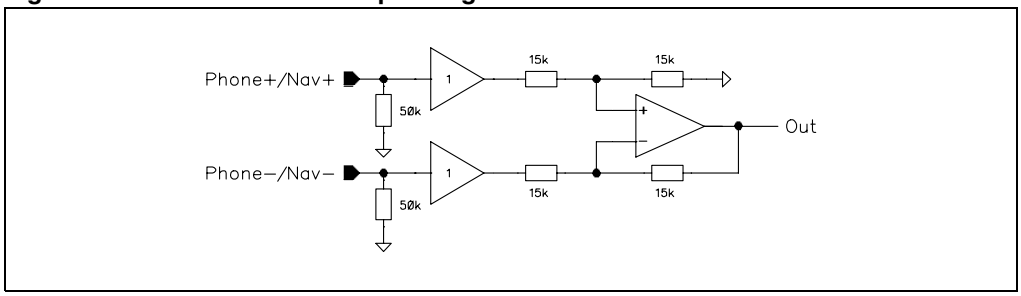
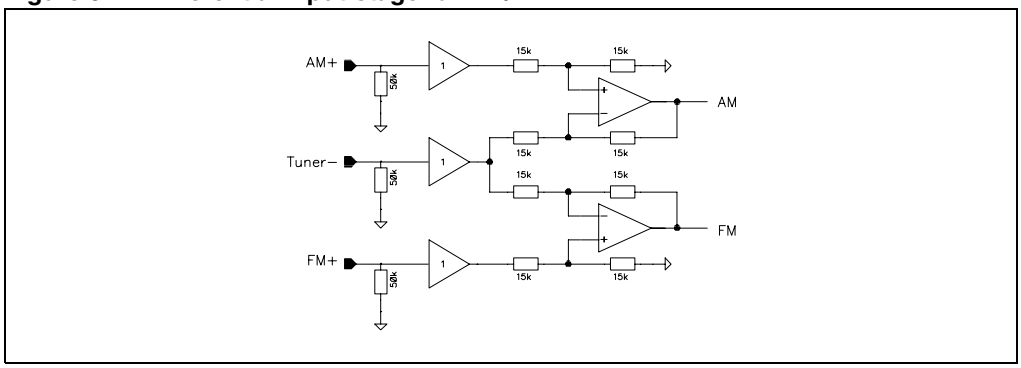


Figure 6. Differential input-stage for AM/FM.



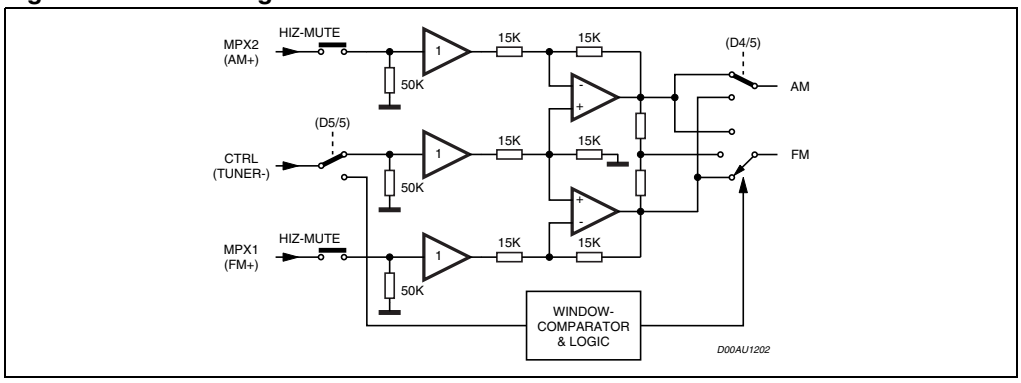
3.2 Dual MPX mode

The TDA7501 is able to support a twin tuner concept via the Dual MPX Mode. In this configuration the FM pin and the AM-pin are acting as MPX1 and MPX2 inputs. The DC Voltage at the TUNER pin controls whether MPX1, both MPX signals or MXX2 is used to decode the stereo FM signal (see *Figure 6* Please note that the thresholds have a hysteresis of 500mV. During this mode the high ohmic mute acts on both inputs in parallel.

Furthermore, a background tuner on the internal AM path can be selected by software aswtching to one of the two MPX inputs.

For the programming of the Dual MPX Mode see the programming section.

Figure 7. Block diagram Dual MPX.

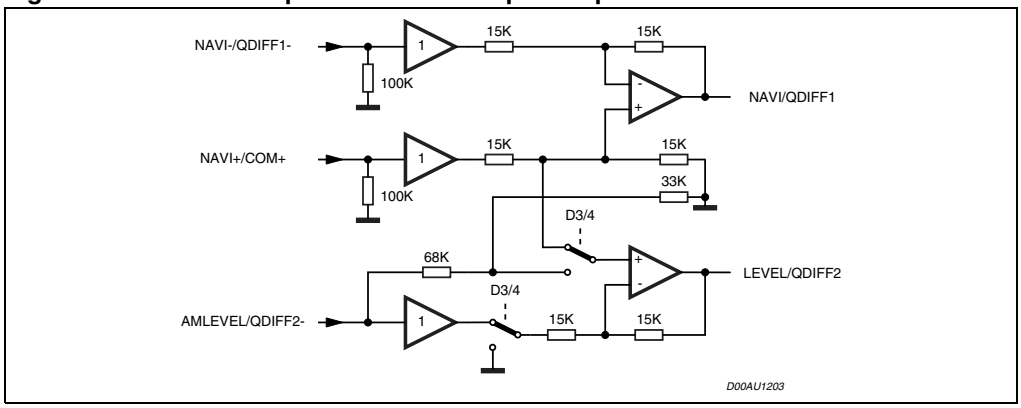


3.3 Additional quasi differential Input

The TDA7501 can be programmed to additional quasi-differential input by rearranging the configuration of the navigation and AM level inputs. Since the AM level input becomes the 2nd differential input, the level shift function is not available.

For the programming of the navigation/AM level input configuration see the programming section.

Figure 8. Additional quasi differential input simplified



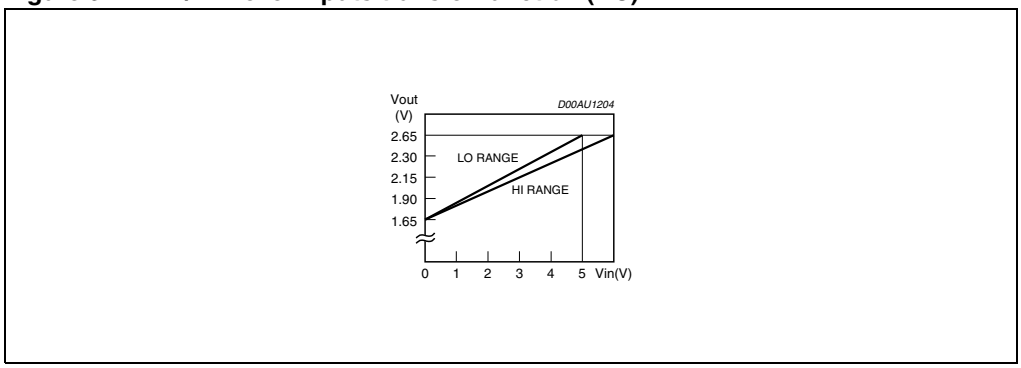
3.4 Transfer function of the AM/FM level inputs

In the TDA7501 two level shift stages convert a tuner level (DC) signal to a unipolar output signal with respect to the Codec Interface reference, that is 1.65V.

The FM level input can be programmed to a signal range of either 0 to 5V (Lo range) which is the default, or 0 to 6V (Hi range). The AM level input is fixed to the lower 0 to 5V input range.

For the programming of the FM level input range see the programming section.

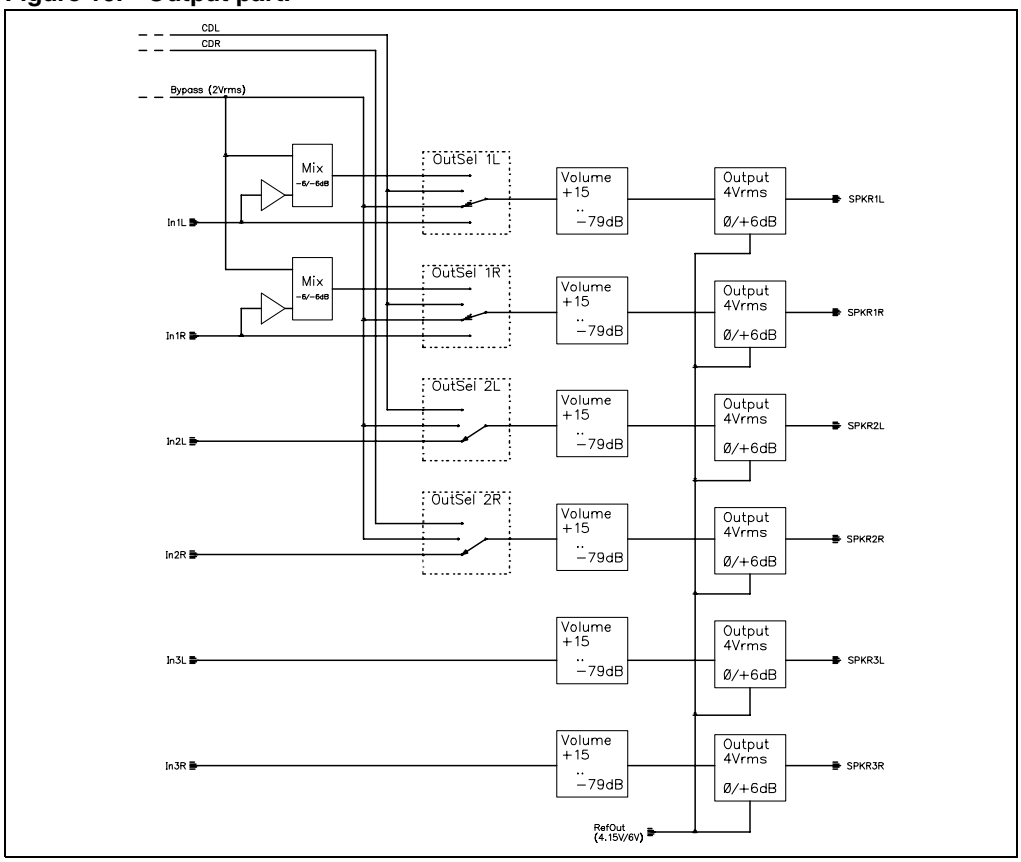
Figure 9. AM/FM level inputs transfer function (DC)



4 Description of the output part

The TDA7501 has 6 independent outputstage with volume control. The first 4 (main) outputs have an input selector which allows to select besides the DAC outputs CD direct or Phone/Navigation-mix. In addition one can mix the SPKR1 with Phone/Navigation so that traffic or navigation announcements can bypass the DSP (see figure 8).
The TDA7500 CODEC outputs have a maximum output voltage of 0.5Vrms . To obtain 4Vrms , (in the dual supply mode only) the signal is first amplified to have a reference amplitude of 2V rms. The following volume stage offers up to 15dB gain which gives along with the programmable 6dB gain in the output-stage enough overdrive capability. To achieve the maximum output swing of 4Vrms the device must be supplied with an additional supply of 12V. With a single supply (V_{dd} = V_{CC} = 8.3V) 2.8Vrms are obtained at the output at maximum.

Figure 10. Output part.

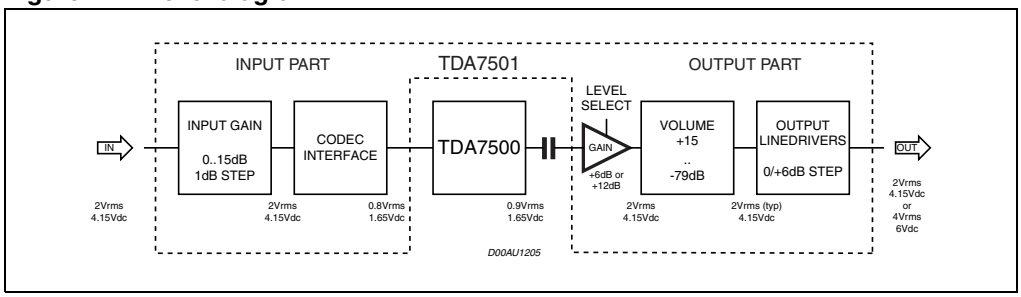


4.1 Overall gain structure

The overall gain structure of the TDA7501 can be shown in its target application together with the V225.

The output part in level select (D6/4) offers an additional adaption to the DSP's output level

Figure 11. Level diagram.



4.2 Speaker (linedriver) outputs

The Speaker outputs can be configured in three different operating modes:

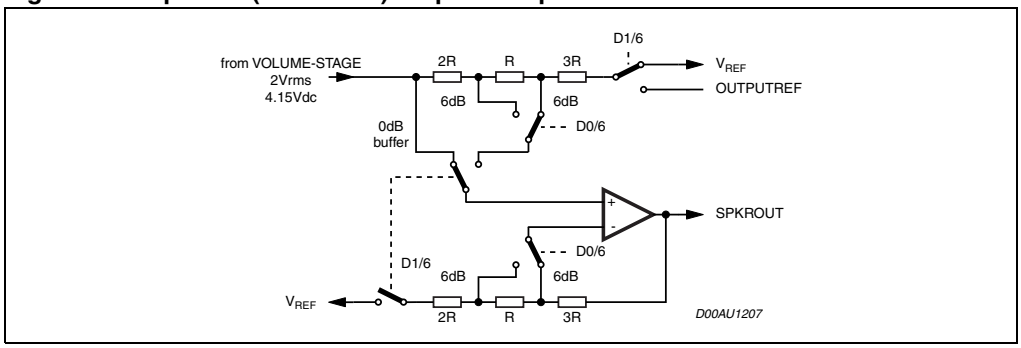
1. - Internal reference mode with 0dB output gain,
2. - External reference mode with 0dB output gain
3. - External reference mode with 6dB output gain

Basically, in the internalreference mode the linedriver amplifier acts as a buffer with 0dB gain regardless of the output gain programmed by bit D0. Since the buffer tracks the internal generated reference, the OUTPUTREF pin may be left floating.

In the external reference mode the linedriver amplifiers reference tracks the voltage present at the OUTPUTREF pin. This reference does not necessary have to be external to the device, it can also be generated by invoking the VCC/2 divider inside the TDA7501 (bit D1/6). In practice, the term external reference implied that the OUTPUTREF pin at least has to connect to an external capacitor. In the external reference mode, an additional gain of 6dB can be added by assessing bit D0. This provides a nominal $4V_{RMS}$ output level in case the TDA7501 is powered from a dual supply (V_{DD} = 8.3V). When fed from a single supply, only $2.8V_{RMS}$ output level can be acheived.

For the programming of output gain and reference selection see the programming section.

Figure 12. Speaker (Linedriver) outputs simplified



5 Reference concept

For the input section the TDA7501 generates the internal reference voltage by multiplying the V33 voltage by 1.2575.

The V33 voltage is also buffered and fed back to the CODEC where it is used to generate all necessary references. For best performance it is recommended to filter the V33 reference pin by means of a passive second order lowpass as shown in *Figure 13*. This concept allows a direct DC coupling between the TDA7501 and the DSP because of the accurate matching of DC levels. On the output side the TDA7501 offers two main modes: a single supply and a dual supply mode.

5.1 Dual supply mode

In this mode the outputs are able to provide up to 4V rms with a minimum supply V_{CC} of 12V as well as a output reference voltage set to half of V_{CC} (bit D0 of the mode select byte set to '1').

If the switch D1/byte mode select is open the output reference voltage must be defined externally e.g. a zener diode with RC lowpass.

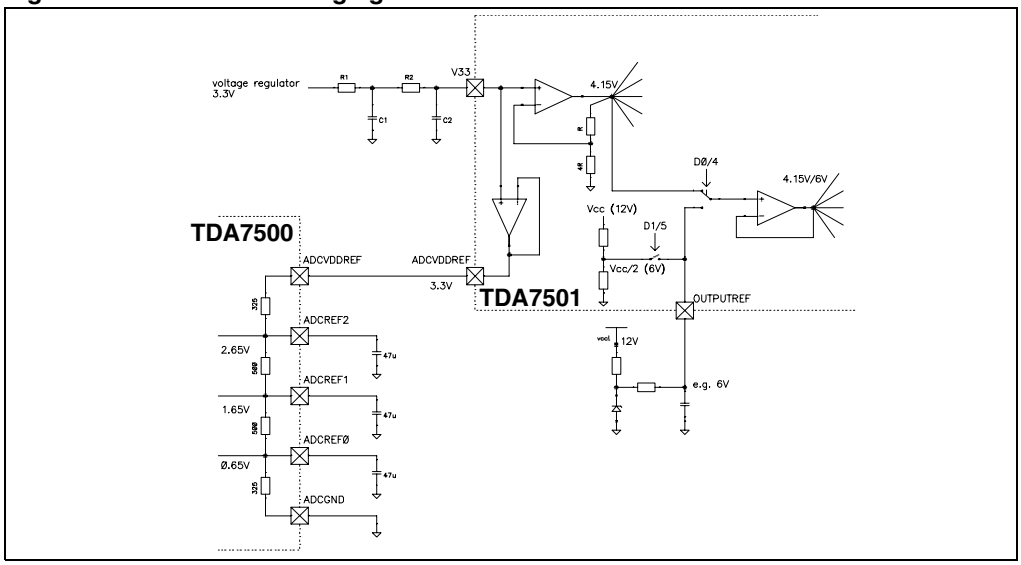
If the switch is closed the reference voltage will be half of V_{CC} and only an external capacitor has to be added.

5.2 Single supply mode

If V_{CC} and V_{dd} are connected to a single supply the maximum possible output swing is about 2.8V rms .

The output reference voltage pin can be left open or otherwise the internal voltage divider can be used to generate for the outputs a $V_{CC}/2$ reference.

Figure 13. Reference voltage generation



6 Digital interface

The TDA7501 digital interface offers two different protocols: SPI and I2C.

To select I2C-mode the SEL-pin has to beconnected to VDD. If the voltage at the SEL-pin is more than about 1V below the VDD voltage the interface switches to SPI-mode.

In both cases the interface is able to work with a 3.3V microprocessor as well as with a 5V microprocessor. For details of both protocols refer to the programming section.

7 SPI bus mode

7.1 Interface protocol

The TDA7501 SPI interface protocol comprises :

- a subaddress and
- a sequence of n databytes

each consisting of 8 bits (see *Figure 14*).

The interface accepts both a positiv (Cpol = 1, Cpha = 1) as well as a negativ (Cpol = 0, Cpha = 0) clocking scheme. However, the data transmitted has to be valid on the rising edges of the serial clock SCL.

Figure 14. Timing diagram for the SPI bus mode.

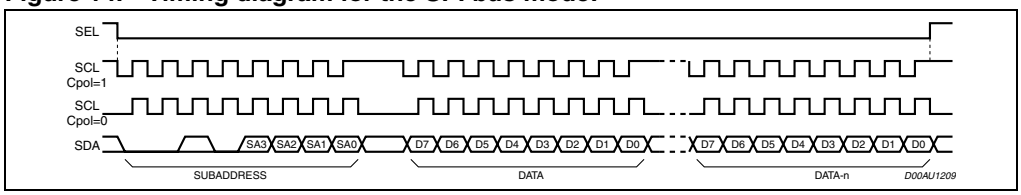
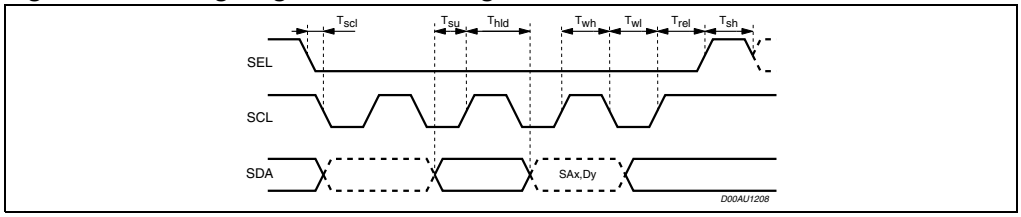


Table 5. Switching characteristics (SPI mode)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCLK}	Serial input clock frequency (SCL)	0		4.0	MHz
T_{su}	Serial data setup time	40			ns
T_{hld}	Serial data hold time	40			ns
T_{wh}	Serial clock high time width	100			ns
T_{wl}	Serial clock low time width	100			ns
T_{scl}	Select (SEL) to select (SCL) falling setup time	200			ns
T_{rel}	Select (SCL) to select (SEL) rising release time	200			ns
t_r	Data rise time			2	ms
t^f	Data fall time			2	ms
T_{sh}	Chip select high time	200			ns

Figure 15. Timing diagram for switching characteristic

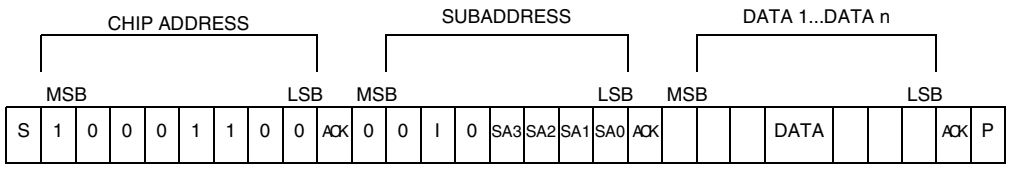


8 I²C bus mode

8.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (write mode only)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)



ACK = Acknowledge
S = Start
P = Stop

9 Software specification for both modes

9.1 Auto increment

If bit I in the subaddress byte is set to "1", the autoincrement of the subaddress is enabled.

9.2 Reset condition

A Power-On-Reset is invoked if the Supply-Voltage V dd is below than 3.5V. After POR the following data is written automatically into the registers of all subaddresses :

MSB							LSB
1	1	1	1	1	1	1	0

The programming after POR is marked bold-face in the programming tables.

With this programming all the outputs are muted to their corresponding reference voltages.

9.3 Programming modes

Table 6. Subaddresses

MSB							LSB	Name
D7	D6	I	D4	SA3	SA2	SA1	SA0	
				0	0	0	0	Input selector 1L
				0	0	0	1	Input selector 1R
				0	0	1	0	Input selector 2L
				0	0	1	1	Input selector 2R
				0	1	0	0	Phone/Navigation
				0	1	0	1	Mode Select
				0	1	1	0	Configuration
				0	1	1	1	Output selector
				1	0	0	0	Volume 1L
				1	0	0	1	Volume 1R
				1	0	1	0	Volume 2L
				1	0	1	1	Volume 2R
				1	1	0	0	Volume 3L
				1	1	0	1	Volume 3R
				1	1	1	0	FM-level
				1	1	1	1	reserved
		0 1						Autoincrement mode off Autoincrement mode on
0	0		0					must be "0"

Table 7. Input selector 1L..3R, bits D7 ..D3 (subaddresses 0..3)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								mute
				0				off
				1				**on**
								gain
0	0	0	0					15dB
0	0	0	1					14dB
0	0	1	0					13dB
0	0	1	1					12dB
0	1	0	0					11dB
0	1	0	1					10dB
0	1	0	0					9dB
0	1	1	1					8dB
1	0	0	0					7dB
1	0	0	1					6dB
1	0	1	0					5dB
1	0	1	1					4dB
1	1	0	0					3dB
1	1	0	1					2dB
1	1	0	0					1dB
1	**1**	**1**	**1**					**0**dB

Table 8. Input selector 1L, bits D2 ..D0 (subaddresses 0)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								source select
					0	0	0	CDL
					0	0	1	Phone/FDL
					0	1	0	Navigation/FDR
					0	1	1	Phone/Navigation mix
					1	0	0	CassL
					1	0	1	MPX-RDS
					1	**1**	**0**	**AM**
					1	1	1	AM-level

Table 9. Input selector 1R, bits D2 ..D0 (subaddresses 1)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								source select
					0	0	0	CDR
					0	0	1	Phone/FDL
					0	1	0	Navigation/FDR
					0	1	1	Phone/Navigation mix
					1	0	0	CassR
					1	0	1	MPX-RDS
					1	**1**	**0**	**FM** (or MPX1/MPX2 in Dual MPX mode)
					1	1	1	AM-spikes

Table 10. Input selector 2L, bits D2 ..D0 (subaddresses 2)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								source select
					0	0	0	CDL
					0	0	1	Phone/FDL
					0	1	0	Navigation/FDR
					0	1	1	Phone/Navigation mix
					1	0	0	CassL
					1	0	1	AM
					1	**1**	**0**	**FM-level**
					1	1	1	AM-level

Table 11. Input selector 2R, bits D2 ..D0 (subaddresses 3)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								source select
					0	0	0	CDR
					0	0	1	Phone/FDL
					0	1	0	Navigation/FDR
					0	1	1	Phone/Navigation mix
					1	0	0	CassR
					1	0	1	MPX-RDS
					1	**1**	**0**	**FM** (or MPX1/MPX2 in Dual MPX mode)
					1	1	1	AM-spikes

Table 12. Phone navigation (subaddress 4)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
								mix level phone/navigation
					0	0	0	0/mute
					0	0	1	-1.6dB/-15.5dB
					0	1	0	-3.6/-9.6dB
					0	1	1	-6/-6dB
					1	0	0	-9.6/-3.6dB
					1	0	1	-15.5/-1.6dB
					1	**1**	**0**	mute/0dB
					1	1	1	mute
				0				**Input configuration** quasidifferential input (no level shift function)
				1				**Navi & AM Level input**
								gain
0	0	0	0					15dB
0	0	0	1					14dB
0	0	1	0					13dB
0	0	1	1					12dB
0	1	0	0					11dB
0	1	0	1					10dB
0	1	0	0					9dB
0	1	1	1					8dB
1	0	0	0					7dB
1	0	0	1					6dB
1	0	1	0					5dB
1	0	1	1					4dB
1	1	0	0					3dB
1	1	0	1					2dB
1	1	0	0					1dB
1	**1**	**1**	**1**					**0**dB

Table 13. Mode select (subaddress 5)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								AM-IF rectifier gain
						0	0	18dB
						0	1	15.5dB
						1	0	12dB
						1	1	6dB
								AM-IF rectifier corner frequency
				0	0			14KHz
				0	1			18.5KHz
				1	0			28KHz
				1	**1**			56KHz
								backkground tuner select (internal AM-path)
			0					FM-in (MPX1)
			1					AM-in (MPX2)
								Dual MPX mode
		0						on (control through Tuner- - voltage)
		1						off
								forced Dual MPX mode
0	0							MPX1 (allows automatic selection)
0	1							MPX2 (overwrites automatic selection)
1	0							MPX1+ MPX2 (overwrites automatic selection)
1	1							MPX1 (overwrites automatic selection)

Table 14. Configuration (subaddress 6)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0	**output gain** **0dB**
							1	+6dB
						0		reference voltage setting for output external reference / internal reference (V33*1.25)
						1		
					01			internal divider for output reference voltage connected to VCC/2 disconnected
				01				fast charge (switches at CD input) open closed
			01					Input level select (output power)12dB6d0

Table 14. Configuration (subaddress 6) (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
		01						RDS-mute (high impedance)mutedunmuted
	01							mute pin function I"0" does not activate the output mute"1" activates the output mute
01								mute pin function II"0" activates the high impedance mute"1" does not activate the high impedance mute

Table 15. Output selector (subaddress 7)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								source select SPKR 1L
						0	0	Bypass
						0	1	CDL
						1	**0**	**Phone/Navigation mix / IN1L**
						1	1	IN1L
								source select SPKR 1R
				0	0			Bypass
				0	1			CDL
				1	0			Phone/Navigation mix / IN1RI
				1	**1**			**N1R**
								source select SPKR 2L
		0	0					Bypass
		0	1					CDL
		1	0					mute
		1	**1**					**IN2L**
								source select SPKR 2R
0	0							Bypass
0	1							CDL
1	0							mute
1	**1**							**IN2R**

Table 16. Volume speaker outputs (subaddresses 8...13)

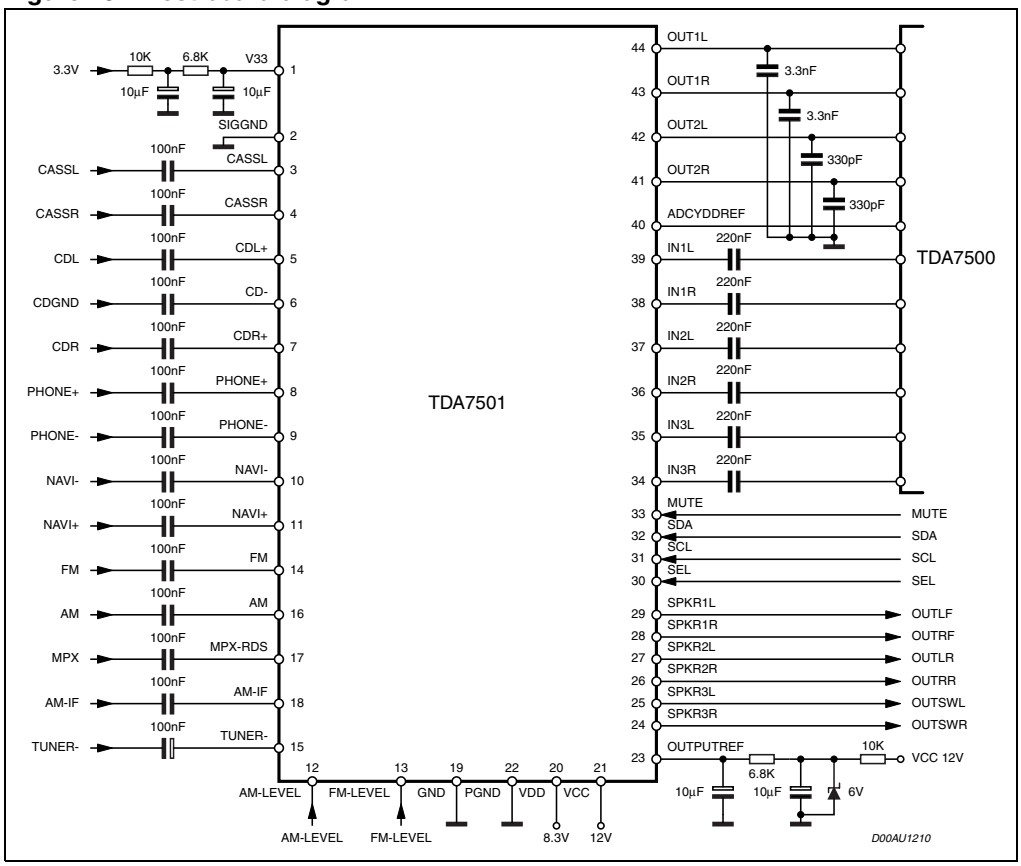
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1	0	0	0	1	1	1	1	+15dB
:	:	:	:	;	;	;	;	:
1	0	0	0	0	0	0	1	+1dB
1	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	1	-1dB
:	:	:	:	:	:	:	:	:
0	0	0	0	1	1	1	1	-15dB
0	0	0	1	0	0	0	0	-16dB
:	:	:	:	:	:	:	:	:
0	1	0	0	1	1	1	0	-78dB
0	1	0	0	1	1	1	1	-79dB
x	**1**	**1**	x	x	x	x	x	**Mute**

Table 17. FM level range (subaddress 14)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1	0	0	0	1	1			0...6Volts
						0		**0...5 Volts**
		:	:			**1**		
1	**1**	**1**	**1**	**1**	**1**		0	**Must be**

The unused subaddresses 14/15 must be programmed to "11111110" to allow software compatibility to future extensions.

Figure 16. Test board diagram



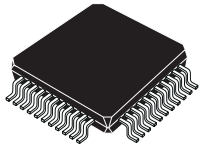
10 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

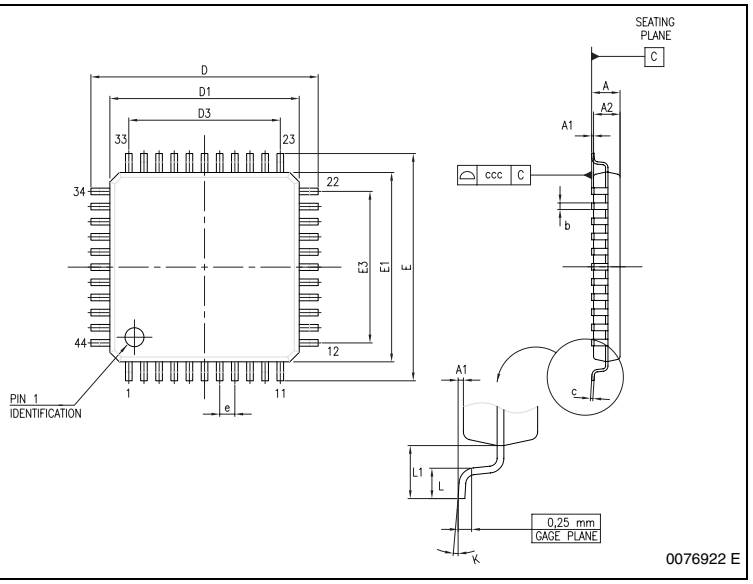
Figure 17. LQFP44 (10x10) mechanical data & package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					
ccc			0.10			0.0039

OUTLINE AND MECHANICAL DATA



LQFP44 (10 x 10 x 1.4mm)



11 Revision history

Table 18. Document revision history

Date	Revision	Changes
21-Jun-2004	1	Initial release.
22-Jun-2004	2	Minor revision, content edit.
9-Sep-2004	3	Minor revision, content edit.
15-Dec-2004	4	Minor revision, content edit.
17-Jan-2007	5	Package changed, layout change, text modifications

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