19-0147; Rev. 2; 6/98

MAXIM

Microprocessor and Non-Volatile Memory Supervisory Circuits

General Description

The MAX792/MAX820 microprocessor (µP) supervisory circuits provide the most functions for power-supply and watchdog monitoring in systems without battery backup. Built-in features include the following:

1) µP reset: Assertion of RESET and $\overline{RESET}$ outputs during power-up, power-down, and brownout conditions. $\overline{RESET}$ is guaranteed valid for V_{CC} down to 1V.
2) Manual-reset input.
3) Two-stage power-fail warning: A separate low-line comparator compares V_{CC} to a preset threshold 120mV above the reset threshold; the low-line and reset thresholds can be programmed externally.
4) Watchdog fault output: Assertion of $\overline{WDO}$ if the watchdog input is not toggled within a preset timeout period.
5) Pulsed watchdog output: Advance warning of impending $\overline{WDO}$ assertion from watchdog timeout that causes hardware shutdown.
6) Write protection of CMOS RAM, EEPROM, or other memory devices.

The MAX792 and MAX820 are identical, except the MAX820 guarantees higher low-line and reset threshold accuracy (±2%).

Applications

Computers
Controllers
Intelligent Instruments
Critical µP Power Monitoring

Features

- ♦ **Manual-Reset Input**
- ♦ **200ms Power-OK/Reset Time Delay**
- ♦ **Independent Watchdog Timer—Preset or Adjustable**
- ♦ **On-Board Gating of Chip-Enable Signals**
- ♦ **Memory Write-Cycle Completion**
- ♦ **10ns (max) Chip-Enable Gate Propagation Delay**
- ♦ **Voltage Monitor for Overvoltage Warning**
- ♦ **±2% Reset and Low-Line Threshold Accuracy (MAX820, external programming mode)**

Ordering Information

PART**	TEMP. RANGE	PIN-PACKAGE
MAX792_CPE	0°C to +70°C	16 Plastic DIP
MAX792_CSE	0°C to +70°C	16 Narrow SO
MAX792_C/D	0°C to +70°C	Dice*

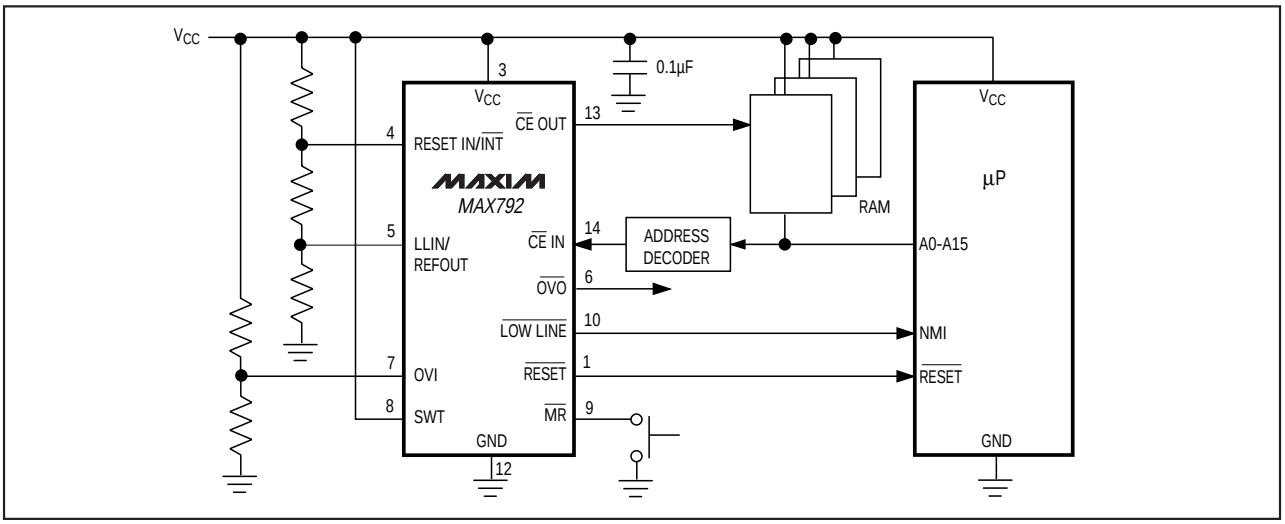
Ordering Information continued at end of data sheet.

** Dice are tested at T_A = +25°C, DC parameters only.*

***These parts offer a choice of five different reset threshold voltages. Select the letter corresponding to the desired nominal reset threshold voltage and insert it into the blank to complete the part number.*

SUFFIX	RESET THRESHOLD (V)
L	4.62
M	4.37
T	3.06
S	2.91
R	2.61

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Input Voltage (with respect to GND)
- V_{CC} .....-0.3V to +6V
- All Other Inputs.....-0.3V to (V_{CC} + 0.3V)

Input Current
- GND 25mA
- All Other Outputs 25mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Narrow SO (derate 9.52mW/°C above +70°C) 762mW
- CERDIP (derate 10.00mW/°C above +70°C).....800mW

Operating Temperature Ranges:
- MAX792_C__/MAX820_C__ .....0°C to +70°C
- MAX792_E__/MAX820_E__ .....-40°C to +85°C
- MAX792_MJE__/MAX820_MJE__.....-55°C to +125°C

Storage Temperature Range .....-65°C to +160°C

Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.65V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range		2.65			V
Supply Current			70	150	µA
RESET COMPARATOR					
Reset Threshold Voltage—Internal Threshold Mode (V_{TH})	MAX792L, MAX820L	4.50	4.62	4.75	V
	MAX792M, MAX820M	4.25	4.37	4.50	
	MAX792R, MAX820R	2.55	2.61	2.70	
	MAX792S, MAX820S	2.85	2.91	3.00	
	MAX792T, MAX820T	3.00	3.06	3.15	
	MAX820L, T_A = +25°C, V_{CC} falling	4.55		4.70	
	MAX820M, T_A = +25°C, V_{CC} falling	4.30		4.45	
	MAX820R, T_A = +25°C, V_{CC} falling (Note 1)	2.55		2.66	
	MAX820S, T_A = +25°C, V_{CC} falling	2.85		2.96	
	MAX820T, T_A = +25°C, V_{CC} falling	3.00		3.11	
Reset Threshold Voltage External Threshold Mode (V_{TH})	MAX792, V_{CC} = 5V or V_{CC} = 3V	1.25	1.30	1.35	V
	MAX820, V_{CC} = 5V or V_{CC} = 3V	1.274	1.30	1.326	
RESET IN/$\overline{INT}$ Mode Threshold (Note 2)	Internal threshold mode			60	mV
RESET IN/$\overline{INT}$ Leakage Current			±0.01	±25	nA
Reset Threshold Hysteresis			0.016 x V_{TH}		V
Reset Comparator Delay	V_{CC} falling		70		µs
Reset Active Timeout Period	V_{CC} rising	140	200	280	ms
$\overline{RESET}$ Output Voltage	I_{SINK} = 50µA, V_{CC} = 1V, V_{CC} falling		0.01	0.3	V
	I_{SINK} = 1.6mA		0.1	0.4	
	I_{SOURCE} = 1mA	V_{CC} - 1			
	I_{SOURCE} = 100µA	V_{CC} - 0.5			
RESET Output Voltage	I_{SINK} = 1.6mA		0.1	0.4	V
	I_{SOURCE} = 1mA	V_{CC} - 1			
	I_{SOURCE} = 100µA	V_{CC} - 0.5			

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.65V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LOW-LINE COMPARATOR						
Low-Line Threshold Voltage (Internal Threshold Mode)—V_{TH}	MAX792/MAX820L/M		50	120	210	mV
	MAX792/MAX820R/S/T		40	100	210	
Low-Line Threshold Voltage (External Programming Mode)	MAX792, V_{CC} = 5V OR V_{CC} = 3V		1.25	1.30	1.35	V
	MAX820, V_{CC} = 5V OR V_{CC} = 3V		1.274	1.30	1.326	
Low-Line Hysteresis (Internal Threshold Mode)				20		mV
LLIN/REFOUT Leakage Current External Programming Mode				±0.01	±25	nA
Low-Line Comparator Delay	V_{CC} falling			450		µs
$\overline{\text{LOWLINE}}$ Voltage	I_{SINK} = 3.2mA				0.4	V
	I_{SOURCE} = 1µA		V_{CC} - 1			
$\overline{\text{LOWLINE}}$ Short-Circuit Current	Output source current, V_{CC} = 5.5V			10	50	µA
WATCHDOG FUNCTION						
Watchdog Timeout Period	SWT connected to V_{CC}, V_{CC} = 5V		1.00	1.60	2.25	sec
	SWT connected to V_{CC}, V_{CC} = 3V		1.00	1.60	2.25	
	4.7nF capacitor connected from SWT to GND, V_{CC} = 3V			70		ms
	4.7nF capacitor connected from SWT to GND, V_{CC} = 5V			100		
Watchdog Input Pulse Width	V_{IL} = 0V, V_{IH} = V_{CC}	V_{CC} = 5V	100			ns
		V_{CC} = 3V	300			
$\overline{\text{WDO}}$ Output Voltage	I_{SINK} = 50µA, V_{CC} = 1V, V_{CC} falling			0.01	0.30	V
	I_{SINK} = 1.6mA			0.1	0.4	
	I_{SOURCE} = 1mA		V_{CC} - 1			
	I_{SOURCE} = 100µA		V_{CC} - 0.5			
$\overline{\text{WDPO}}$ to $\overline{\text{WDO}}$ Delay				70		ns
$\overline{\text{WDPO}}$ Duration			0.5	1.7	6.0	ms
$\overline{\text{WDPO}}$ Output Voltage	I_{SINK} = 50µA, V_{CC} = 1V, V_{CC} falling			0.01	0.3	V
	I_{SINK} = 1.6mA			0.1	0.4	
	I_{SOURCE} = 1mA		V_{CC} - 1			
	I_{SOURCE} = 100µA		V_{CC} - 0.5			
WDI Threshold Voltage	V_{CC} = 4.25V	V_{IH}	0.75 x V_{CC}			V
		V_{IL}			0.8	
	V_{CC} = 2.55V	V_{IH}	0.9 x V_{CC}			
		V_{IL}			0.2	
WDI Input Current					±1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.65V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OVERVOLTAGE COMPARATOR						
OVI Input Threshold	V_{CC} = 5V or V_{CC} = 3V		1.25	1.30	1.35	V
OVI Leakage Current				±0.01	±25	nA
$\overline{OVO}$ Output Voltage	I_{SINK} = 3.2mA				0.4	V
	I_{SOURCE} = 1µA		V_{CC} - 1			
$\overline{OVO}$ Short-Circuit Current	Output source current, V_{CC} = 5.5V			10	50	µA
OVI to $\overline{OVO}$ Delay	V_{OD} = 100mV, OVI rising			13		µs
	V_{OD} = 100mV, OVI falling			55		
CHIP-ENABLE GATING						
$\overline{CE}$ IN Threshold Voltage	V_{CC} = 4.25V	V_{IH}	0.75 x V_{CC}			V
		V_{IL}			0.8	
	V_{CC} = 2.55V	V_{IH}	0.75 x V_{CC}			
		V_{IL}			0.2	
$\overline{CE}$ IN Leakage Current	Disabled mode			±0.005	±1	µA
$\overline{CE}$ IN to $\overline{CE}$ OUT Resistance	Enabled mode	V_{CC} = 5V		75	150	Ω
		V_{CC} = 3V		150	300	
$\overline{CE}$ OUT Short-Circuit Current	Disabled mode, $\overline{CE}_{OUT}$ = 0V	V_{CC} = 5V	0.5		2.5	mA
		V_{CC} = 3V	0.05	0.2	0.4	
Chip-Enable Propagation Delay (Note 3)	50Ω source impedance driver, C_{LOAD} = 50pF	V_{CC} = 5V		6	10	ns
		V_{CC} = 3V		8	13	
Chip-Enable Output Voltage High (Reset Active)	I_{OUT} = -100µA		V_{CC} - 1			V
	I_{OUT} = 10µA		V_{CC} - 0.5			
Reset Active to $\overline{CE}$ OUT High	V_{CC} falling			15		µs
MANUAL RESET						
$\overline{MR}$ Minimum Pulse Width			25			µs
$\overline{MR}$ to $\overline{RESET}$ Propagation Delay				12		µs
$\overline{MR}$ Threshold Range			1.1	1.3	1.5	V
$\overline{MR}$ Pull-Up Current	$\overline{MR}$ = 0V	V_{CC} = 4.25V to V_{CC} = 5.5V	5	23	80	µA
		V_{CC} = 2.5V	1			

Note 1: The minimum operating voltage is 2.65V; however, the device is guaranteed to operate down to its preset reset threshold.

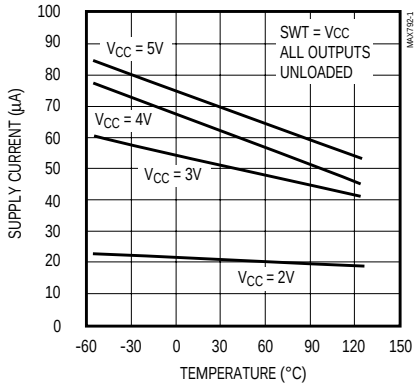
Note 2: Pulling RESET IN/$\overline{INT}$ below 60mV selects internal threshold mode and connects the internal voltage divider to the reset and low-line comparators. External programming mode allows an external resistor divider to set the low-line and reset thresholds (see Figure 4).

Note 3: The Chip-Enable Propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

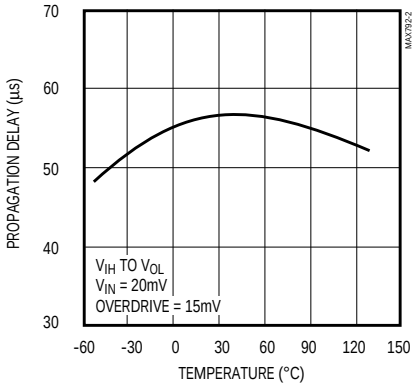
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

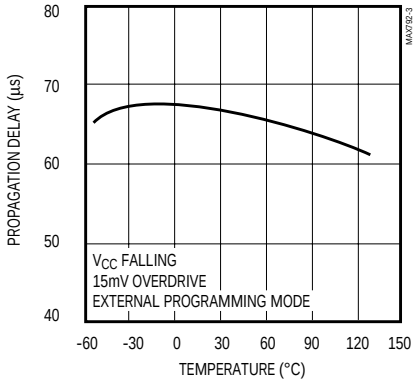
SUPPLY CURRENT vs. TEMPERATURE



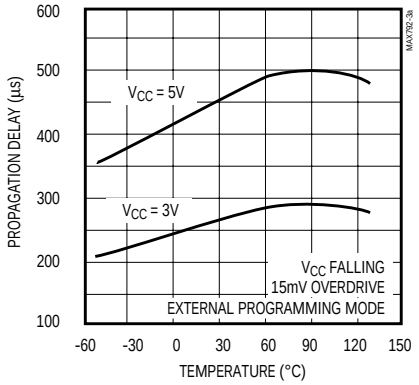
OVERVOLTAGE COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



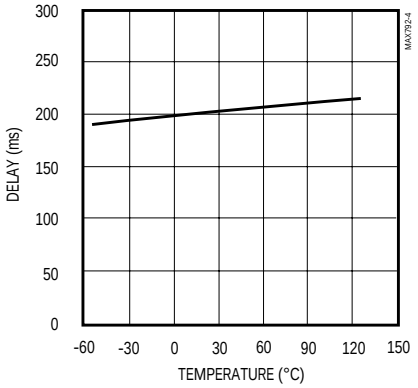
RESET COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



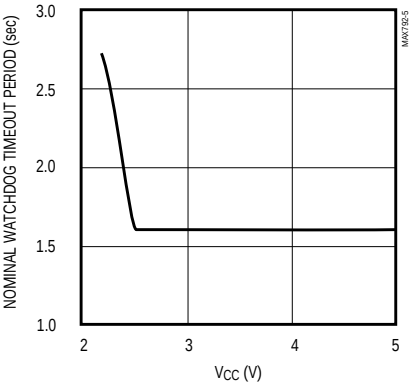
LOW-LINE COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



POWER-UP RESET DELAY vs. TEMPERATURE



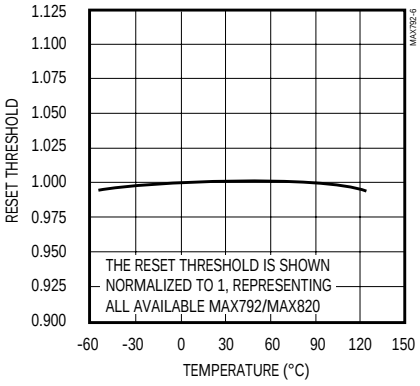
NOMINAL WATCHDOG TIMEOUT PERIOD vs. V_{CC}



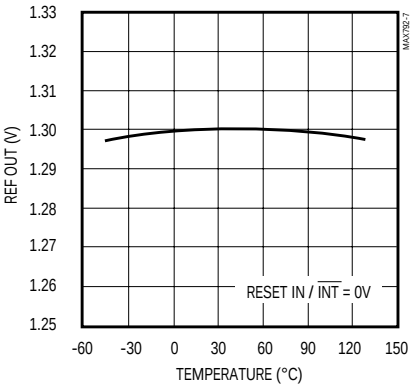
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

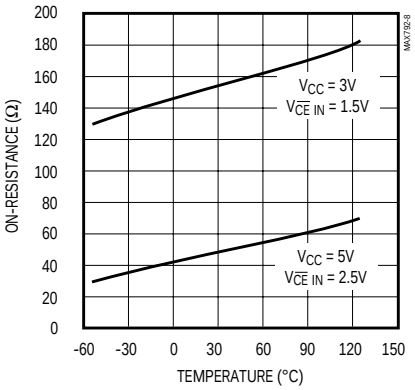
INTERNAL-MODE RESET THRESHOLD vs. TEMPERATURE (NORMALIZED)



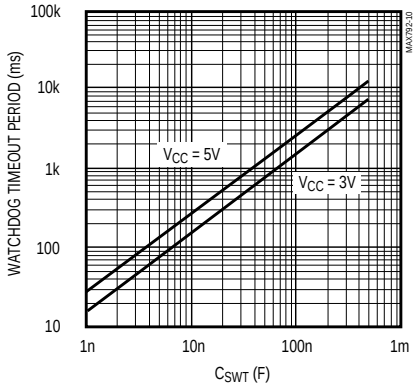
REF OUT VOLTAGE vs. TEMPERATURE



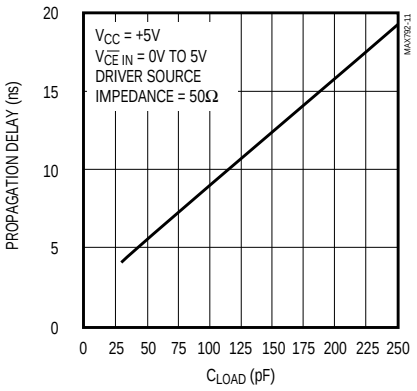
CHIP-ENABLE ON-RESISTANCE vs. TEMPERATURE



WATCHDOG TIMEOUT PERIOD vs. SWT LOAD CAPACITANCE



CHIP-ENABLE PROPAGATION DELAY vs. $\overline{CE}$ OUT LOAD CAPACITANCE



Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{RESET}}$	Active-Low Reset Output goes low whenever V_{CC} falls below the reset threshold in internal threshold programming mode, or RESET IN falls below 1.30V in external threshold programming mode. $\overline{\text{RESET}}$ remains low for 200ms typ after the threshold is exceeded on power-up.
2	RESET	Reset is the inverse of $\overline{\text{RESET}}$.
3	V_{CC}	Input Supply Voltage
4	RESET IN/$\overline{\text{INT}}$	Reset-Input/Internal-Mode Select. Connect this input to GND to select internal threshold mode. Select external programming mode by pulling this input 600mV or higher through an external voltage divider.
5	LLIN/REF OUT	Low-Line Input/Reference Output connects directly to the low-line comparator in external programming mode (RESET IN/$\overline{\text{INT}}$ ≥ 600mV). Connects directly to the internal 1.30V reference in internal threshold mode (RESET IN/$\overline{\text{INT}}$ ≤60mV).
6	$\overline{\text{OVO}}$	Overvoltage Comparator Output goes low when OVI is greater than 1.30V. This is an uncommitted comparator and has no effect on any other internal circuitry.
7	OVI	Inverting Input to the Overvoltage Comparator. When OVI is greater than 1.30V, $\overline{\text{OVO}}$ goes low. Connect OVI to GND or V_{CC} when not used.
8	SWT	Set Watchdog-Timeout Input. Connect this input to V_{CC} to select the default 1.6sec watchdog timeout period. Connect a capacitor between this input and GND to select another watchdog-timeout period. Watchdog timeout period = k x (capacitor value in nF)mV, where k = 27 for V_{CC} = 5V and k = 16.2 for V_{CC} = 3V. If the watchdog function is unused, connect SWT to V_{CC}.
9	$\overline{\text{MR}}$	Manual-Reset Input. This input can be tied to an external momentary pushbutton switch, or to a logic gate output. Internally pulled up to V_{CC}.
10	$\overline{\text{LOW LINE}}$	Low-Line Output. $\overline{\text{LOW LINE}}$ goes low 120mV above the reset threshold in internal threshold mode, or when LLIN/REFOUT goes below 1.30V in external programming mode.
11	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{WDPO}}$ pulses low and $\overline{\text{WDO}}$ goes low. $\overline{\text{WDO}}$ remains low until the next transition at WDI. Connect to GND or V_{CC} if unused.
12	GND	Ground
13	$\overline{\text{CE}}$ OUT	Chip-Enable Output. $\overline{\text{CE}}$ OUT goes low only when $\overline{\text{CE}}$ IN is low and reset is not asserted. If $\overline{\text{CE}}$ IN is low when reset is asserted, $\overline{\text{CE}}$ OUT will stay low for 15µs or until $\overline{\text{CE}}$ IN goes high, whichever occurs first.
14	$\overline{\text{CE}}$ IN	Chip-Enable Input—the input to the chip-enable transmission gate. Connect to GND or V_{CC} if not used.
15	$\overline{\text{WDO}}$	Watchdog Output. $\overline{\text{WDO}}$ goes low if WDI remains either high or low longer than the watchdog timeout period. $\overline{\text{WDO}}$ returns high on the next transition at WDI.
16	$\overline{\text{WDPO}}$	Watchdog-Pulse Output. Upon the absence of a transition at WDI, $\overline{\text{WDPO}}$ will pulse low for a minimum of 500µs. $\overline{\text{WDPO}}$ precedes $\overline{\text{WDO}}$ by typically 70ns.

Microprocessor and Non-Volatile Memory Supervisory Circuits

Detailed Description

Manual-Reset Input

Many µP-based products require manual-reset capability, allowing the operator to initiate a reset. The manual/external-reset input ($\overline{MR}$) can connect directly to a switch without an external pull-up resistor or debouncing network. $\overline{MR}$ internally connects to a 1.30V comparator, and has a high-impedance pull-up to V_{CC}, as shown in Figure 1. The propagation delay from asserting $\overline{MR}$ to reset asserted is typically 12µs. Pulsing $\overline{MR}$ low for a minimum of 25µs asserts the reset function (see *Reset Function* section). The reset output remains active as long as $\overline{MR}$ is held low, and the reset timeout period begins after $\overline{MR}$ returns high (Figure 2). To provide extra noise immunity in high-noise environments, pull $\overline{MR}$ up to V_{CC} with a 100kΩ resistor.

Use $\overline{MR}$ as either a digital logic input or as a second low-line comparator. Normal TTL/CMOS levels can be wire-OR connected via pull-down diodes (Figure 3), and open-drain/collector outputs can be wire-ORed directly.

Monitoring the Regulated Supply

The MAX792/MAX820 offer two modes for monitoring the regulated supply and providing reset and non-maskable interrupt (NMI) signals to the µP: internal threshold mode uses the factory preset low-line and reset thresholds, and external programming mode allows the low-line and reset thresholds to be programmed externally using a resistor voltage divider (Figure 4).

Internal Threshold Mode

Connecting the reset-input/internal-mode select pin (RESET IN/$\overline{INT}$) to ground selects internal threshold mode (Figure 4a). In this mode, the low-line and reset thresholds are factory preset by an internal voltage divider (Figure 1) to the threshold voltages specified in the *Electrical Characteristics* (Reset Threshold Voltage and Low-Line Threshold Voltage). Connect the low-line output ($\overline{LOWLINE}$) to the µP NMI pin, and connect the active-high reset output (RESET) or active-low reset output ($\overline{RESET}$) to the µP reset input pin.

Additionally, the low-line input/reference-output pin (LLIN/REFOUT) connects to the internal 1.30V reference in internal threshold mode. Buffer LLIN/REFOUT with a high-impedance buffer to use it with external circuitry. In this mode, when V_{CC} is falling, $\overline{LOWLINE}$ is guaranteed to be asserted prior to reset assertion.

External Programming Mode

Connecting RESET IN/$\overline{INT}$ to a voltage above 600mV selects external programming mode. In this mode, the low-line and reset comparators disconnect from the internal voltage divider and connect to LLIN/REFOUT and RESET IN/$\overline{INT}$, respectively (Figure 1). This mode allows flexibility in determining where in the operating voltage range the NMI and reset are generated. Set the low-line and reset thresholds with an external resistor divider, as in Figure 4b or Figure 4c. RESET typically remains valid for V_{CC} down to 2.5V; $\overline{RESET}$ is guaranteed to be valid with V_{CC} down to 1V.

Calculate the values for the resistor voltage divider in Figure 4b using the following equations:

1) $R3 = (1.30 \times V_{CC}\ MAX)/(V_{LOW\ LINE} \times I_{MAX})$

2) $R2 = [(1.30 \times V_{CC}\ MAX)/(V_{RESET} \times I_{MAX})] - R3$

3) $R1 = (V_{CC}\ MAX/I_{MAX}) - (R2 + R3)$.

First choose the desired maximum current through the voltage divider (I_{MAX}) when V_{CC} is at its highest (V_{CC} MAX). There are two things to consider here. First, I_{MAX} contributes to the overall supply current for the circuit, so you would generally make it as small as possible. Second, I_{MAX} cannot be too small or leakage currents will adversely affect the programmed threshold voltages; 5µA is often appropriate. Determine R3 after you have chosen I_{MAX}. Use the value for R3 to determine R2, then use both R2 and R3 to determine R1.

For example, to program a 4.75V low-line threshold and a 4.4V reset threshold, first choose I_{MAX} to be 5µA when V_{CC} = 5.5V and substitute into equation 1.

$R3 = (1.30 \times 5.5)/(4.75 \times 5E\text{-}6) = 301.05k\Omega$.

301kΩ is the nearest standard 0.1% value. Substitute into equation 2:

$R2 = [(1.30 \times 5.5)/(4.4 \times 5E\text{-}6)] - 301k\Omega = 23.95k\Omega$.

The nearest 0.1% resistor value is 23.7kΩ. Finally, substitute into equation 3:

$R1 = (5.5/5E\text{-}6) - (23.7k\Omega + 301k\Omega) = 775k\Omega$.

The nearest 0.1% value resistor is 787kΩ. Determine the actual low-line threshold by rearranging equation 1 and plugging in the standard resistor values. The actual low-line threshold is 4.75V and the actual reset threshold is 4.40V. An additional resistor allows the MAX792/MAX820 to monitor the unregulated supply and provide an NMI before the regulated supply begins to fall (Figure 4c).

Both of these thresholds will vary from circuit to circuit with resistor tolerance, reference variation, and comparator offset variation. The initial thresholds for each circuit will also vary with temperature due to reference and offset drift. For highest accuracy, use the MAX820.

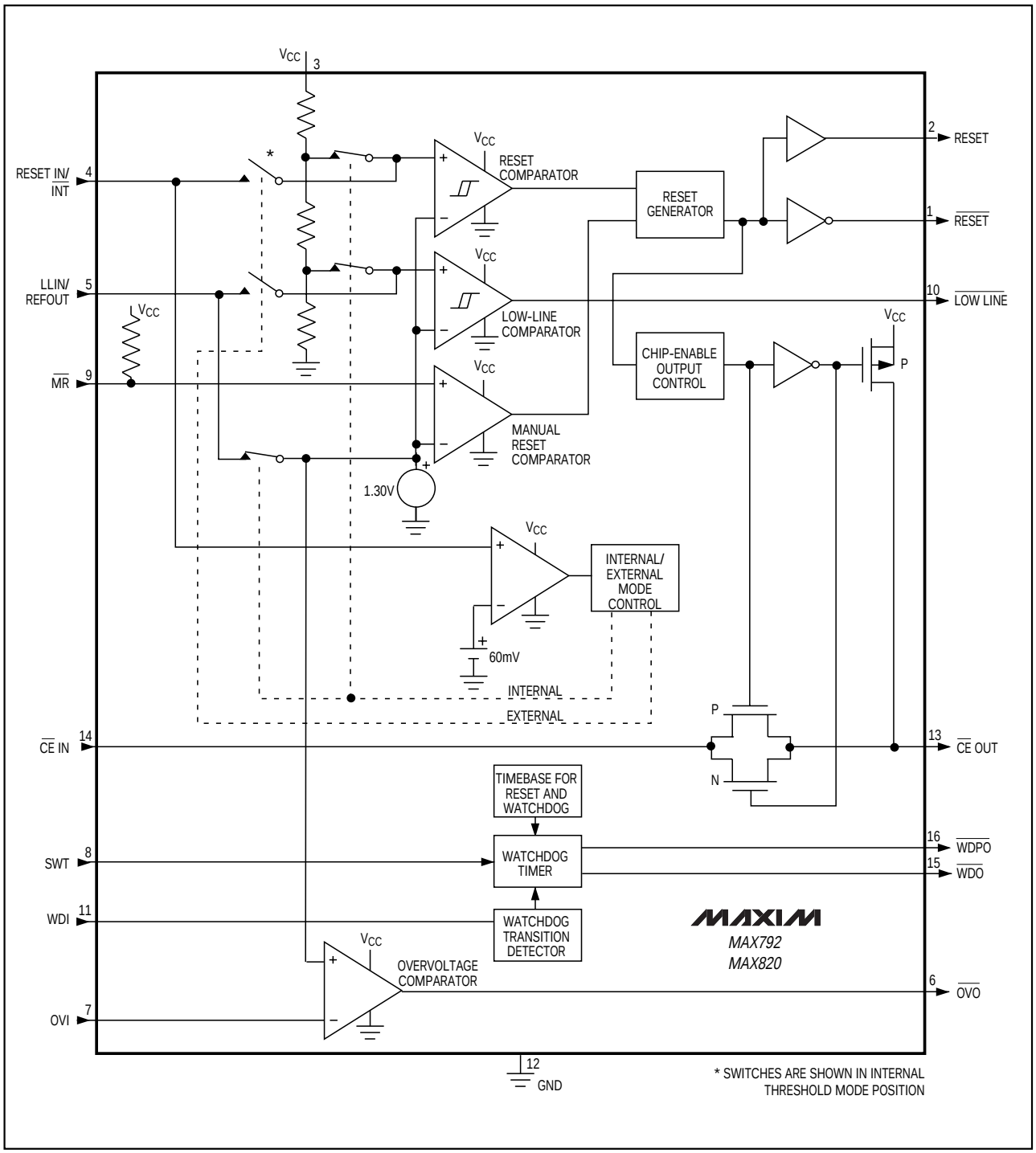


Figure 1. Block Diagram

Microprocessor and Non-Volatile Memory Supervisory Circuits

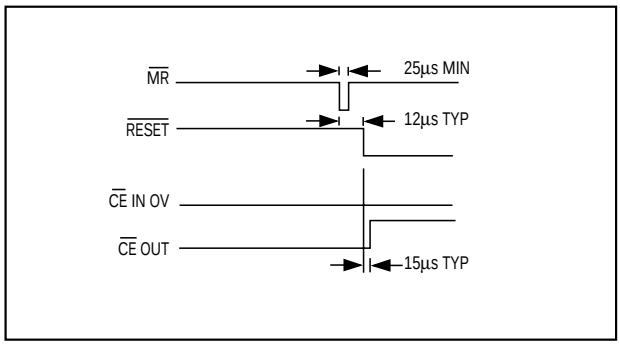


Figure 2. Manual-Reset Timing Diagram

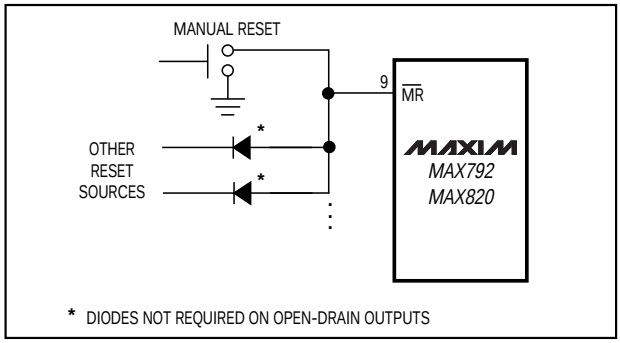


Figure 3. Diode "OR" connections allow multiple reset sources to connect to MR.

Low-Line Output

In internal threshold mode, the low-line comparator monitors V_{CC} with a threshold voltage typically 120mV above the reset threshold, and with 15mV of hysteresis. For normal operation (V_{CC} above the reset threshold), LOWLINE is pulled to V_{CC}. Use LOWLINE to provide an NMI to the µP, as described in the previous section, when V_{CC} begins to fall (Figure 4).

Reset Function

The MAX792/MAX820 provide both RESET and RESET outputs. The RESET and RESET outputs ensure that the µP powers up in a known state, and prevent code-execution errors during power-up, power-down, or brownout conditions.

The reset function will be asserted during the following conditions:

1) V_{CC} less than the programmed reset threshold.
2) MR less than 1.30V typ.
3) Reset remains asserted for 200ms typ after V_{CC} rises above the reset threshold or after MR has exceeded 1.30V typ.

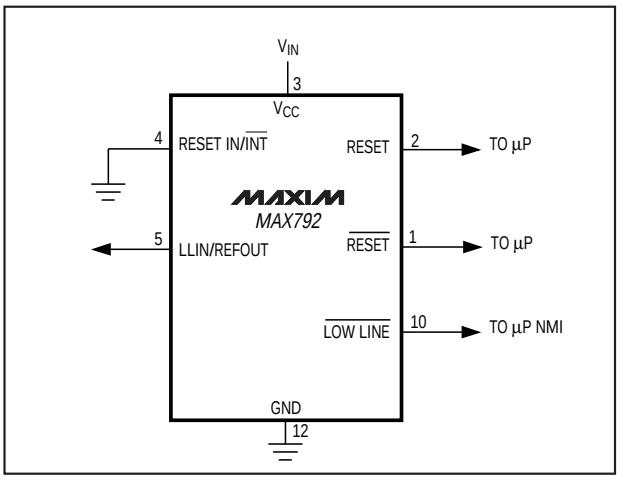


Figure 4a. Connection for Internal Threshold Mode

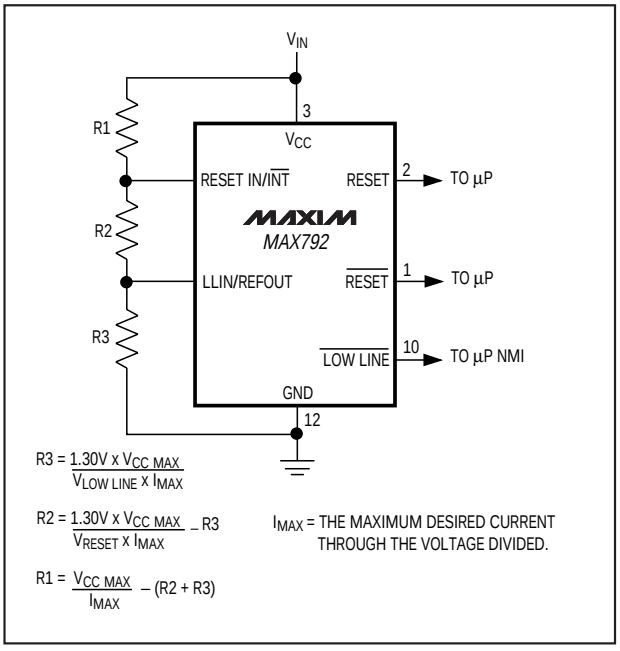


Figure 4b. Connection for External Threshold Programming Mode

When reset is asserted, all the internal counters are reset, the watchdog output (WDO) and watchdog-pulse output (WDPO) are set high, and the set watchdog-timeout input (SWT) is set to (V_{CC} - 0.6V) if it is not already connected to V_{CC} (for internal timeouts). The chip-enable transmission gate is also disabled while reset is asserted; the chip-enable input (CE IN) becomes high impedance and the chip-enable output (CE OUT) is pulled up to V_{CC}.

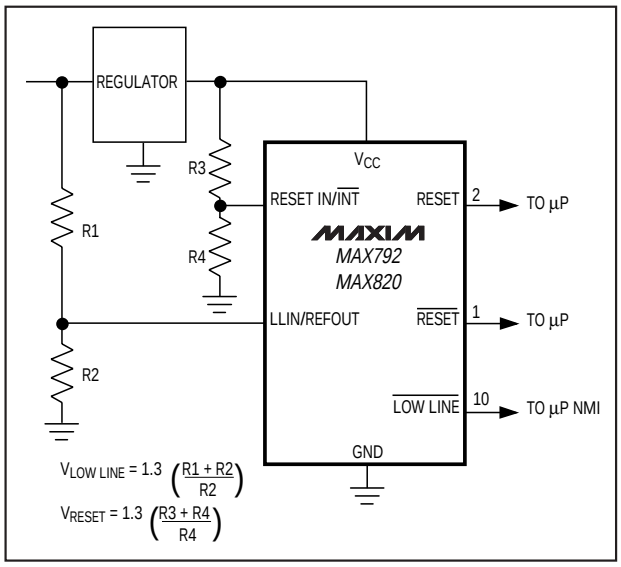


Figure 4c. Alternative Connection for External Programming Mode

Reset Outputs (RESET and $\overline{RESET}$)

The $\overline{RESET}$ output is active low and typically sinks 1.6mA at 0.1V. When deasserted, $\overline{RESET}$ sources 1.6mA at typically V_{CC} - 1.5V. The RESET output is the inverse of $\overline{RESET}$. $\overline{RESET}$ is guaranteed to be valid down to V_{CC} = 1V, and an external 10kΩ pull-down resistor on $\overline{RESET}$ ensures that it will be valid with V_{CC} down to GND (Figure 5). As V_{CC} goes below 1V, the gate drive to the $\overline{RESET}$ output switch reduces accordingly, increasing the $r_{DS(ON)}$ and the saturation voltage. The 10kΩ pull-down resistor ensures that the parallel combination of switch plus resistor will be around 10kΩ and the saturation voltage will be below 0.4V while sinking 40µA. When using an external pull-down resistor of 10kΩ, the high state for the $\overline{RESET}$ output with V_{CC} = 4.75V is typically 4.60V.

Overvoltage Comparator

The overvoltage comparator is an uncommitted comparator that has no effect on the operation of other chip functions. Use this input to provide overvoltage indication by connecting a voltage divider from the input supply, as in Figure 6.

Connect OVI to ground if the overvoltage function is not used. $\overline{OVO}$ goes low when OVI goes above 1.30V. With OVI below 1.30V, $\overline{OVO}$ is actively pulled to V_{CC} and can source1µA.

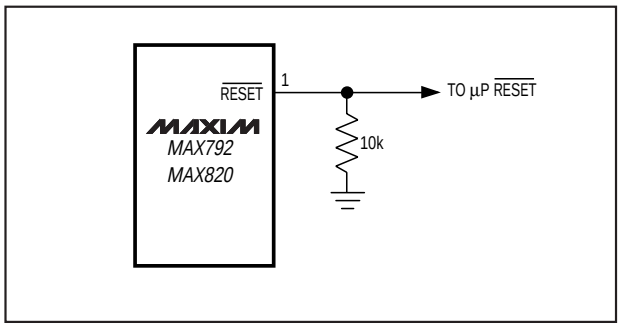


Figure 5. Adding an external pull-down resistor ensures $\overline{RESET}$ is valid with V_{CC} down to GND.

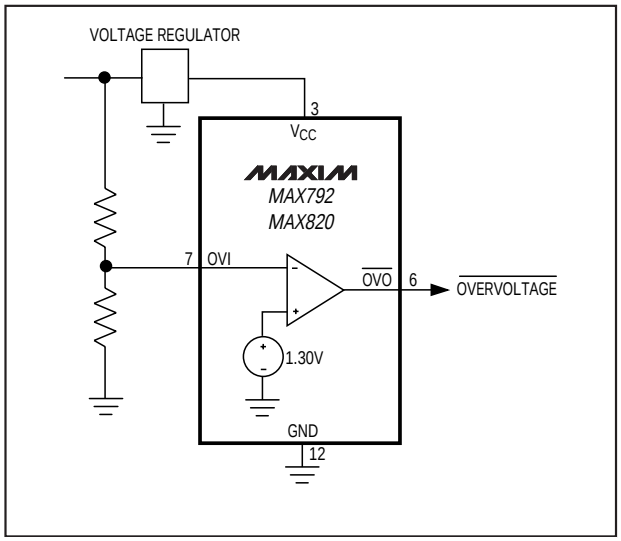


Figure 6. Detecting an Overvoltage Condition

Watchdog Function

The watchdog monitors µP activity via the watchdog input (WDI). If the µP becomes inactive, $\overline{WDO}$ and $\overline{WDPO}$ are asserted. To use the watchdog function, connect WDI to a µP bus line or I/O line. If WDI remains high or low for longer than the watchdog timeout period (1.6sec nominal), $\overline{WDPO}$ and $\overline{WDO}$ are asserted, indicating a software fault condition (see *Watchdog-Pulse Output* and *Watchdog Output* sections).

Watchdog Input

If the watchdog function is unused, connect WDI to V_{CC} or GND. A change of state (high-to-low, low-to-high, or a minimum 100ns pulse) at WDI during the watchdog period resets the watchdog timer. The watchdog timer

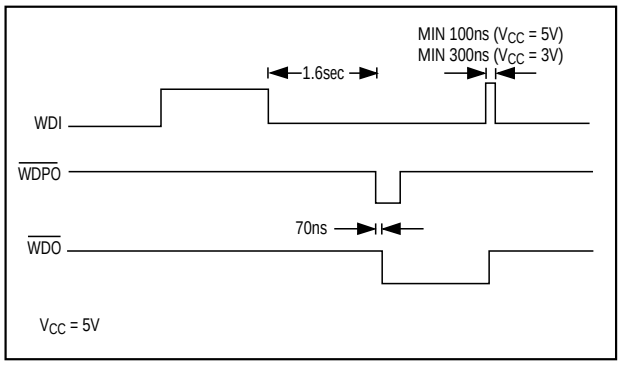


Figure 7. WDI, WDO and WDPO Timing Diagram

default is 1.6sec. Select alternative timeout periods by connecting an external capacitor from SWT to GND (see *Selecting an Alternative Watchdog Timeout* section). When V_{CC} is below the reset threshold, the watchdog function is disabled.

Watchdog Output

WDO remains high if there is a transition or pulse at WDI during the watchdog timeout period. The watchdog function is disabled and WDO is a logic high when V_{CC} is below the reset threshold. If a system reset is desired on every watchdog fault, simply diode-OR connect WDO to MR (Figure 8). When a watchdog fault occurs in this mode, WDO goes low, pulling MR low and causing a reset pulse to be issued. As soon as reset is asserted, the watchdog timer clears and WDO goes high. With WDO connected to MR, a continuous high or low on WDI will cause 200ms reset pulses to be issued every 1.6sec (SWT connected to V_{CC}). When reset is not asserted, if no transition occurs at WDI during the watchdog timeout period, WDO goes low 70ns after the falling edge of WDPO and remains low until the next transition at WDI (Figure 7). A single additional flip-flop can force the system into a hardware shutdown if there are two successive watchdog faults (Figure 8). When the MAX792/MAX820 are operated from a 5V supply, WDO has a 2 x TTL output characteristic.

Watchdog-Pulse Output

As described in the preceding section, WDPO can be used as the clock input to an external D flip-flop. Upon the absence of a watchdog edge or pulse at WDI at the end of a watchdog timeout period, WDPO will pulse low for 1.7ms. The falling edge of WDPO precedes WDO by 70ns. Since WDO is high when WDPO goes low, the flip-flop's Q output remains high after WDO goes low (Figure 8). If the watchdog timer is not reset by a transition at

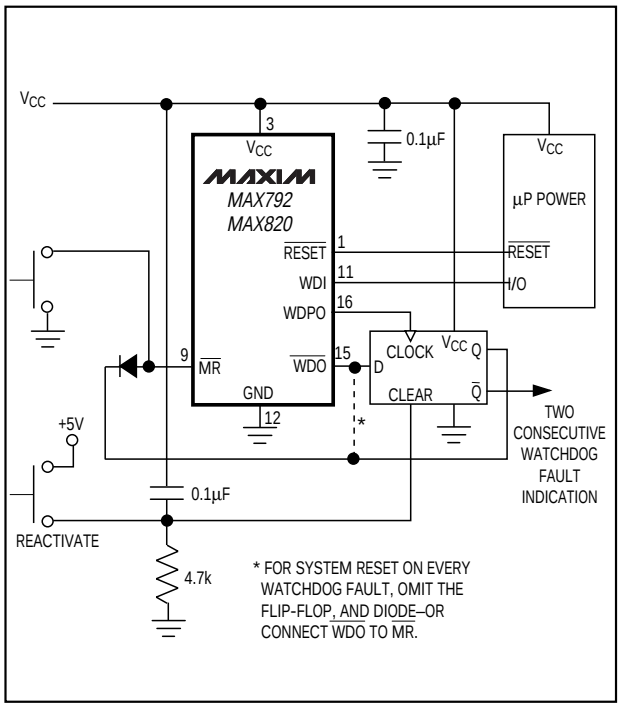


Figure 8. Two consecutive watchdog faults latch the system in reset.

WDI, WDO remains low and the next WDPO following a second watchdog timeout period clocks a logic low to the Q output, pulling MR low and causing the MAX792/MAX820 latch in reset. If the watchdog timer is reset by a transition at WDI, WDO will go high and the flip-flop's Q output will remain high. Thus a system shutdown is only caused by two successive watchdog faults.

Selecting an Alternative Watchdog Timeout Period

The SWT input controls the watchdog timeout period. Connecting SWT to V_{CC} selects the internal 1.6sec watchdog timeout period. Select an alternative watchdog timeout period by connecting a capacitor between SWT and GND. Do not leave SWT floating and do not connect it to ground. The following formula determines the watchdog timeout period:

Watchdog Timeout Period =
k x (capacitor value in nF)ms

where k = 27 for V_{CC} = 3V, and k = 16.2 for V_{CC} = 5V.

This applies for capacitor values in excess of 4.7nF. If the watchdog function is unused, connect SWT to V_{CC}.

Chip-Enable Signal Gating

The MAX792/MAX820 provide internal gating of chip-enable (CE) signals, which prevents erroneous data from corrupting CMOS RAM in the event of an undervoltage condition. The MAX792/MAX820 use a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT (Figure 1).

During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The 10ns max CE propagation delay from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the MAX792/MAX820 to be used with most µPs. If $\overline{CE}$ IN is low when reset asserts, $\overline{CE}$ OUT remains low for a short period to permit completion of the current write cycle.

Chip-Enable Input

The CE transmission gate is disabled and $\overline{CE}$ IN is high impedance (disabled mode) while reset is asserted.

During a power-down sequence when V_{CC} passes the reset threshold, the CE transmission gate disables and $\overline{CE}$ IN immediately becomes high impedance if the voltage at $\overline{CE}$ IN is high. If $\overline{CE}$ IN is low when reset is asserted, the CE transmission gate will disable at the moment $\overline{CE}$ IN goes high or 15µs after reset is asserted, whichever occurs first (Figure 9). This permits the current write cycle to complete during power-down.

During a power-up sequence, the CE transmission gate remains disabled and $\overline{CE}$ IN remains high impedance regardless of $\overline{CE}$ IN activity, until reset is deasserted following the reset timeout period.

While disabled, $\overline{CE}$ IN is high impedance. When the CE transmission gate is enabled, the impedance of $\overline{CE}$ IN will appear as a 75Ω (V_{CC} = 5V) resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on V_{CC}, the source impedance of the drive connected to $\overline{CE}$ IN, and the loading on $\overline{CE}$ OUT (see the Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance graph in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on $\overline{CE}$ IN to the 50% point on $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 10). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT, and use a low-output-impedance driver.

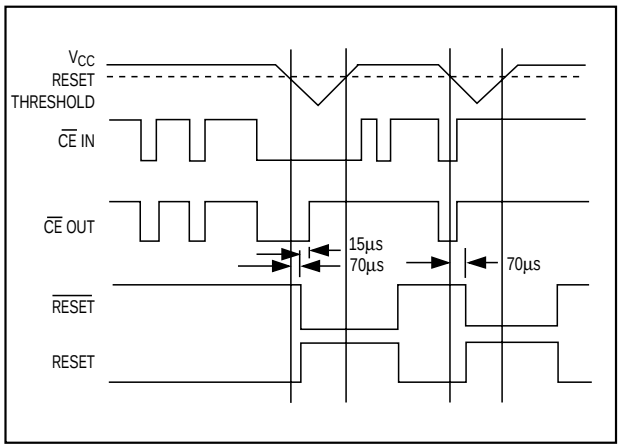


Figure 9. Reset and Chip-Enable Timing

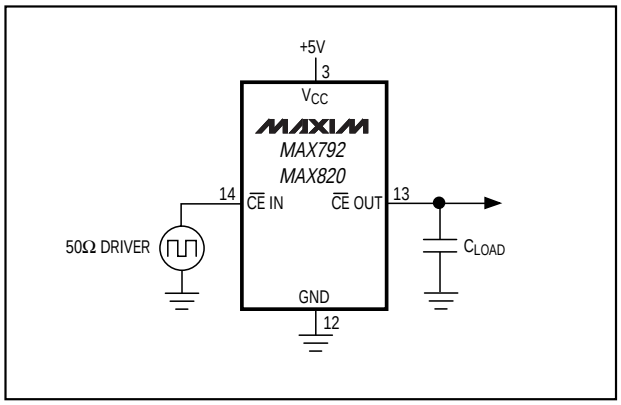


Figure 10. CE Propagation Delay Test Circuit

Chip-Enable Output

When the CE transmission gate is enabled, the impedance of $\overline{CE}$ OUT is equivalent to 75Ω in series with the source driving $\overline{CE}$ IN. In the disabled mode, the 75Ω transmission gate is off and an active pull-up connects from $\overline{CE}$ OUT to V_{CC}. This source turns off when the transmission gate is enabled.

Applications Information

Connect a 0.1µF ceramic capacitor from V_{CC} to GND, as close to the device pins as possible. This reduces the probability of resets due to high-frequency power-supply transients. In a high-noise environment, additional bypass capacitance from V_{CC} to ground may be required. If long leads connect to the chip inputs, ensure that these lines are free from ringing, etc., which would forward bias the chip's protection diodes.

Microprocessor and Non-Volatile Memory Supervisory Circuits

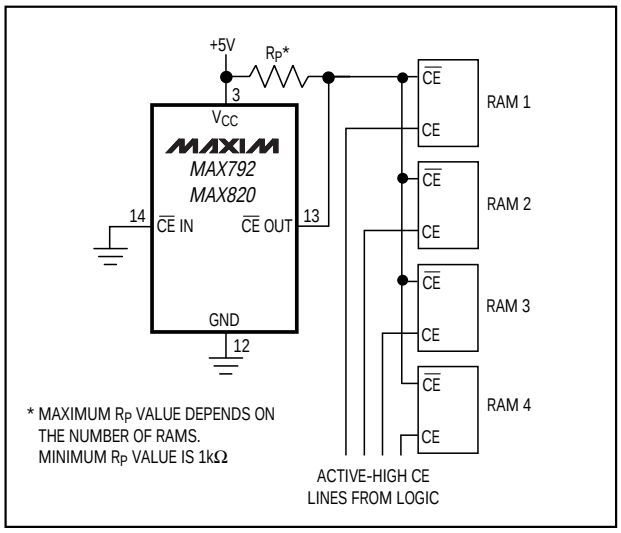


Figure 11. Alternate CE Gating

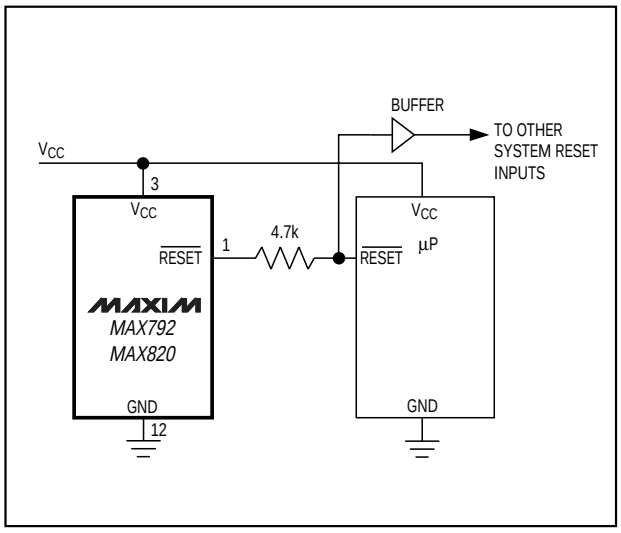


Figure 12. Interfacing to µPs with Bidirectional RESET Pins

Alternative Chip-Enable Gating

Using memory devices with both CE and $\overline{CE}$ inputs allows the MAX792/MAX820 CE propagation delay to be bypassed. To do this, connect $\overline{CE}$ IN to ground, pull up $\overline{CE}$ OUT to V_{CC}, and connect $\overline{CE}$ OUT to the $\overline{CE}$ input of each memory device (Figure 11). The CE input of each memory device then connects directly to the chip-select logic, which does not have to be gated by the MAX792/MAX820.

Interfacing to µPs with Bidirectional Reset Inputs

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX792/MAX820 $\overline{RESET}$ output. If, for example, the MAX792/MAX820 $\overline{RESET}$ output is asserted high and the µP wants to pull it low, indeterminate logic levels may result. To avoid this, connect a 4.7kΩ resistor between the MAX792/MAX820 $\overline{RESET}$ output and the µP reset I/O, as in Figure 12. Buffer the MAX792/MAX820 $\overline{RESET}$ output to other system components.

Negative-Going V_{CC} Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

Figure 13 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset-comparator overdrive). The graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 30µs or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

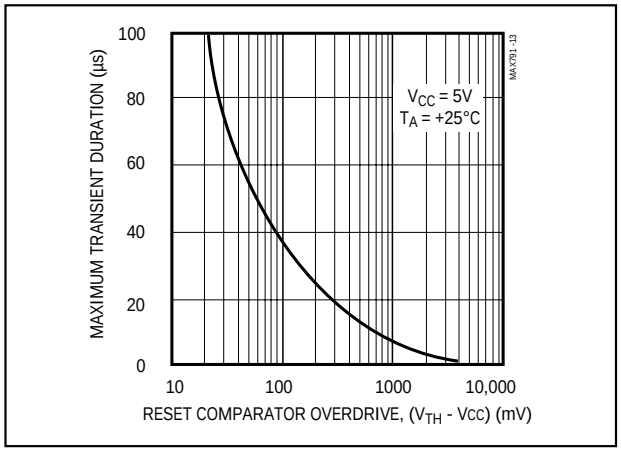


Figure 13. Maximum Transient Duration without Causing a Reset Pulse vs. Reset-Comparator Overdrive

_Ordering Information (continued)

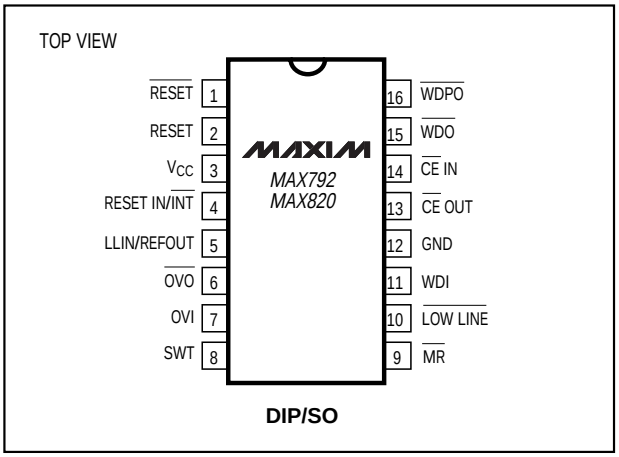
PART**	TEMP. RANGE	PIN-PACKAGE
MAX792_EPE	-40°C to +85°C	16 Plastic DIP
MAX792_ESE	-40°C to +85°C	16 Narrow SO
MAX792_EJE	-40°C to +85°C	16 CERDIP
MAX792_MJE	-55°C to +125°C	16 CERDIP
MAX820_CPE	-0°C to +70°C	16 Plastic DIP
MAX820_CSE	-0°C to +70°C	16 Narrow SO
MAX820_EPE	-40°C to +85°C	16 Plastic DIP
MAX820_ESE	-40°C to +85°C	16 Narrow SO
MAX820_EJE	-40°C to +85°C	16 CERDIP
MAX820_MJE	-55°C to +125°C	16 CERDIP

** Dice are tested at T_A = +25°C.*

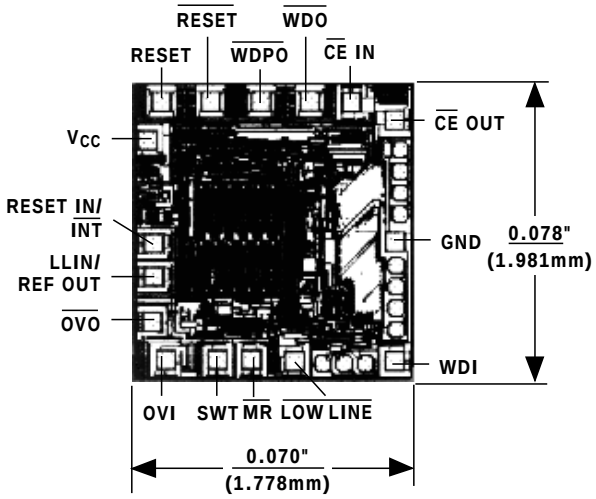
***These parts offer a choice of five different reset threshold voltages. Select the letter corresponding to the desired nominal reset threshold voltage and insert it into the blank to complete the part number.*

SUFFIX	RESET THRESHOLD (V)
L	4.62
M	4.37
T	3.06
S	2.91
R	2.61

Pin Configuration



Chip Topography

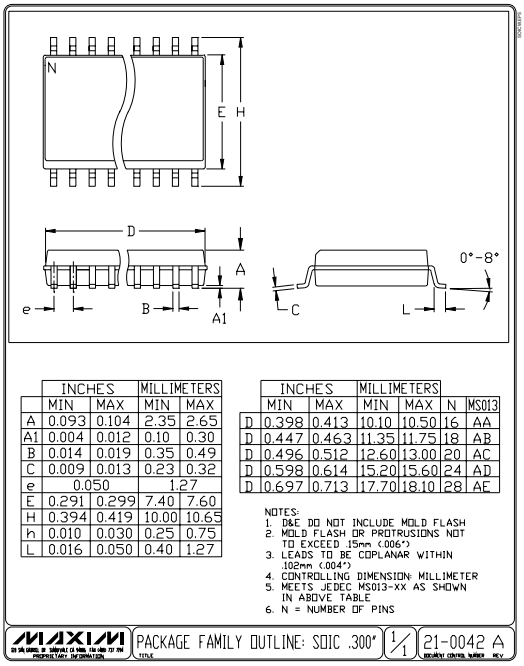


TRANSISTOR COUNT: 950

SUBSTRATE CONNECTED TO V_{CC}

Microprocessor and Non-Volatile Memory Supervisory Circuits

Package Information

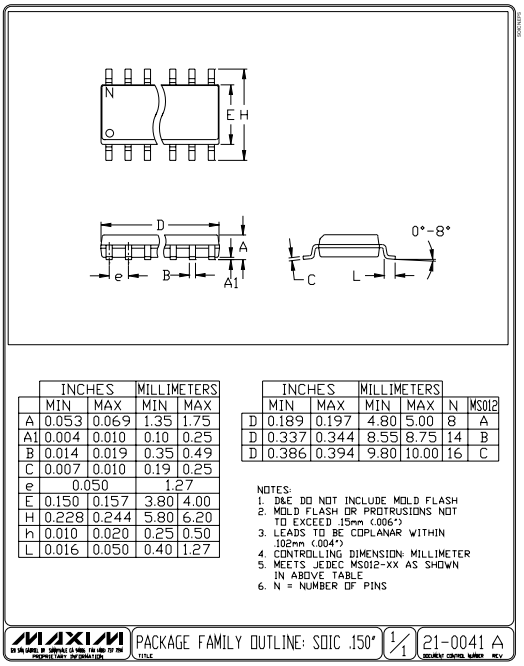


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .300" | 1/1 | 21-0042 A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A