MC74VHCT50A

Noninverting Buffer / CMOS Logic Level Shifter
with LSTTL–Compatible Inputs

The MC74VHCT50A is a hex noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffered output which provides high noise immunity and stable output.

The device input is compatible with TTL–type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high–voltage power supply.

The MC74VHCT50A input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHCT50A to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when V_{CC} = 0 V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 3.5 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- CMOS–Compatible Outputs: V_{OH} > 0.8 V_{CC}; V_{OL} < 0.1 V_{CC} @Load
- Power Down Protection Provided on Inputs and Outputs

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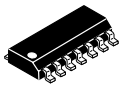
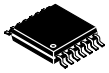
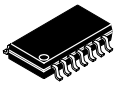


14–LEAD SOIC
D SUFFIX
CASE 751A

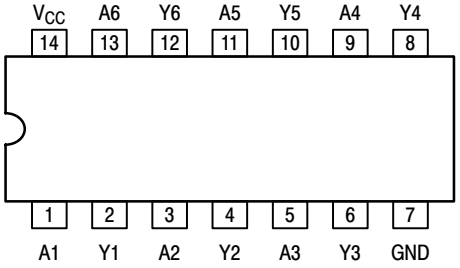


14–LEAD TSSOP
DT SUFFIX
CASE 948G



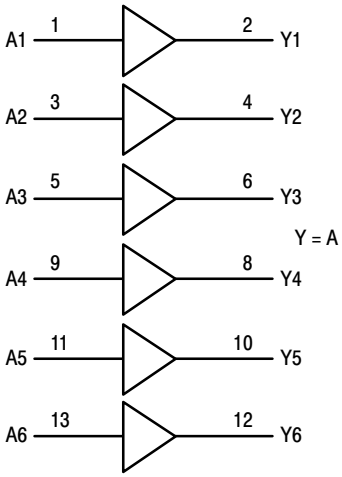
14–LEAD SOIC EIAJ
M SUFFIX
CASE 965

PIN CONNECTION AND MARKING DIAGRAM (Top View)

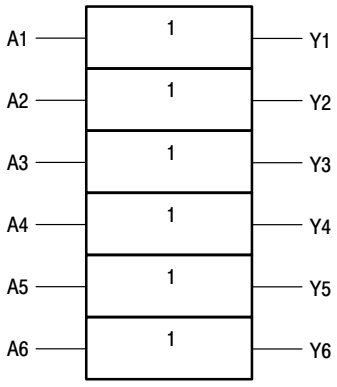


For detailed package marking information, see the Marking Diagram section on page 4 of this data sheet.

LOGIC DIAGRAM



LOGIC SYMBOL



ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT50AD	SOIC	55 Units/Rail
MC74VHCT50ADT	TSSOP	96 Units/Rail
MC74VHCT50AM	SOIC EIAJ	50 Units/Rail

FUNCTION TABLE

A Input	Y Output
L	L
H	H

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0	V
V_{IN}	DC Input Voltage	$-0.5 \le V_I \le +7.0$	V
V_{OUT}	DC Output Voltage Output in HIGH or LOW State (Note 1)	$-0.5 \le V_O \le +7.0$	V
I_{IK}	DC Input Diode Current	−20	mA
I_{OK}	DC Output Diode Current	±20	mA
I_O	DC Output Source/Sink Current	±25	mA
I_{CC}	DC Supply Current per Supply Pin	±50	mA
I_{GND}	DC Ground Current per Ground Pin	±50	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature under Bias	+150	°C
θ_{JA}	Thermal Resistance SOIC TSSOP	 125 170	°C/W
P_D	Power Dissipation in Still Air SOIC TSSOP	 500 450	mW
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 2000	V
$I_{Latch–Up}$	Latch–Up Performance Above V_{CC} and Below GND at 85°C (Note 5)	±300	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22–A114–A.
3. Tested to EIA/JESD22–A115–A.
4. Tested to JESD22–C101–A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	0.0 0.0	5.5 V_{CC}	V
Operating Temperature Range		T_A	–55	+125	°C
Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	t_r, t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage		4.5 5.5	2.0 2.0			2.0 2.0		2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 5.5			0.8 0.8		0.8 0.8		0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = –50 μA	4.5	4.4	4.5		4.4		4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = –8 mA	4.5	3.94			3.80		3.66		V
V_{OL}	Maximum Low–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	4.5		0.0	0.1		0.1		0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 8 mA	4.5			0.36		0.44		0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I_{OFF}	Output Leakage Current	V_{OUT} = 5.5 V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A to Y	V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF		4.7 5.5	6.7 7.7		7.5 8.5		8.5 9.5	ns
C_{IN}	Maximum Input Capacitance			5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	15	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Characteristic	T_A = 25°C Typ	T_A = 25°C Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.8	–1.0	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

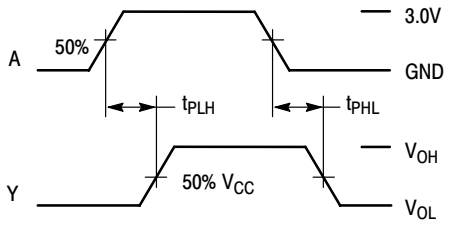
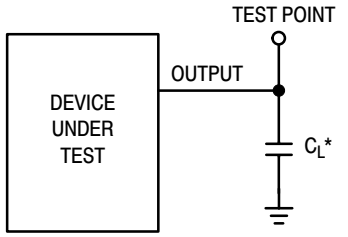


Figure 1. Switching Waveforms

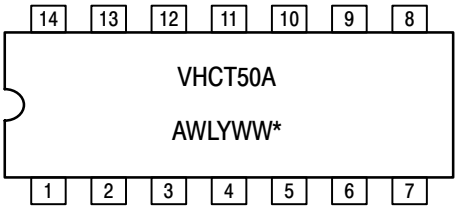


*Includes all probe and jig capacitance

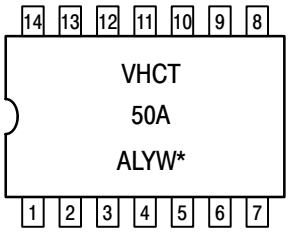
Figure 2. Test Circuit

MARKING DIAGRAMS

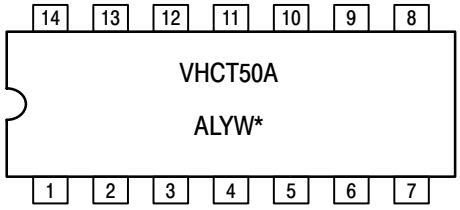
(Top View)



14–LEAD SOIC
D SUFFIX
CASE 751A



14–LEAD TSSOP
DT SUFFIX
CASE 948G

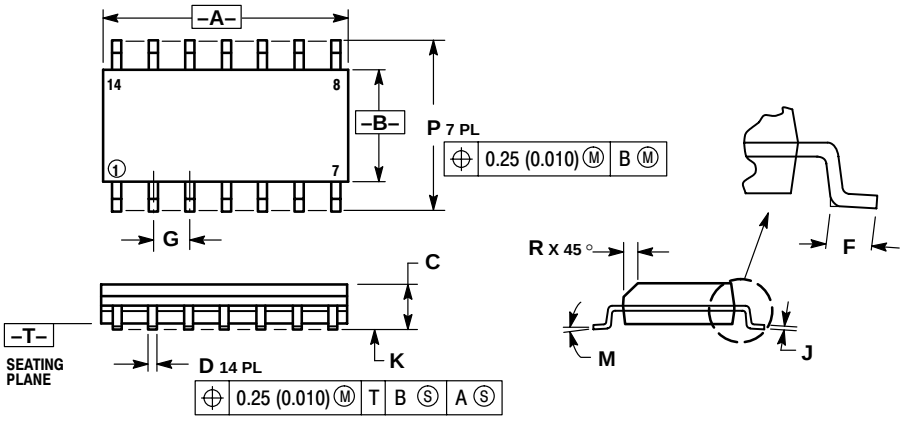


14–LEAD SOIC EIAJ
M SUFFIX
CASE 965

*See Applications Note #AND8004/D for date code and traceability information.

PACKAGE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F

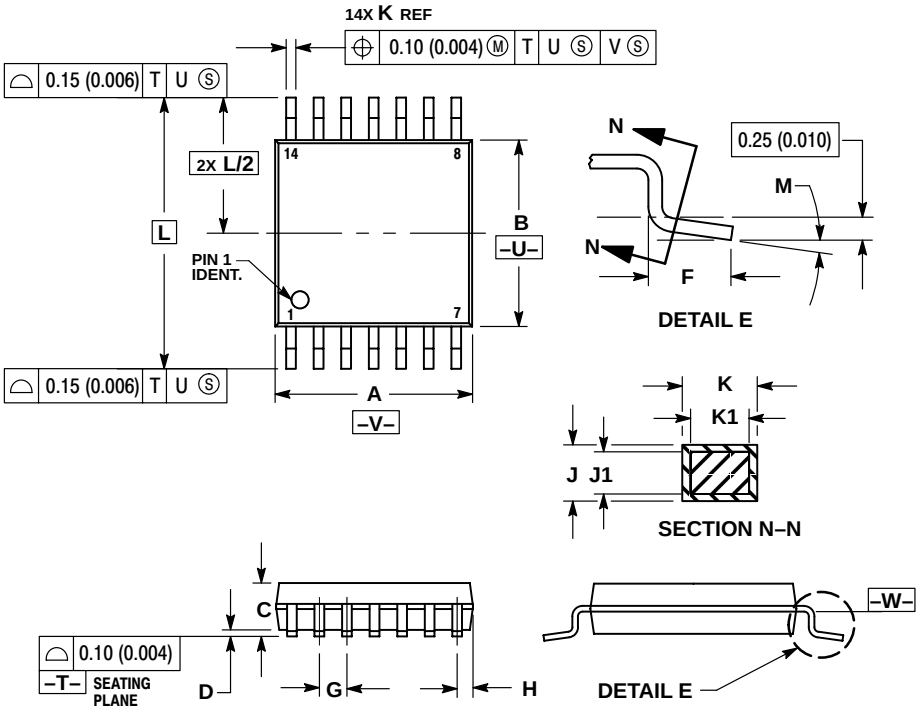


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O

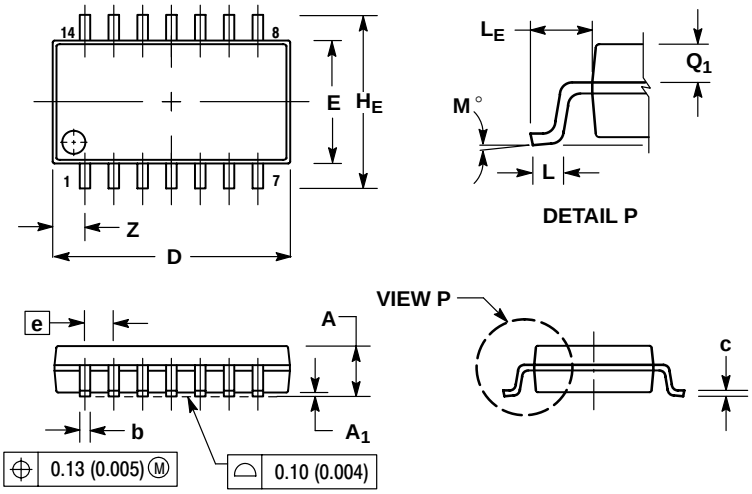


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

PUBLICATION ORDERING INFORMATION

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