# Noninverting Buffer / CMOS Logic Level Shifter with LSTTL-Compatible Inputs

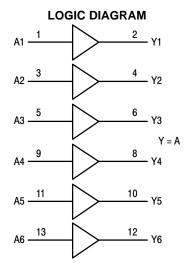
The MC74VHCT50A is a hex noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffered output which provides high noise immunity and stable output.

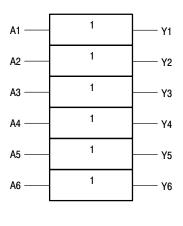
The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHCT50A input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHCT50A to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when  $V_{CC}=0$  V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed:  $t_{PD} = 3.5 \text{ ns (Typ)}$  at  $V_{CC} = 5 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 2 \mu A \text{ (Max)}$  at  $T_A = 25^{\circ}\text{C}$
- TTL-Compatible Inputs:  $V_{IL} = 0.8 \text{ V}$ ;  $V_{IH} = 2.0 \text{ V}$
- CMOS–Compatible Outputs:  $V_{OH} > 0.8 V_{CC}$ ;  $V_{OL} < 0.1 V_{CC}$  @Load
- Power Down Protection Provided on Inputs and Outputs



#### LOGIC SYMBOL





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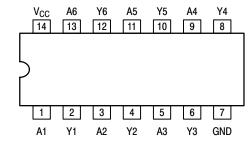


14-LEAD SOIC D SUFFIX CASE 751A 14-LEAD TSSOP DT SUFFIX CASE 948G



14-LEAD SOIC EIAJ M SUFFIX CASE 965

## PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 4 of this data sheet.

#### **ORDERING INFORMATION**

Device	Package	Shipping	
MC74VHCT50AD	SOIC	55 Units/Rail	
MC74VHCT50ADT	TSSOP	96 Units/Rail	
MC74VHCT50AM	SOIC EIAJ	50 Units/Rail	

#### **FUNCTION TABLE**

A Input	Y Output
L	L
Н	Н

#### **MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5  to  +7.0	V
V <sub>IN</sub>	DC Input Voltage	$-0.5 \le V_{\parallel} \le +7.0$	V
V <sub>OUT</sub>	DC Output Voltage Output in HIGH or LOW State (Note 1)	$-0.5 \le V_{O} \le +7.0$	V
I <sub>IK</sub>	DC Input Diode Current	-20	mA
I <sub>OK</sub>	DC Output Diode Current	±20	mA
Io	DC Output Source/Sink Current	±25	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±50	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±50	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
TJ	Junction Temperature under Bias	+150	°C
$\theta_{JA}$	Thermal Resistance SOIC TSSOP	125 170	°C/W
P <sub>D</sub>	Power Dissipation in Still Air SOIC TSSOP		mW
V <sub>ESD</sub>	ESD Withstand Voltage  Human Body Model (Note 2)  Machine Model (Note 3)  Charged Device Model (Note 4)	> 200	V
I <sub>Latch-Up</sub>	Latch–Up Performance Above V <sub>CC</sub> and Below GND at 85°C (Note 5)	±300	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

- 1. I<sub>O</sub> absolute maximum rating must be observed.
- 2. Tested to EIA/JESD22–A114–A.
- 3. Tested to EIA/JESD22-A115-A.
- 4. Tested to JESD22-C101-A.
- 5. Tested to EIA/JESD78.

#### **RECOMMENDED OPERATING CONDITIONS**

С	Characteristics		Min	Max	Unit
DC Supply Voltage		V <sub>CC</sub>	4.5	5.5	V
DC Input Voltage		V <sub>IN</sub>	0.0	5.5	V
DC Output Voltage	V <sub>CC</sub> = 0 High or Low State	V <sub>OUT</sub>	0.0 0.0	5.5 V <sub>CC</sub>	V
Operating Temperature Ra	ange	T <sub>A</sub>	<b>-</b> 55	+125	°C
Input Rise and Fall Time	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	t <sub>r</sub> , t <sub>f</sub>	0 0	100 20	ns/V

#### DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	1	Γ <sub>A</sub> = 25°(	C	T <sub>A</sub> ≤	85°C	T <sub>A</sub> ≤ 125°C		
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage		4.5 5.5	2.0 2.0			2.0 2.0		2.0 2.0		V
V <sub>IL</sub>	Maximum Low–Level Input Voltage		4.5 5.5			0.8 0.8		0.8 0.8		0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50  \mu\text{A}$	4.5	4.4	4.5		4.4		4.4		V
	$V_{IN} = V_{IH}$ or $V_{IL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -8 \text{ mA}$	4.5	3.94			3.80		3.66		V
V <sub>OL</sub>	Maximum Low–Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50  \mu\text{A}$	4.5		0.0	0.1		0.1		0.1	V
	$V_{IN} = V_{IH}$ or $V_{IL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 8 \text{ mA}$	4.5			0.36		0.44		0.52	V
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μΑ
I <sub>CC</sub>	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μΑ
I <sub>CCT</sub>	Quiescent Supply Current	Input: V <sub>IN</sub> = 3.4 V	5.5			1.35		1.50		1.65	mA
I <sub>OFF</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0.0			0.5		5.0		10	μΑ

#### AC ELECTRICAL CHARACTERISTICS ( $C_{load} = 50 \text{ pF}$ , Input $t_r = t_f = 3.0 \text{ns}$ )

				T <sub>A</sub> = 25°C		$T_A \le 85^{\circ}C$ $T_A \le 125^{\circ}C$		125°C			
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propogation Delay, Input A to Y	$V_{CC} = 5.0 \pm 0.5 \text{ V}$	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		4.7 5.5	6.7 7.7		7.5 8.5		8.5 9.5	ns
C <sub>IN</sub>	Maximum Input Capacitance				5	10		10		10	pF

		Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
C <sub>PD</sub>	Power Dissipation Capacitance (Note 6)	15	pF

<sup>6.</sup> C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no–load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

#### **NOISE CHARACTERISTICS** (Input $t_r = t_f = 3.0 \text{ns}$ , $C_L = 50 \text{pF}$ , $V_{CC} = 5.0 \text{V}$ )

		T <sub>A</sub> = 25°C		
Symbol	Characteristic	Тур	Max	Unit
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.8	1.0	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-0.8	-1.0	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		2.0	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		0.8	V

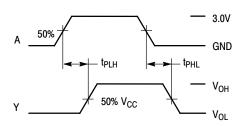
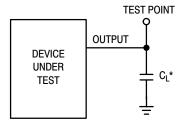


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

#### **MARKING DIAGRAMS** (Top View) 14 13 12 11 10 9 8 12 11 10 9 8 14 13 **VHCT** VHCT50A 50A AWLYWW\* ALYW\* 1 2 3 4 5 6 7 2 3 4 5 14-LEAD SOIC 14-LEAD TSSOP **D SUFFIX DT SUFFIX CASE 751A CASE 948G** 13 12 11 10 9 8 VHCT50A ALYW\* 2 3 4 5 6 14-LEAD SOIC EIAJ **M SUFFIX**

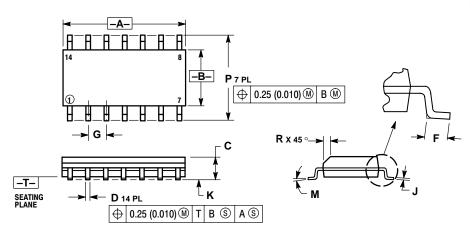
\*See Applications Note #AND8004/D for date code and traceability information.

**CASE 965** 

#### **PACKAGE DIMENSIONS**

#### **D SUFFIX**

PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



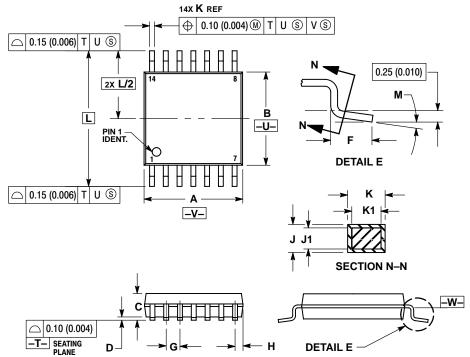
- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INCHES				
DIM	MIN	MAX	MIN	MAX			
Α	8.55	8.75	0.337	0.344			
В	3.80	4.00	0.150	0.157			
С	1.35	1.75	0.054	0.068			
D	0.35	0.49	0.014	0.019			
F	0.40	1.25	0.016	0.049			
G	1.27	BSC	0.050 BSC				
J	0.19	0.25	0.008	0.009			
K	0.10	0.25	0.004	0.009			
M	0°	7°	0°	7°			
Р	5.80	6.20	0.228	0.244			
R	0.25	0.50	0.010	0.019			

#### PACKAGE DIMENSIONS

#### **DT SUFFIX**

PLASTIC TSSOP PACKAGE CASE 948G-01 **ISSUE O** 



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

- O'NTROILING DIMENSION: MILLIMETER.

  JIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

  DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

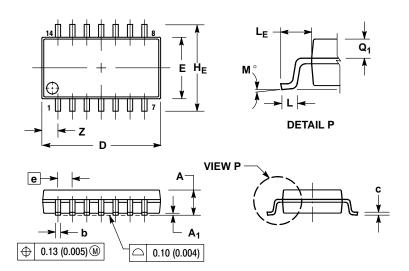
  DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. MATERIAL CONDITION.
  TERMINAL NUMBERS ARE SHOWN FOR
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
   DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE W–.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С	-	1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40 BSC 0.252 BS				
M	0°	8°	0°	8°	

#### PACKAGE DIMENSIONS

#### M SUFFIX

PLASTIC SOIC EIAJ PACKAGE CASE 965-01 **ISSUE O** 



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTR
- PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006)
  PER SIDE.
  TERMINAL NUMBERS ARE SHOWN FOR
  REFERENCE ONLY.
  THE LEAD WIDTH DIMENSION (b) DOES NOT
  INCLUDE DAMBAR PROTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
  TOTAL IN EXCESS OF THE LEAD WIDTH
  DIMENSION AT MAXIMUM MATERIAL CONDITION.
  DAMBAR CANNOT BE LOCATED ON THE LOWER
  RADIUS OR THE FOOT. MINIMUM SPACE
  BETWEEN PROTRUSIONS AND ADJACENT LEAD
  TO BE 0.46 (0.018). TO BE 0.46 ( 0.018).

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α		2.05		0.081	
A <sub>1</sub>	0.05	0.20	0.002	0.008	
b	0.35	0.50	0.014	0.020	
С	0.18	0.27	0.007	0.011	
D	9.90	10.50	0.390	0.413	
Е	5.10	5.45	0.201	0.215	
е	1.27	BSC	0.050 BSC		
HE	7.40	8.20	0.291	0.323	
0.50	0.50	0.85	0.020	0.033	
LE	1.10	1.50	0.043	0.059	
M	0 °	10 °	0 °	10°	
$Q_1$	0.70	0.90	0.028	0.035	
7		1 //2		0.056	

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