

Noninverting Buffer / CMOS Logic Level Shifter with LSTTL-Compatible Inputs

MC74VHC1GT50

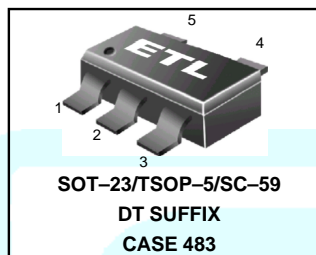
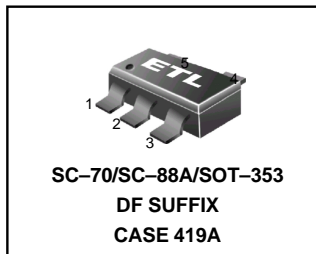
The MC74VHC1GT50 is a single gate noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT50 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT50 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: $t_{PD} = 3.5$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 2$ mA (Max) at $T_A = 25^\circ\text{C}$
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$;
 $V_{OL} < 0.1 V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 104; Equivalent Gates = 26



| PIN ASSIGNMENT | |
|----------------|----------|
| 1 | NC |
| 2 | IN A |
| 3 | GND |
| 4 | OUT Y |
| 5 | V_{CC} |

MARKING DIAGRAMS

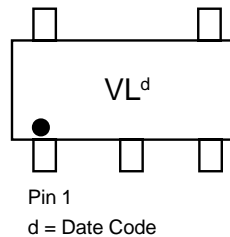


Figure 1. Pinout (Top View)

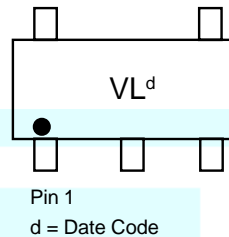


Figure 2. Logic Symbol

| FUNCTION TABLE | |
|----------------|--------|
| Inputs | Output |
| A | Y |
| L | L |
| H | H |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------------|--------------------------------------------|--------------------------------------------------------------------------------------|-----------------------------------------------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V _{IN} | DC Input Voltage | -0.5 to +7.0 | V |
| V _{OUT} | DC Output Voltage | V _{CC} =0 High or Low State | -0.5 to +7.0 -0.5 to V _{CC} + 0.5 |
| I _{IK} | Input Diode Current | -20 | mA |
| I _{OK} | Output Diode Current | V _{OUT} < GND; V _{OUT} > V _{CC} | +20 |
| I _{OUT} | DC Output Current, per Pin | | +25 |
| I _{CC} | DC Supply Current, V _{CC} and GND | | +50 |
| P _D | Power dissipation in still air | SC-88A, TSOP-5 | 200 |
| θ _{JA} | Thermal resistance | SC-88A, TSOP-5 | 333 |
| T _L | Lead Temperature, 1 mm from Case for 10 s | | 260 |
| T _J | Junction Temperature Under Bias | | +150 |
| T _{stg} | Storage temperature | | -65 to +150 |
| V _{ESD} | ESD Withstand Voltage | Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) | >2000 >200 N/A |
| I _{LATCH-UP} | Latch-Up Performance | Above V _{CC} and Below GND at 125°C (Note 5) | ±500 |

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22-A114-A
3. Tested to EIA/JESD22-A115-A
4. Tested to JESD22-C101-A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------------------------|-----------------------------|----------------------------------------------------------------|------------------------|------|
| V _{CC} | DC Supply Voltage | 3.0 | 5.5 | V |
| V _{IN} | DC Input Voltage | 0.0 | 5.5 | V |
| V _{OUT} | DC Output Voltage | V _{CC} = 0 High Low State | 0.0 V _{CC} | V |
| T _A | Operating Temperature Range | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time | V _{CC} = 3.3 ± 0.3 V V _{CC} = 5.0 ± 0.5 V | 0 100 | ns/V |

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

| Junction Temperature °C | Time, Hours | Time, Years |
|-------------------------|-------------|-------------|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

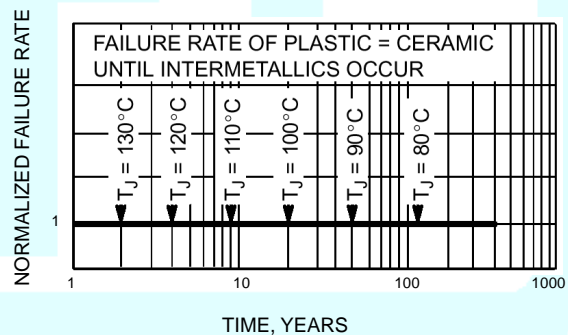


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | T _A ≤ 85°C | | -55°C ≤ T _A ≤ 125°C | | Unit |
|------------------|-------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|------------------------|-----------------------|------------|--------------------|-----------------------|--------------------|--------------------------------|--------------------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 3.0 4.5 5.5 | 1.4 2.0 2.0 | | | 1.4 2.0 2.0 | | 1.4 2.0 2.0 | V | |
| V _{IL} | Maximum Low-Level Input Voltage | | 3.0 4.5 5.5 | | | 0.53 0.8 0.8 | | 0.53 0.8 0.8 | | 0.53 0.8 0.8 | V |
| V _{OH} | Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA | 3.0 4.5 | 2.9 4.4 | 3.0 4.5 | | 2.9 4.4 | | 2.9 4.4 | | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA | 3.0 | 2.58 | | | 2.48 | | 2.34 | | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -8 mA | 4.5 | 3.94 | | | 3.80 | | 3.66 | | |
| V _{OL} | Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA | 3.0 4.5 | | 0.0 0.0 | 0.1 0.1 | | 0.1 0.1 | | 0.1 0.1 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA | 3.0 | | | 0.36 | | 0.44 | | 0.52 | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OL} = 8 mA | 4.5 | | | 0.36 | | 0.44 | | 0.52 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 2.0 | | 20 | | 40 | μA |
| I _{CCT} | Quiescent Supply Current | Input: V _{IN} = 3.4 V | 5.5 | | | 1.35 | | 1.50 | | 1.65 | mA |
| I _{OPD} | Output Leakage Current | V _{OUT} = 5.5 V | 0.0 | | | 0.5 | | 5.0 | | 10 | μA |

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r = t_f = 3.0 ns

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A ≤ 85°C | | -55°C ≤ T _A ≤ 125°C | | Unit |
|----------------------------------------|-----------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------|------------|--------------|-----------------------|--------------|--------------------------------|--------------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Y | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF | | 4.5 6.3 | 10.0 13.5 | | 11.0 15.0 | | 13.0 17.5 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF | | 3.5 4.3 | 6.7 7.7 | | 7.5 8.5 | | 8.5 9.5 | |
| C _{IN} | Maximum Input Capacitance | | | 5 | 10 | | 10 | | 10 | pF |
| | | | Typical @ 25°C, V_{CC} = 5.0 V | | | | | | | |
| C _{PD} | Power Dissipation Capacitance (Note 6) | | | 12 | | | | | pF | |

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC1GT50

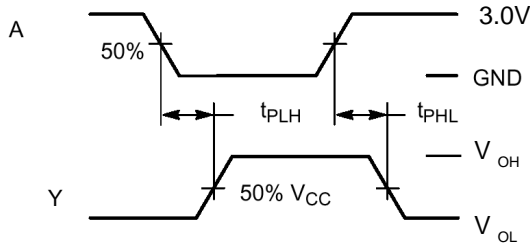
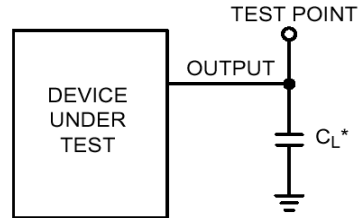


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance

Figure 5. Test Circuit

DEVICE ORDERING INFORMATION

| Device Order Number | Device Nomenclature | | | | | | Package Type (Name/SOT#/Common Name) | Tape and Reel Size |
|---------------------|---------------------|-----------------------|------------|-----------------|----------------|--------------------|-----------------------------------------|-------------------------------|
| | Circuit Indicator | Temp Range Identifier | Technology | Device Function | Package Suffix | Tape & Reel Suffix | | |
| MC74VHC1GT50DFT1 | MC | 74 | VHC1G | T50 | DF | T1 | SC-70/SC-88A/ SOT-353 | 178 mm (7 in) 3000 Unit |
| MC74VHC1GT50DFT2 | MC | 74 | VHC1G | T50 | DF | T2 | SC-70/SC-88A/ SOT-353 | 178 mm (7 in) 3000 Unit |
| MC74VHC1GT50DFT4 | MC | 74 | VHC1G | T50 | DF | T4 | SC-70/SC-88A/ SOT-353 | 330 mm (13 in) 10,000 Unit |
| MC74VHC1GT50DTT1 | MC | 74 | VHC1G | T50 | DT | T1 | SOT-23/TSOPS/ SC-59 | 178 mm (7 in) 3000 Unit |
| MC74VHC1GT50DTT3 | MC | 74 | VHC1G | T50 | DT | T3 | SOT-23/TSOPS/ SC-59 | 330 mm (13 in) 10,000 Unit |