HD74AC Series Common Information

HITACHI

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FACT Descriptions and Family Characteristics

1. Advanced CMOS FACT Logic

FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fanout capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies.

For direct replacement of LS, ALS and other TTL devices, HD74ACT circuits with TTL-type input thresholds are included in the FACT family. These include the more popular bus drivers/transceivers as well as many other HD74ACTXXX devices.

1.1 Characteristics

- Full logic product line
- Industry standard functions and pinouts for SSI and MSI
- Meets or exceeds JEDEC standards for HD74ACXX family
- TTL inputs on selected circuits
- High performance outputs
  - — Common output structure for standard and buffer drivers
  - — Output Sink/Source Current of 24 mA
  - — Transmission line driving 50 Ω guaranteed
- Operation from 2 to 6 volts guaranteed
- Temperature range –40°C to +85°C
- Improved ESD protection network
- High current latch-up immunity

1.2 Interfacing

FACT devices have a wide operating voltage range (V_{CC} = 2 to 6 VDC) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

- HD74AC is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive ±24 mA of I_{OH} and I_{OL} current. Industry standard HD74AC nomenclature and pinouts are used.
- HD74ACT is a high-speed CMOS device with a TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a V_{CC} = 5 V ±0.5 V with V_{OH} = 2.4 V and V_{OL} = 0.4 V, but are functional over the entire FACT operating voltage range of 2.0 to 5.5 VDC. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. HD74ACT devices have the same output structures as HD74AC devices.

1.3 Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws three orders of magnitude less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated. FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

- FACT = 0.1 mW/gate
- ALS = 1.2 mW/gate
- LS = 2.0 mW/gate
- HC = 0.1 mW/gate

Figure 1 illustrates the effects of I_{CC} versus power supply voltage (V_{CC}) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

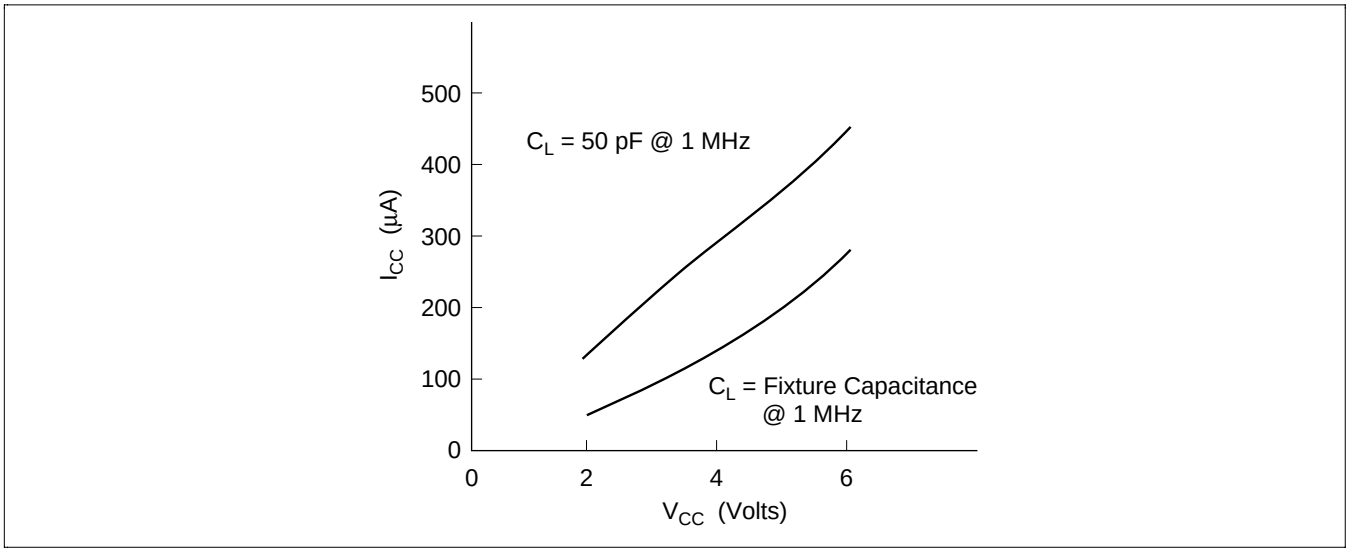


Figure 1 I_{CC} vs V_{CC}

1.4 AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays as well as the basic gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The example below describes typical values for a HD74XX138, 3 to 8 line decoder.

- FACT = 6.0 ns @ C_L = 50 pF
- ALS = 12.0 ns @ C_L = 50 pF
- LS = 27.0 ns @ C_L = 15 pF
- HC = 17.0 ns @ C_L = 50 pF

AC performance specifications are guaranteed at 5.0 V ± 0.5 V and 3.3 V ± 0.3 V. For worst case design at 2.0 V V_{CC} on all device types, the formula below can be used to determine AC performance.

AC performance at 2.0 V V_{CC} = 1.9 × AC specification at 3.3 V

1.5 Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and 5.0 V ± 10% V_{CC}.

1.6 Noise Immunity

The noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $|V_{IL}–V_{OL}|$ / $|V_{IH}–V_{OH}|$ at 4.5 V V_{CC}.

- FACT = 1.25/1.25 V
- ALS = 0.4/0.7 V
- LS = 0.3/0.7 V@ 4.75 V V_{CC}
- HC = 1.25/1.25 V

1.7 Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both HD74AC and HD74ACT device types have the same output structures. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications witch can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All devices (HD74AC or HD74ACT) are guaranteed to source and sink 24 mA. HD74AC/ACTXXX, are capable of driving 50 Ω transmission lines.

1.7.1 I_{OL}/I_{OH} Characteristics

- FACT = 24/–24 mA
- ALS = 24/–15 mA
- LS = 8/–0.4 mA @ 4.75 V V_{CC}
- HC = 4/–4 mA

1.7.2 Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time-consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied 'typical' output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these 'typical' performance values across the operating voltage and temperature limits. Hitachi has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 50 Ω.

Figure 2 shows a Bergerton diagram for switching both high-to-low and low-to-high. On the right side of the graph ($I_{out} > 0$), are the V_{OH} and I_{IH} curves for FACT logic while on the left side ($I_{out} < 0$), are the curves for V_{OL} and I_{IL}. Although we will only discuss here the low-to-high transition, the information presented may be applied to a high-to-low transition.

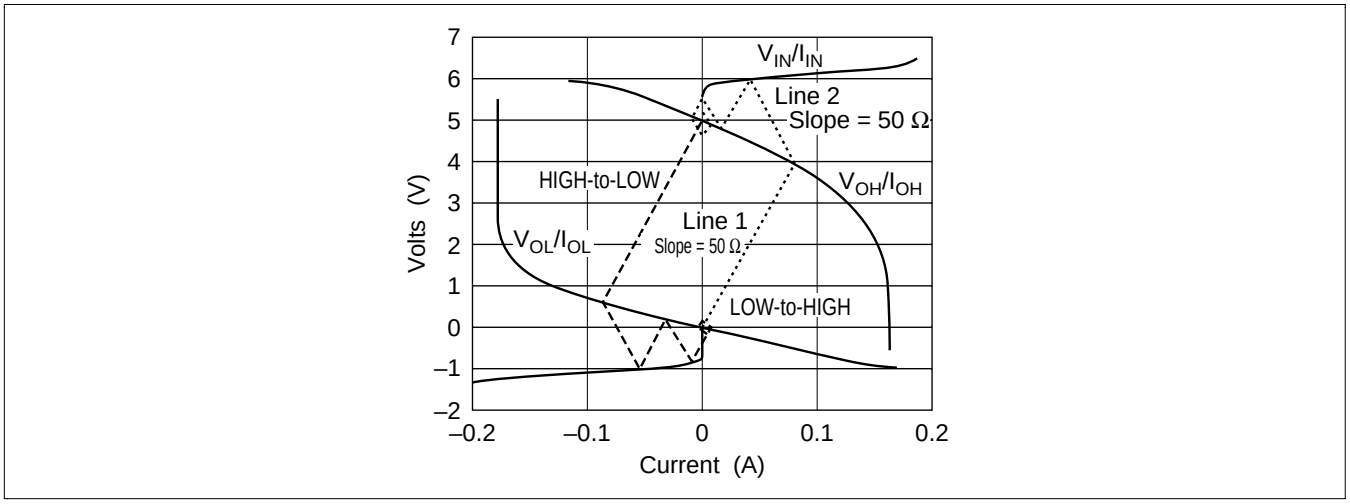


Figure 2 Gate Driving 50 Ω Line Reflection Diagram

Begin analysis at the V_{OL} (quiescent) point. This is the intersection of the V_{OL}/I_{OL} curve for the output and the V_{IN}/I_{IN} curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV. Then draw a 50 Ω load line from this intersection to the V_{OH}/I_{OH} curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95 V. Then draw a line with a slope of –50 Ω from this first intersection point to the V_{IN}/I_{IN} curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load line from each intersection to the next. Lines terminating on the V_{OH}/I_{OH} curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes.

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves travelling from the driver to the receiver while intersection points on the V_{IN}/I_{IN} curve will be waves travelling from the receiver to the driver.

Figure 3 and 4 show the resultant waveforms. Each division on the time scale represents the propagation delay of the transmission line.

While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

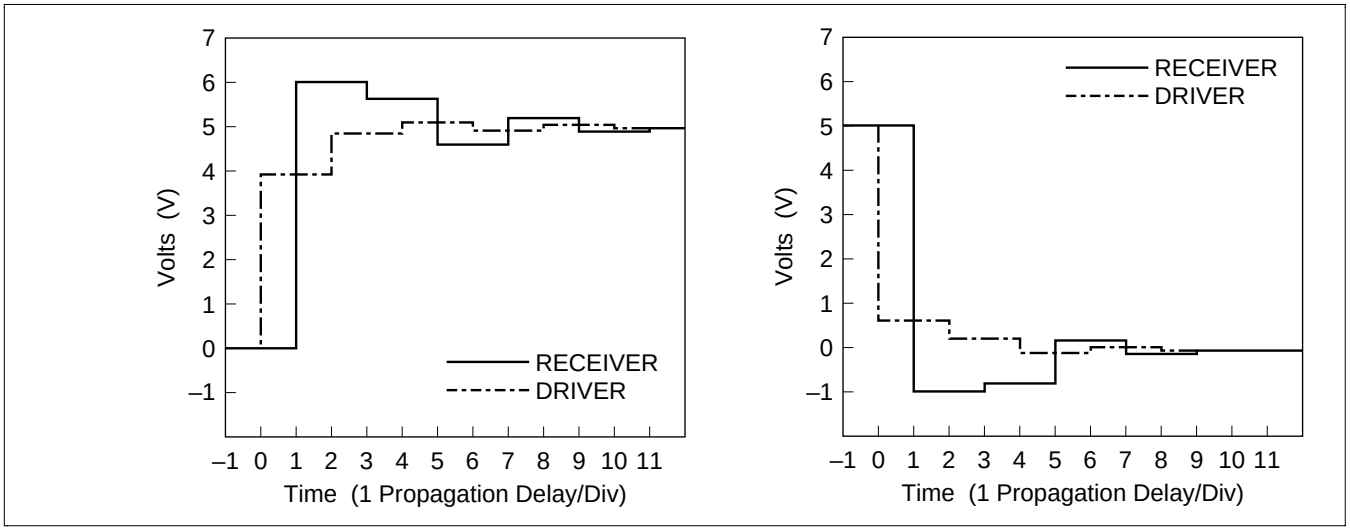


Figure 3 Resultant Waveforms Driving 50 Ω Line–Theoretical

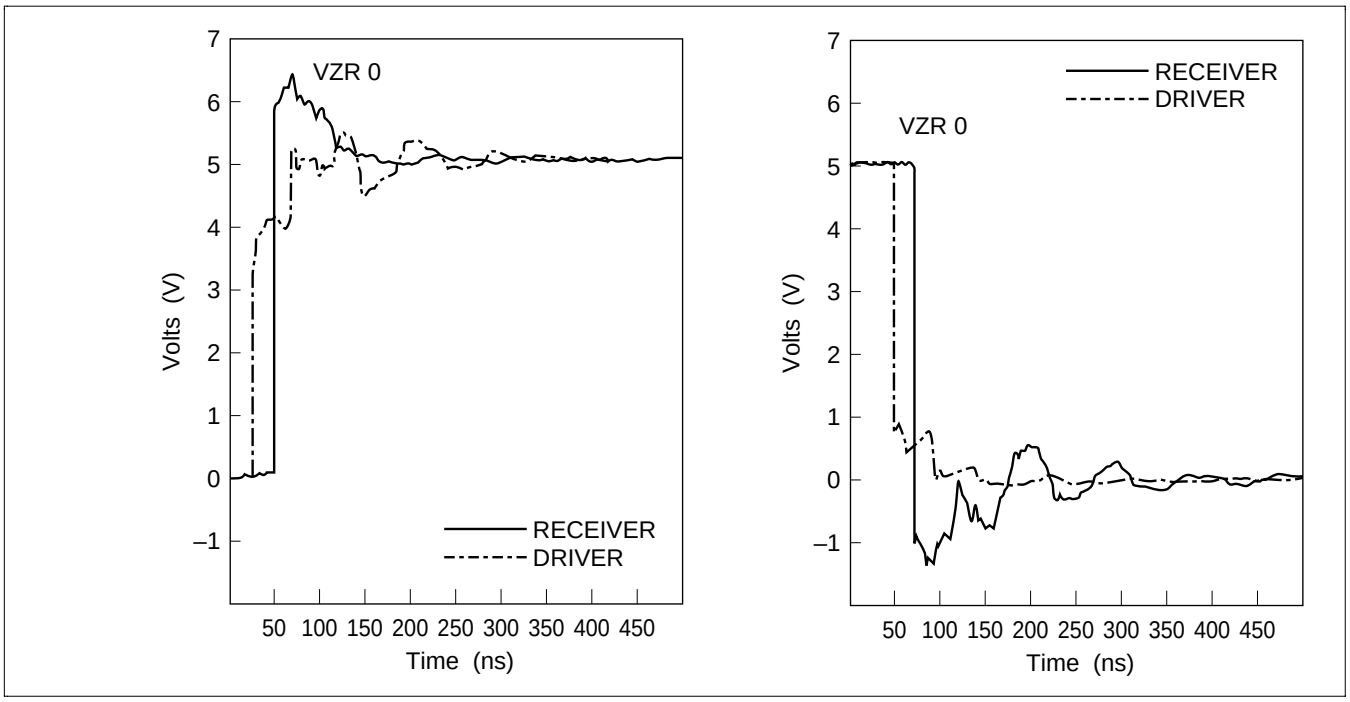


Figure 4 Resultant Waveforms Driving 50 Ω Line–Actual

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V_{CC}. The formula for calculating the current and voltage required is $| (V_{OQ}–V_I)/Z_O |$ at V_I. For V_{OQ} = 100 mV, V_{IH} = 3.85 V, V_{CC} = 5.5 V and Z_O = 50 Ω, the required I_{OH} at 3.85 V is 75 mA. For the high-to-low transition, V_{QQ} = 5.4 V, V_{IL} = 1.65 V, and Z_O = 50 Ω, I_{OL} is 75 mA at 1.65 V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50 Ω, the current requirements are less and switching is still guaranteed.

It is important to note that the typical 24 mA drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid V_{IN} level.

The performance charts in figures 5 to 7 are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltage.

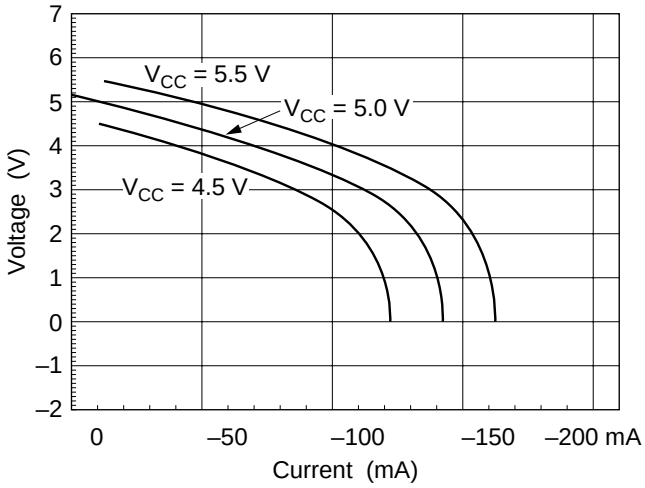


Figure 5 Output Characteristics V_{OH}/I_{OH}, HD74AC00

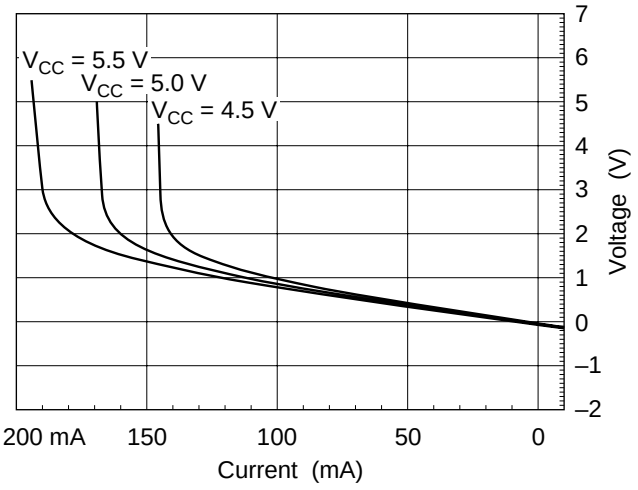


Figure 6 Output Characteristics V_{OL}/I_{OL}, HD74AC00

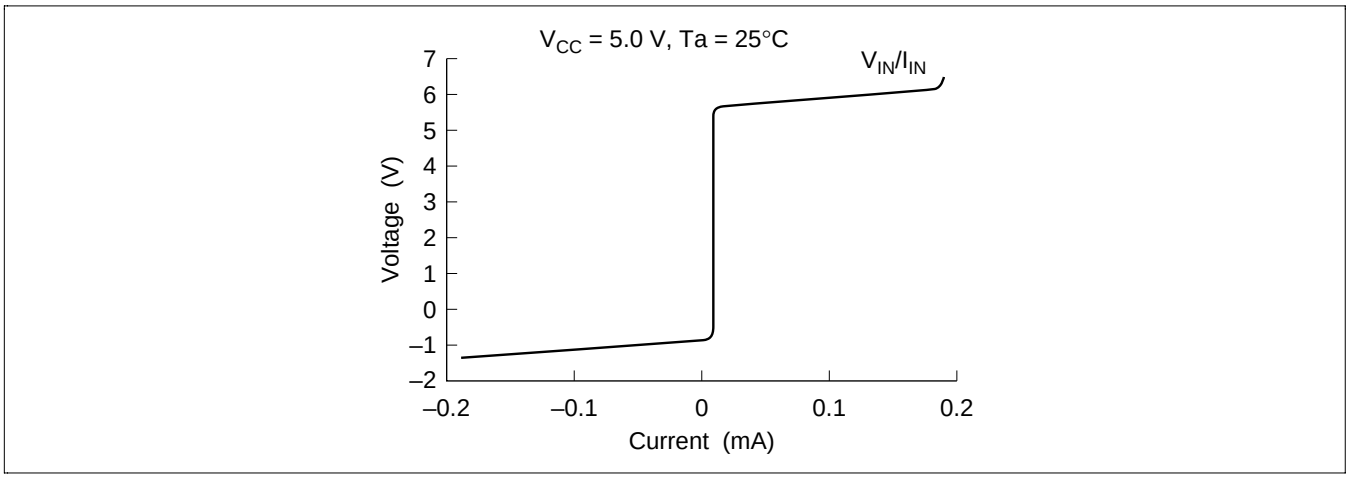


Figure 7 Input Characteristics V_{IN}/I_{IN}

1.8 Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low-voltage operation in memory cards, the JEDEC committee decided to establish interface standards for devices operating at 3.3 V ±0.3 V. To this end, Hitachi guarantees all of its devices operational at 3.3 V ±0.3 V. Note also that AC and DC specifications are guaranteed between 3.0 and 5.5 V. Operation of FACT logic is also guaranteed from 2.0 to 6.0 V on V_{CC}.

Operating Voltage Ranges

- FACT = 2.0 to 6.0 V
- ALS = 5.0 V ±10%
- LS = 5.0 V ±5%
- HC = 2.0 to 6.0 V

1.9 FACT Replaces LS, ALS, HCMOS

The Advanced CMOS family is specifically designed to outperform the LS, ALS, and HCMOS families. Figure 8 shows the relative position of various logic families in speed/power performance.

Table 1 summarizes the key performance specifications for various competitive technology logic families. Table 2 compares propagation delays.

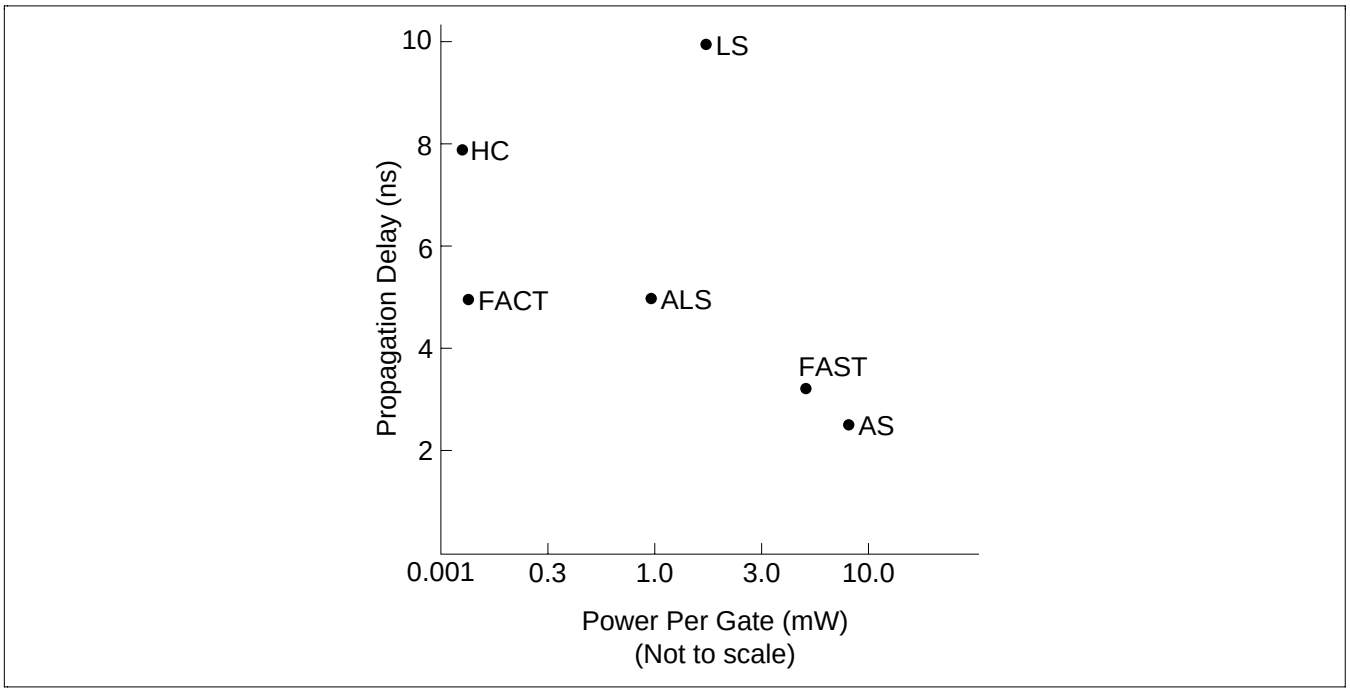


Figure8 Propagation Delays

Table 1a Logic Family Comparisons General Characteristics (All Max Ratings)

					FACT		
Characteristics	**Symbol**	**LS**	**ALS**	**HCMOS**	**HD74AC**	**HD74ACT**	**Unit**
Operating voltage range	$V_{CC/EE/DD}$	5 ± 5%	5 ± 10%	2.0 to 6.0	2.0 to 6.0	4.5 to 5.5	V
Operating temperature range		–20 to +75	0 to +70	–40 to +85	–40 to +85	–40 to +85	°C
Input voltage (limits)	V_{IH} (min)	2.0	2.0	3.15	3.15	2.0	V
	V_{IL} (max)	0.8	0.8	1.35	1.35	0.8	V
Output voltage (limits)	V_{OH} (min)	2.7	2.7	V_{CC} – 0.1	V_{CC} – 0.1	V_{CC} – 0.1	V
	V_{OL} (max)	0.5	0.5	0.1	0.1	0.1	V
Input current	I_{IH}	20	20	+1.0	+1.0	+1.0	µA
	I_{IL}	–400	–200	–1.0	–1.0	–1.0	µA
Output current at V_0 (limit)	I_{OH}	–0.4	–0.4	–4.0 @ V_{CC}– 0.37	–24 @ V_{CC}– 0.7	–24 @ V_{CC}– 0.7	mA
	I_{OL}	8.0	8.0	4.0 @ 0.33 V	24 @ 0.37 V	24 @ 0.37 V	mA
DC noise margin low/high	DCM	0.3/0.7	0.4/0.7	1.25/1.25	1.25/1.25	0.7/2.4	V

Table 1b Logic Family Comparisons Speed/Power Characteristics (All Typical Ratings)

					FACT		
Characteristics	**Symbol**	**LS**	**ALS**	**HCMOS**	**HD74AC**	**HD74ACT**	**Unit**
Quiescent supply current/Gate	I_G	0.4	0.2	0.0005	0.0005		mA
Power/gate (Quiescent)	P_G	2.0	1.2	0.0025	0.0025		mW
Propagation delay	t_P	10	5.0	8.0	5.0		ns
Speed power product	—	20	6.0	0.02	0.01		pJ
Clock frequency D/FF	f_{max}	33	50	50	160		MHz

Table 2 Propagation Delay

	Product		**LS**	**ALS**	**HCMOS**	**FACT**	**unit**
t_{PLH}/t_{PHL}	HD74XX00	Typ	10.0	5.0	8.0	5.0	ns
		Max	15.0	11.0	23.0	8.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	HD74XX74	Typ	25.0	12.0	14.0	8.0	ns
		Max	40.0	18.0	40.0	10.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	HD74XX163	Typ	18.0	10.0	18.0	5.0	ns
		Max	27.0	17.0	40.0	10.0	ns

Note: continuous: (LS) V_{CC} = 5.0 V, C_L = 15pF, 25°C;
(ALS/HC/FACT) V_{CC} = 5.0 V ± 10%, C_L = 50 pF, typ values at 25˚C, max values at 0 to 70˚C for ALS. –40 to +85˚C for HC/FACT.

2. Circuit Characteristics

2.1 Power Dissipation

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, FACT will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Power consumption of a circuit can be calculated using the formula:

$$P_D = [(C_L + C_{PD}) \bullet V_{CC} \bullet V_S \bullet f] + [I_Q \bullet V_{CC}]$$

where:

P_D = power dissipation
C_L = load capacitance
C_{PD} = device power capacitance
V_{CC} = power supply
V_S = output voltage swing
f = frequency of operation
I_Q = quiescent current

Power consumption for FACT is dependent on the supply voltage, frequency of operation, internal capacitance and load. V_S will be V_{CC} and I_Q can be considered negligible for CMOS. Therefore, the simplified formula for CMOS is:

$$P_D = (C_L + C_{PD})V_{CC}^2 f$$

C_{PD} values for CMOS devices are calculated by measuring the power consumption of a device at two different frequencies. C_{PD} is calculated in the following manner.

1. The power supply voltage is set to V_{CC} = 5.0 VDC.
2. Signal inputs are set up so that as many outputs as possible are switching, giving a worst-case situation per JEDEC C_{PD} conditions.

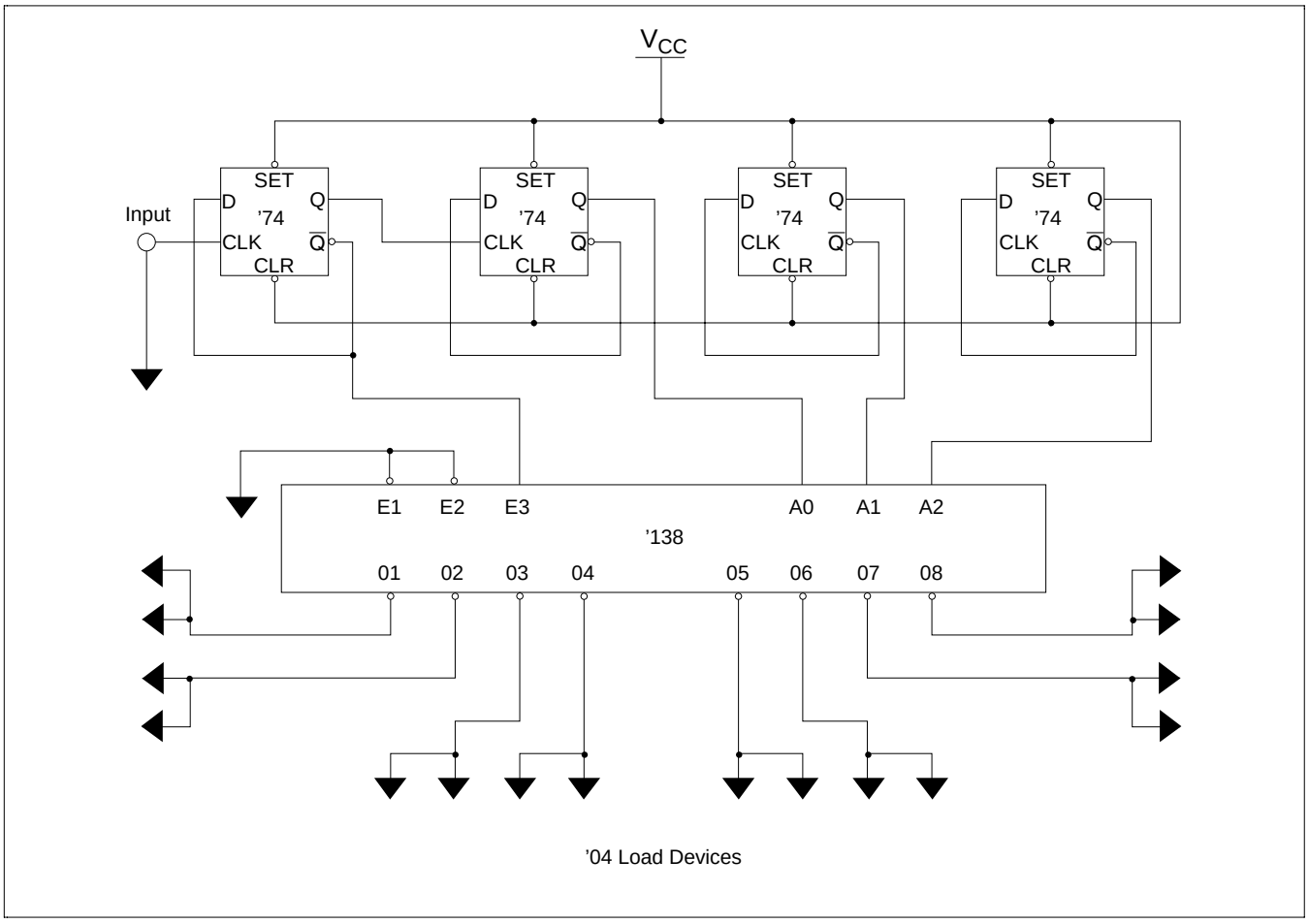


Figure 9 Power Demonstration Circuit Schematic

3. The power supply current is measure and recorded at input frequencies of 200 kHz and 1 MHz.
4. The power dissipation capacitance is calculated by solving the two simultaneous equations

$$P_1 = (C_{PD} \bullet V_{CC}^2 \bullet f_1) + (I_{CC} \bullet V_{CC})$$

$$P_2 = (C_{PD} \bullet V_{CC}^2 \bullet f_2) + (I_{CC} \bullet V_{CC})$$

giving

$$C_{PD} = (P_1 - P_2)/V_{CC}^2 (f_1 - f_2)$$

or

$$C_{PD} = (I_1 - I_2)/V_{CC}(f_1 - f_2)$$

where

I_1 = supply current at f_1 = 200 kHz.

I_2 = supply current at f_2 = 1 MHz

On FACT device data sheets, C_{PD} is a typical value and is given either for the package or for the individual device (i.e., gates, flip-flops, etc.) within the package.

The circuit shown in Figure 9 was used to compare the power consumption of FACT versus ALS devices.

Two identical circuits were built on the same board and driven from the same input. In the circuit, the input signal was driven into four D-type flip-flops which act as divide-by-2 frequency dividers. The outputs from the flip-flops were connected to the inputs of a HD74AC138/74ALS138 decoder. This generated eight non-overlapping clock pulses on the outputs of the HD74AC138/74ALS138, which were then connected to an HD74AC04/74ALS04 inverter. The input frequency was then varied and the power consumption was measured. Figure 10 illustrates the results of these measurements.

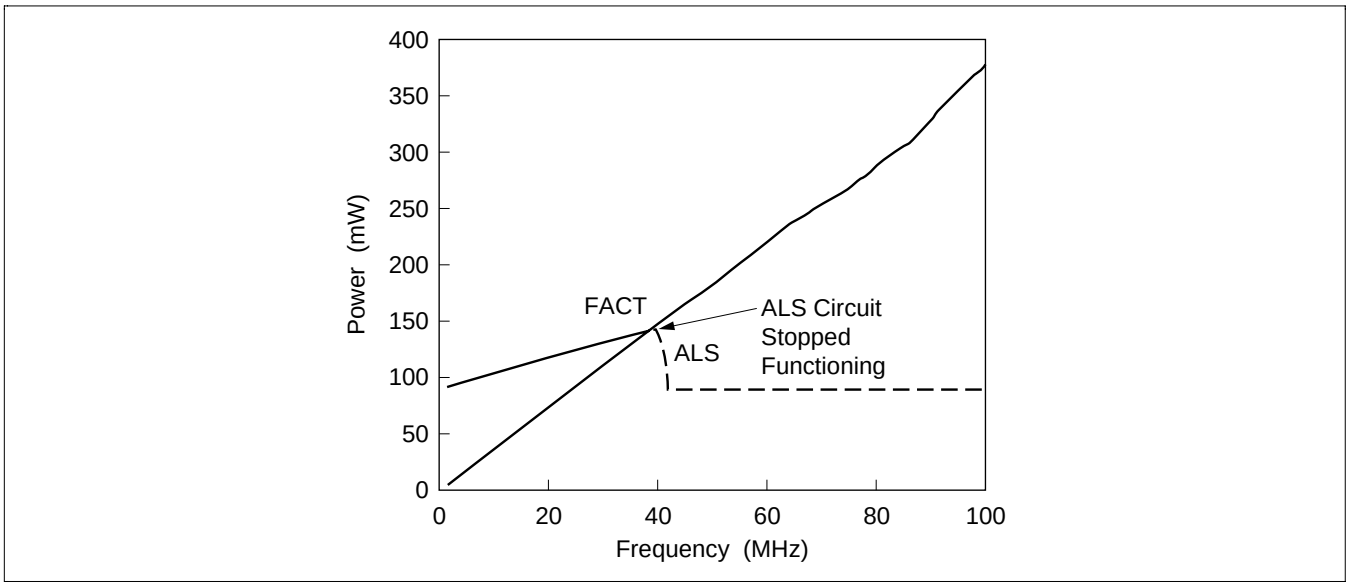


Figure 10 FACT vs ALS Circuit Power

Below 40 MHz, the FACT circuit dissipates much less power than the ALS version. It is interesting to note that when the frequency went to zero, the FACT circuit's power consumption also went to zero; the ALS circuit continued to dissipate almost 100 mW. Another advantage of FACT is its capabilities above 40 MHz. At this frequency, the first 74ALS74 D-type flip-flop ceased to operate. Once this occurred, the entire circuit stopped working and the power consumption fell to its quiescent value. The FACT device, however, continued functioning beyond the limit of the frequency generator, which was 100 MHz.

This graph shows two advantages of FACT circuits (power and speed). FACT logic delivers increased performance in addition to offering the power savings of CMOS.

2.2 Capacitive Loading Effects

In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of FACT devices. Minimum delay numbers may be determined from table 3. Propagation delays are measured to the 50% point of the output waveform.

Table 3 Minimum Propagation Delay

	Voltage(V)			
Parameter	**3.0**	**4.5**	**5.5**	**Units**
T_{rise}	31	22	19	ps/pF
t_{fall}	18	13	12.5	ps/pF

Note: TA = 25˚C

The two graphs following, figures 11 and 12, describe propagation delays on FACT devices as affected by variations in power supply voltage (V_{CC}) and lumped load capacitance (C_L). Figures 13 and 14 show the effects of lumped load capacitance on rise and fall times for FACT devices.

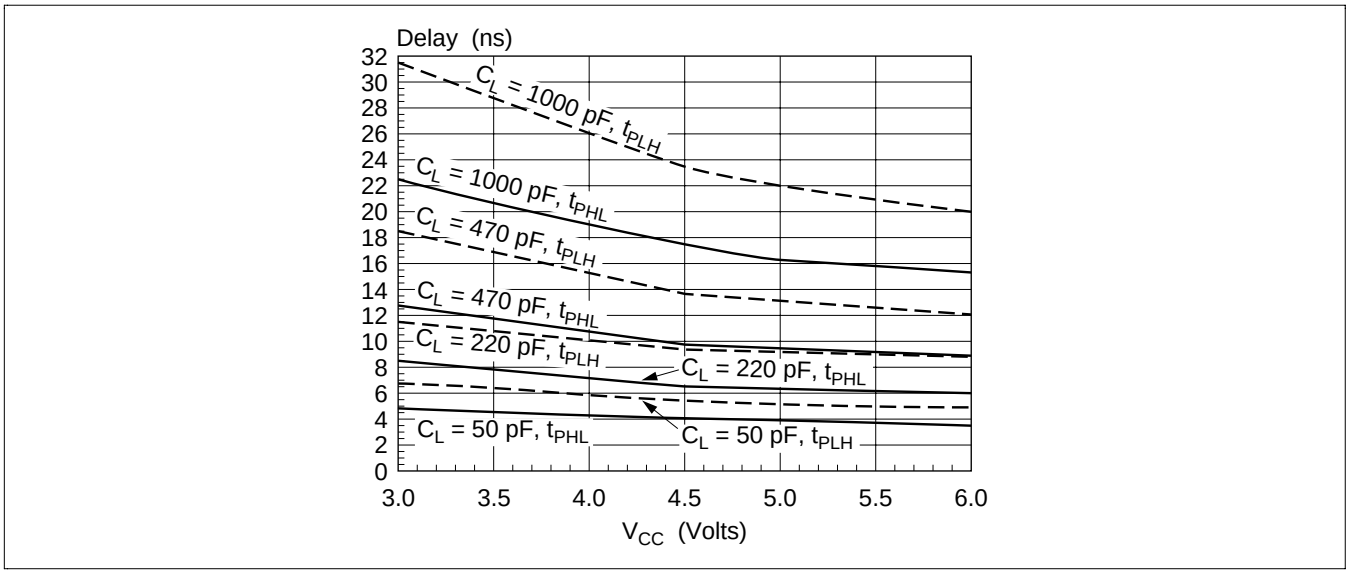


Figure 11 Propagation Delay vs. V_{CC} (HD74AC00)

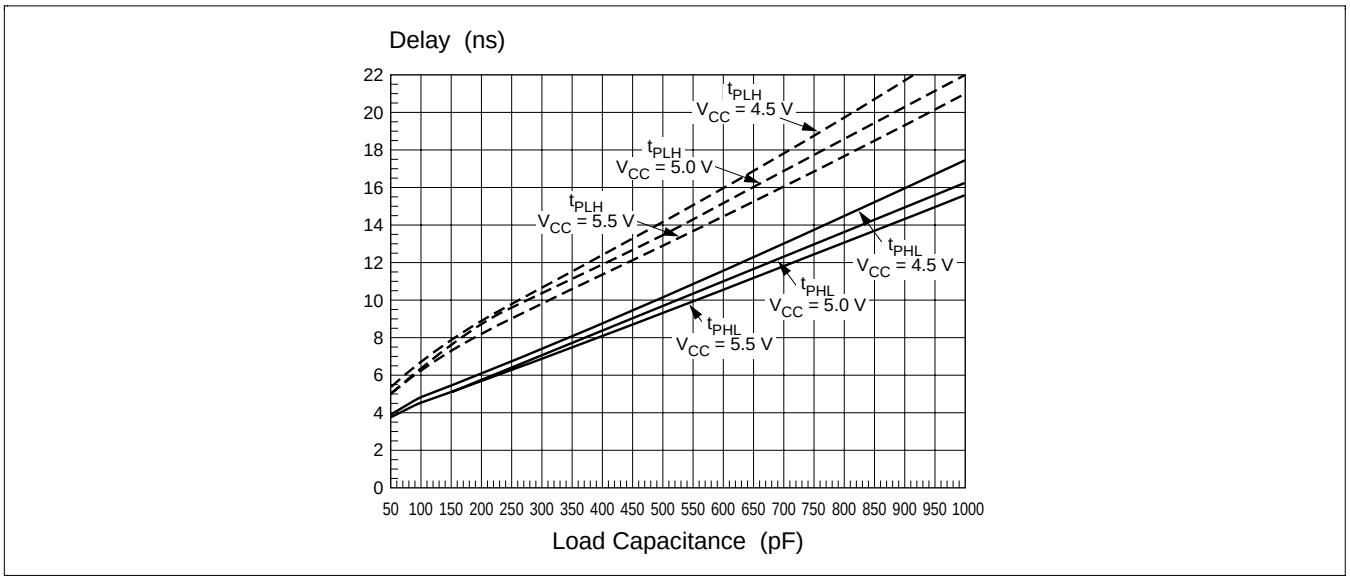


Figure 12 Propagation Delay vs. C_L (HD74AC00)

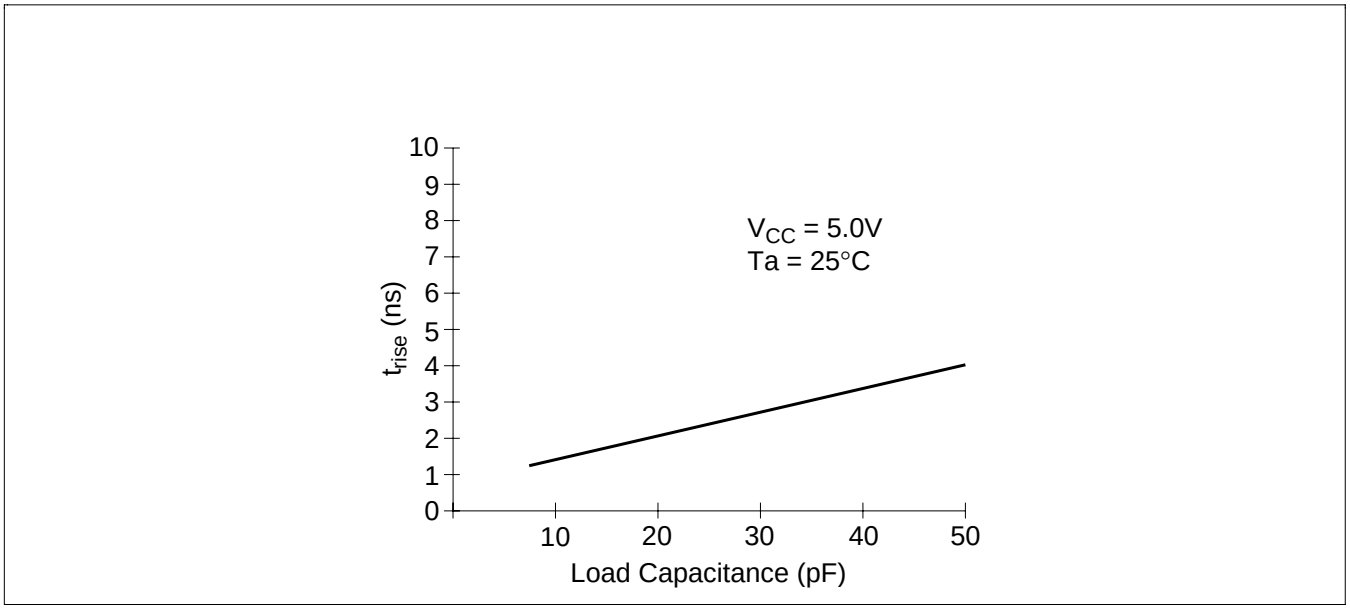


Figure 13 t_{rise} vs. Capacitance

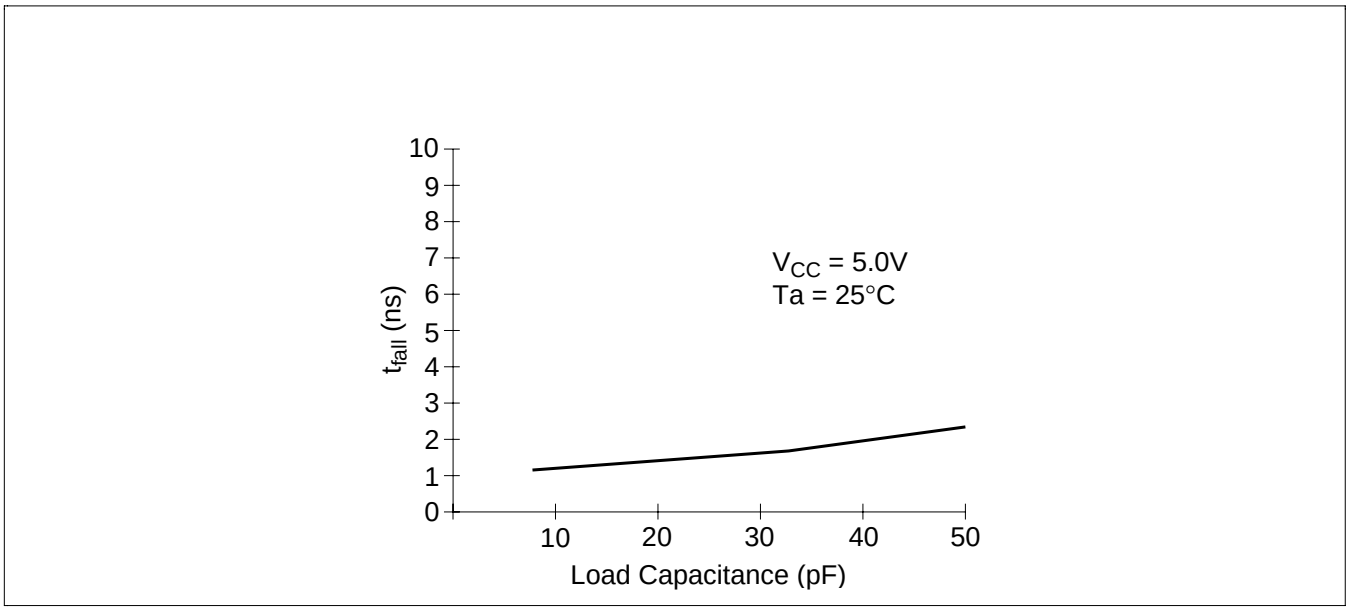


Figure 14 t_{fall} vs. Capacitance

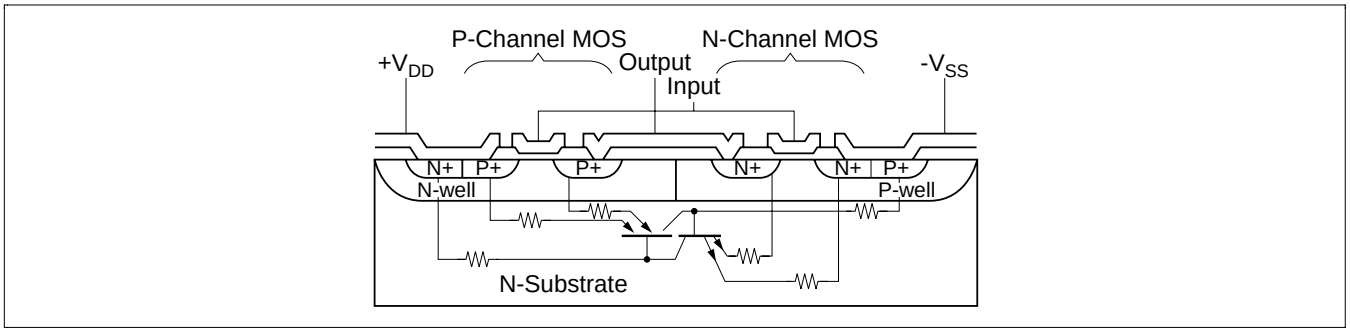


Figure 15 CMOS Inverter Cross Section with Latch-up Circuit Schematic

2.3 Latch-up

A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance (figure 15). FACT logic is guaranteed not to latch-up with dynamic currents of 100 mA forced into or out of the inputs or the outputs under worst case conditions (Ta = 85˚C and V_{CC} = 5.5 VDC). At room temperature the parts can typically withstand dynamic currents of over 450 mA. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

FACT devices have been specifically designed to reduce the possibility of latch -up occurring; Hitachi accomplished this by lowering the gain of the parasitic transistors, reducing N-well and p-well resistivity to increase external drive current required to cause a parasitic to turn on, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

2.4 Electrostatic Discharge (ESD) Sensitivity

FACT circuits show excellent resistance to ESD-type damage. These logic devices are classified as category 'B' of MIL-STD-883C, test method 3015, and withstand 4000 V typically. FACT logic is guaranteed to have 2000 V ESD immunity on all inputs and outputs. FACT parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 16 shows the ESD test circuit used in the sensitivity analysis for this specification. Figure 17 is the pulse waveform required to perform the sensitivity test.

The test procedure is as follows: five pulses, each of 2000 V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MIL-STD-883C, TM-3015. For further specifications of TM-3015, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.

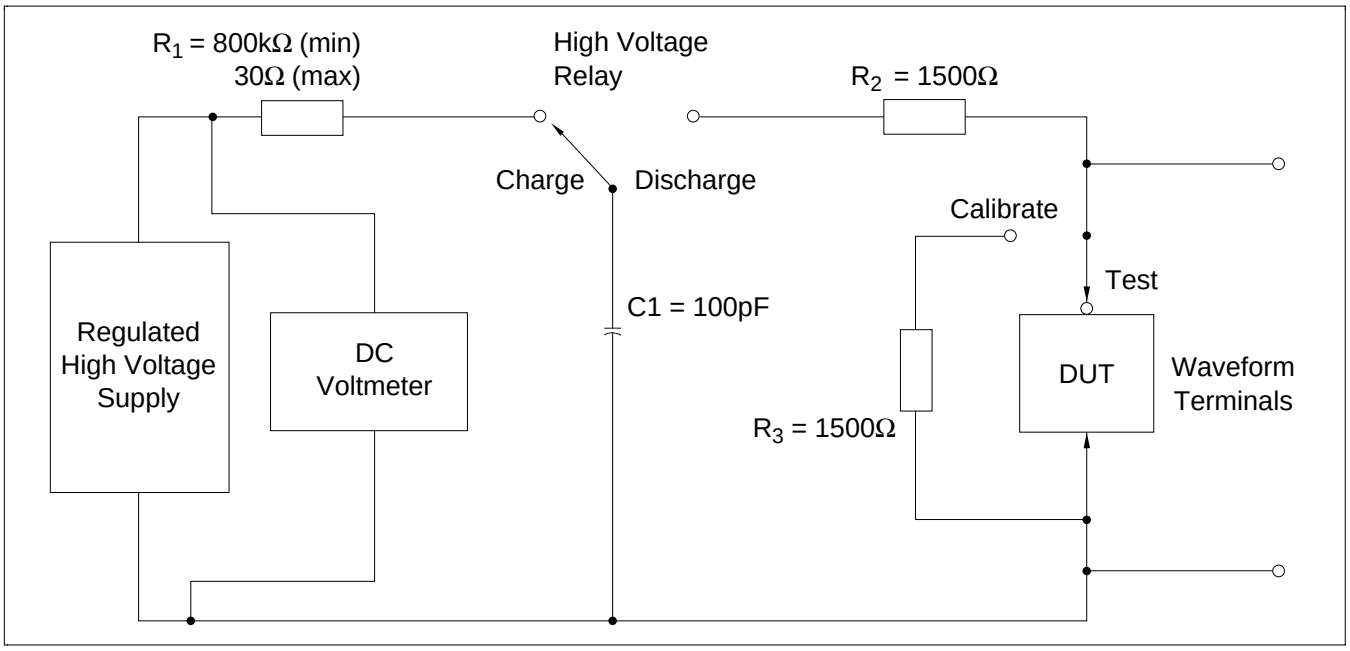


Figure 16 ESD Test Circuit

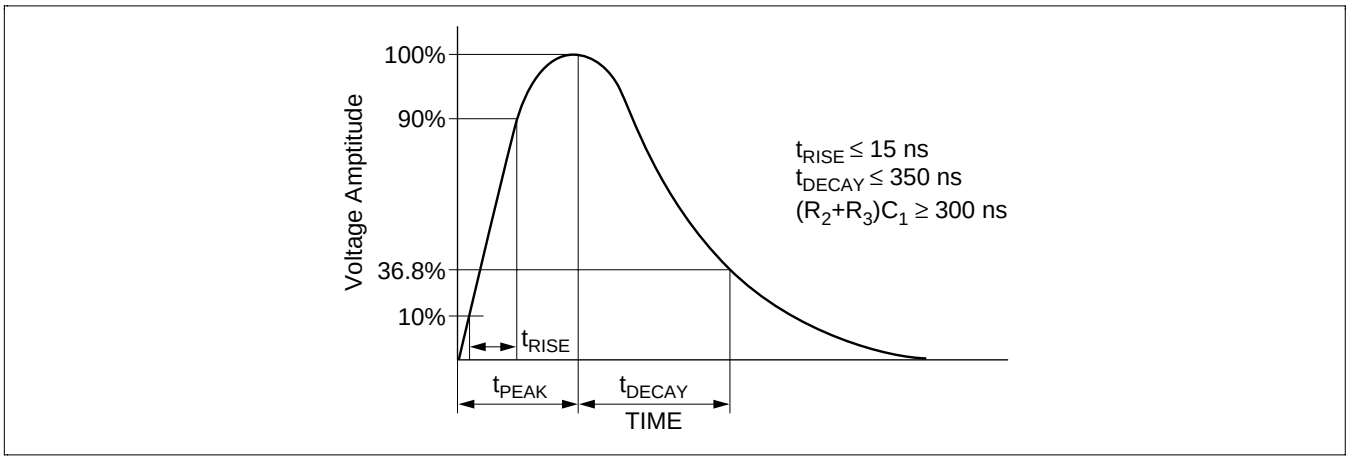


Figure 17 ESD Pulse Waveform

Definition of Specifications

1. Power Dissipation-Test Philosophy

In an erfort to reduce confusion about measuring C_{PD}, a JEDEC standard test procedure (7A Appendix E) has been adopted, which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison. All device measurements are made with V_{CC} = 5.0 V at 25°C, with 3-state outputs both enabled and disabled.

- Gates: Switch one input. Bias the remaining inputs such that the output switches.
- Latches: Switch the Enable and D inputs such that the latch toggles.
- Flip-Flops: Switch the clock pin while changing D (or bias J and K) such that the output (s) change each clock cycle. For parts with a common clock, exercise only one flip - flop.
- Decoders: Switch one address pin which changes two outputs.
- Multiplexers: Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.
- Counters: Switch the clock pin with other inputs biased such that the device counts.
- Shift Registers: Switch the clock pin with other inputs biased such that the device counts.
- Transceivers: Switch one data input. For bidirectional devices enable only one direction.
- Parity Generator: Switch one input.
- Priority Encoders: Switch the lowest priority input.
- Load Capacitance: Each output which is switching should be loaded with the standard 50 pF. The equivalent load capacitance, based upon the number of outputs switching and their respective frequency, is then subtracted form the measured gross C_{PD} number to obtain the device's actual C_{PD} value.

If the device is tested at a high enough frequency, the static supply current can be ignored. Thus at 1 MHz, the following formula can be used to calculate C_{PD}:

$$C_{PD} = I_{CC} / (V_{CC}) (1 \times 10^{6}) - \text{Equivalent Load Capacitance}$$

2. Ratings and Specifications

Table 1 Absolute Maximum Ratings*1

Parameter	Symbol	Limit	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7.0	V	
DC input Diode current or DC input voltage	I_{IK}	–20	mA	V_I = –0.5
		20	mA	V_I = V_{CC} +0.5
	V_I	–0.5 to V_{CC} +0.5	V	
DC output Diode current or DC output voltage	I_{OK}	–50	mA	V_O = –0.5
		50	mA	V_O = V_{CC} +0.5
	V_O	–0.5 to V_{CC} +0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC} or I_{GND}	±50	mA	
Storage temperature	T_{STG}	–65 to 150	°C	

Note: 1. Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. Hitachi does not recommend operation of FACT circuits outside databook specifications.

Table 2 Recommended Operating Conditions

Parameter		Symbol	Limit	Unit	Condition
Supply Voltage (unless otherwise specified)	AC devices	V_{CC}	2.0 to 6.0	V	
	ACT devices		4.5 to 5.5		
Input voltage		V_I	0 to V_{CC}	V	
Output voltage		V_O	0 to V_{CC}	V	
Operating temperature		T_A	–40 to +85	°C	
Input rise and Fall time*1 (typical)		tr, tf	150	ns/V	V_{CC} @ 3.0V
(except Schmitt inputs) 'AC devices V_{IN} from			40	ns/V	V_{CC} @ 4.5V
30% to 70% of V_{CC}			25	ns/V	V_{CC} @ 5.5V
Input rise and Fall time*1 (typical)		tr, tf	10	ns/V	V_{CC} @ 4.5V
(except schmitt inputs) 'ACT devices V_{IN} from			8	ns/V	V_{CC} @ 5.5V
0.8 to 2.0 V, V_{meas} from 0.8 to 2.0V					

Note: 1. See individual data sheets for those devices which differ from the typical input rise and fall times noted here.

Table 3 DC Characteristics for HD74AC Family Devices

			Ta = +25°C	Ta = –40 to +85°C			
Parameter	**Symbol**	**V_{CC} (V)**	**Typ**	**Guaranteed Limit**		**Unit**	**Condition**
Minimum	V_{IH}	3.0	1.5	2.1	2.1	V	Vout = 0.1V or
High Level Input		4.5	2.25	3.15	3.15		V_{CC} –0.1V
Voltage		5.5	2.75	3.85	3.85		
Maximum	V_{IL}	3.0	1.5	0.9	0.9	V	Vout = 0.1 V or
Low Level Input		4.5	2.25	1.35	1.35		V_{CC} –0.1V
Voltage		5.5	2.75	1.65	1.65		
Maximum	V_{OH}	3.0	2.99	2.9	2.9	V	I_{OUT} = –50 µA
High Level		4.5	4.49	4.4	4.4		
Output Voltage		5.5	5.49	5.4	5.4		
		3.0		2.58	2.48	V	V_{IN} = V_{IL} or V_{IH}
		4.5		3.94	3.80		–12 mA I_{OH} –24 mA
		5.5		4.94	4.80		*[1] –24 mA
Maximum	V_{OL}	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 µ A
Low Level		4.5	0.001	0.1	0.1		
Output Voltage		5.5	0.001	0.1	0.1		
		3.0		0.32	0.37	V	V_{IN} = V_{IL} or V_{IH}
		4.5		0.32	0.37		12 mA I_{OL} 24 mA
		5.5		0.32	0.37		*[1] 24 mA
Maximum Input Leakage Current	I_{IN}	5.5		±0.1	±1.0	µA	V_I = V_{CC}, GND
Maximum 3-State Current	I_{OZ}	5.5		±0.5	±5.0	µA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
Minimum Dynamic Output Current *[2]	I_{OLD}	5.5			86	mA	V_{OLD} = 1.1 V
	I_{OHD}	5.5			–75	mA	V_{OHD} = 3.85 V

Notes: 1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0 ms, one output loaded at a time.

Table 4 DC Characteristics for HD74ACT Family Devices

			Ta = +25°C	Ta = –40 to +85°C			
Parameter	**Symbol**	**V_{CC} (V)**	**Typ**	**Guaranteed Limit**		**Unit**	**Condition**
Minimum High	V_{IH}	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or
Level Input		5.5	1.5	2.0	2.0		V_{CC} –0.1V
Voltage							
Maximum Low	V_{IL}	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1 V or
Level Input		5.5	1.5	0.8	0.8		V_{CC} –0.1V
Voltage							
Maximum High	V_{OH}	4.5	4.49	4.4	4.4	V	I_{OUT} = –50 µA
Level		5.5	5.49	5.4	5.4		
Output Voltage		4.5		3.94	3.80	V	V_{IN} = V_{IL} or V_{IH}
		5.5		4.94	4.80		I_{OH} –24 mA
							*[1] –24 mA
Maximum Low	V_{OL}	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 µA
Level Output		5.5	0.001	0.1	0.1		
Voltage		4.5		0.32	0.37	V	V_{IN} = V_{IL} or V_{IH}
		5.5		0.32	0.37		I_{OL} 24 mA
							*[1] 24 mA
Maximum Input Current	I_{IN}	5.5		±0.1	±1.0	µA	V_I = V_{CC}, GND
Maximum 3-State Current	I_{OZ}	5.5		±0.5	±5.0	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
Maximum I_{CC}/Input Current	I_{CCT}	5.5	0.6		1.5	mA	V_I = V_{CC} – 2.1V
Minimum Dynamic Output Current *[2]	I_{OLD}	5.5			86	mA	V_{OLD} = 1.1 V
	I_{OHD}	5.5			–75	mA	V_{OHD} = 3.85 V

Notes: 1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0 ms, one output loaded at a time.

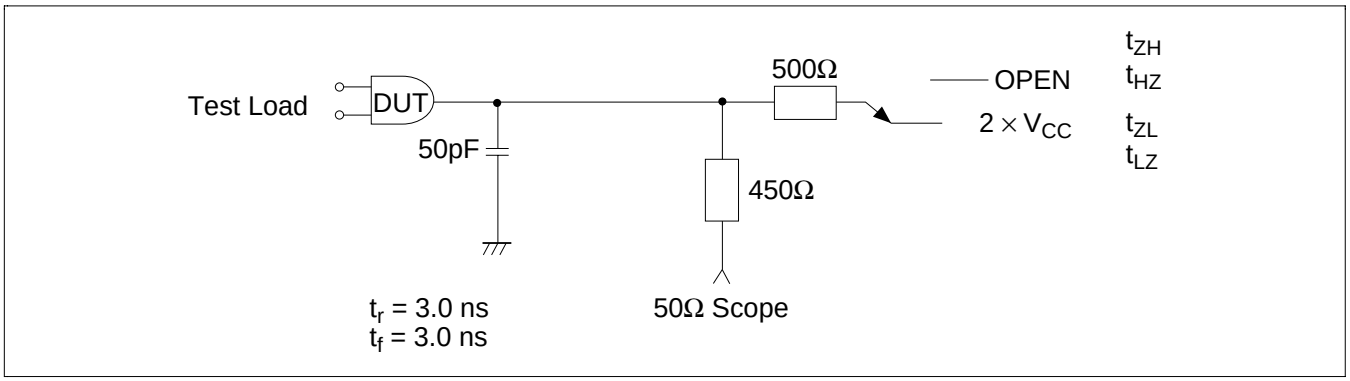


Figure 1 AC Loading Circuit

3. AC Loading and Waveforms

3.1 Loading Circuit

Figure 1 shows the AC loading circuit used in characterizing and specifying propagation delays of all FACT devices (HD74AC and HD74ACT) unless otherwise specified in the data sheet of a specific device.

The use of this load, differs somewhat from previous practice provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance and implied the use of high-impedance, high-frequency scope probes. FACT circuits changed to 50 pF of capacitance, allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions.

This more closely resembles the inloading to be expected in average applications and thus gives the designer more useful delay figures. We have incorporated this scheme into the FACT product line. The net effect of the change in AC load is to increase the average observed propagation delay by about 1 ns.

The 500 Ω resistor to ground can be a high-frequency passive probe for a sampling oscilloscope, which costs much less than the equivalent high-impedance probe. Alternately, the 500 Ω resistor to ground can simply be a 450 Ω resistor feeding into a 50 Ω coaxial cable leading to a sampling scope input connector, with the internal 50 Ω termination of the scope completing the path to ground. This is the preferred scheme for correlation. (See figure 1.) With this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50 Ω termination for the pulse generator that supplies the input signal.

Shown in figure 1 is a second 500 Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring one set of the Enable/Disable parameters (low-to-off and off-to-low) of a 3-state output. With the switch closed, the pair of 500 Ω resistors and the $2 \times V_{CC}$ supply voltage establish a quiescent high level.

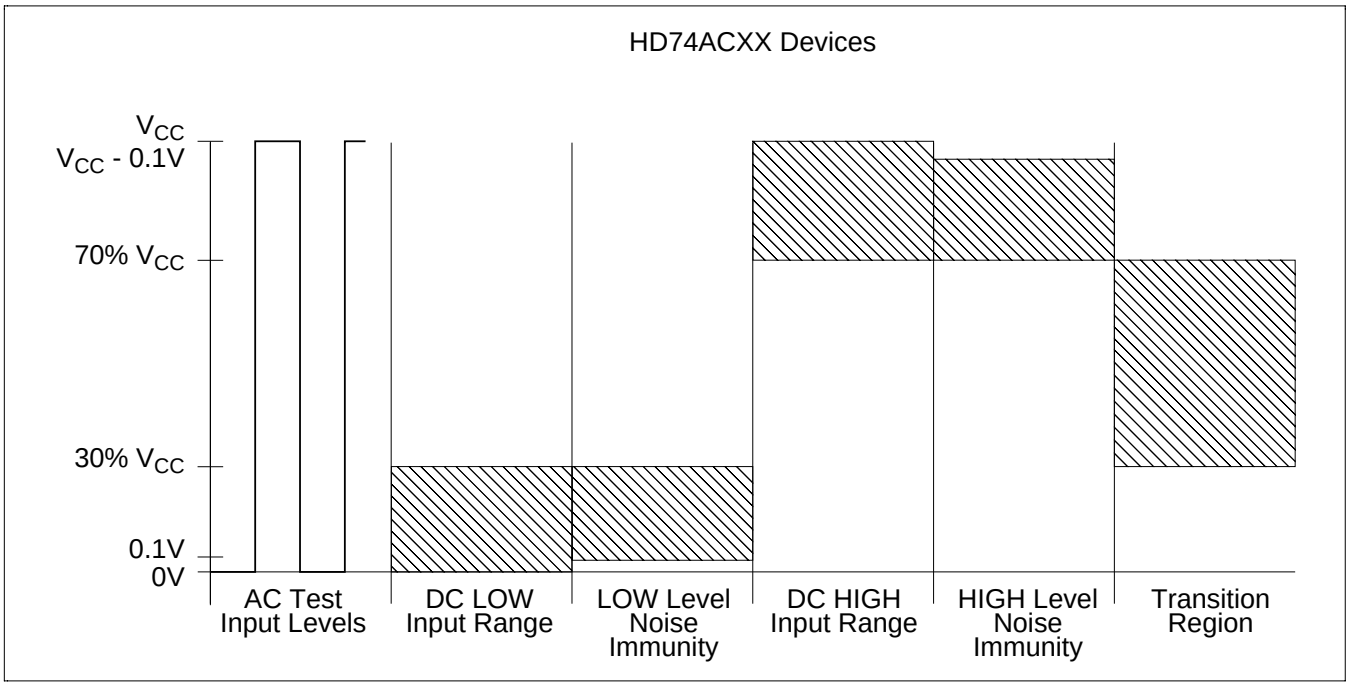


Figure 2a Test Input Signal Levels

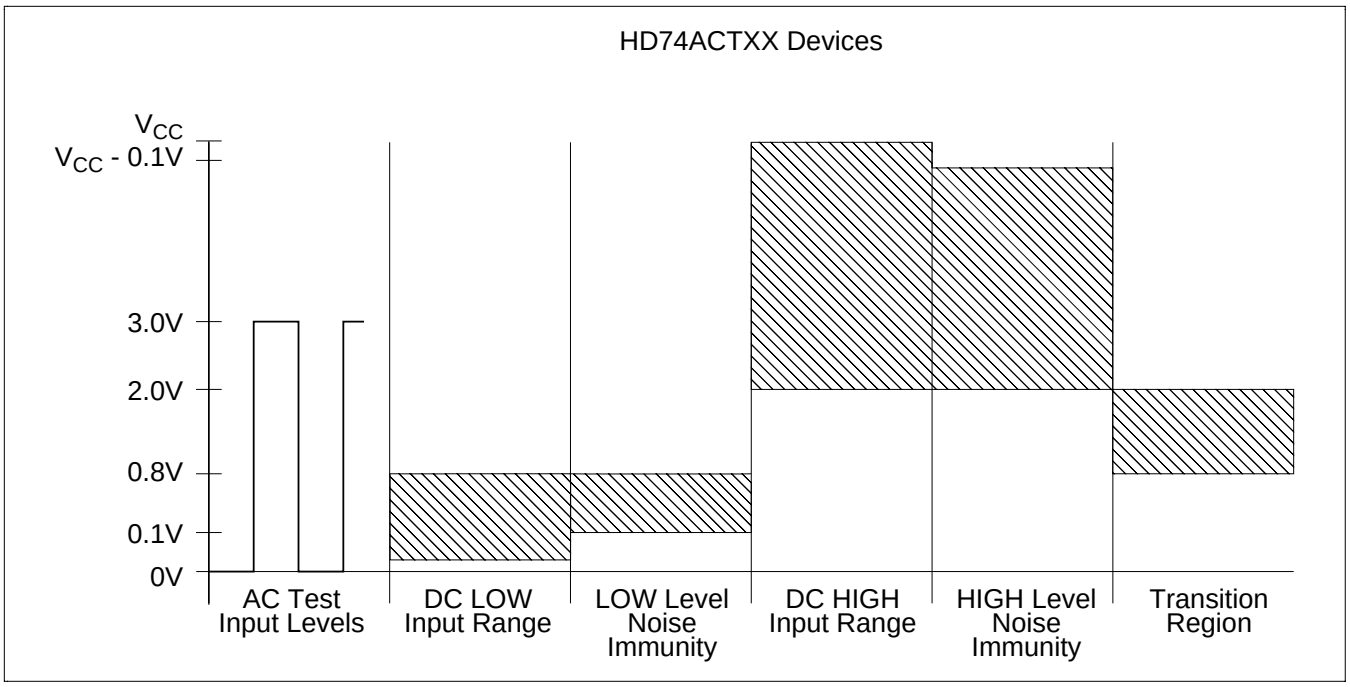


Figure 2b Test Input Signal Levels (cont)

3.2 Test Conditions

Figure 2 describes the input signal voltage levels to be used when testing FACT circuits. The AC test conditions follow industry convention requiring V_{IN} to range from 0 V for a logic low to 3.0 V for a logic high for HD74ACT devices and 0 V to V_{CC} for HD74AC devices. The DC parameters are normally tested with V_{IN} at guaranteed input levels, that is V_{IH} to V_{IL} (see tables 3 and 4 for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handlder not specifically designed for high-speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be see in a system.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 5.0 V then dropping it to a level corresponding to V_{IH}, and then raising it again to the 5.0 V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0 V to V_{IL}, then returning it to 0 V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs of the FACT device.

Good high-frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

3.3 Rise and Fall Times

Input signals should have rise and fall times of 3.0 ns and signal swing of 0 V to 3.0 V for HD74ACT devices or 0 V to V_{CC} for HD74ACT devices. Rise and fall times less than or equal to 1 ns should be used for testing f_{max} or pulse widths.

CMOS devices, including, 4000 Series CMOS, HC, HCT and FACT families, tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, FACT devices can be more sensitive to slow input rise and fall times than other lower performance technologies.

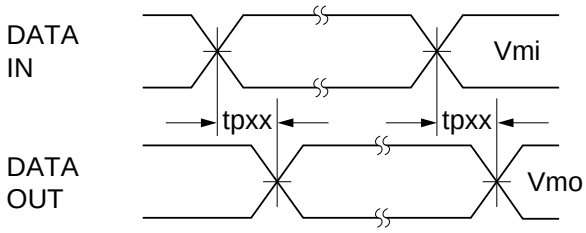
It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a high level to a low level, or from a low level to a high level, this capacitance has to be charged or discharged. With the present high performance technologies, this charging or discharging takes place in a very short time, typically 2-3 ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the V_{CC} or ground leads inside the package due to the inductance of these leads. The internal ground of the chip will change in reference to the outside world become of this induced voltage.

Consider the input. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the device threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold region enough so that it re-crosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have V_{CC} and ground leads with a finite inductance. This inductance needs to be added to the inductance in the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems. With FACT logic having gains as high as 100, it merely takes a 50 mV change in the input to generate a full 5 V swing on the output.

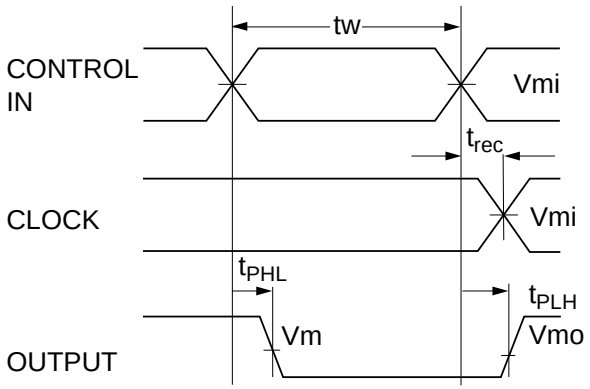
3.4 Propagation Delays, f_{max}, Set and Hold Times

A 1.0 MHz square wave is recommended for most propagation delay tests (figures 3 and 4) The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time etc.



Vmi = 50% V_{CC} for HD74AC devices; 1.5 V for HD74ACT devices
Vmo = 50% V_{CC} for HD74AC/HD74ACT devices

Figure 3 Waveform for Inverting and Non-Inverting Functions

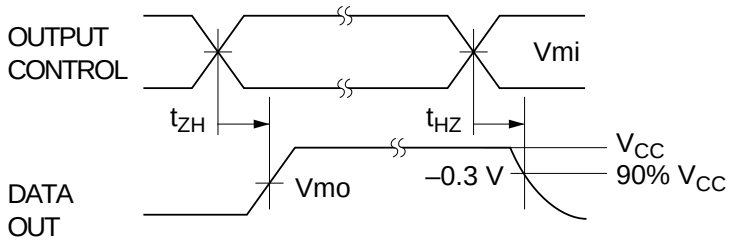


Vmi = 50% V_{CC} for HD74AC devices; 1.5 V for HD74ACT devices
Vmo = 50% V_{CC} for HD74AC/HD74ACT devices

Figure 4 Propagation Delay, Pulse Width, and t_{rec} Waveforms

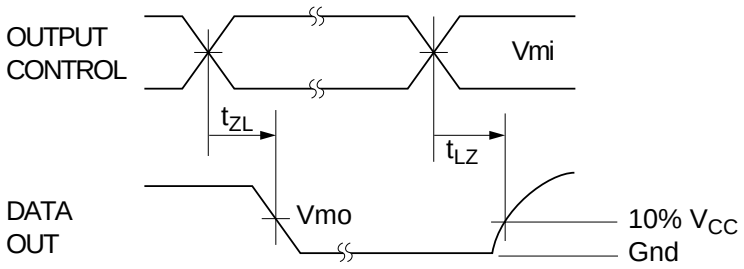
3.5 Enable and Disable Times

Figures 5 and 6 show that the disable times are measured at the point where the output voltage has risen or fallen by 10% from the voltage rail level (i.e., ground for t_{LZ} or V_{CC} for t_{HZ}) . This change enhances the repeatability of measurements, reduces test time, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high-impedance state rising or falling waveform is RC-controlled, the first 10% of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 10% is adequate to ensure that a device output has turned off. Measuring to a larger change in voltage merely exaggerates the apparent Disable time and thus penalizes system performance since the designer must use the Enable and Disable times to device worst case timing signals to ensure that the output of one device is disabled befor that of another device is enabled.



Vmi = 50% V_{CC} for HD74AC devices; 1.5 V for HD74ACT devices
Vmo = 50% V_{CC} for HD74AC/HD74ACT devices

Figure 5 3-State Output High Enable and Disable Times

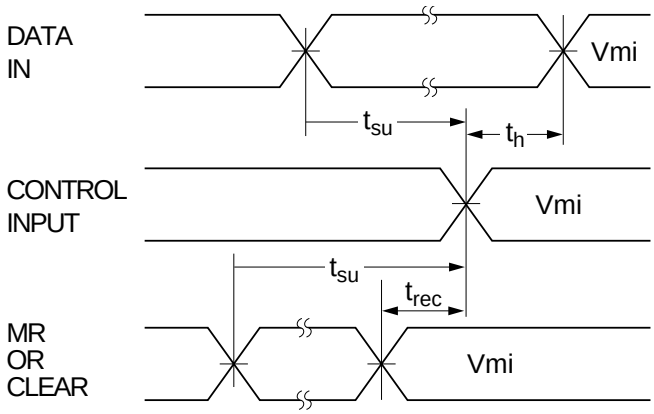


Vmi = 50% V_{CC} for HD74AC devices; 1.5 V for HD74ACT devices
Vmo = 50% V_{CC} for HD74AC/HD74ACT devices

Figure 6 3-State Output Low Enable and Disable Times

3.6 Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. More often, handling equipment that is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, that are near the device, are conductive and connected to ground.



Vmi = 50% V_{CC} for HD74AC devices; 1.5 V for HD74ACT devices
Vmo = 50% V_{CC} for HD74AC/HD74ACT devices

Figure 7 Setup Time, Hold Time and Recovery Time

4. Symbols and Terms Defined for HD74AC Series

Explanation of Symbols Used in Electrical Characteristics and Recommended Operating Conditions

Table 5 DC Characteristics

Symbol	Term	Description
V_{IH}	High level input voltage	High level input voltage to ensure that a logic element operates under some constraint
V_{IL}	Low level input voltage	Low level input voltage to ensure that a logic element operates under some constraint
V_{OL}	Low level output voltage	Output voltage in effect when, under the input condition for bringing the output low, the rated output current is allowed to flow to the output terminal
V_{OH}	High level output voltage	Output voltage in effect when, under the input condition for bringing the output high, the rated output current is allowed to flow to the output terminal
V_t^+	Forward input threshold voltage	Input voltage in effect when the operation of a logic element varies as the input is allowed to go up form a voltage level lower than the reverse input threshold voltage V_t^-
V_t^-	Reverse input threshold voltage	Input voltage in effect when the operation of a logic element varies as the input is allowed to drop up form a voltage level higher than the forward input threshold voltage V_t^+
V_h	Hysteresis voltage	Difference between forward input threshold voltage V_t^+ and reverse threshold voltage V_t^-
I_{IN}	Input leakage current	Input current that flows in when the rated maximum input voltage is applied to the input terminal
I_{OZ}	Off-state output current (high-impedance)	Current that flows to the 3-state output of an element under the input condition for bringing the output to high-impedance state
I_{CC}	Quiescent Supply current	Current that flows to the supply therminal (V_{CC}) under the rated input condition
I_{OLD}	Minimum Dynamic Output Current	Output current that flows in when, under the condition for bringing the output low,the output terminal is tied to the rated out voltage V_{OLD}.
I_{OHD}		Output current that flows out when, under the condition for bringing the output high, the output terminal is tied to the rated out voltage V_{OHD}.
I_{CCT}	Maximum I_{CC} /Input	Current that flows to the supply terminal (V_{CC}) under the rated input condition

Table 6 AC Characteristics

Symbol	Term	Description
f_{max}	Maximum clock frequency	Maximum clock frequency that maintains the stable changes in output logic level in the rated sequence under the I/O condition allowing clock pulses to change the output state
t_{TLH}	Rise (transient) time	Rated time from low level to high level of a wavefrom during the defined transient period changing from low level to high level
t_{THL}	Fall (transient) time	Rated time from high level to low level of a wavefrom during the defined transient period changing from high level to low level
t_{PLH}	Output rise propagation delay time	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the output changing from low level to high level
t_{PHL}	Output fall propagation delay time	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the output changing from high level to low level
t_{HZ}	3-state output disable time (high level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from high level to the high-impendance state
t_{LZ}	3-state output disable time (low level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from low level to the high-impendance state
t_{ZH}	3-state output enable time (high level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from the high-impendance state to high level
t_{ZL}	3-state output enable time (low level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from the high-impendance state to low level
t_w	Pulse width	Duration of time between the rated levels from a leading edge to a trailing edge of a pulse waveform
t_h	Hold time	Time in which to hold data at the specified input terminal after a change at another related input terminal (e.g., clock input)
t_{SU}	Setup time	Time in which to set up and keep data at the specified input terminal before a change at another related input terminal (e.g., clock input)

Symbol	Term	Description
t_{rec}	Recovery time	Time period between the time when data at the specified input terminal is released and the time when another related input terminal (e.g., clock input) can be changed
C_{IN}	Input capacitance	Capacitance between GND terminal and an input terminal to which 0 V is applied
C_{PD}	Power Dissipation Capacitance	Equivalent device power capacitance in dynamic state

Table 7 Explanation of Symbols Used in Function Tables

Symbol	Description
H	High level (in steady state; written H or "H" level in sentences)
L	Low level (in steady state; written L or "L" level in sentences)
⎍	Transition from L level to H level
⎏	Transition from H level to L level
X	Either H or L
Z	3-state output off (high impedance)
a·····h	Input level of steady state for each of inputs A-H
Q_0	Q level immediately before the indicated input condition is established
$\overline{Q}_0$	Complement of Q_0
Q_n	Q level immediately before the latest active change (⎍ or ⎏) occurs
⎍⎏	Single H level pulse
⎏⎍	Single L level pulse
TOGGLE	Each output is changed to the complement of the preceding state by an active input change (⎍ or ⎏)

Design Considerations

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. Hitachi's Advanced CMOS helps designers achieve these goals.

FACT (Fairchild Advanced CMOS Technology) logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading, and a 50 Ω transmission line drive capability to offer a complete family of SSI and MSI devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

There are five items of interest which need to be evaluated when implementing FACT devices in new designs:

- Interfacing—interboard and technology interfaces, battery backup, and power down or live insert/ extract systems require some special thought.
- Transmission line driving—FACT has line driving capabilities superior to all CMOS families and most TTL families.
- Noise effects—As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve FACT's resistance to crosstalk problems.
- Board layout—Prudent board layout will ensure that most noise effects are minimized.
- Power supplies and decoupling—Maximize ground and V_{CC} traces to keep V_{CC}/ground impedance as low as possible; full ground/V_{CC} planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.

1. Interfacing

FACT devices have outputs which combine balanced CMOS outputs with high current line driving capability. Each standard output is guaranteed to source or sink 24 mA of current at worst case conditions. This allows FACT circuits to drive more loads than standard advanced Schottky parts; FACT can directly drive ALS, AS, LS, HC, and HCT devices.

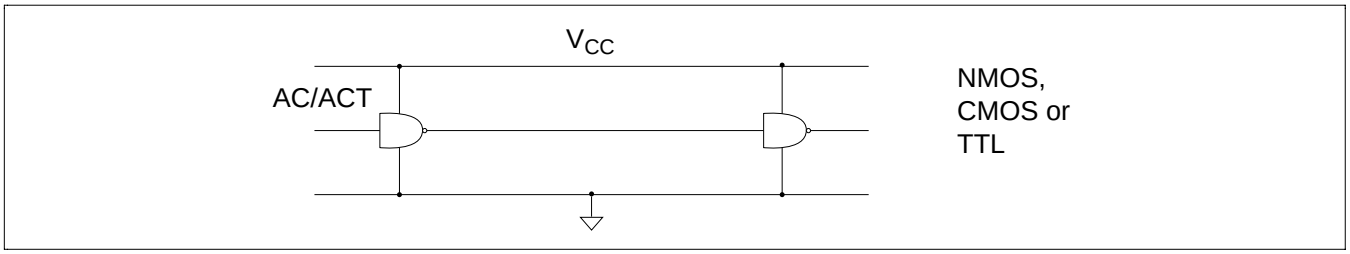


Figure 1 Interfacing FACT to NMOS, CMOS and TTL

FACT devices can be directly driven by both NMOS and CMOS families, as shown in figure 1, operating at the same rail potential without special considerations. This is possible due to the low input loading of FACT product, guaranteed to be less than 1 µA per input.

Some older technologies, including all existing TTL families, will not be able to drive FACT circuits directly; this is due to inadequate high level capability, which is guaranteed to 2.4 V. There are two simple approaches to the TTL-to-FACT interface problem. A TTL-to-CMOS converter can be constructed employing a resistor pull-up to V_{CC} of approximately 4.7 kΩ, which is depicted in figure 2. The correct high level is seen by the CMOS device while not loading down the TTL driver.

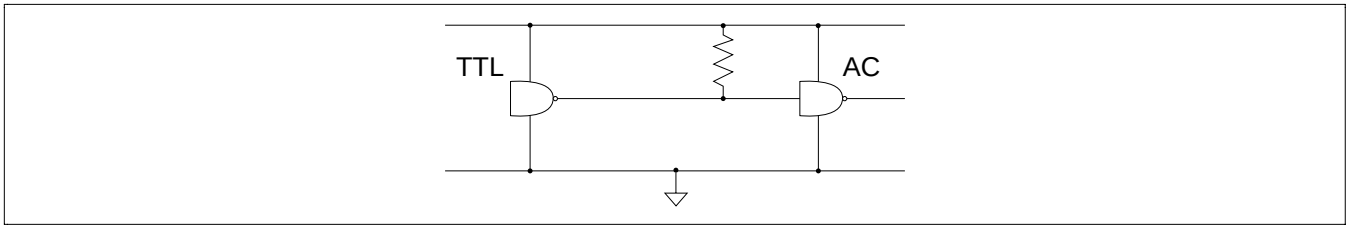


Figure 2 V_{IH} Pull-Up on TTL Outputs

Unfortunately, there will be designs where including a pull-up resistor will not be acceptable. In these cases, such as a terminated TTL bus, Hitachi has designed devices which offer thresholds that are TTL-compatible (figure 3). These interfaces tend to be slightly slower than their CMOS-level counter-parts due to an extra buffer stage required for level conversion.

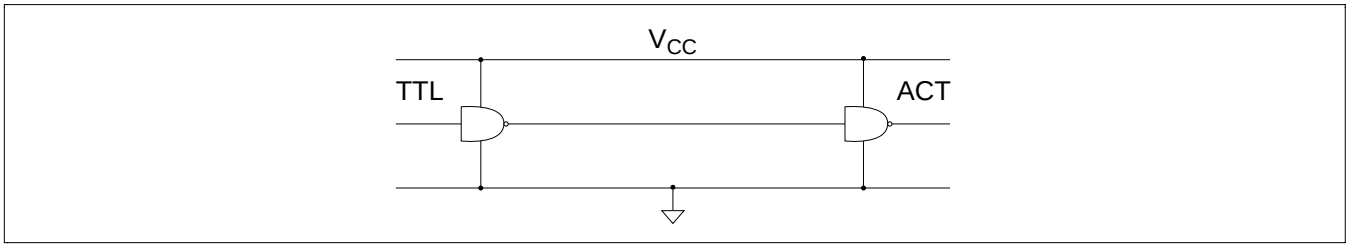


Figure 3 TTL Interfacing to HD74ACT

ECL devices cannot directly drive FACT devices. Interfacing FACT-to-ECL can be accomplished by using TTL-to-ECL translators and 10125 ECL-to-TTL translators in addition to following the same rules on the TTL outputs to CMOS inputs (i.e., a resistor pull-up to V_{CC} of approximately 4.7 kΩ). The translation can also be accomplished by a resistive network. A three-resistor interface between FACT and ECL logic is illustrated in figure 4. Figures 5 and 6 show the translation from ECL-to-FACT, which is somewhat more complicated. These two examples offer some possible interfaces between ECL and FACT logic.

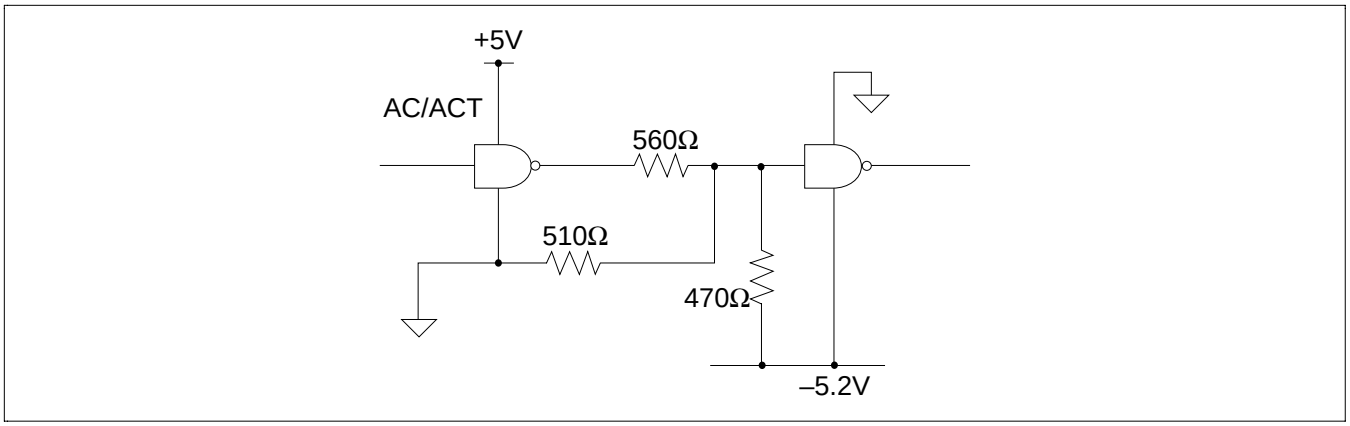


Figure 4 Resistive FACT-to-ECL Translation

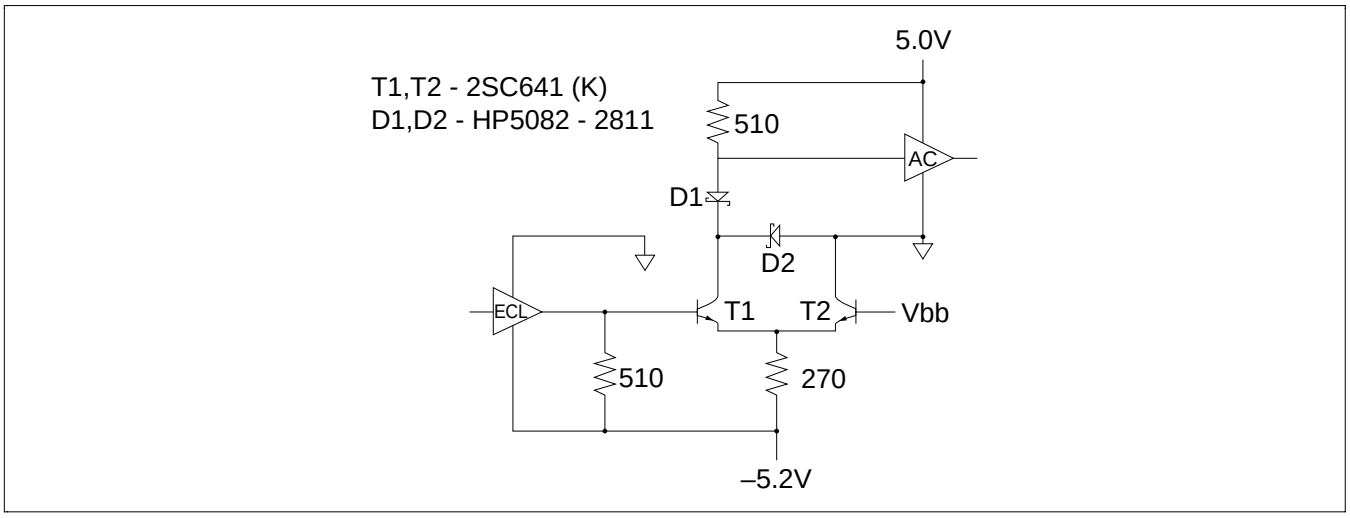


Figure 5 Single-Ended ECL-to-HD74AC Circuit

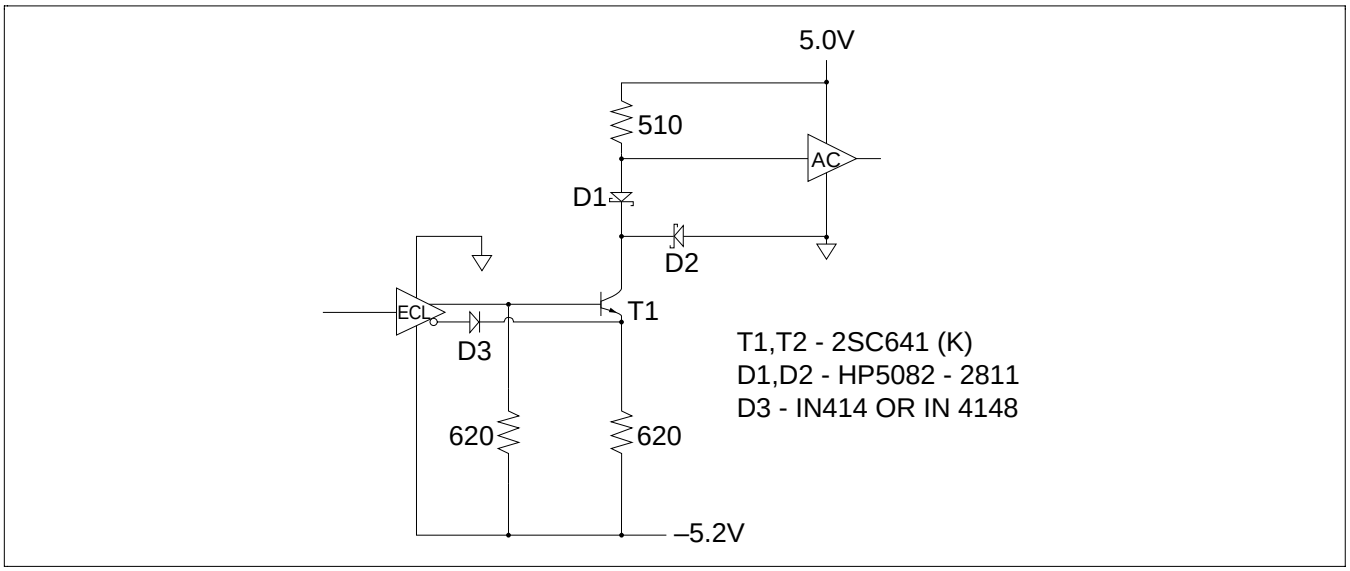


Figure 6 Differential Output ECL-to-HD74AC Circuit

It should be understood that for FACT, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.

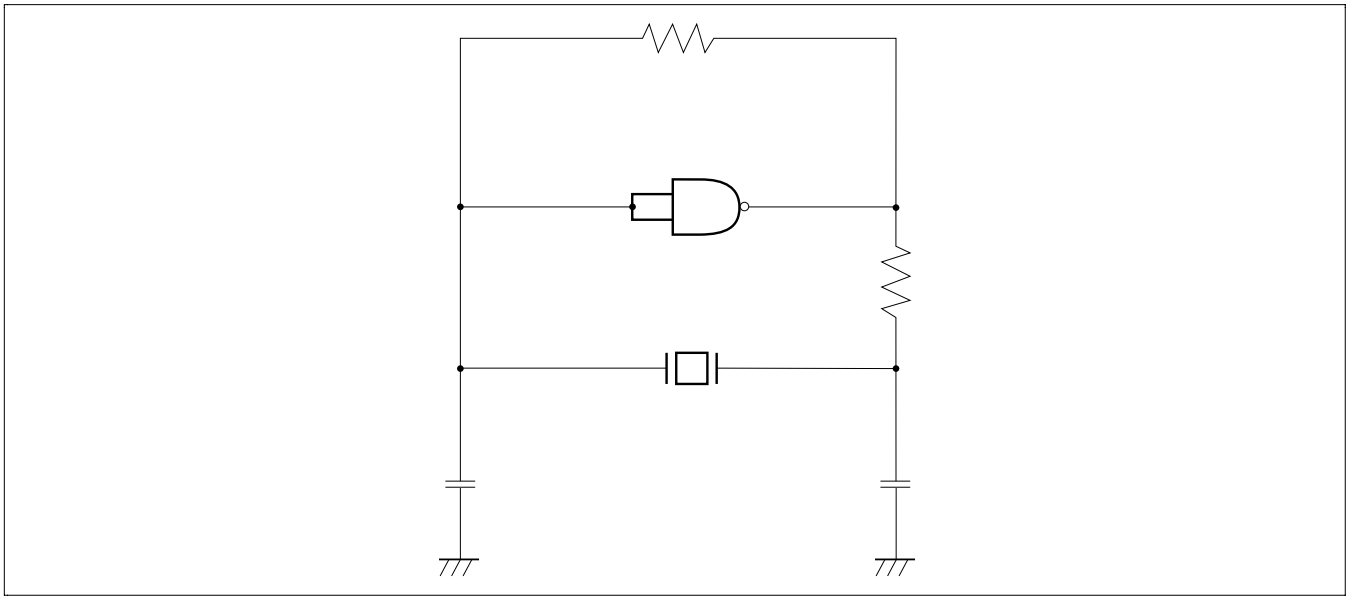


Figure 7 Crystal Oscillator Circuit Implemented with FACT HD74AC00

2. Line Driving

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Zoe, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_O and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Zoe and t_{pde} can be calculated with:

$$Z_{oe} = \frac{Z_O}{\sqrt{1 + C_t / C_I}}$$

$$t_{pde} = t_{pd}\sqrt{1 + C_t / C_I}$$

where C_I = intrinsic line capacitance and Ct = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

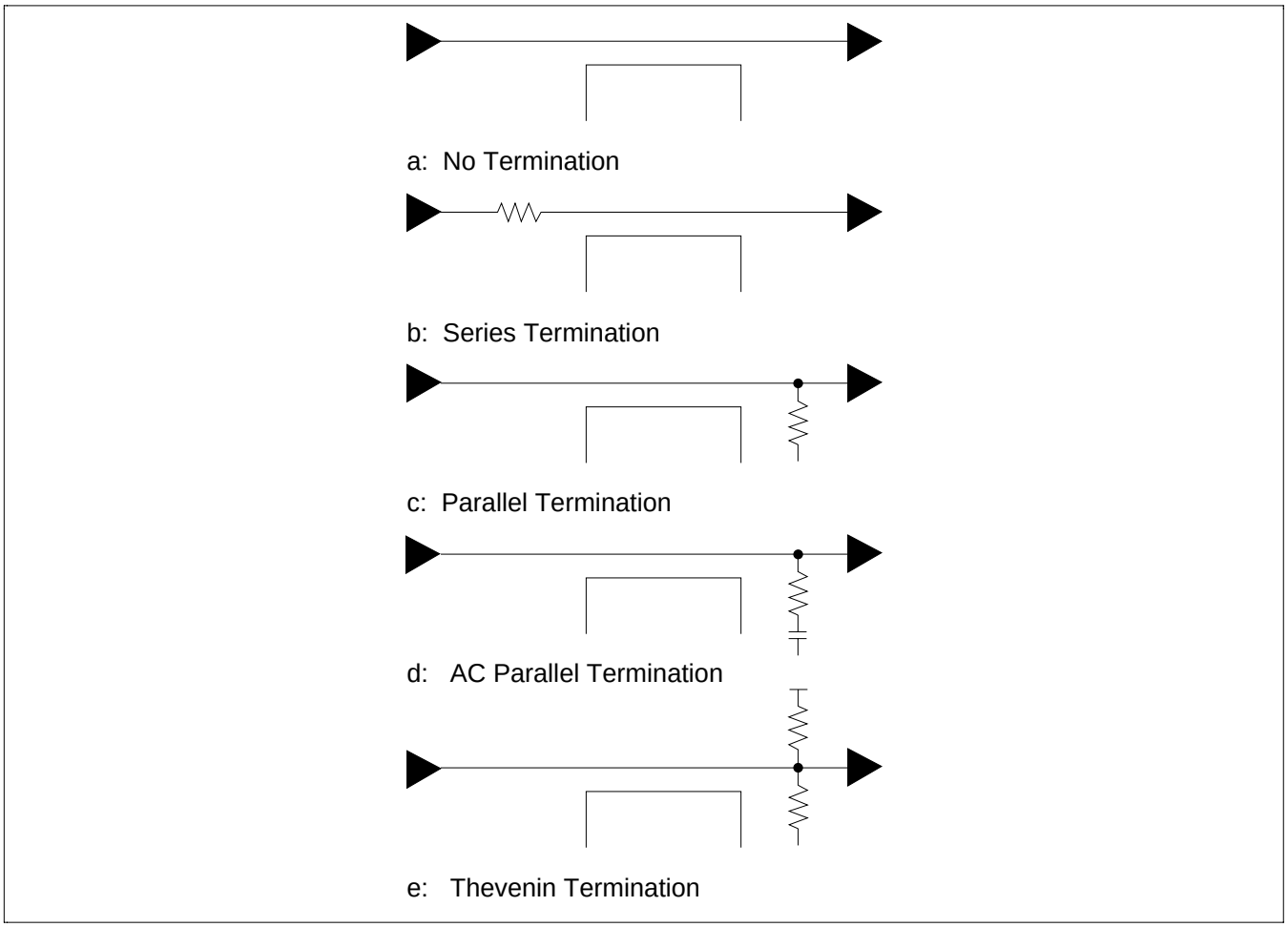


Figure 8 Termination Schemes

There are several termination schemes which may be used (figure 8). Included are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations cause high DC power consumption.

2.1 Series Terminations

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula

$$V_W = V_{CC} \cdot Z_{oe}/(Z_{oe} + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

2.2 Parallel Termination

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

2.3 AC Parallel Termination

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

2.4 Thevenin Termination

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{CC} or ground, increasing power consumption.

FACT circuits have been designed to drive 50 Ω transmission lines over the full temperature range. This is guaranteed by the FACT family's specified dynamic drive capability of 86 mA sink and 75 mA source current. This ensures incident wave switching on 50 Ω transmission lines and is consistent with the 3 ns rated edge transition time.

FACT devices also feature balanced output totem pole structures to allow equal source and sink current capability. This gives rise to balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminate both the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

FACT product inputs have been created to take full advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} are specified at 70% and 30% of V_{CC} respectively. The corresponding output levels, V_{OH} and V_{OL}, are specified to be within 0.1 V of the rails, of which the output is sourcing or sinking 50 µA or less. These noise margins are outlined in figure 9.

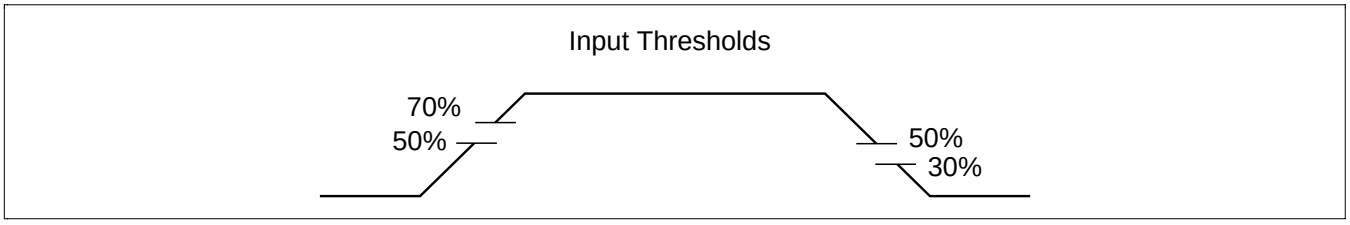


Figure 9 Input Threshold

3. CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to V_{CC} and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 10 exemplifies the situation when power is removed. Any input driven above the V_{CC} pin will forward-bias the clamp diode. Current can then flow into the device, and out V_{CC} or any output that is high. Depending upon the system, this current, I_{IN}, can be quite high, and may not allow the bus voltage to reach a valid high state. One possible solution to eliminate this problem is to place a series resistor in the line.

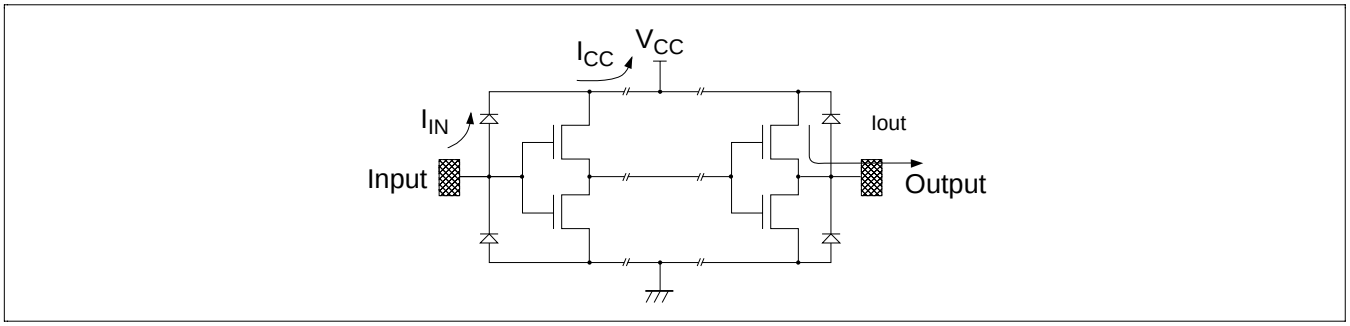


Figure 10 Clamp Diode Operation

4. Noise Effects

FACT offers the best noise immunity of any competing technology available today. With input thresholds specified at 30% and 70% of V_{CC} and outputs that drive to within 100 mV of the rails, FACT devices offer noise margins approaching 30% of V_{CC}. At 5 V V_{CC}, FACT's specified input and output levels give almost 1.5 V of noise margin for both ground and V_{CC}-born noise. With realistic input thresholds closer to 50% of V_{CC}, the actual margins approach 2.5 V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of FACT circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per ship. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

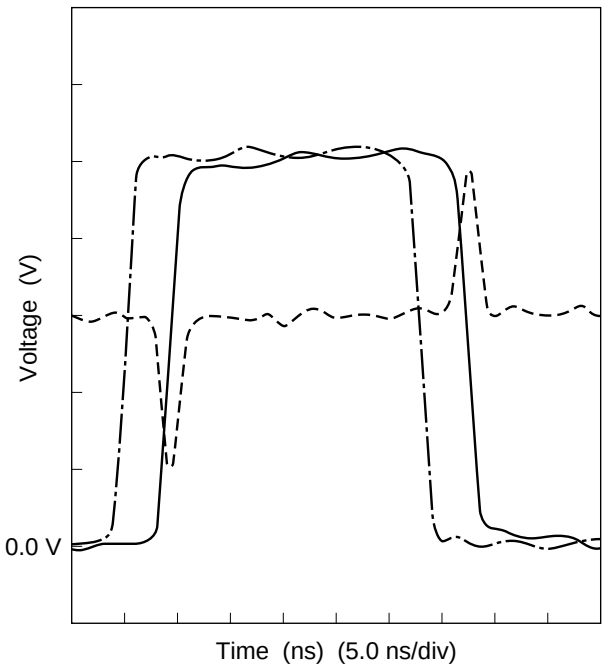
4.1 Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the capacitive coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, figure 11, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air (Er = 1.0) and epoxy glass (Er = 4.7). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. this delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, figure 12, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

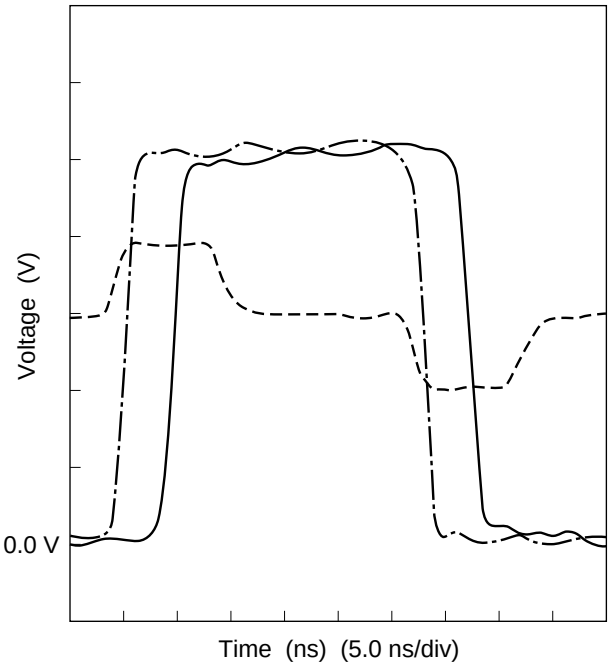
Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. FACT's industry-leading noise margins make systems immune to crosstalk-related problems easier to design. FACT's AC noise margins, shown in figures 13 and 14, exemplify the outstanding immunity to everyday noise which can effect system reliability.



Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Forward Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

Figure 11 Forward Crosstalk on PCB Traces



Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Forward Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

Figure 12 Reverse Crosstalk on PCB Traces

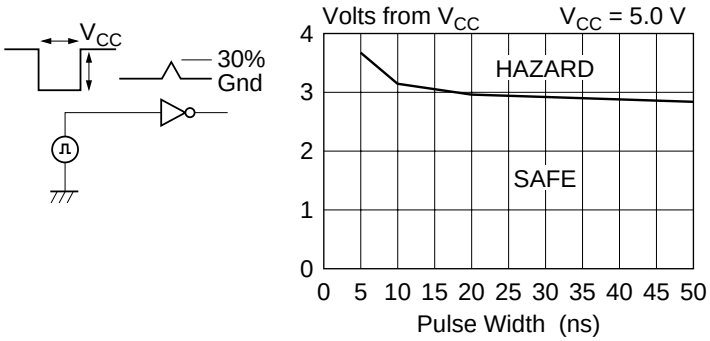


Figure 13 High Noise Margin

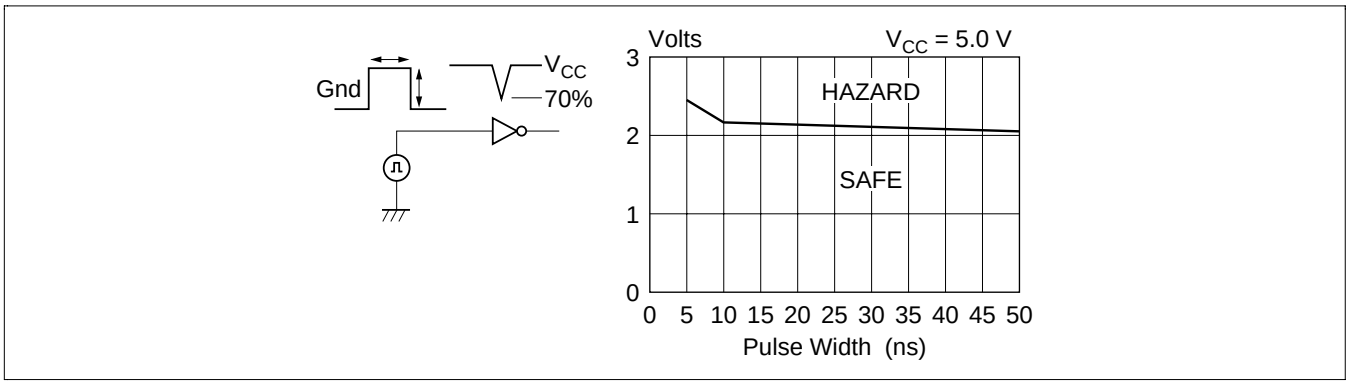


Figure 14 Low Noise Margin

With over 2.0 V of noise margins, the FACT family offers better noise rejection than any other comparable technology.

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing (figure 15). Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

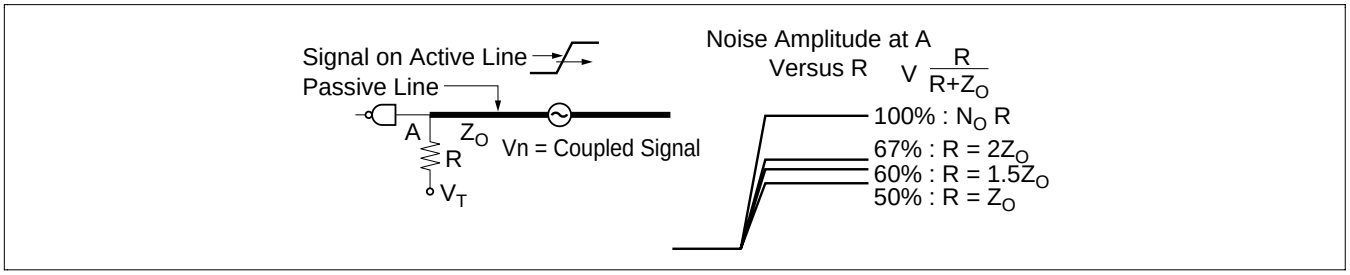


Figure 15 Effects of Termination on Crosstalk

4.2 Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced.

Figure 16 shows a simple circuit model for a device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

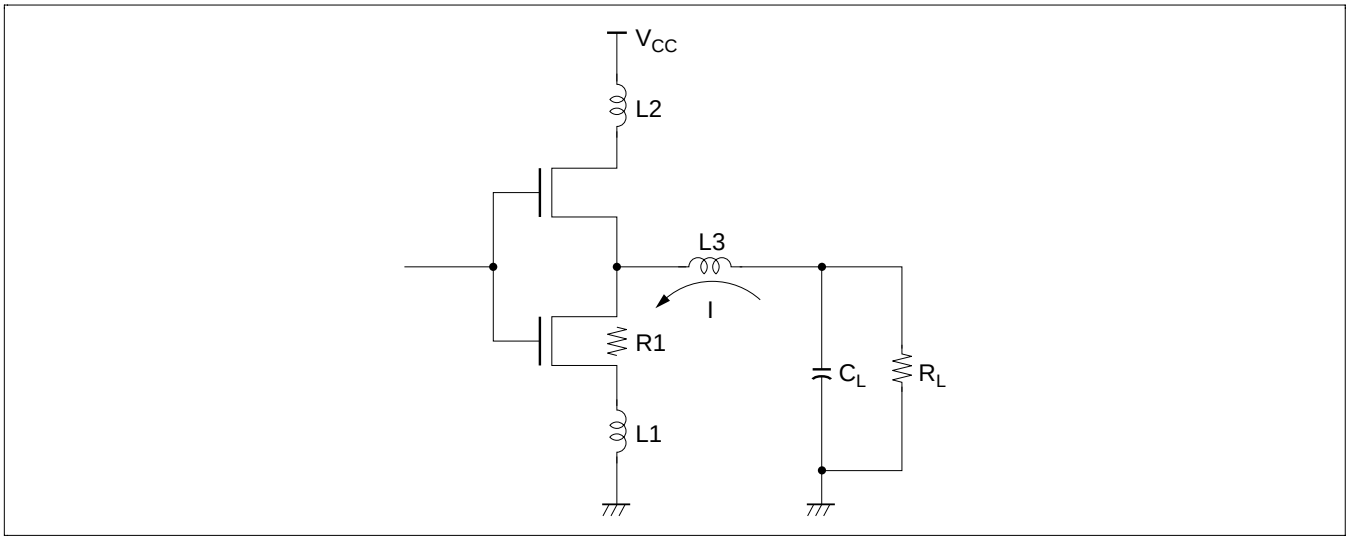
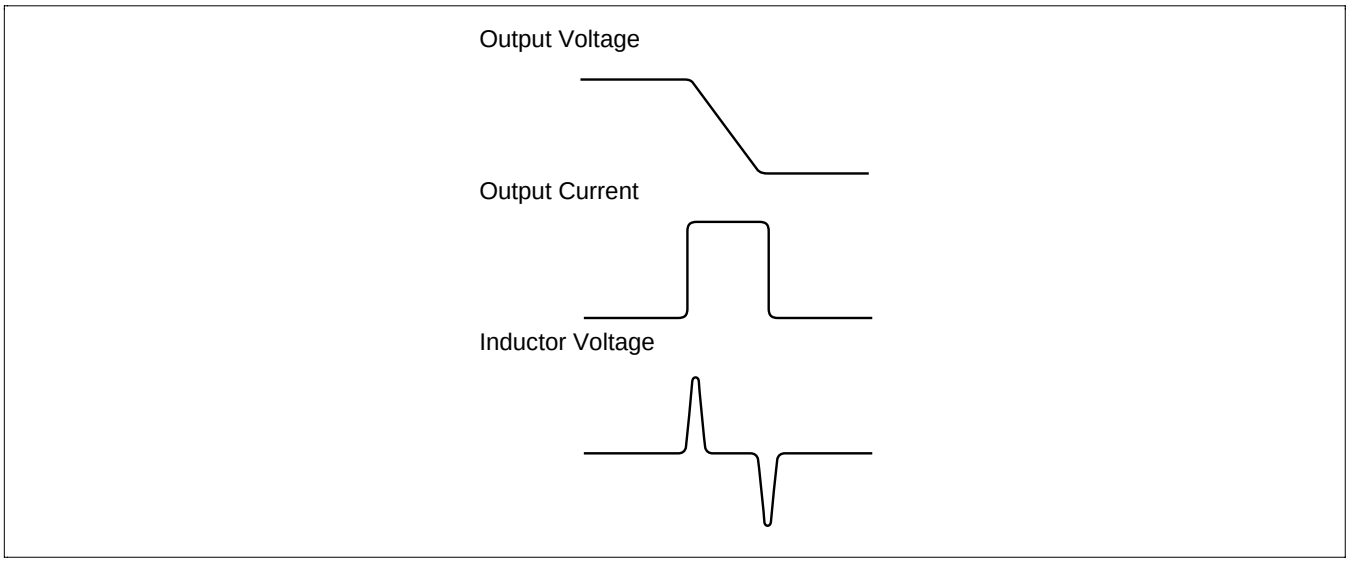


Figure 16 Ground Bounce Output Model



The three waveforms shown in figure 16 depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic high to a logic low. The output slue rate is dependent upon the characteristics of the output transistor, the inductors L1 and L3, and C_L, the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = C_L \bullet dv/dt$]. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$Vgb = -L \bullet (di/dt)$].

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60 to 70 pF increases ground bounce. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: lowering V_{CC} reduces ground bounce.
- Test fixtures: standard test fixtures generate 30 to 50% more ground bounce than a typical system since they use capacitive loads which both increase the AC load and form LCR tank circuits that oscillate.

Ground bounce produces several symptoms:

- Altered device states. FACT logic does not exhibit this symptom.
- Propagation delay degraduation. FACT devices are characterized not to degrade more than 250 ps per additional output switching
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise. FACT logic's worst-case quiet output noise has been measured to be approximately 500 to 1100 mV in actual system applications.

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

- First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs, or
- Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

- Locate these outputs as close to the ground pin as possible.
- Use the lowest V_{CC} possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections etc.

5. Design Rules

The set of design rules listed below are recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines as those they have employed with advanced bipolar logic families.

- Use multi-layer boards with V_{CC} and ground planes, with the device power pins soldered directly to the planes to insure the lowest power line impedances possible.
- Use decoupling capacitors for every device, usually 0.10 µF should be adequate. These capacitors should be located as close to the ground pin as possible.
- Avoid sockets or wirewrap boards whenever possible.
- Do not connect capacitors from the outputs directly to ground.

5.1 Decoupling Requirements

FACT, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with FACT products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a low to a high value. This power is necessary to charge the load capacitance or drive a line impedance. Figure 17 displays various V_{CC} and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 50 and 100 Ω. This impedance appears in series with the load impedance and will cause a droop in the V_{CC} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used.

This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in figure 18 to calculate the amount of decoupling necessary. This circuit utilizes an HD74AC240 driving a 100 Ω bus from a point somewhere in the middle.

Being in the middle of the bus, the driver will see two 100 Ω loads in parallel, or an effective impedance of 50 Ω. To switch the line from rail to rail, a drive of 78 mA is needed; more than 624 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage with acceptable limits and keep rise and fall times to minimum. The necessary values for decoupling capacitors can be calculated with the formula given in figure 19.

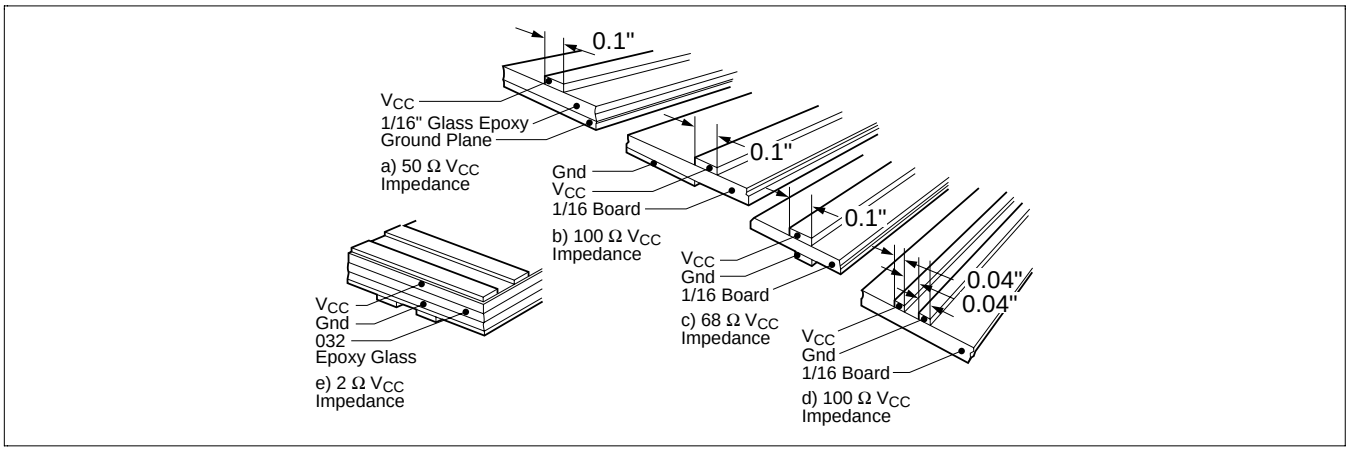


Figure 17 Power Distribution Impedances

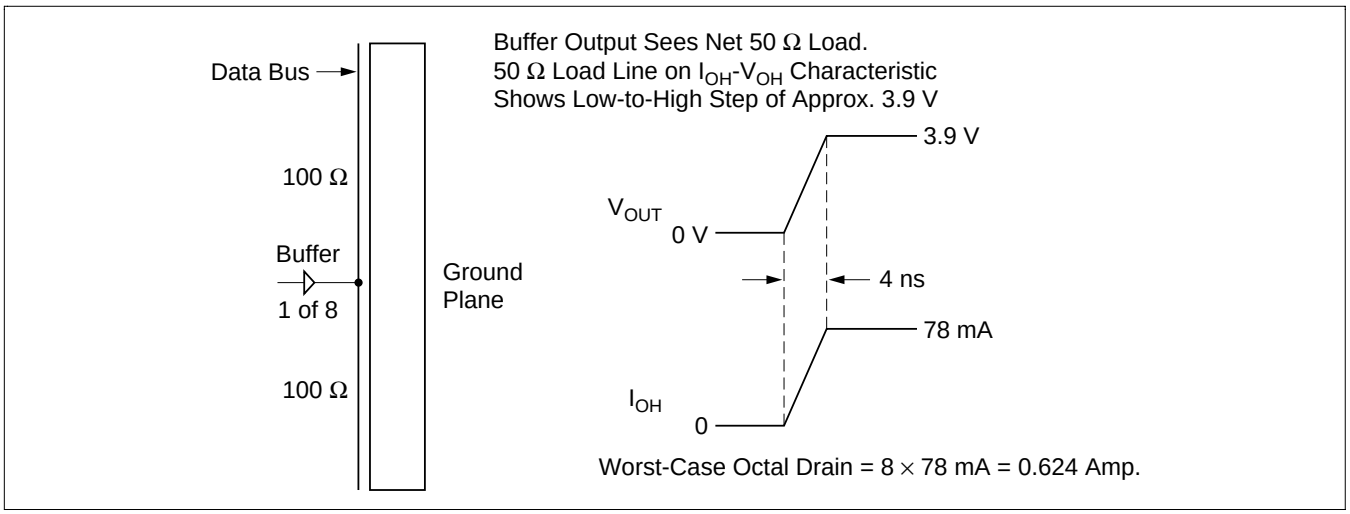


Figure 18 Octal Buffer Driving a 100 Ω Bus

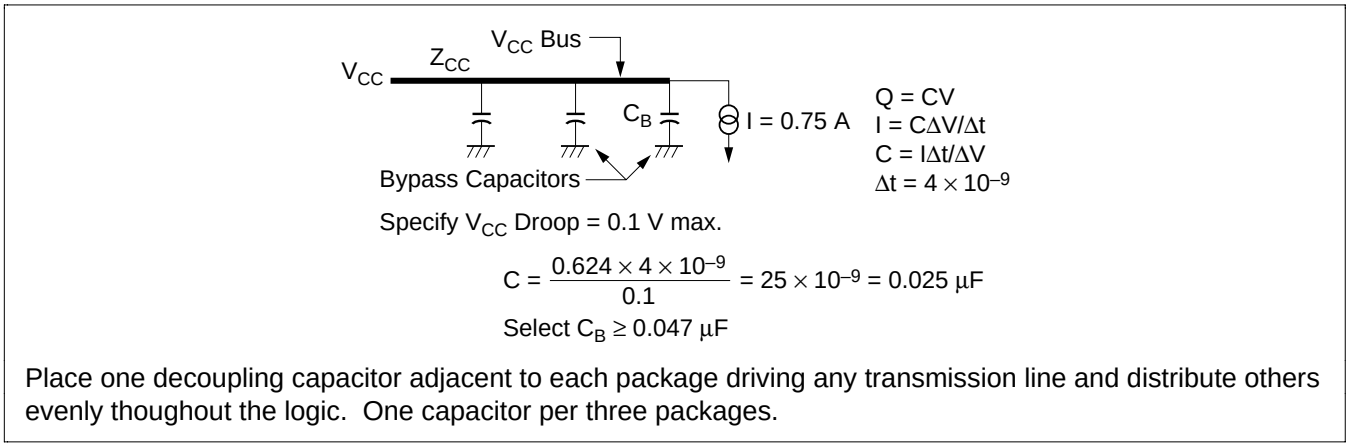


Figure 19 Formula for Calculating Decoupling Capacitors

In this example, if the V_{CC} droop is to be kept below 0.1 V and the edge rate equals 4 ns, a 0.025 µF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.

5.2 Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

6. TTL-Compatible CMOS Designs Require Delta I_{CC} Consideration

The FACT product line is composed of two types of advanced CMOS circuits: HD74AC and HD74ACT devices. HD74ACT indicates an advanced CMOS device with TTL-type input thresholds for direct replacement of LS and ALS circuits. As this HD74ACT series is used to replace TTL, the Delta I_{CCT} specification must be considered; this spec may be confusing and misleading to the engineer unfamiliar with CMOS.

It is important to understand the concept of Delta I_{CCT} and how to use it within a design. First, consider where Delta I_{CCT} initiates. Most CMOS input structures are of the totem pole type with an n-channel transistor in a series with a p-channel transistor as illustrated in figure 20.

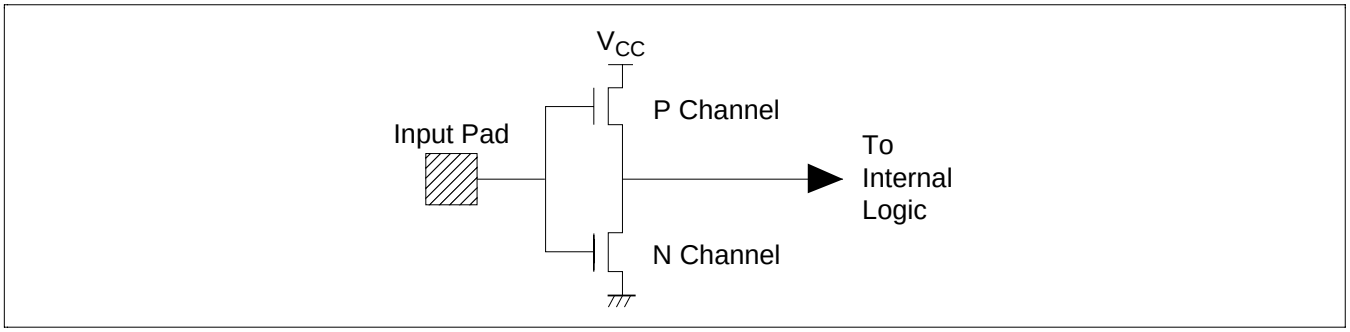


Figure 20 CMOS Input Structure

These two transistors can be modeled as variable resistors with resistances varying according to the input voltage. The resistance of an on transistor is approximately 50 Ω while the resistance of an off transistor is generally greater than 5 MΩ. When the input to this structure is at either ground or V_{CC}, one transistor will be on and one will be off. The total series resistance of this pair will be the combination of the two individual resistances, greater than 5 MΩ. The leakage current will then be less than 1 µA. When the input is between ground and V_{CC}, the resistance of the on transistor will increase while the resistance of the off transistor will decrease. The net resistance will drop due to the much larger value of the off resistance. The total series resistance can be as low as 600 Ω. This reduction in series resistance of the input structure will cause a corresponding increase in I_{CC} as current flows through the input structure. Figure 21 depicts typical I_{CC} variance with input voltage for an HD74ACT device.

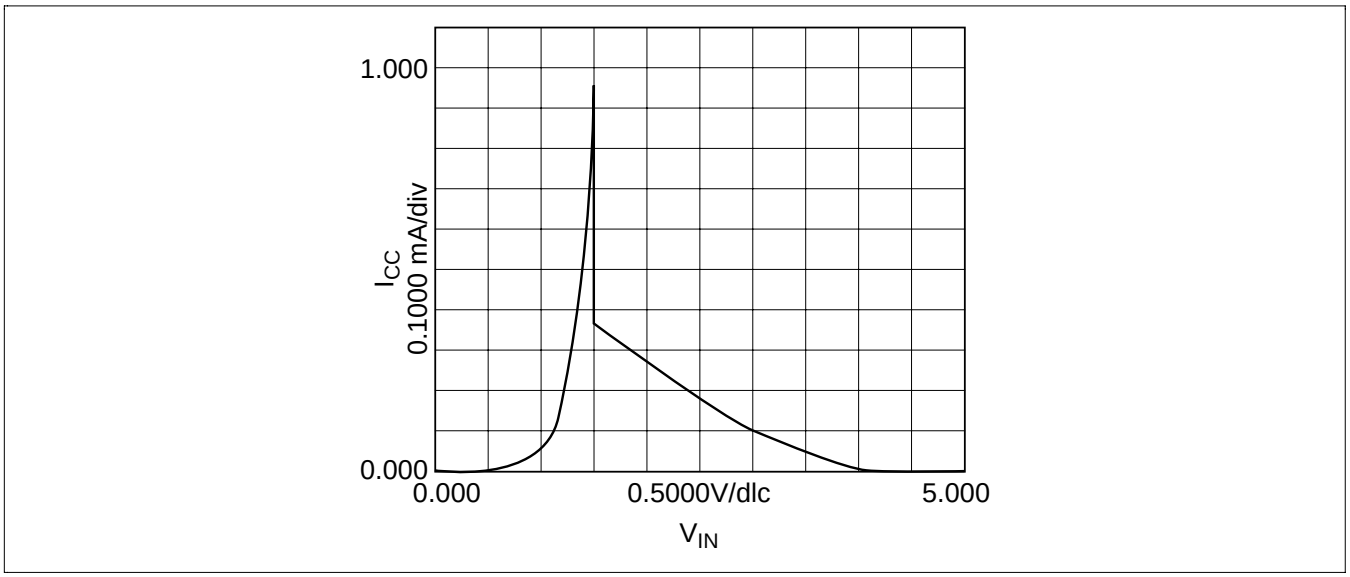


Figure 21 I_{CC} versus Input Voltage for HD74ACT Devices

The Delta I_{CC} specification is the increase in I_{CC}. For each input at V_{CC}-2.1 V, the Delta I_{CC} value should be added to the quiescent supply current to arrive at the circuit's worst-case static I_{CC} value.

Fortunately, there are several factors which tend to reduce the increase in I_{CC} per input. Most TTL devices will be able to drive FACT inputs well beyond the TTL output specification due to FACT's low input loading in a typical system. For example, FAST logic outputs can drive HD74ACT-type inputs down to 200 mV and up to 3.5 V. Additionally, the typical I_{CC} increase per input will be less than the specified limit. As shown in the graph above, the I_{CC} increase at V_{CC}-2.1 V is less than 200 µA in the typical system. Experiments have shown that the I_{CC} of an HD74ACT240 series device typically increases only 200 µA when all of the inputs are connected to a FAST device instead of ground or V_{CC}.

It is important when designing with FACT, as with any TTL-compatible CMOS technology, that the Delta I_{CC} specification be considered. Designers should be aware of the spec's significance and that the data book specification is a worst-case value; most systems will see values that are much less.

7. Testing Advanced CMOS Devices with I/O Pins

There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

Such is the case with parts that have a bidirectional pin, exemplified by the HD74AC245/HD74ACT245 octal transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for I_{CC} and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static I_{CC} specification orders of magnitude less than standard load currents. Most CMOS I_{CC} specifications are usually less than 100 µA. When conducting an I_{CC} test, greater care must be taken so that other currents will not mask the actual I_{CC} so that other currents will not mask the actual I_{CC} of the device. These currents are usually sourced from the inputs and outputs.

Since the static I_{CC} requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an I_{CC} test. Even a standard 500 Ω load resistor will sink 10 mA at 5 V, which is more than twice the I_{CC} level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during I_{CC} tests.

Another area of concern is identified when considering the inputs of the device. When the input is in the transition region, I_{CC} can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly on, and a conduction is created from V_{CC} to ground. This conduction path leads to the increased I_{CC} current seen in the I_{CC} vs. V_{IN} curve (figure 22). When the input is at either rail, the input structure no longer conducts. Most I_{CC} testing is done with all of the inputs tied to either V_{CC} or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual I_{CC} of the device under test which is being measured by the tester.

When testing the I_{CC} of a CMOS HD74AC245/HD74ACT245, problems can arise depending upon how the test is conducted. Note the structure of the HD74AC245/HD74ACT245's I/O pins illustrated figure 23.

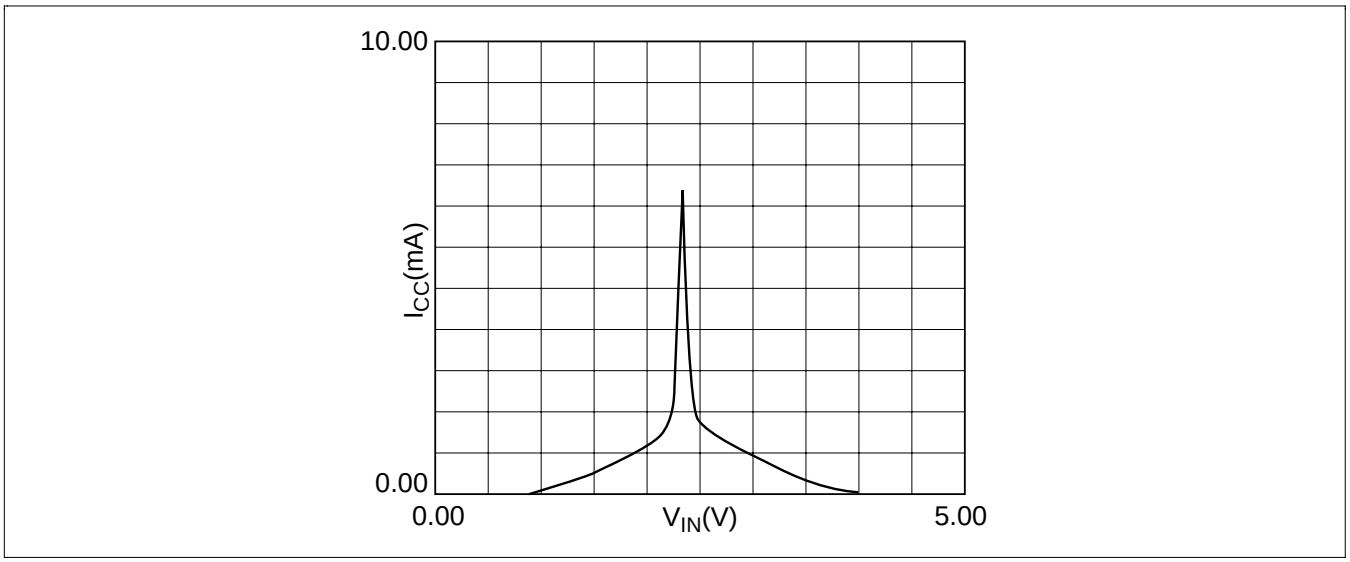


Figure 22 I_{CC} versus I_{IN}

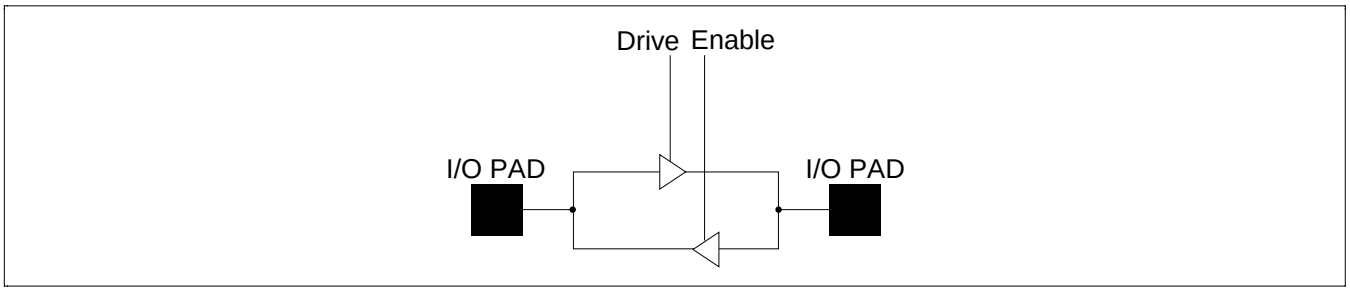


Figure 23 HD74AC245/HD74ACT245 I/O Structure

Each I/O pin is connected to both an input device and an output device. The pin can be viewed as having three states: input, output and output disabled. However, only two states actually exist.

The pin is either an input or an output. When testing the I_{CC} of the device, the pins selected as outputs by the T/R signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and allowed to float, the input device will also float, and an excessive amount of current will flow from V_{CC} to ground.

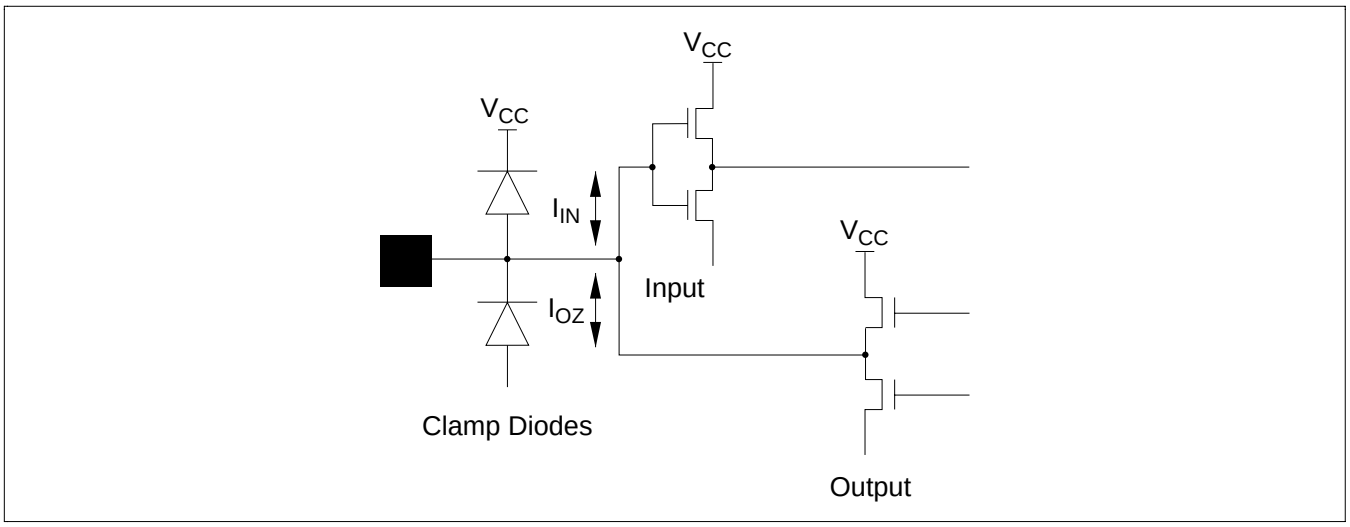


Figure 24 I/O Pin Internal Structure

A simple rule to follow is to treat any output which is disable as an input. This will help insure the integrity of an I_{CC} test.

Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted in figure 24.

The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined I_{IN} specification of the input and the I_{OZ} specification of the output. For FACT devices, I_{IN} is specified at ±1 µA while I_{OZ} is specified at ±5 µA. Combining these gives a limit of ±6 µA for I/O pins. Usually, I/O pins will show leakages that are less than the I_{OZ} specification of the output alone.

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning to work with CMOS. Becoming familiar with and understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

8. Testing Disable Times of 3-State Outputs in a Transmission Line Environment

Traditionally, the disable time of a 3-state buffer has been measured from the 50% point on the disable input, to the 10% or 90% point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown in figure 25.

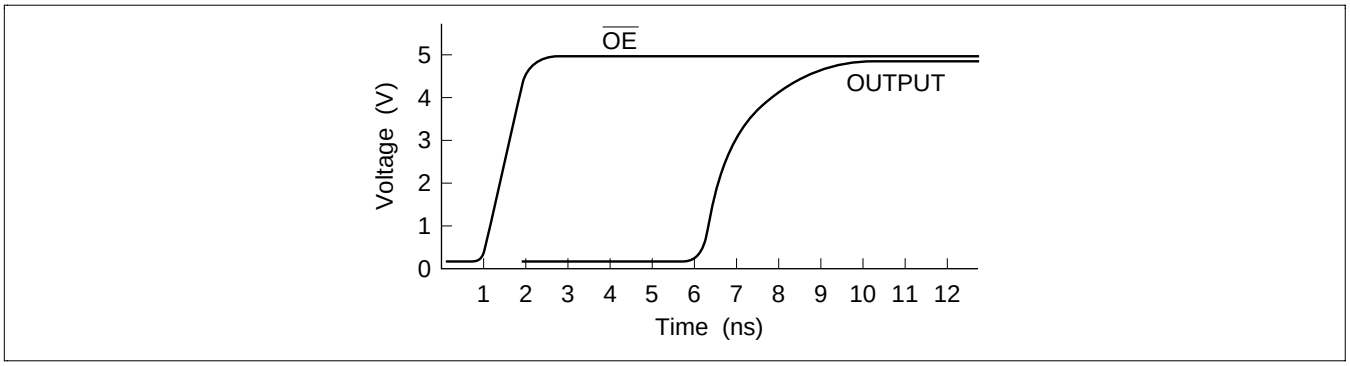


Figure 25 Typical Bench 3-State Waveform

ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. Figure 26 illustraters the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.

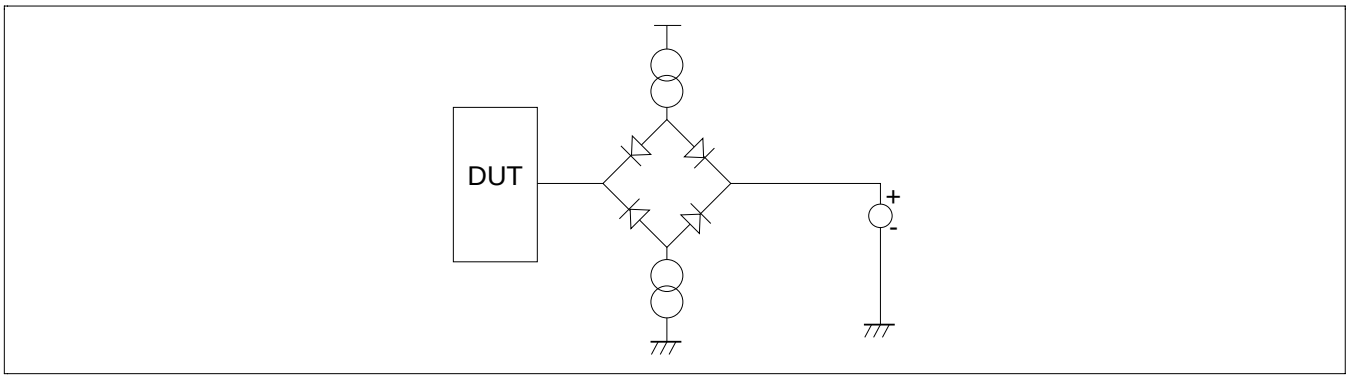


Figure 26 MCT Wheatstone Bridge Test Load

The voltage source provides a pull-up/pull-down voltage while the current sources provide I_{OH} and I_{OL}. When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the 10% or 90% level. Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge

flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in figure 27.

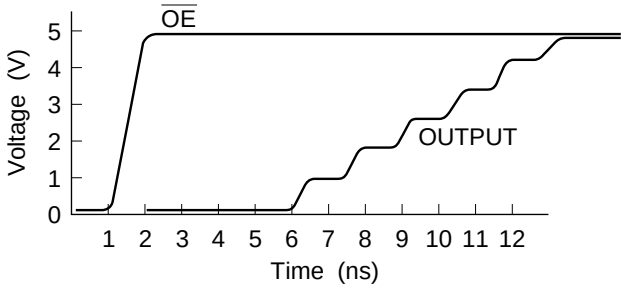


Figure 27 Typical ATE 3-State Waveform

Transmission line theory states that the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA and impedances of 50 to 60 Ω, this voltage step can be as minimal as 250 mV. If the comparator was programmed to the 10% point, it would be looking for a step of 550 mV at 5.5 V V_{CC}. Three reflections of the current pulse would be required before the comparator would detect the level. It is this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customers' incoming tests, even though the device meets specifications. Figure 28 graphically shows this stepout.

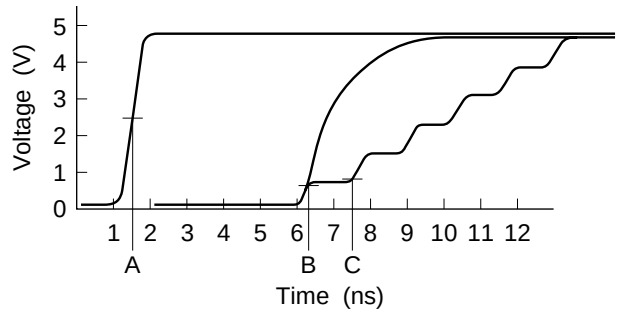


Figure 28 Measurement Stepout

Point A represents the typical 50% measurement point on tester driven waveforms. Point B represents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become non-repeatable.