Integrated Circuit Systems, Inc.

MK9173-01
MK9173-15

Video Genlock PLL

General Description

The MK9173-01 and MK9173-15 provide the analog PLL circuit blocks to implement a frequency multiplier. Because the device is configured to use an external divider in the PLL clock feedback path, a large divider can be used to result in a large frequency multiplication ratio. This is useful when using a low frequency input clock to generate a high frequency output clock. The MK9173-01/15 contains a phase detector, charge pump, loop filter, and voltage-controlled oscillator (VCO). The ICS674-01 can be used as the external feedback divider.

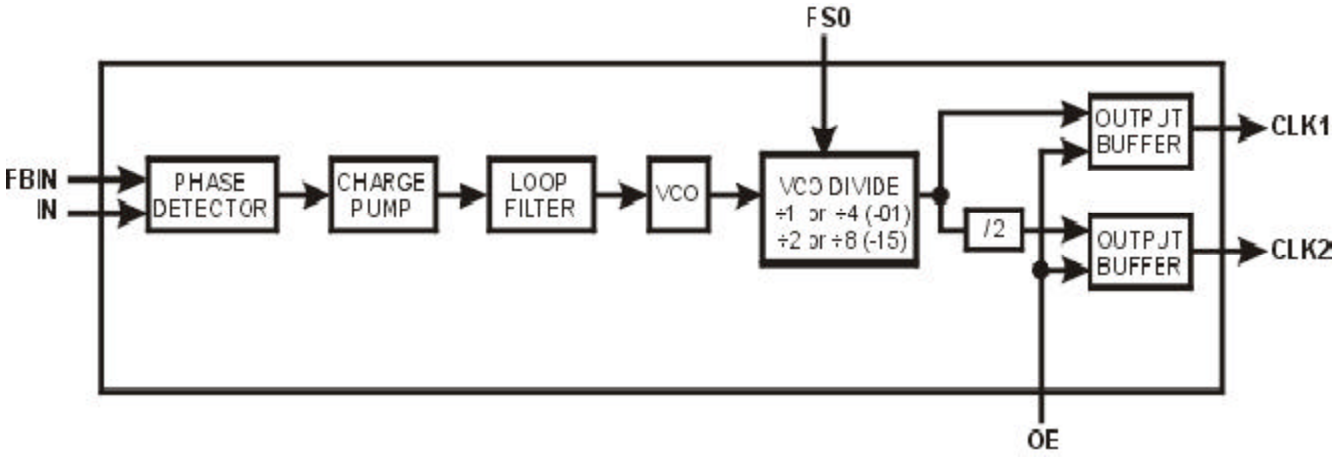
A common application of the MK9173-01/-15 is the implementation of a video genlock circuit. Because of this, the MK9173-01/-15 inputs operate on the negative-going clock edge.

The MK9173-01/15 is pin and function compatible to the AV9173-01/15. Please refer to page 4 regarding performance differences. For new video genlock designs, please refer to the ICS673-01, ICS1522 or ICS1523.

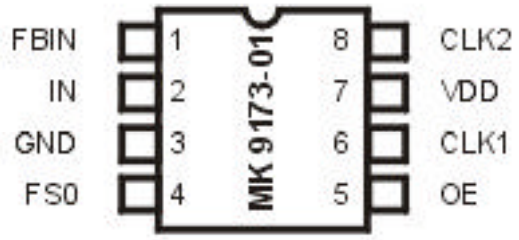
Features

- Designed to replace the AV9173 in most applications
- Phase-detector/VCO circuit block
- Ideal for genlock system
- Reference clock range 12 kHz to 1MHz for full output clock range
- Output clock range 1.25 to 75 MHz (-01), 0.625 to 37.5 MHz (-15), see Table 1 for conditions
- On-chip loop filter
- Single 5 volt power supply
- Low power CMOS technology
- Small 8-pin SOIC package

Block Diagram



Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FBIN	Input	Feedback Input
2	IN	Input	Input for reference sync pulse
3	GND	—	Ground
4	FS0	Input	Frequency Select 0 input
5	OE	Input	Output Enable
6	CLK1	Output	Clock Output 1
7	VDD	—	Power Supply (+5V)
8	CLK2	Output	Clock Output 2 (Divided-by-2 from Clock 1)

Table 1: Allowable Input Frequency to Output Frequency (Outputs in MHz)MK9173-01

(MK9173-15 outputs run at exactly 1/2 the MK9173-01 frequencies)

f_{IN} (kHz)	f_{OUT} for FS = 0 (MHz)		f_{OUT} for FS = 1 (MHz)	
	CLK1 Output	CLK2 Output	CLK1 Output	CLK2 Output
$12 \le f_{IN} \le 14$ kHz	44.0 to 75	22.0 to 37.5	11.0 to 18.75	5.5 to 9.375
$14 < f_{IN} \le 17$ kHz	30.0 to 75	15.0 to 37.5	7.5 to 18.75	3.75 to 9.375
$17 < f_{IN} \le 30$ kHz	25.0 to 75	12.5 to 37.5	6.25 to 18.75	3.125 to 9.375
$30 < f_{IN} \le 35$ kHz	15.0 to 75	7.5 to 37.5	3.75 to 18.75	1.875 to 9.375
$35 < f_{IN} \le 1000$ kHz	10.0 to 75	5.0 to 37.5	2.5 to 18.75	1.25 to 9.375

Using the MK9173-01/15 in Genlock Applications

Most video sources, such as video cameras, are asynchronous, free-running devices. To digitize video or synchronize one video source to another free-running reference video source, a video "genlock" (generator lock) circuit is required. The MK9173-01 and MK9173-15 integrate the analog blocks which make the task much easier.

In the complete video genlock circuit, the primary function of the MK9173-01 and MK9173-15 is to provide the analog circuitry required to generate the video dot clock within a PLL. This application is illustrated in Figure 1. The input reference signal for this circuit is the horizontal synchronization (H-SYNC) signal. If a composite video reference source is being used, the h-sync pulses must be separated from the composite signal. A video sync separator circuit, such as the National Semiconductor LM1881, can be used for this purpose.

The clock feedback divider shown in Figure 1 is a digital divider used within the PLL to multiply the reference frequency. Its divide ratio establishes how many video dot clock cycles occur per h-sync pulse. For example, if 880 pixel clocks are desired per h-sync pulse, then the divider ratio is set to 880. Hence, together the h-sync frequency and external divider ratio establish the dot clock frequency:

$f_{OUT} = f_{IN} \cdot N$ where N is external divide ratio

Both input pins IN and FBIN respond only to negative-going clock edges of the input signal. The H-SYNC signal must be constant frequency in the 12 kHz to 1MHz range and stable (low clock jitter) for creation of a stable output clock.

Refer to Application Brief (AB01) for additional details on use of input frequencies below 25kHz. By following the guidelines in this brief and meeting the test conditions in the AC specifications (VCO frequency), an input as low as 12kHz (such as NTSC or PAL H-SYNC) can be used.

The output hook-ups of the MK9173-01 and MK9173-15 are dictated by the desired dot clock frequency. The primary consideration is the internal VCO which operates over a frequency range of 10 MHz to 75 MHz. Because of the selectable VCO output divider and the additional divider on output CLK2, four distinct output frequency ranges can be achieved. The following Table lists these ranges and the corresponding device configuration.

FS0 State	Output Used	Frequency Range MK9173-01	Frequency Range MK9173-15
0	CLK1	10 - 75 MHz	5 - 37.5 MHz
0	CLK2	5 - 37.5 MHz	2.5 - 18.75 MHz
1	CLK1	2.5 - 18.75 MHz	1.25 - 9.375 MHz
1	CLK2	1.25 - 9.375 MHz	0.625-4.6875 MHz

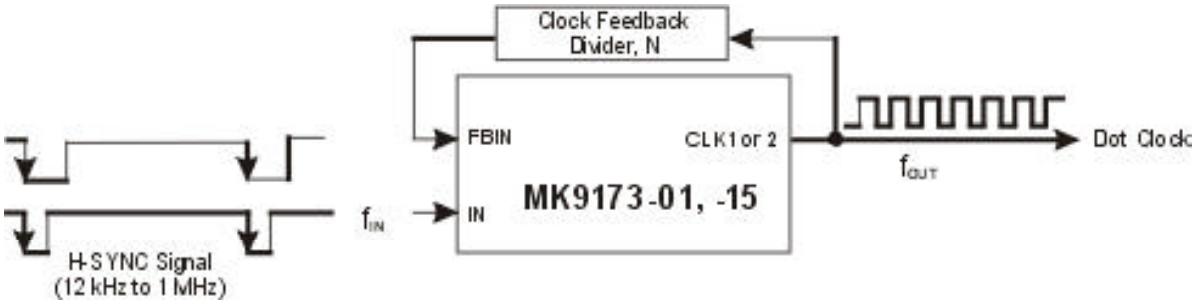
Note that both outputs, CLK1 and CLK2, are available during operation even though only one is fed back via the external clock divider.

Pin 5, OE, tristates both CLK1 and CLK2 upon logic low input. This feature can be used to revert dot clock control to the system clock when not in genlock mode (hence, when in genlock mode the system dot clock must be tristated).

When unused, inputs FS0 and OE must be tied to either GND (logic low) or VDD (logic high).

For further discussion of VCO/PLL operation as it applies to the MK9173-01 and MK9173-15, please refer to the AV9170 application note. The AV9170 is a similar device with fixed feedback dividers for skew control applications.

Figure 1: Typical Application of MK9173-01/-15 in a Video Genlock System



Using the MK9173-01/15 to replace the AV9173-01/15

Increasing leadtimes from our wafer fab on the AV917x family of products led us to introduce the MK917x family. The MK917x have been designed for a 0.6 micron CMOS process, whereas the AV917x devices are on a 1.2 micron process. There are characteristic differences between the old and new products which may lead to problems in the application. The most commonly reported problem is increased jitter.

Design Considerations

The primary difference between old (AV) and new (MK) products is that the MK series is built on a faster process. To compensate for this process difference, we recommend the following design considerations.

1. Because the MK series is faster, good power supply decoupling is more important. A board layout which works well with the AV parts may require better decoupling to work with the MK parts. The recommended decoupling is 0.01 uF mounted as close as possible (within 0.2") to the VDD pin (if a larger value device is in place, such as a 0.1 uF, try replacing this with a 0.01 uF device). To determine if improved decoupling would help performance, connect a disc capacitor directly across the VDD and ground pins. Trim the leads as short as possible.

2. Due to differences in behavior between the AV and MK parts, the MK parts may not be a viable substitute in some applications. Accordingly, ICS is working to establish a new source of supply for the AV part.

3. Keep in mind the following advice for PLLs, which might help you troubleshoot problems in migrating to the MK917x family:

a) Don't open the external clock feedback path. In doing so, the MK917x will start to run as its maximum frequency, which might be faster than the logic in your feedback path is able to handle.

b) Fast transitions on the input pins reduce jitter. Remove any filters or unneeded loads on the inputs.

c) Terminate the clock output lines properly. Try adding a 33 ohm series termination resistor.

For new video genlock applications, please consider the ICS673-01, ICS1522, or ICS1523.

Absolute Maximum Ratings

V_{DD} (referenced to GND) . . . . . 7.0 V
Operating Temperature under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . – 65°C to +150°C
Voltage on I/O pins referenced to GND . . . . . GND – 0.5V to V_{DD} + 0.5V
Power Dissipation . . . . . 0.5 watts

Stresses above those listed under *Absolute Maximum Ratings* above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristic

V_{DD} = +5V ±5%, T_A = 0°C to 70°C, unless otherwise stated

DC CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	VIL	VDD = 5V	—	—	0.8	V
Input High Voltage	VIH	VDD = 5V	2.0	—	—	V
Input Low Current	IIL	VIN = 0V	-5	—	—	µA
Input High Current	IIH	VIN = VDD	-5	—	5	µA
Output Low Voltage[1]	VOL	IOL = 8mA	—	—	0.4	V
Output High Voltage[1]	VOH1	IOH = -1mA, VDD = 5.0V	VDD -0.4V	—	—	V
Output High Voltage[1]	VOH2	IOH = -4mA, VDD = 5.0V	VDD -0.8V	—	—	V
Output High Voltage[1]	VOH3	IOH = -8mA	2.4	—	—	V
Supply Current	IDD	Unloaded, 50 MHZ	—	20	50	mA

Notes:

1. Duty cycle measured at 1.4V.
2. Input Reference Frequency = 25 kHz, Output Frequency = 25 MHz. Jitter measured between adjacent vertical pixels.
3. CLK1 frequency applies for FS = 0. For FS = 1 condition, divide allowable CLK1 range by the factor of 4.

Electrical Characteristics

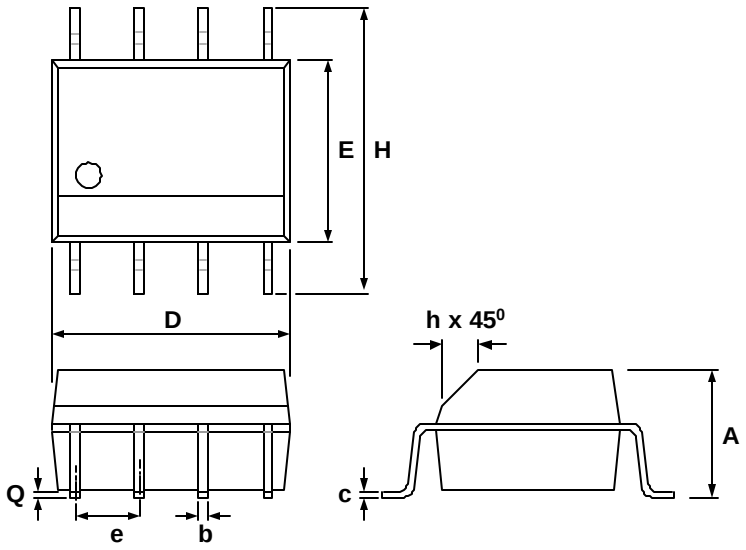
V_{DD} = +5V ±5%, T_A = 0°C to 70°C, unless otherwise stated

AC CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time[1]	ICLKr		—	—	10	ns
Input Clock Fall Time[1]	ICLKf		—	—	10	ns
Output Rise Time[1]	tr1	15pF load; 0.8 to 2.0V	—	0.6	1.5	ns
Output Rise time[1]	tr2	15pF load; 20% to 80% VDD	—	1.4	3.0	ns
Output Fall time[1]	tf1	15pF load; 2.0 to 0.8V	—	0.8	2.0	ns
Output Fall time[1]	tf2	15pF load; 80% to 20% VDD	—	0.8	2.0	ns
Output Duty Cycle[1]	dt	15pF load	40	47	55	%
Jitter, one sigma[1,5]	T1s1	CLK1 frequency[3] 25 MHz	—	120	250	ps
Jitter, absolute[1, 5]	Tabs1	CLK1 frequency[3] 25 MHz	-400	±250	400	ps
Jitter, one sigma[1, 5]	T1s2	CLK1 frequency < 25 MHz	—	—	1	%
Jitter, absolute[1, 5]	Tabs2	CLK1 frequency < 25 MHz	—	—	2	%
Line-to-line jitter,[1] absolute[2]	TLabs		—	±4	—	ns
Input Frequency,[1] IN or FBIN	fin	See allowable fi below:	12	—	1000	kHz
CLK1 Frequency[1, 3, 4] MK9173-01	f_{CLK1}	12 ≤ fin ≤ 14 kHz	44.0	—	75	MHz
		14 < fin ≤ 17 kHz	30.0	—	75	MHz
		17 < fin ≤ 30 kHz	25.0	—	75	MHz
		30 < fin ≤ 35 kHz	15.0	—	75	MHz
		35 < fin ≤ 1000 kHz	10.0	—	75	MHz
CLK1 Frequency[1, 3, 4] MK9173-15	f_{CLK1}	12 ≤ fin ≤ 14 kHz	22.0	—	37.5	MHz
		14 < fin ≤ 17 kHz	15.0	—	37.5	MHz
		17 < fin ≤ 30 kHz	12.5	—	37.5	MHz
		30 < fin ≤ 35 kHz	7.5	—	37.5	MHz
		35 < fin ≤ 1000 kHz	5.0	—	37.5	MHz

Notes:

1. Parameter is guaranteed by design and characterization. Not 100% tested in production.
2. Input Reference Frequency = 25 kHz, Output Frequency = 25 MHz. Jitter measured between adjacent vertical pixels.
3. CLK1 frequency applies for FS = 0. For FS = 1 condition, divide allowable CLK1 range by the factor of 4.
4. An Application Brief (AB01) documents the operation of the AV9173 for low input frequencies. This provides guidelines for usable output frequencies and feedback ratios required to use inputs below 25 kHz. By following these guidelines, the MK9173 will operate down to 12 kHz inputs across temperature, voltage and lot-to-lot variation.
5. Jitter values are measured at frequencies ≥25 MHz for MK9173-01, for MK9173-15, jitter is measured at frequency ≥12.5 MHz.

8-Pin SOIC PACKAGE



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	0.0532	0.0688
A1	1.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	0.1497	0.1574
e	1.27 Basic		0.050 Basic	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
a	0°	8°	0°	8°

Ordering Information

Order Number	Part Marking	Package	Shipping Packaging
MK9173-01CS08	MK73-1	8 pin SOIC	Tubes
MK9173-01CS08T	MK73-1	8 pin SOIC	Tape and Reel
MK9173-15CS08	MK73-15	8 pin SOIC	Tubes
MK9173-15CS08T	MK73-15	8 pin SOIC	Tape and Reel