

MC74HC589A

8-Bit Serial or Parallel-Input/Serial-Output Shift Register with 3-State Output

High-Performance Silicon-Gate CMOS

The MC74HC589A device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table). The shift register output, Q_H , is a three-state output, allowing this device to be used in bus-oriented systems.

The HC589A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

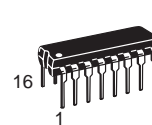
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 526 FETs or 131.5 Equivalent Gates



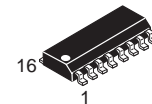
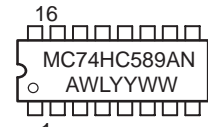
ON Semiconductor

<http://onsemi.com>

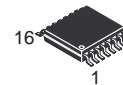
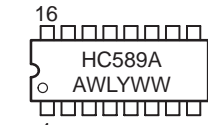
MARKING DIAGRAMS



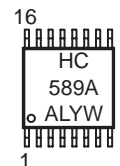
PDIP-16
N SUFFIX
CASE 648



SO-16
D SUFFIX
CASE 751B

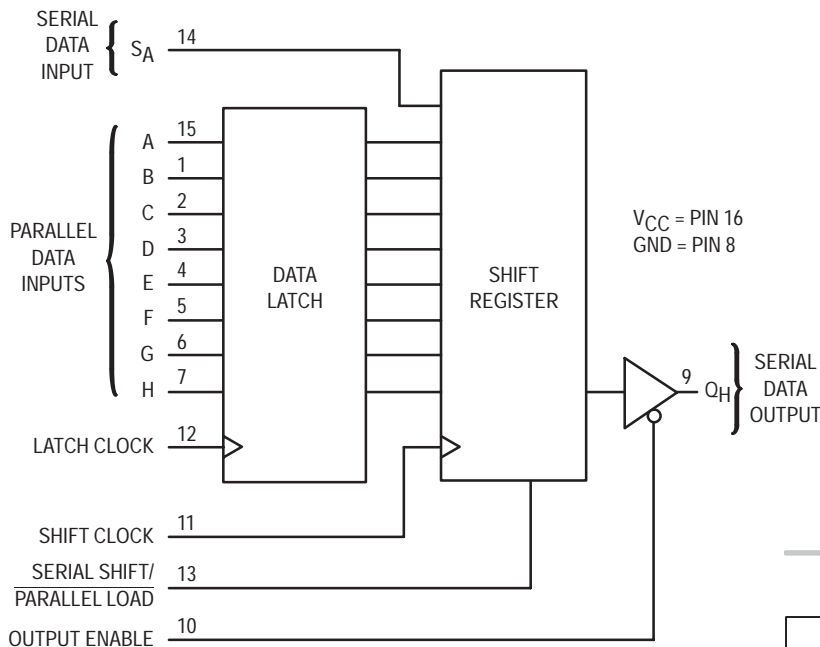


TSSOP-16
DT SUFFIX
CASE 948F

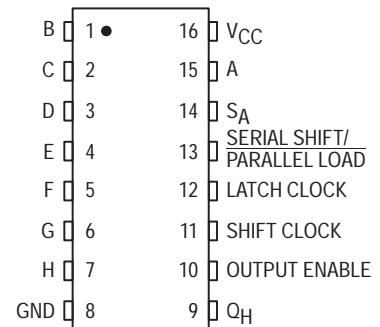


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

LOGIC DIAGRAM



PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC589AN	PDIP-16	2000 / Box
MC74HC589AD	SOIC-16	48 / Rail
MC74HC589ADR2	SOIC-16	2500 / Reel
MC74HC589ADT	TSSOP-16	96 / Rail
MC74HC589ADTR2	TSSOP-16	2500 / Reel

MC74HC589A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

TSSOP Package: -6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			ns
	V _{CC} = 2.0 V	0	1000	
	V _{CC} = 3.0 V	0	TBD	
	V _{CC} = 4.5 V	0	500	
	V _{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	± 0.5	± 5.0	± 10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0	6.0	4.8	4.0	MHz
		3.0	TBD	TBD	TBD	
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _H (Figures 1 and 8)	2.0	175	225	275	ns
		3.0	100	110	125	
		4.5	40	50	60	
		6.0	30	40	50	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to Q _H (Figures 2 and 8)	2.0	160	200	240	ns
		3.0	90	130	160	
		4.5	30	40	48	
		6.0	25	30	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q _H (Figures 4 and 8)	2.0	160	200	240	ns
		3.0	90	130	160	
		4.5	30	40	48	
		6.0	25	30	40	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q _H (Figures 3 and 9)	2.0	150	170	200	ns
		3.0	80	100	130	
		4.5	27	30	40	
		6.0	23	25	30	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q _H (Figures 3 and 9)	2.0	150	170	200	ns
		3.0	80	100	130	
		4.5	27	30	40	
		6.0	23	25	30	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	60	75	90	ns
		3.0	TBD	TBD	TBD	
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

CPD	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	
		50	

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, A–H to Latch Clock (Figure 5)	2.0	100	125	150	ns
		3.0	TBD	TBD	TBD	
		4.5	20	25	30	
		6.0	17	21	26	
t _{su}	Minimum Setup Time, Serial Data Input S _A to Shift Clock (Figure 6)	2.0	100	125	150	ns
		3.0	TBD	TBD	TBD	
		4.5	20	25	30	
		6.0	17	21	26	
t _{su}	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0	100	125	150	ns
		3.0	TBD	TBD	TBD	
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Latch Clock to A–H (Figure 5)	2.0	25	30	40	ns
		3.0	TBD	TBD	TBD	
		4.5	5	6	8	
		6.0	5	6	7	
t _h	Minimum Hold Time, Shift Clock to Serial Data Input S _A (Figure 6)	2.0	5	5	5	ns
		3.0	5	5	5	
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Shift Clock (Figure 2)	2.0	75	95	110	ns
		3.0	TBD	TBD	TBD	
		4.5	15	19	23	
		6.0	13	16	19	
t _w	Minimum Pulse Width, Latch Clock (Figure 1)	2.0	80	100	120	ns
		3.0	TBD	TBD	TBD	
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 4)	2.0	80	100	120	ns
		3.0	TBD	TBD	TBD	
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	TBD	TBD	TBD	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Output Enable	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S _A	Parallel Inputs A–H	Data Latch Contents	Shift Register Contents	Output Q _H
Force output into high impedance state	H	X	X	X	X	X	X	X	Z
Load parallel data into data latch	L	H		L, \overline{R}_L	X	a–h	a–h	U	U
Transfer latch contents to shift register	L	L	L, \overline{R}_L	X	X	X	U	LR _N SR _N	LR _H
Contents of input latch and shift register are unchanged	L	H	L, \overline{R}_L	L, \overline{R}_L	X	X	U	U	U
Load parallel data into data latch and shift register	L	L		X	X	a–h	a–h	a–h	h
Shift serial data into shift register	L	H	X		D	X	*	SR _A = D, SR _N SR _{N+1}	SR _G SR _H
Load parallel data in data latch and shift serial data into shift register	L	H			D	a–h	a–h	SR _A = D, SR _N SR _{N+1}	SR _G SR _H

LR = latch register contents

SR = shift register contents

a–h = data at parallel data inputs A–H

D = data (L, H) at serial data input S_A

U = remains unchanged

X = don't care

Z = high impedance

* = depends on Latch Clock input

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SWITCHING WAVEFORMS

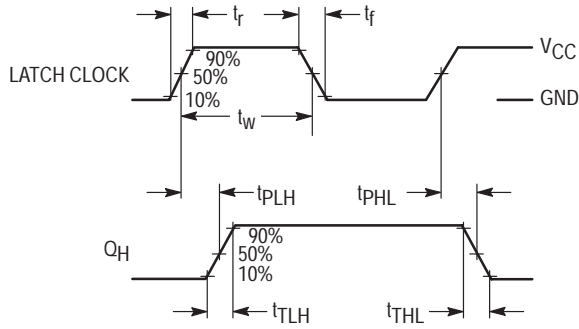


Figure 1. (Serial Shift/Parallel Load = L)

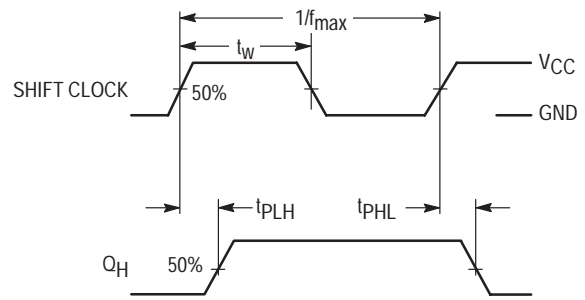


Figure 2. (Serial Shift/Parallel Load = H)

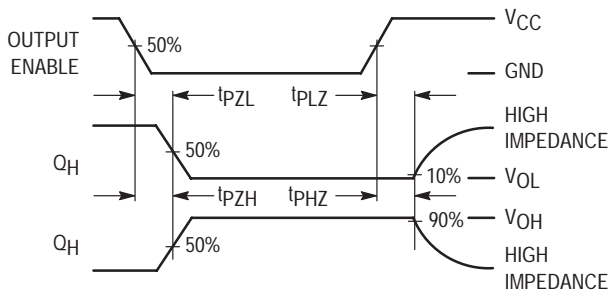


Figure 3.

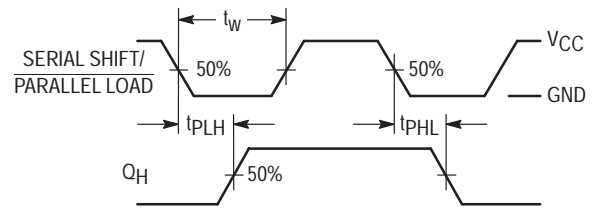


Figure 4.

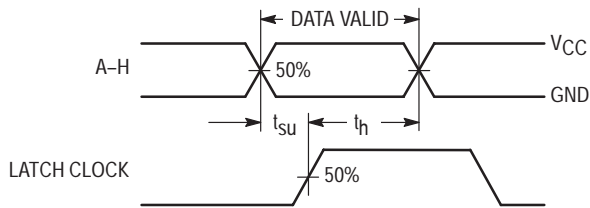


Figure 5.

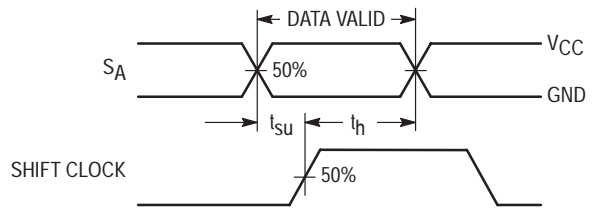


Figure 6.

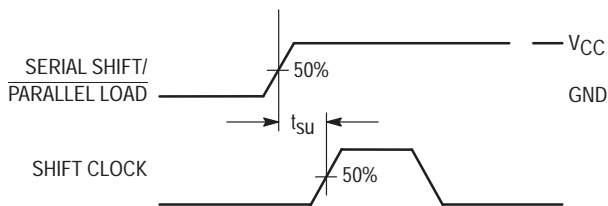
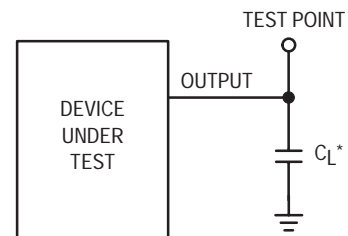


Figure 7.

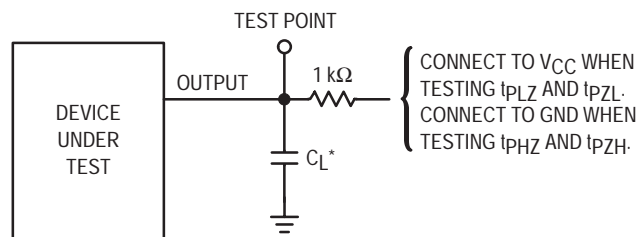


*Includes all probe and jig capacitance

Figure 8. Test Circuit

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TEST CIRCUIT



*Includes all probe and jig capacitance

Figure 9.

PIN DESCRIPTIONS

DATA INPUTS

A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Parallel data inputs. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.

SA (Pin 14)

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

CONTROL INPUTS

Serial Shift/Parallel Load (Pin 13)

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.

Shift Clock (Pin 11)

Serial shift clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and

data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

Latch Clock (Pin 12)

Data latch clock. A low-to-high transition on this input loads the parallel data on inputs A–H into the data latch.

Output Enable (Pin 10)

Active-low output enable A high level applied to this pin forces the Q_H output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.

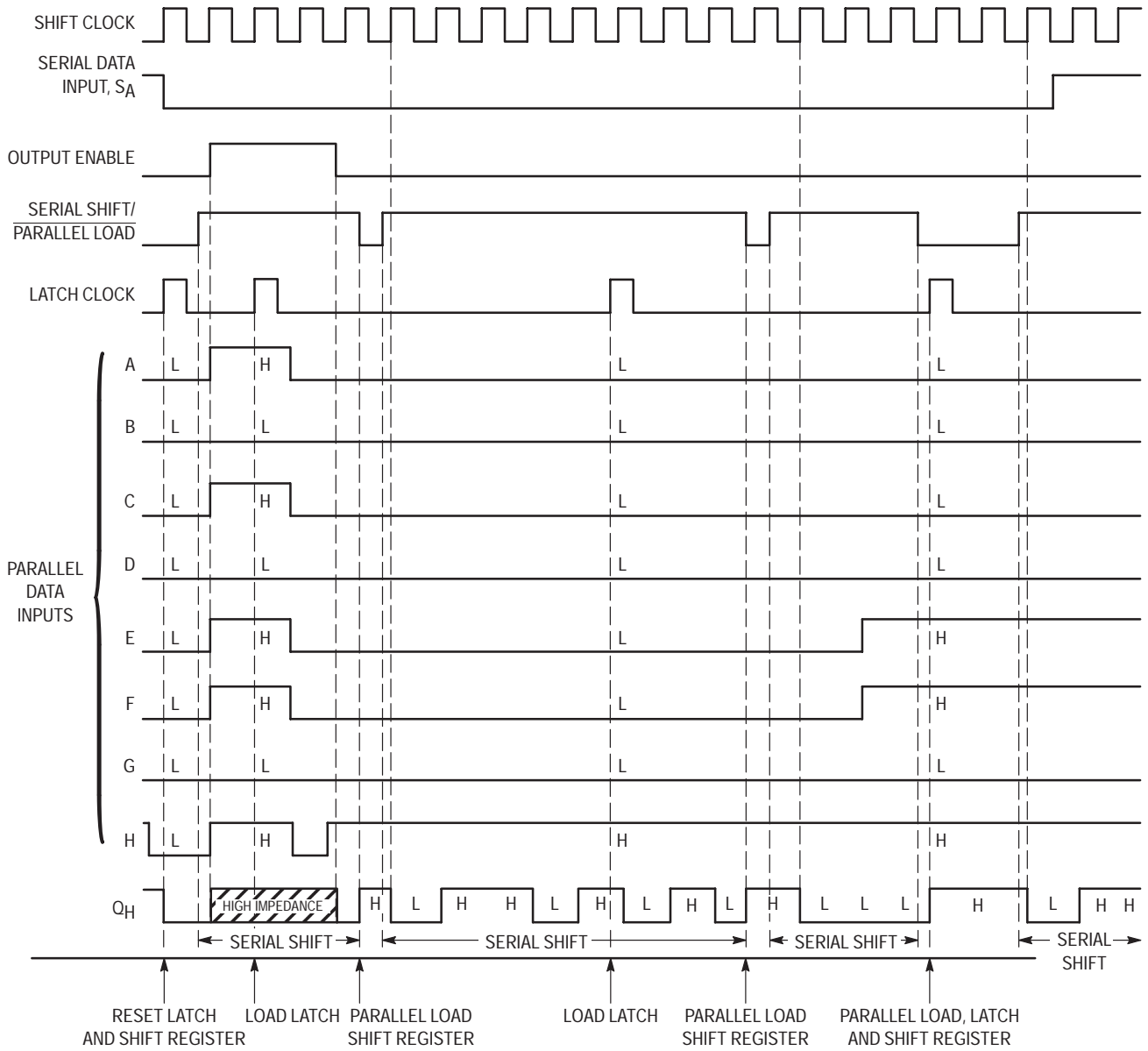
OUTPUT

Q_H (Pin 9)

Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.

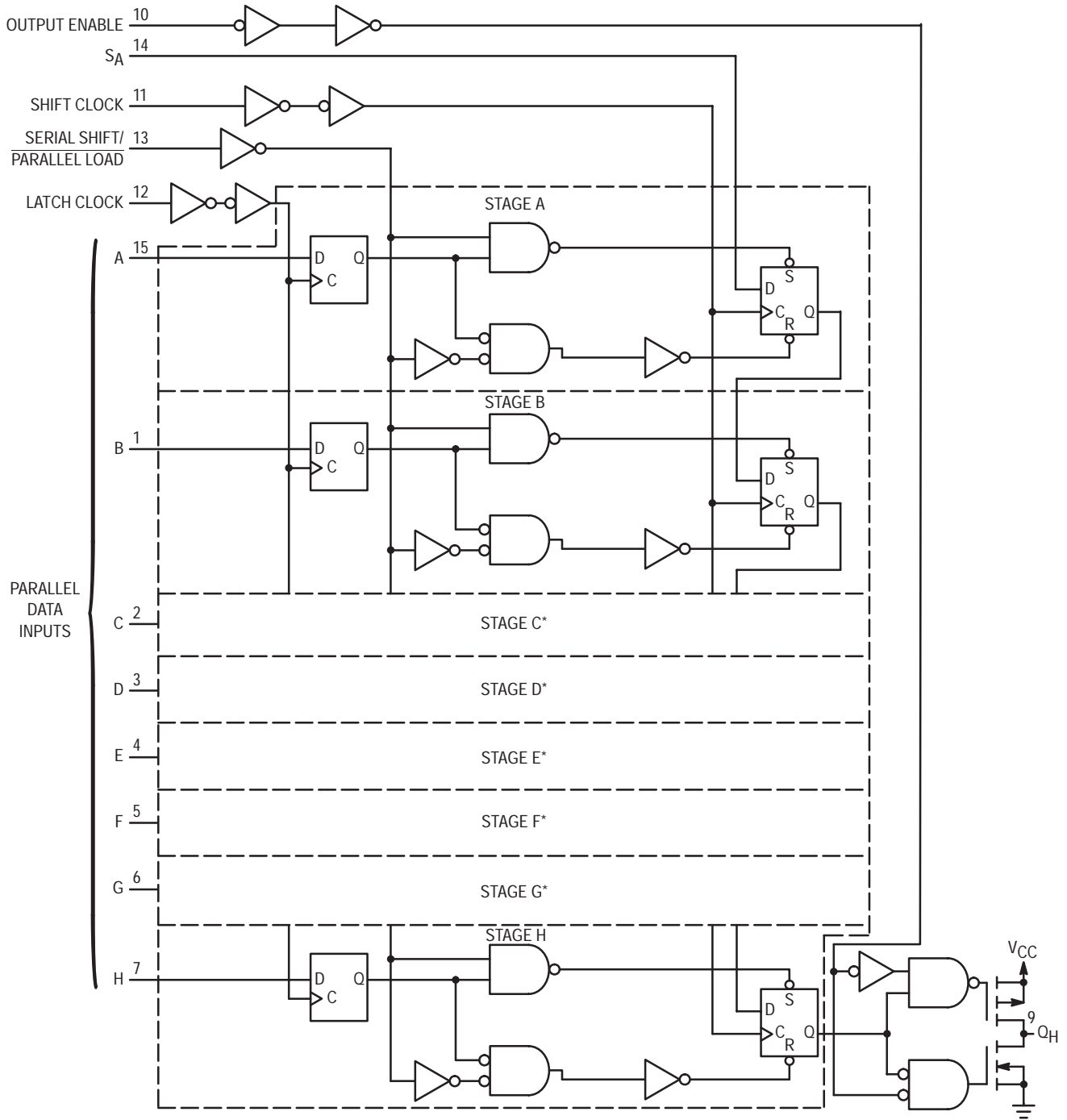
MC74HC589A

TIMING DIAGRAM



MC74HC589A

LOGIC DETAIL

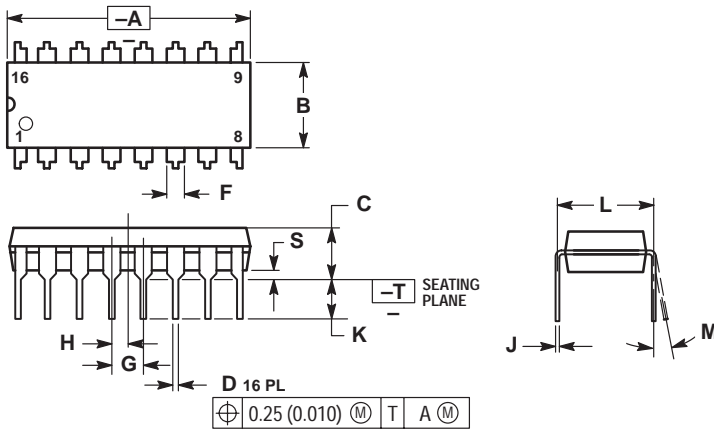


*NOTE: Stages C thru G (not shown in detail) are identical to stages A and B above.

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PACKAGE DIMENSIONS

PDIP-16
N SUFFIX
CASE 648-08
ISSUE R

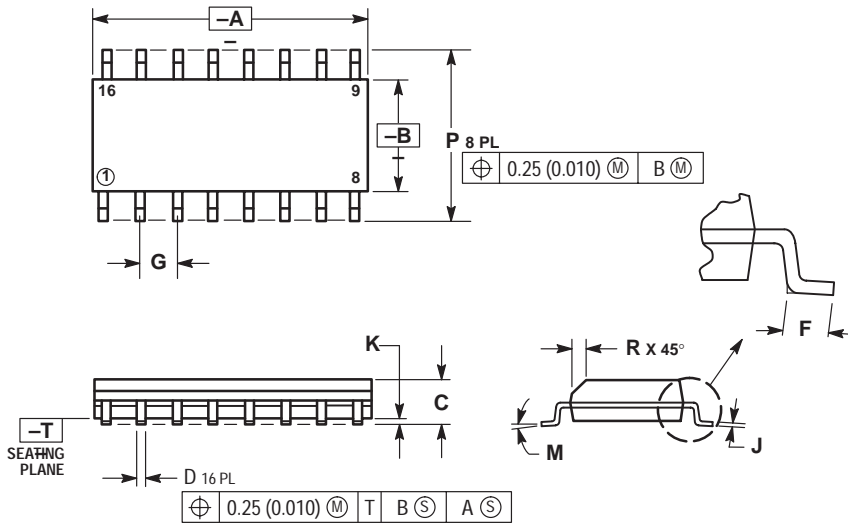


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J



NOTES:

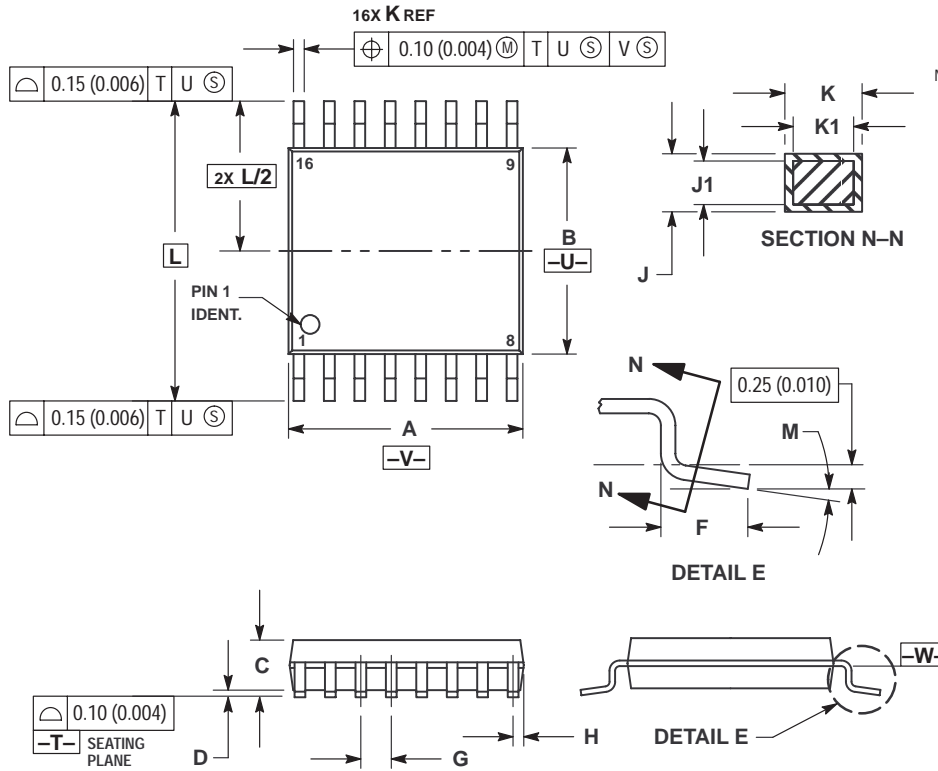
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

MC74HC589A

PACKAGE DIMENSIONS


TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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