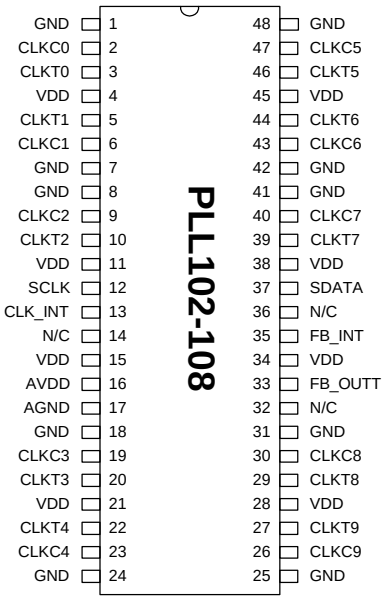
PLL102-108

Programmable DDR Zero Delay Clock Driver

FEATURES

- PLL clock distribution optimized for Double Data Rate SDRAM application up to 266Mhz.
- Distributes one clock Input to one bank of ten differential outputs.
- Track spread spectrum clocking for EMI reduction.
- Programmable delay between CLK_INT and CLK[T/C] from –0.8ns to +3.1ns by programming CLKINT and FBOUT skew channel, or from –1.1ns to +3.5ns if additional DDR skew channels are enabled.
- Four independent programmable DDR skew channels from –0.3ns to +0.4ns with step size ±100ps.
- Support 2-wire I2C serial bus interface.
- 2.5V Operating Voltage.
- Available in 48-Pin 300mil SSOP.

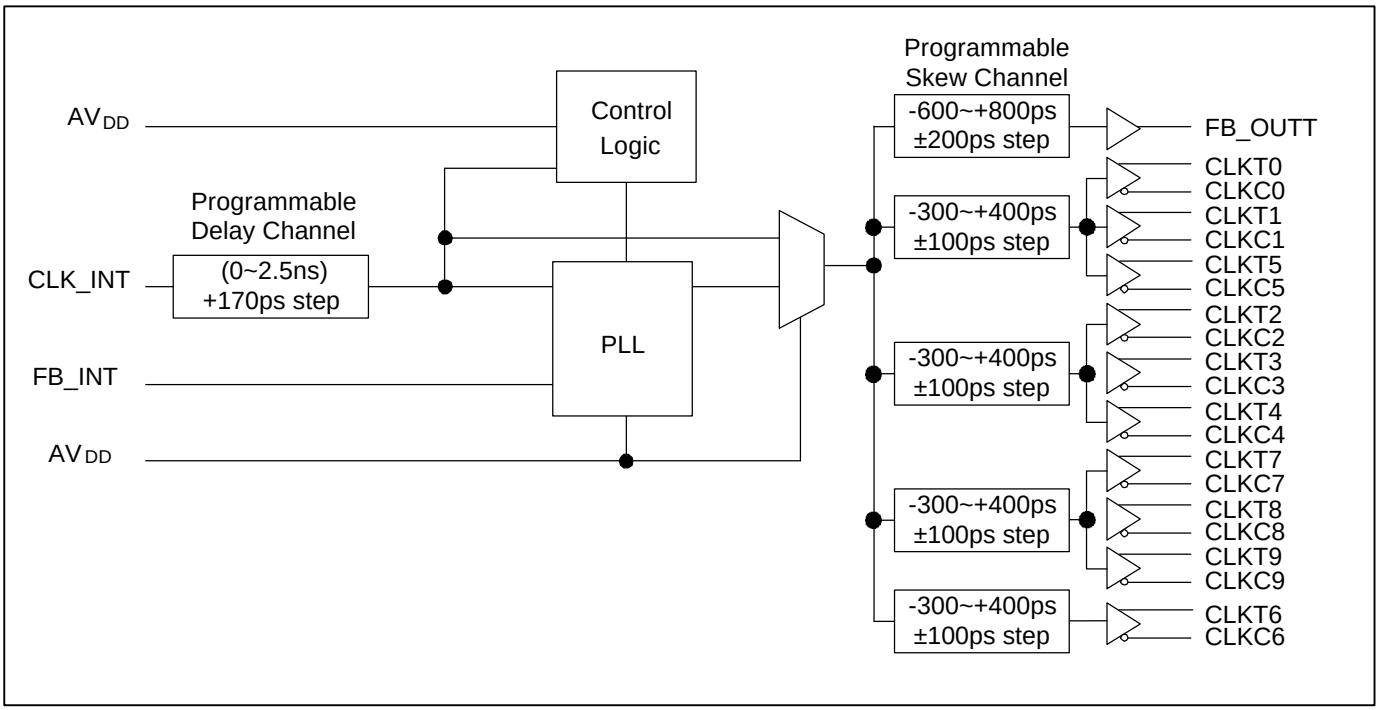
PIN CONFIGURATION



DESCRIPTIONS

The PLL102-108 is a zero delay buffer that distributes a single-ended clock input to ten pairs of differential clock outputs and one feedback clock output. Output signal duty cycles are adjusted to 50%, independent of the duty cycle at CLK_INT. The PLL can be bypassed for test purposes by strapping AV_{dd} to ground.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
VDD	4,11,15,21,28,34, 38,45	P	2.5V power supply.
GND	1,7,8,18,24, 25,31,41,42,48	P	Ground
AVDD	16	P	Analog power supply (2.5V).
AGND	17	P	Analog ground.
CLKT(0:9)	3,5,10,20,22,46, 44,39,29,27	I	“True” clocks of differential pair outputs.
CLKC(0:9)	2,6,9,19,23,47, 43,40,30,26	I	“Complementary” clocks of differential pair outputs.
CLK_INT	13	I	Single-ended 3.3V tolerant input.
N/C	14,32,36		Not connected.
FB_OUTT	33	O	“True” feedback output. Dedicated for external feedback. It switches at the same frequency as the CLK_INT.
FB_INT	35	I	“True” feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
SDATA	37	B	Serial data input for serial interface port.
SCLK	12	I	

Functionality

INPUTS			OUTPUTS			PLL State
AVDD	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	
2.5V (Nom)	L	H	L	H	L	On
2.5V (Nom)	H	L	H	L	H	On
GND	L	H	L	H	L	Bypass/Off
GND	H	L	H	L	H	Bypass/Off

I2C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	_
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Data Protocol	This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD4) or a read condition (0xD5). Following the acknowledge of this address byte, in **Write Mode:** the **Command Byte** and **Byte Count Byte must be sent by the master** but ignored by the slave, in **Read Mode:** the **Byte Count Byte** will be **read by the master** then all other **Data Byte**. **Byte Count Byte** default at power-up is = (0x09).							

I2C CONTROL REGISTERS

1. BYTE 0: Outputs Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	39,40	1	CLKT7, CLKC7 (1= active, 0=inactive)
Bit 6	43,44	1	CLKT6, CLKC6 (1= active, 0=inactive)
Bit 5	46,47	1	CLKT5, CLKC5 (1= active, 0=inactive)
Bit 4	22,23	1	CLKT4, CLKC4 (1= active, 0=inactive)
Bit 3	19,20	1	CLKT3, CLKC3 (1= active, 0=inactive)
Bit 2	9,10	1	CLKT2, CLKC2 (1= active, 0=inactive)
Bit 1	5,6	1	CLKT1, CLKC1 (1= active, 0=inactive)
Bit 0	2,3	1	CLKT0, CLKC0 (1= active, 0=inactive)

TABLE 1: Output Signals SKEW Programming Summary:

Bit<2:0>	DDR Skew Setting (±100ps/step)		FBOUT Skew Setting (±200ps/step)	
111	+400ps	Setting applies to the following outputs: 1. DDRA: CLK0, CLK1, CLK5 2. DDRB: CLK7, CLK8, CLK9 3. DDRC: CLK2, CLK3, CLK4 4. DDRD: CLK6	+800ps	Setting applies to the following outputs: 1. FB_OUTT
110	+300ps		+600ps	
101	+200ps		+400ps	
100	+100ps		+200ps	
011	**Default**		**Default**	
010	-100ps		-200ps	
001	-200ps		-400ps	
000	-300ps		-600ps	

2. BYTE 1: SKEW Register (1=Enable, 0=Disable)

Bit	Name		Default	Description
Bit 7	26,27		1	CLKT9, CLKC9 (1= active, 0=inactive)
Bit 6	29,30		1	CLKT8, CLKC8 (1= active, 0=inactive)
Bit 5	Skew DDRA	Bit <2>	0	These three bits will adjust timing of DDRA signals (CLK0, CLK1, CLK5) either positive or negative delay up to +400ps or –300ps with ±100ps per step. (see Table 1)
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	Skew DDRB	Bit <2>	0	These three bits will adjust timing of DDRB signals (CLK7, CLK8, CLK9) either positive or negative delay up to +400ps or –300ps with ±100ps per step. (see Table 1)
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

3. BYTE 2: SKEW Register (1=Enable, 0=Disable)

Bit	Name		Default	Description
Bit 7	DDR-SKEWEN		1	1= disable, 0= enable
Bit 6	FBOUT-SKEWEN		1	1= disable, 0= enable
Bit 5	Skew DDRC	Bit <2>	0	These three bits will adjust timing of DDRC signals (CLK2, CLK3, CLK4) either positive or negative delay up to +400ps or –300ps with ±100ps per step. (see Table 1)
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	Skew DDRD	Bit <2>	0	These three bits will adjust timing of DDRD signals (CLK6) either positive or negative delay up to +400ps or –300ps with ±100ps per step. (see Table 1)
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

4. BYTE 3: Outputs Register (1=Enable, 0=Disable)

Bit	Name		Default	Description
Bit 7	-		1	Reserved
Bit 6	Skew FBOUT	Bit <2>	0	These three bits will adjust timing of FBOUTT signal either positive or negative delay up to +800ps or –600ps with ±200ps per step. (see Table 1)
Bit 5		Bit <1>	1	
Bit 4		Bit <0>	1	
Bit 3	Delay CLKINT	Bit <3>	0	These four bits will program the propagation delay from CLK_INT to the input of PLL within the range between 0ps and 2.5ns with 170ps step size. (see Table 2)
Bit 2		Bit <2>	0	
Bit 1		Bit <1>	0	
Bit 0		Bit <0>	0	

TABLE 2: CLK_INT Delay Programming Summary:

Bit<3:0>	CLK_INT to CLK Delay
1111	+2,550 ps
1110	+2,380 ps
1101	+2,210 ps
1100	+2,040 ps
1011	+1,870 ps
1010	+1,700 ps
1001	+1,530 ps
1000	+1,360 ps
0111	+1,190 ps
0110	+1,020 ps
0101	+850 ps
0100	+680 ps
0011	+510 ps
0010	+340 ps
0001	+170 ps
0000	Default

TABLE 3: Output Drive Strength Programming Summary:

Bit<2:0>	Programming Setting	
111	+40%	Setting applies to the following outputs 1. DDRA (CLK0, CLK1, CLK5) 2. DDRB (CLK7, CLK8, CLK9) 3. DDRC (CLK2, CLK3, CLK4) 4. DDRD (CLK6) 5. FBOUT
110	+30%	
101	+20%	
100	+10%	
011	**Default**	
010	-10%	
001	-20%	
000	-30%	

5. Byte 4: Buffer Drive Strength Control Register

Bit	Name		Default	Description
Bit 7	-		1	Reserved.
Bit 6	-		1	Reserved.
Bit 5	DDRA Strength	Bit <2>	0	These three bits will program drive strength for CLK0, CLK1 and CLK5 output clocks (see Table 3).
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	DDRB Strength	Bit <2>	0	These three bits will program drive strength for CLK7, CLK8 and CLK9 output clocks (see Table 3).
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

6. Byte 5: Buffer Drive Strength Control Register

Bit	Name		Default	Description
Bit 7	-		1	Reserved.
Bit 6	-		1	Reserved.
Bit 5	DDRC Strength	Bit <2>	0	These three bits will program drive strength for CLK2, CLK3 and CLK4 output clocks (see Table 3).
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	DDRD Strength	Bit <2>	0	These three bits will program drive strength for CLK6 output clock (see Table 3).
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

7. Byte 6: Buffer Drive Strength Control Register

Bit	Name		Default	Description
Bit 7	-		1	Reserved.
Bit 6	-		1	Reserved.
Bit 5	-		1	Reserved.
Bit 4	-		1	Reserved.
Bit 3	-		1	Reserved.
Bit 2	FBOUT Strength	Bit <2>	0	These three bits will program drive strength for FBOUTT output clock (see Table 3).
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{CC}	-0.5	3.6	V
Input Voltage Range	V_I	-0.5	V_{CC}+0.5	V
Output Voltage Range	V_O	-0.5	V_{CC}+0.5	V
Storage Temperature	T_S	-65	150	°C
Maximum power dissipation at T_A = 55°C in still air	PW		0.7	W

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating supply current	$I_{DD2.5}$	CL = 0 pF (Fclk=100Mhz)		250		mA
	I_{DDPD}	CL = 0 pF			100	uA
High Impedance output current	I_{OZ}	VDD=2.7V, V_{OUT}=VDD or GND			±10	uA
Input clamp voltage	V_{IK}	I_{in} = -18mA			-1.2	V
Input Capacitance	C_{IN}	V_I = VDD or GND		2		pF
Output Capacitance	C_{OUT}	V_O = VDD or GND		3		pF
High level output voltage	V_{OH}	VDD = Min to Max, I_{OH} = -1mA	VDD-0.1			V
		VDD = 2.3V, I_{OH} = -12mA	1.7			V
Low level output voltage	V_{OL}	VDD = Min to Max, I_{OL} = 1mA			0.1	V
		VDD = 2.3V, I_{OL} = 12mA			0.6	V
Output differential-pair crossing voltage	V_{OC}		(VDD/2)-0.2		(VDD/2)+0.2	V

3. Recommended Operating Conditions

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Output supply voltage	V_{CC}	2.3	2.5	2.7	V
Analog Supply voltage	A_{CC}	2.3	2.5	2.7	V
High level input voltage	V_{IH}	0.7 x V_{CC}			V
Low level input voltage	V_{IL}			0.3 x V_{CC}	V
Operating free-air temperature	T_A	0		70	°C

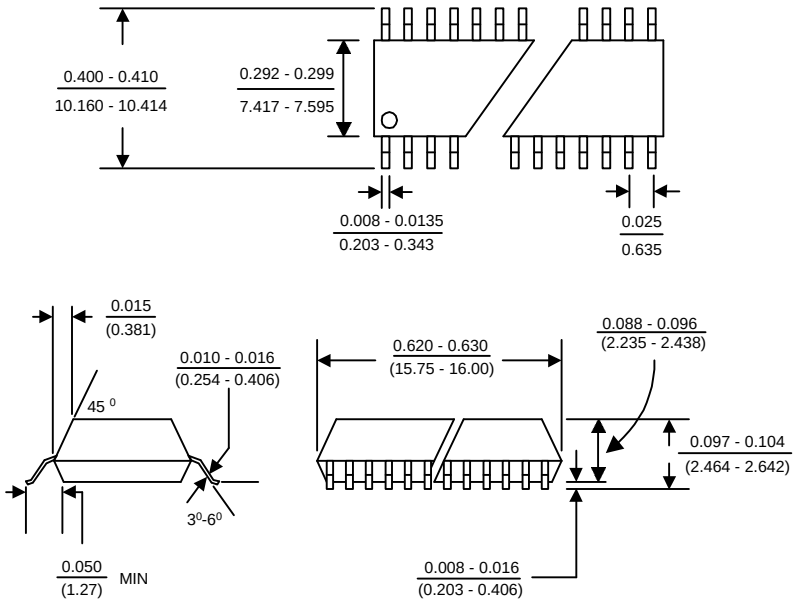
4. Timing requirements

SYMBOL	PARAMETERS	MIN.	MAX.	UNITS
F_{CLK}	Input clock frequency	66	266	MHz
D_{IN}	Input clock duty cycle	40	60	%
T_S	Stabilization time after power up		0.1	ms

5. Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Low to high level propagation delay time	T_{PLH}	CLK_INT to any output		0		ns
High to low level propagation delay time	T_{PHL}	CLK_INT to any output		0		ns
Jitter (peak to peak)	T_{p-p}	66MHz			120	ps
		100/133/200/266MHz			75	ps
Jitter (cycle to cycle)	$T_{cyc-cyc}$	66MHz			110	ps
		100/133/200/266MHz			65	ps
Phase error	$t_{(phase\ error)}$	All differential input and output terminals are terminated with 120Ω/16pF	-150		150	ps
Output to output skew	T_{oskew}				100	ps
Pulse skew	T_{pskew}				100	ps
Duty Cycle	D_T	66MHz to 100MHz	49.5		50.5	%
		101MHz to 266MHz	49		51	%
Rise time, Fall time	t_r, t_f	Load = 120Ω/16pF	650	800	950	ps

PACKAGE INFORMATION



48PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL102-108 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Phaselink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY: PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.