MC14538B

Dual Precision Retriggerable/Resettable Monostable Multivibrator

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

Output Pulse Width = $(Cx)(Rx)$ where:
Rx is in kΩ
Cx is in μF

- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10 μs to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive (A Input) or Negative–Going Edge (B–Input)
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin–for–pin Compatible with MC14528B and CD4528B (CD4098)
- Use the MC54/74HC4538A for Pulse Widths Less Than 10 μs with Supplies Up to 6 V.

http://onsemi.com

MARKING DIAGRAMS

PDIP–16
P SUFFIX
CASE 648

16 | MC14538BCP
 o AWLYYWW
1

SOIC–16
D SUFFIX
CASE 751B

16 | 14538B
 o AWLYWW
1

TSSOP–16
DT SUFFIX
CASE 948F

16 | 14
538B
 o ALYW
1
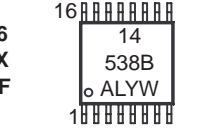
SOIC–16
DW SUFFIX
CASE 751G

16 | 14538B
O AWLYYWW
1
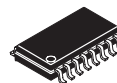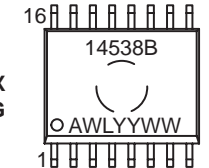
SOEIAJ–16
F SUFFIX
CASE 966

16 | MC14538B
AWLYWW
 o
1
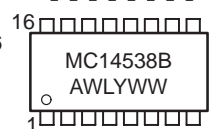
A   = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to $+18.0$	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Operating Temperature Range	-55 to $+125$	°C
T_{stg}	Storage Temperature Range	-65 to $+150$	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
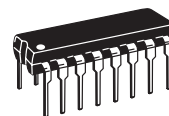
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
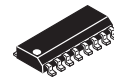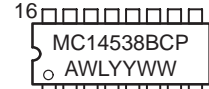
ORDERING INFORMATION

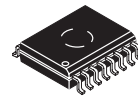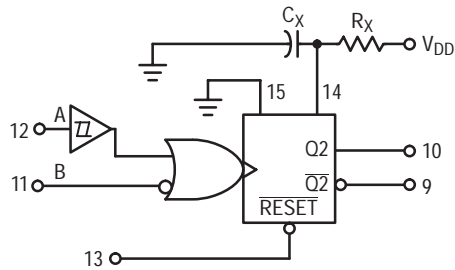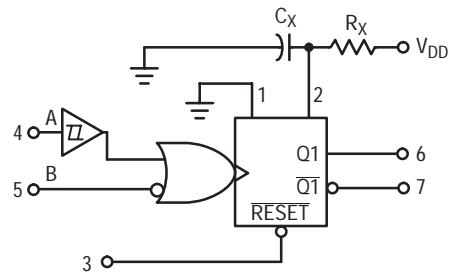| Device	Package	Shipping
MC14538BCP	PDIP–16	2000/Box
MC14538BD	SOIC–16	48/Rail
MC14538BDR2	SOIC–16	2500/Tape & Reel
MC14538BDT	TSSOP–16	96/Rail
MC14538BDTR2	TSSOP–16	2500/Tape & Reel
MC14538BDW	SOIC–16	47/Rail
MC14538BDWR2	SOIC–16	1000/Tape & Reel
MC14538BF	SOEIAJ–16	See Note 1.
MC14538BFEL	SOEIAJ–16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.
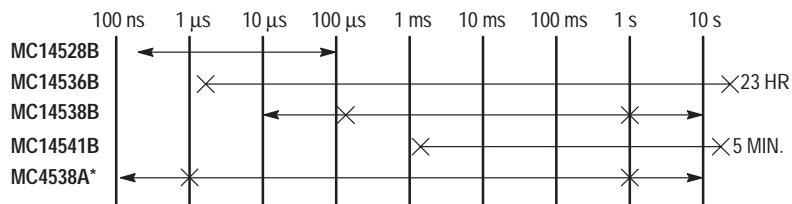
MC14538B

PIN ASSIGNMENT

V_{SS}	1 ●	16	V_{DD}
C_X/R_XA	2	15	V_{SS}
$\overline{RESET}$ A	3	14	C_X/R_XB
A_A	4	13	$\overline{RESET}$ B
$\overline{B}_A$	5	12	A_B
Q_A	6	11	$\overline{B}_B$
$\overline{Q}_A$	7	10	Q_B
V_{SS}	8	9	$\overline{Q}_B$
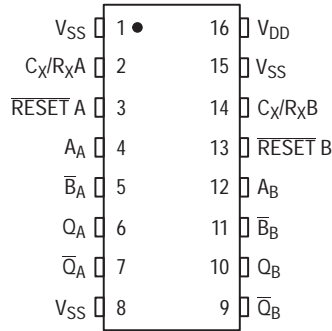
BLOCK DIAGRAM

R_X AND C_X ARE EXTERNAL COMPONENTS.
V_{DD} = PIN 16
V_{SS} = PIN 8, PIN 1, PIN 15

ONE–SHOT SELECTION GUIDE

*LIMITED OPERATING VOLTAGE (2 – 6 V)

TOTAL OUTPUT PULSE WIDTH RANGE
RECOMMENDED PULSE WIDTH RANGE

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ [4.]	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	− 3.0 − 0.64 − 1.6 − 4.2	— — — —	− 2.4 − 0.51 − 1.3 − 3.4	− 4.2 − 0.88 − 2.25 − 8.8	— — — —	− 1.7 − 0.36 − 0.9 − 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current, Pin 2 or 14	I_{in}	15	—	±0.05	—	±0.00001	±0.05	—	±0.5	µAdc
Input Current, Other Inputs	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance, Pin 2 or 14	C_{in}	—	—	—	—	25	—	—	—	pF
Input Capacitance, Other Inputs (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) Q = Low, $\overline{Q}$ = High	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Quiescent Current, Active State (Both) (Per Package) Q = High, $\overline{Q}$ = Low	I_{DD}	5.0 10 15	— — —	2.0 2.0 2.0	— — —	0.04 0.08 0.13	0.20 0.45 0.70	— — —	2.0 2.0 2.0	mAdc
Total Supply Current at an external load capacitance (C_L) and at external timing network (R_X, C_X) [5.]	I_T	5.0 10								µAdc

Total Supply Current formulas:

$$I_T = (3.5 \times 10^{-2})\, R_X C_X f + 4 C_X f + 1 \times 10^{-5}\, C_L f$$
$$I_T = (8.0 \times 10^{-2})\, R_X C_X f + 9 C_X f + 2 \times 10^{-5}\, C_L f$$
$$I_T = (1.25 \times 10^{-1})\, R_X C_X f + 12 C_X f + 3 \times 10^{-5}\, C_L f$$

where: I_T in µA (one monostable switching only), C_X in µF, C_L in pF, R_X in k ohms, and f in Hz is the input frequency.

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS [6.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ [7.]	Max	
Output Rise Time t_{TLH} = (1.35 ns/pF) C_L + 33 ns t_{TLH} = (0.60 ns/pF) C_L + 20 ns t_{TLH} = (0.40 ns/pF) C_L + 20 ns	t_{TLH}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Output Fall Time t_{THL} = (1.35 ns/pF) C_L + 33 ns t_{THL} = (0.60 ns/pF) C_L + 20 ns t_{THL} = (0.40 ns/pF) C_L + 20 ns	t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay Time A or B to Q or $\overline{Q}$ t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 300 150 100	 600 300 220	ns
$\overline{Reset}$ to Q or $\overline{Q}$ t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 205 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		 5.0 10 15	 — — —	 250 125 95	 500 250 190	ns
Input Rise and Fall Times $\overline{Reset}$	t_r, t_f	5 10 15	— — —	— — —	15 5 4	µs
B Input		5 10 15	— — —	300 1.2 0.4	1.0 0.1 0.05	ms
A Input		5 10 15	No Limit			—
Input Pulse Width A, B, or Reset	t_{WH}, t_{WL}	5.0 10 15	170 90 80	85 45 40	— — —	ns
Retrigger Time	t_{rr}	5.0 10 15	0 0 0	— — —	— — —	ns
Output Pulse Width — Q or $\overline{Q}$ Refer to Figures 8 and 9 C_X = 0.002 µF, R_X = 100 kΩ	T	 5.0 10 15	 198 200 202	 210 212 214	 230 232 234	µs
C_X = 0.1 µF, R_X = 100 kΩ		5.0 10 15	9.3 9.4 9.5	9.86 10 10.14	10.5 10.6 10.7	ms
C_X = 10 µF, R_X = 100 kΩ		5.0 10 15	0.91 0.92 0.93	0.965 0.98 0.99	1.03 1.04 1.06	s
Pulse Width Match between circuits in the same package. C_X = 0.1 µF, R_X = 100 kΩ	100 $[(T_1 - T_2)/T_1]$	5.0 10 15	— — —	± 1.0 ± 1.0 ± 1.0	± 5.0 ± 5.0 ± 5.0	%

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14538B

OPERATING CONDITIONS

External Timing Resistance	R_X	—	5.0	—	(8.)	kΩ
External Timing Capacitance	C_X	—	0	—	No Limit (9.)	µF

8. The maximum usable resistance R_X is a function of the leakage of the capacitor C_X, leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for $R_X > 1$ MΩ..
9. If $C_X > 15$ µF, use discharge protection diode per Fig. 11.
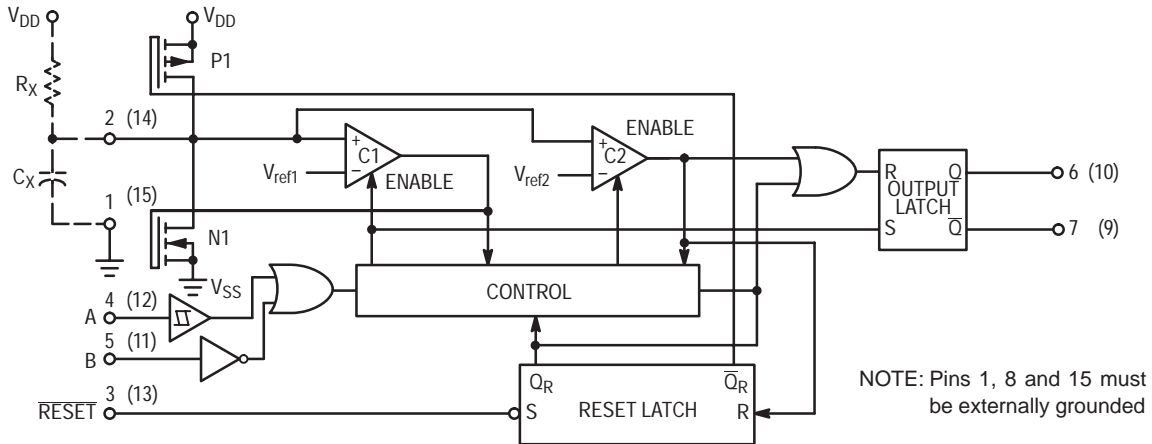
Figure 1. Logic Diagram
(1/2 of DevIce Shown)
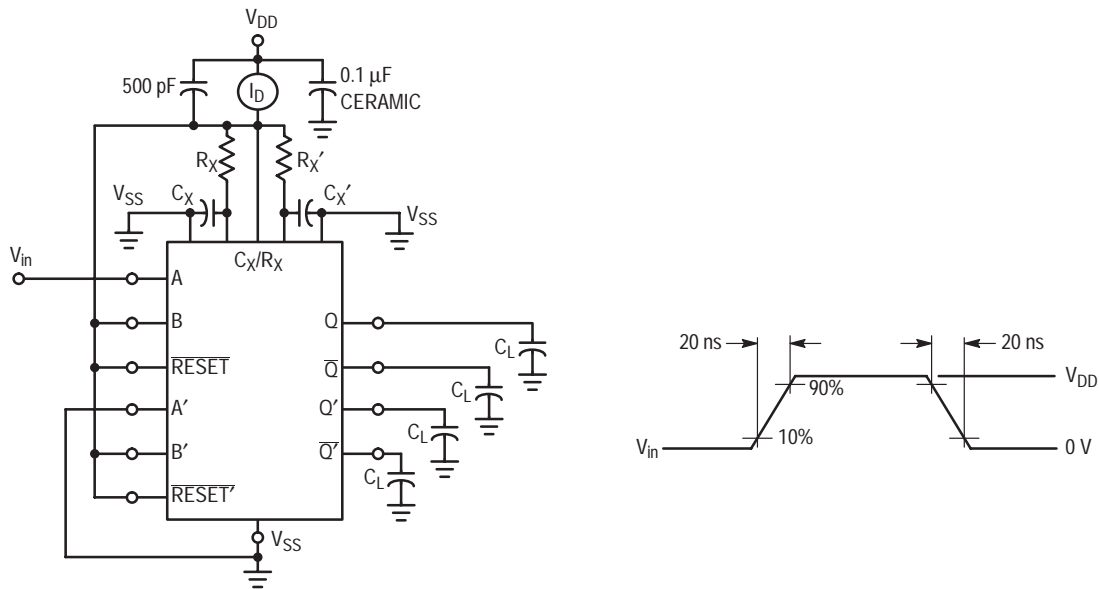
Figure 2. Power Dissipation Test Circuit and Waveforms

MC14538B

Figure 3. Switching Test Circuit

INPUT CONNECTIONS

Characteristics	Reset	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

* Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown In Figure 4.

PG1 =

PG2 =

PG3 =
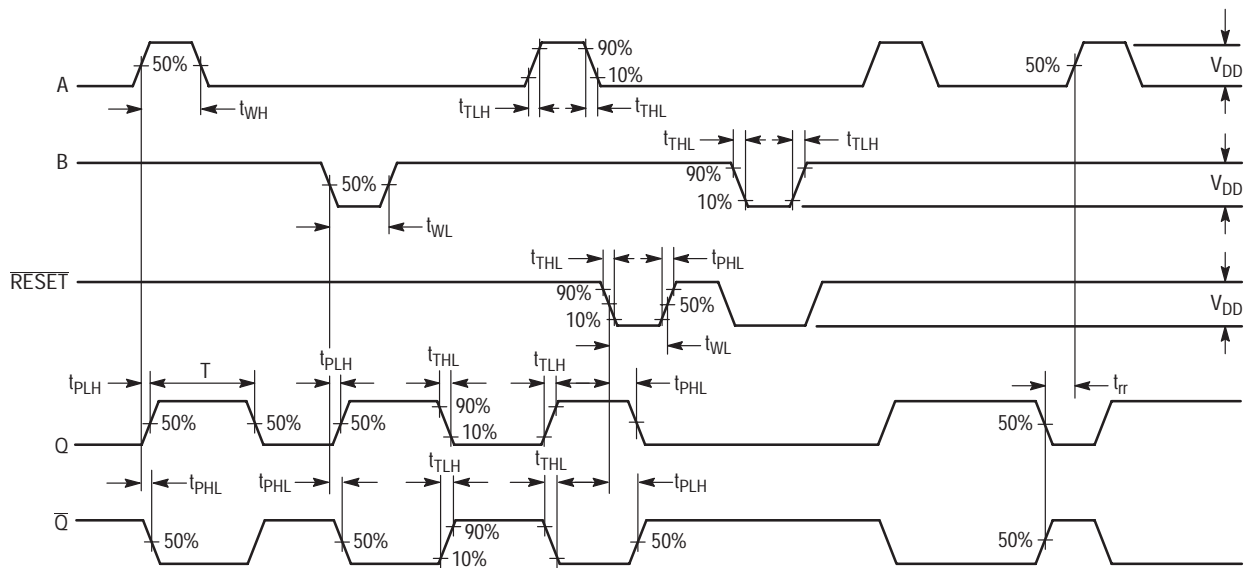
Figure 4. Switching Test Waveforms
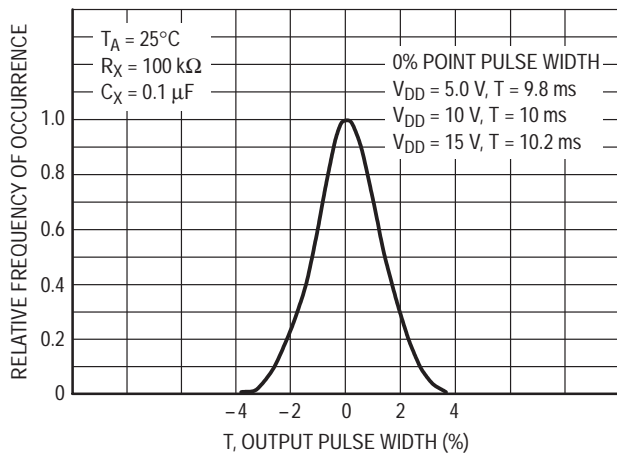
Figure 5. Typical Normalized Distribution of Units for Output Pulse Width
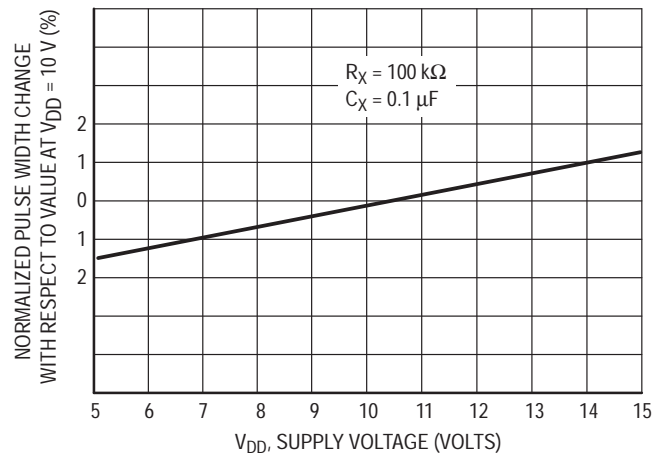
Figure 6. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

MC14538B
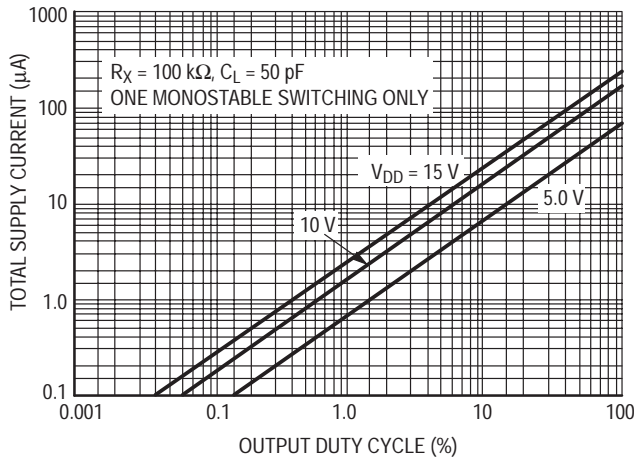
Figure 7. Typical Total Supply Current
versus Output Duty Cycle

FUNCTION TABLE

Inputs			Outputs	
$\overline{\text{Reset}}$	A	B	Q	$\overline{\text{Q}}$
H	⌐	H	⊓	⊔
H	L	⌐	⊓	⊔
H	⌐⌐	L	Not Triggered	
H	H	⌐⌐	Not Triggered	
H	L, H, ⌐	H	Not Triggered	
H	L	L, H, ⌐	Not Triggered	
L	X	X	L	H
⌐⌐	X	X	Not Triggered	
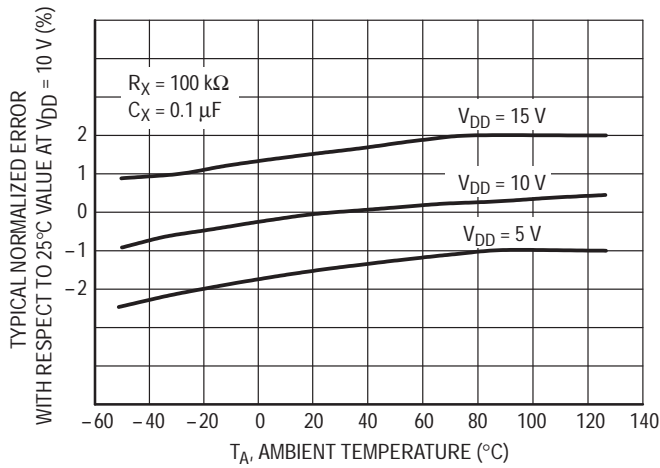
Figure 8. Typical Error of Pulse Width
Equation versus Temperature
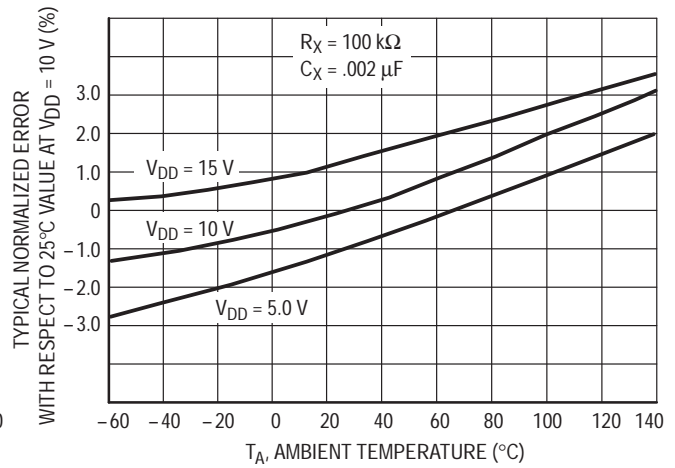
Figure 9. Typical Error of Pulse Width
Equation versus Temperature

MC14538B

THEORY OF OPERATION
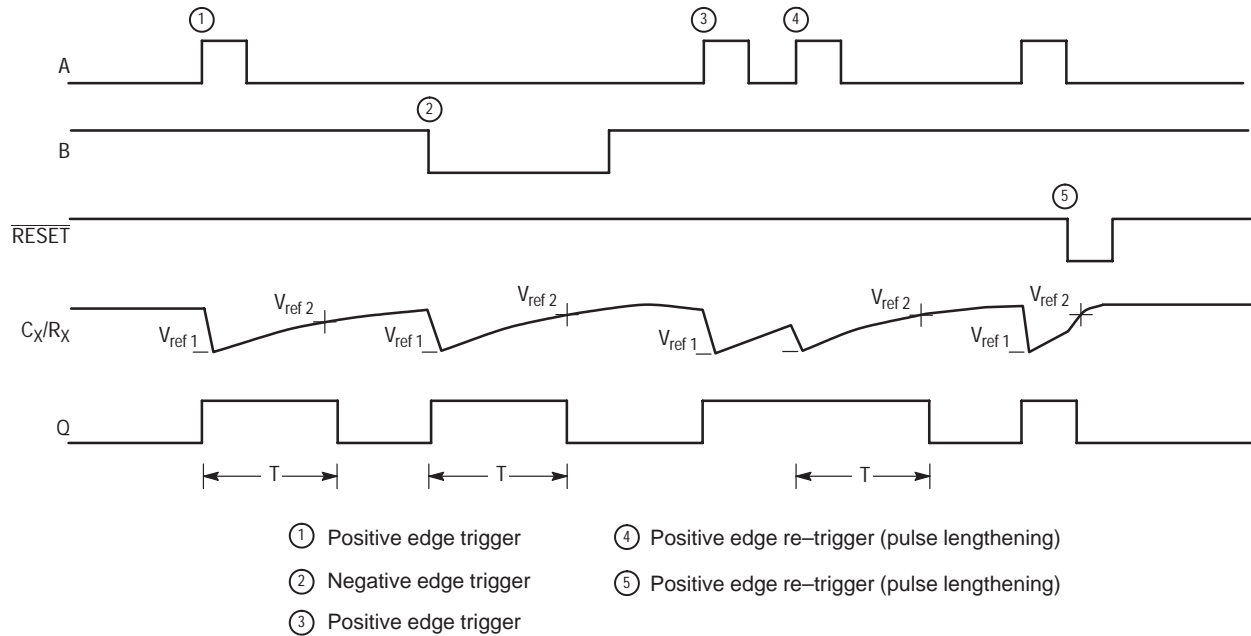
Figure 10. Timing Operation

TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and $\overline{Reset}$ are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N–channel transistor N1 . At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{ref1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals V_{ref2}, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 . This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state, C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are "off" with total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs followed by another valid trigger before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{ref1}, but has not yet reached V_{ref2}, will cause an increase in output pulse width T. When a valid retrigger is initiated , the voltage at C_X/R_X will again drop to V_{ref1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on $\overline{Reset}$ sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1 . When the voltage on the capacitor reaches V_{ref2}, the reset latch will clear, and will then be ready to accept another pulse. It the $\overline{Reset}$ input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the $\overline{Reset}$ input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER–DOWN CONSIDERATIONS

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B is powered down, the capacitor voltage may discharge from V_{DD} through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the V_{DD} supply must not be faster than (V_{DD}). $(C)/(10$ mA$)$. For example, if $V_{DD} = 10$ V and $C_X = 10\,\mu$F, the V_{DD} supply should discharge no faster than $(10$ V$)$ x $(10\,\mu$F$)/(10$ mA$)$ = 10 ms. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode, D_X, connected as shown in Fig. 11.
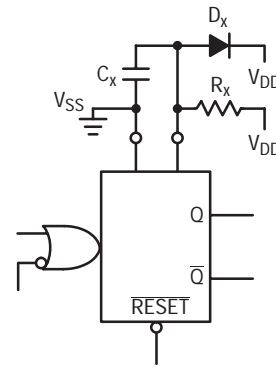
Figure 11. Use of a Diode to Limit Power Down Current Surge

TYPICAL APPLICATIONS
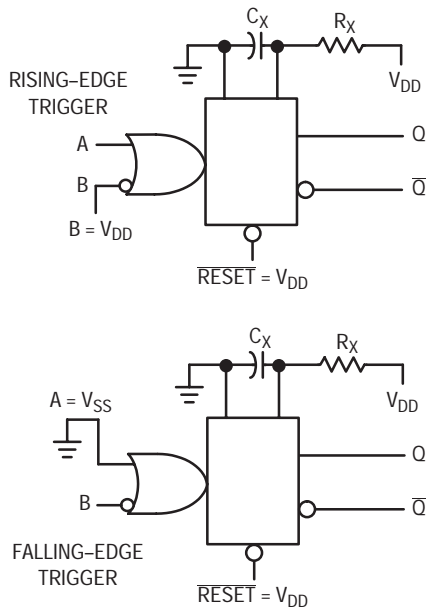
Figure 12. Retriggerable Monostables Circuitry
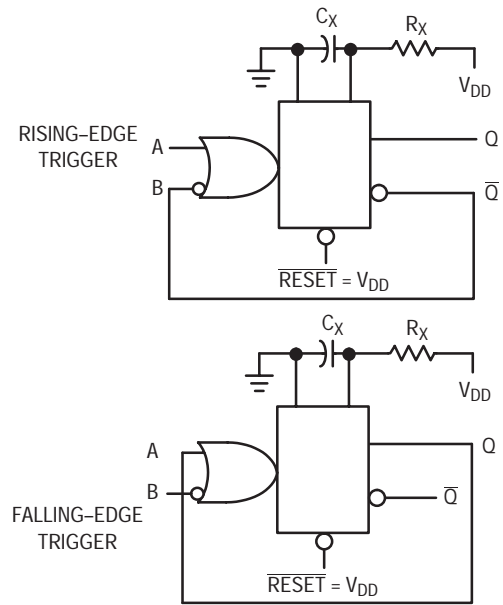
Figure 13. Non–Retriggerable Monostables Circuitry
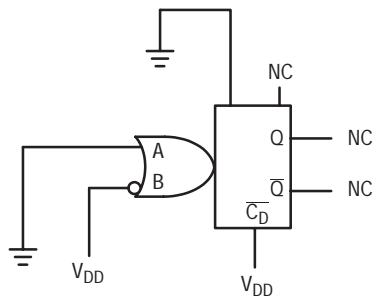
Figure 14. Connection of Unused Sections

MC14538B

PACKAGE DIMENSIONS

PDIP–16
**P SUFFIX**
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R
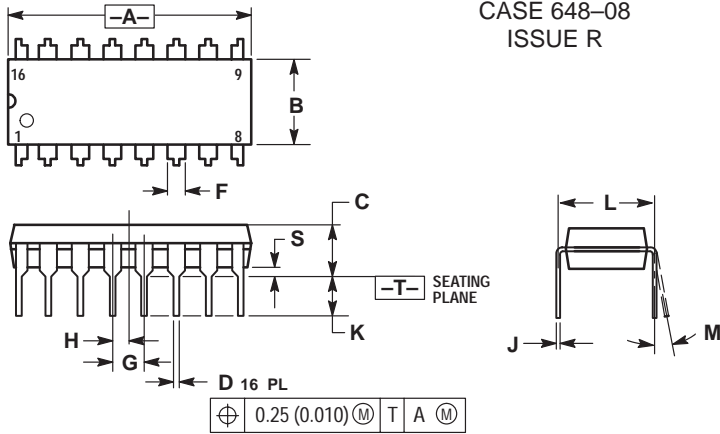
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC–16
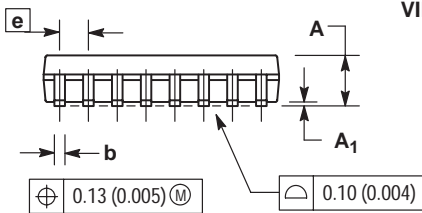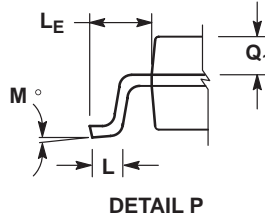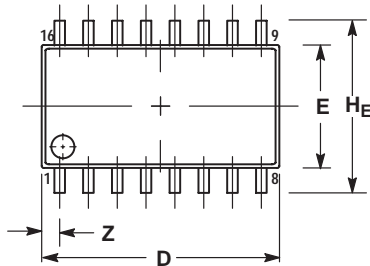**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J
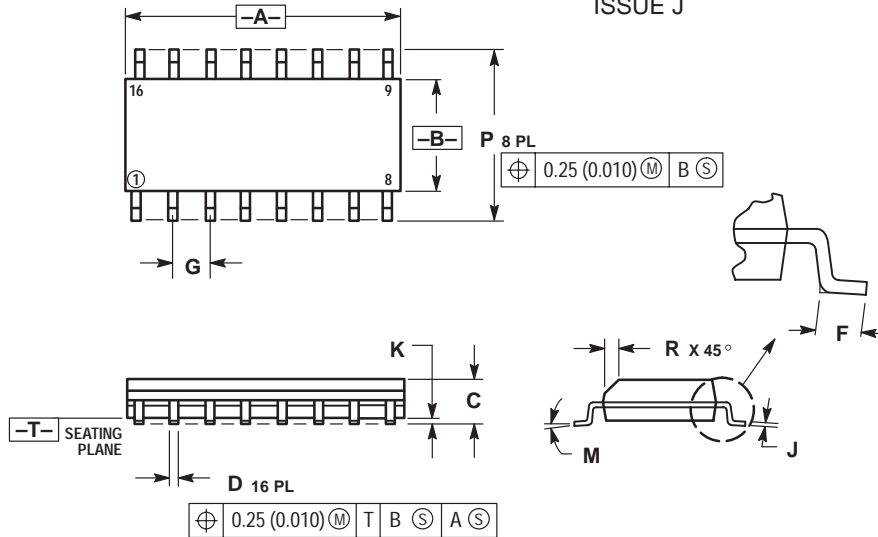
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

MC14538B

PACKAGE DIMENSIONS

SOIC–16
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–03
ISSUE B
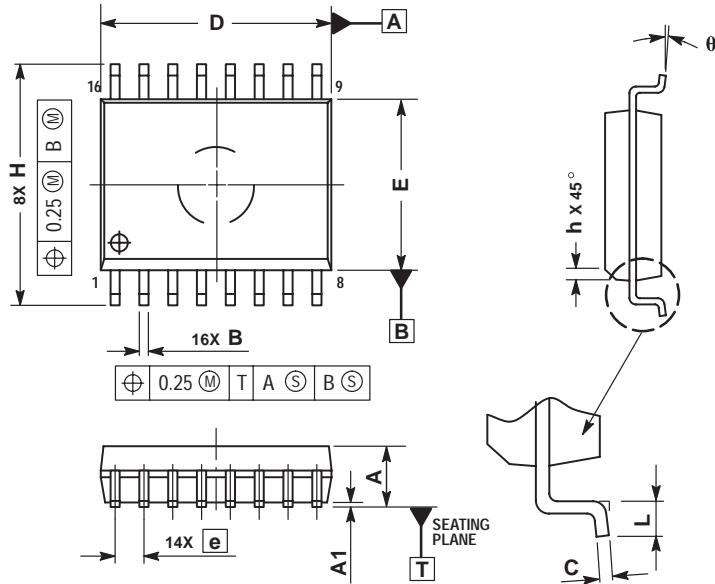
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

TSSOP–16
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O
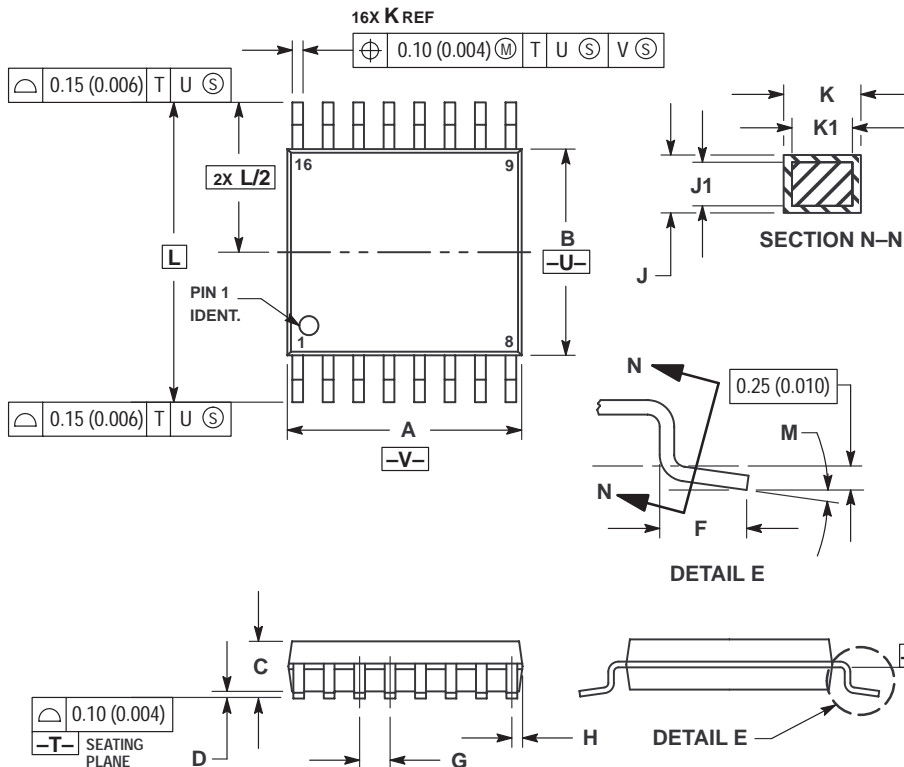
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	–––	1.20	–––	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

PACKAGE DIMENSIONS

SOEIAJ–16
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966–01
ISSUE O
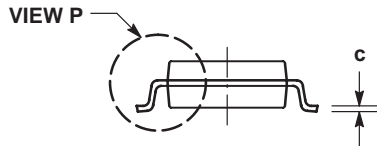
DETAIL P

VIEW P

⊕ 0.13 (0.005) Ⓜ

◻ 0.10 (0.004)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–––	2.05	–––	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	–––	0.78	–––	0.031

MC14538B/D