

HEF4952B

Dual 3-channel analog multiplexer/demultiplexer with supplementary switches

Rev. 03 — 16 December 2009

Product data sheet

1. General description

The HEF4952B is a dual 3-channel analog multiplexer/demultiplexer with supplementary switches and common select logic. Each switch features three independent inputs/outputs (pins nY0, nY1 and nY2) an input/output nY3 that can be connected to nY2 or V_{SS} and an input/output (nZ) common to nY0, nY1 and nY2. Three digital select inputs (S1, S2 and S3) are common to both switches. Inputs include clamp diodes, this enables the use of current limiting resistors to interface inputs in excess of V_{DD} .

V_{SS} and V_{DD} are the digital control supply pins.

The HEF4952B is suitable for use over the full industrial ($-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$) temperature range.

2. Features

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Schmitt-trigger action at control inputs
- Small signal switch
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Applications

- Industrial
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Type number	Package		Version
	Name	Description	
HEF4952BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

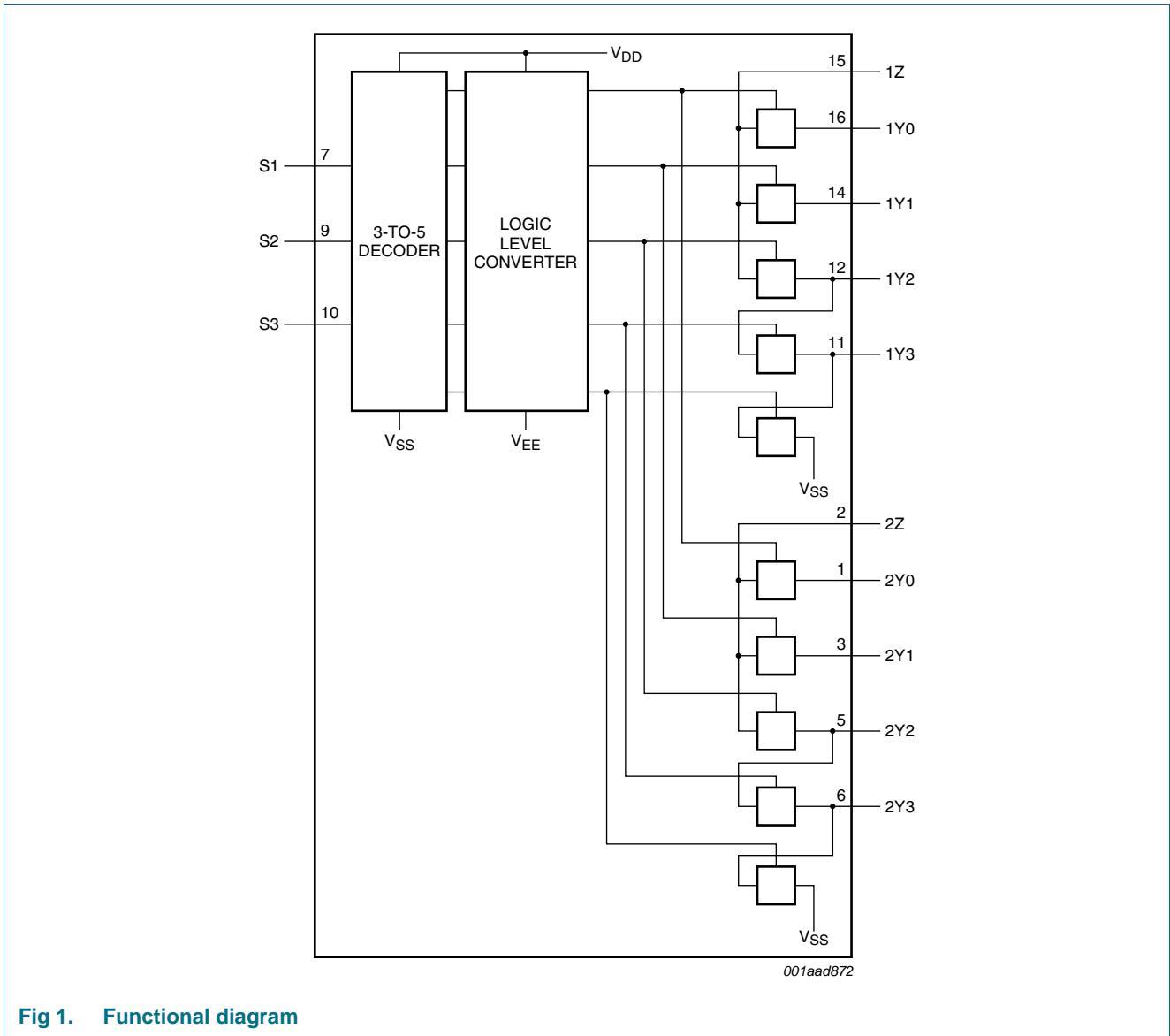
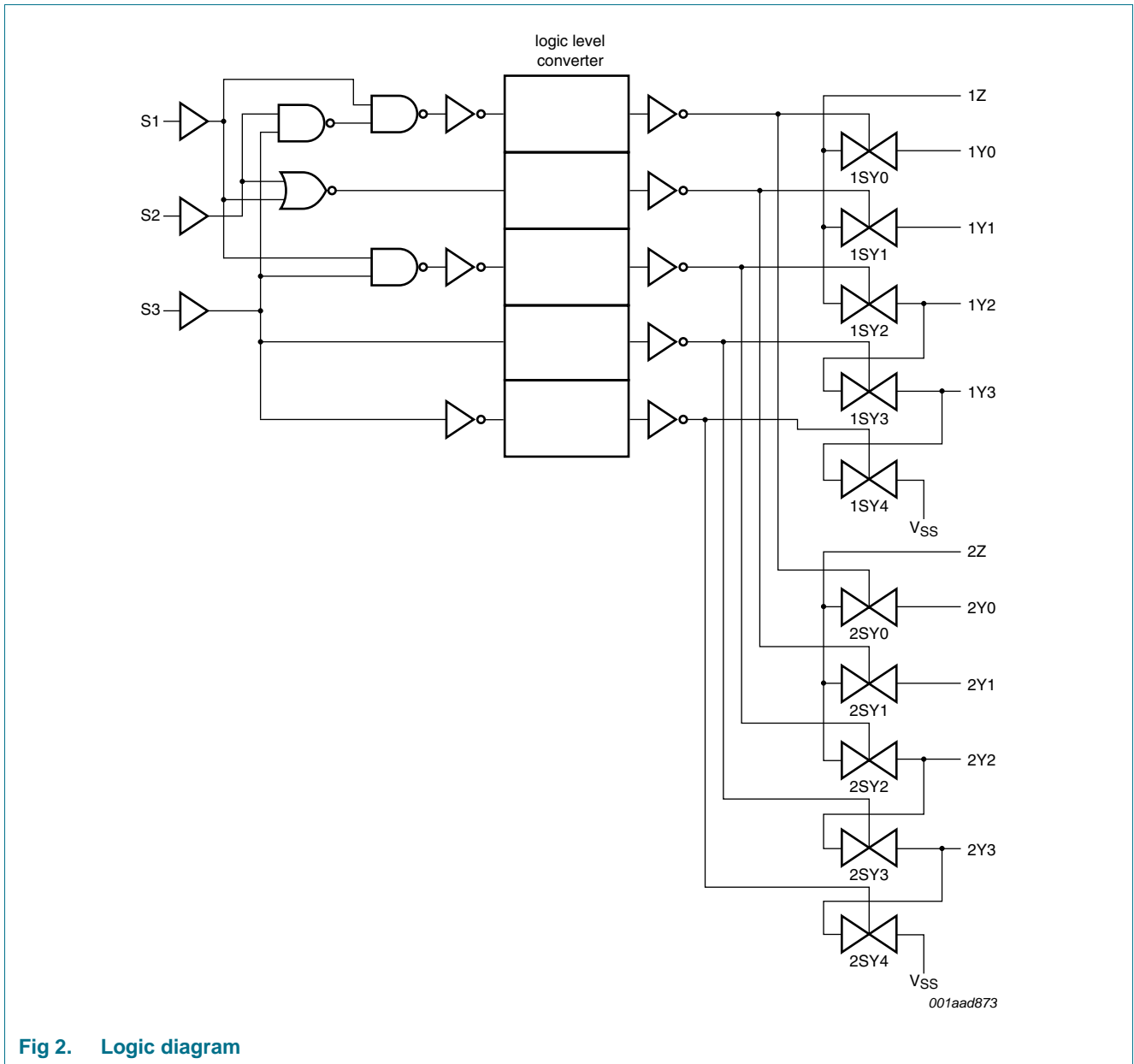
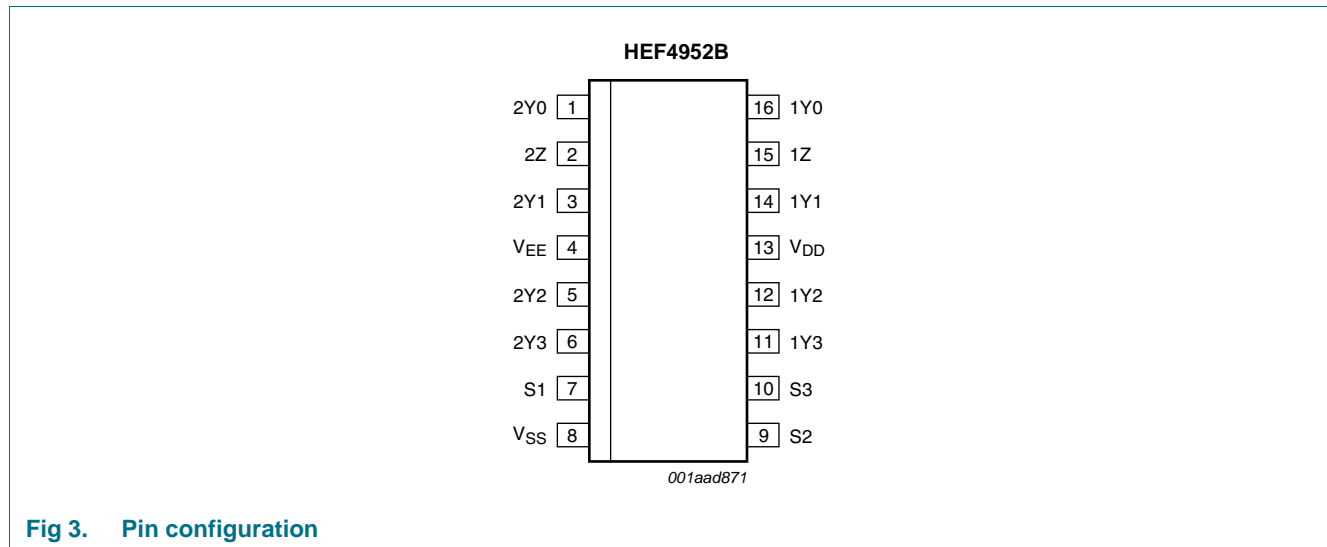


Fig 1. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V _{EE}	4	supply voltage
V _{SS}	8	ground supply voltage
S1, S2, S3	7, 9, 10	select input
1Y0, 1Y1, 1Y2, 1Y3, 2Y0, 2Y1, 2Y2, 2Y3	16, 14, 12, 11, 1, 3, 5, 6	independent input or output
1Z, 2Z	15, 2	common output or input
V _{DD}	13	supply voltage

7. Functional description

7.1 Function table

Table 3. Function table

Input			Switch				
S3	S2	S1	nSY0	nSY1	nSY2	nSY3	nSY4
L	L	L	open	nY1 to nZ	open	open	nY3 to V _{SS}
L	L	H	nY0 to nZ	open	open	open	nY3 to V _{SS}
L	H	L	open	open	nY2 to nZ	open	nY3 to V _{SS}
L	H	H	nY0 to nZ	open	nY2 to nZ	open	nY3 to V _{SS}
H	L	L	open	nY1 to nZ	open	nY2 to nY3	open
H	L	H	nY0 to nZ	open	open	nY2 to nY3	open
H	H	L	open	open	nY2 to nZ	nY2 to nY3	open
H	H	H	open	open	open	nY2 to nY3	open

- [1] H = HIGH voltage level;
L = LOW voltage level.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
V _{EE}	supply voltage	referenced to V _{DD}	[1] -18	+0.5	V
I _{IK}	input clamping current	pins Sn; V _I < -0.5 V or V _I > V _{DD} + 0.5 V	-	±10	mA
V _I	input voltage		-0.5	V _{DD} + 0.5	V
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	[2] -	500	mW
P	power dissipation	per output	-	100	mW

- [1] To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, and in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

- [2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	see Figure 4	5	-	15	V
V_{EE}	supply voltage	see Figure 4	-15	-	0	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

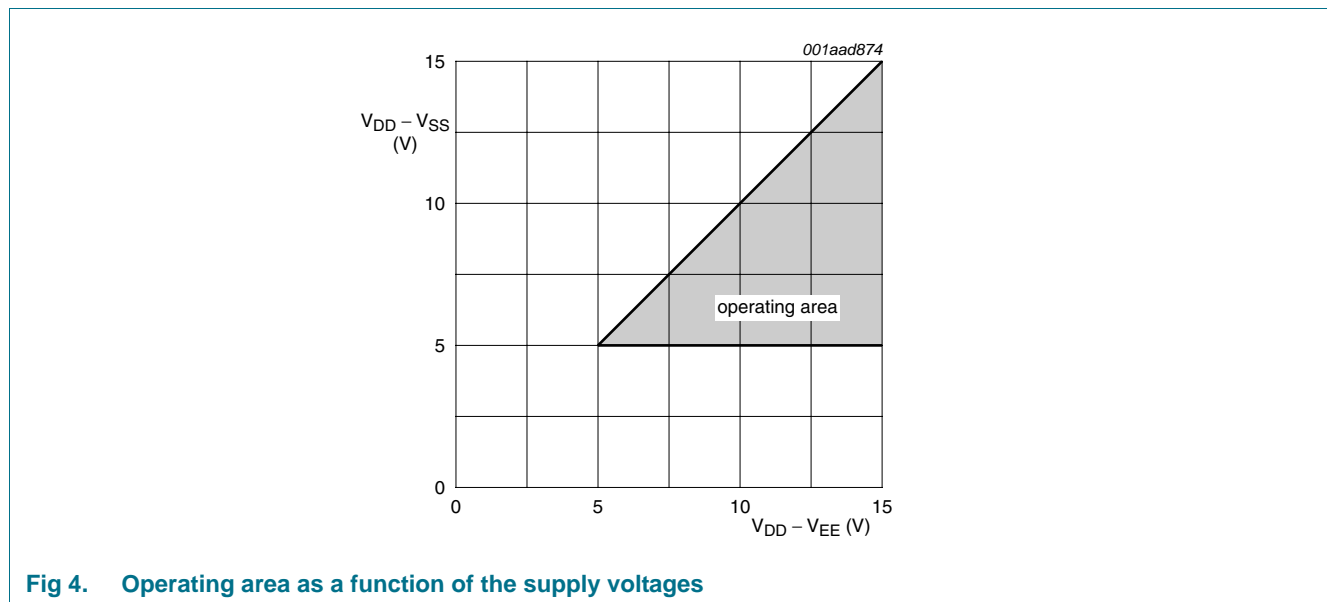


Fig 4. Operating area as a function of the supply voltages

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = V_{EE} = 0$ V; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40$ °C		$T_{amb} = 25$ °C		$T_{amb} = 85$ °C		Unit
				Min	Max	Min	Max	Min	Max	
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	Y port; per channel; see Figure 5	15 V	-	-	-	200	-	-	nA
I_{DD}	supply current	$I_O = 0$ A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance	Sn inputs	-	-	-	7.5	-	-	pF	

10.1 Test circuits

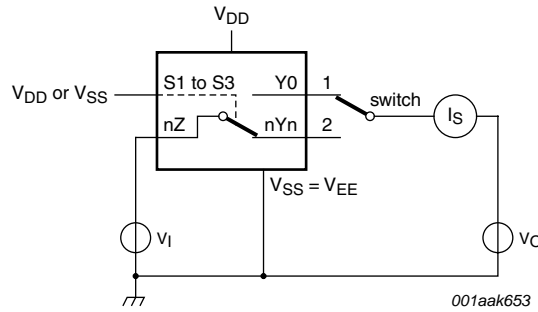


Fig 5. Test circuit for measuring OFF-state leakage current nYn port

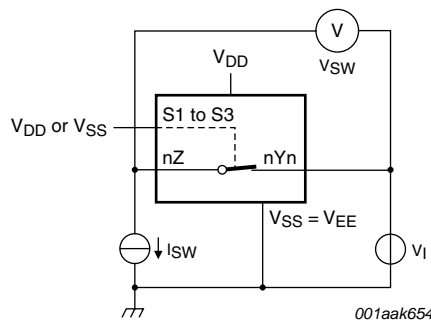
10.2 On resistance

Table 7. ON resistance

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $I_{SW} = 200\text{ }\mu\text{A}$; $V_{SS} = V_{EE} = 0\text{ V}$.

Symbol	Parameter	Conditions	$V_{DD} - V_{EE}$	Typ	Max	Unit
R_{ON}	ON resistance	$V_I = 0\text{ V}$; see Figure 6 and Figure 7	10 V	45	150	Ω
		$V_I = 2.5\text{ V}$; see Figure 6 and Figure 7	10 V	65	365	Ω
		$V_I = 5.0\text{ V}$; see Figure 6 and Figure 7	10 V	110	360	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 2.5\text{ V}$; see Figure 6	10 V	10	-	Ω

10.2.1 On resistance waveform and test circuit



$$R_{ON} = V_{SW} / I_{SW}$$

Fig 6. Test circuit for measuring R_{ON}

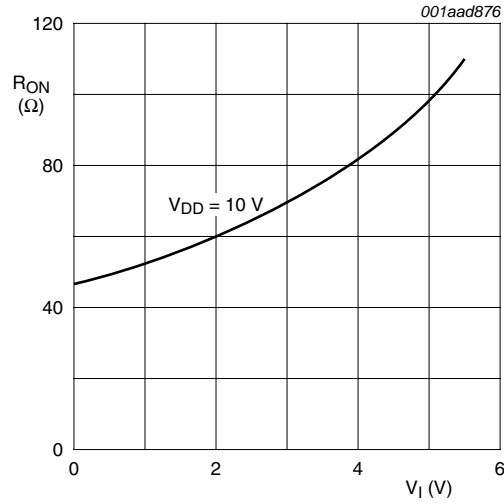


Fig 7. Typical RON as a function of input voltage

11. Dynamic characteristics

Table 8. Dynamic characteristics

Tamb = 25 °C; VSS = VEE = 0 V; for test circuit see Figure 10.

Symbol	Parameter	Conditions	VDD	Typ	Max	Unit
tPHL	HIGH to LOW propagation delay	nYn, nZ to nZ, nYn; VI = 1.0 V; see Figure 8	5 V	5	-	ns
			10 V	3	6	ns
			15 V	2	-	ns
tPLH	LOW to HIGH propagation delay	nYn, nZ to nZ, nYn; VI = 1.0 V; see Figure 8	5 V	5	-	ns
			10 V	3	6	ns
			15 V	2	-	ns
tPZL	OFF-state to LOW propagation delay	Sn to nYn, nZ; VI = VEE; see Figure 9	5 V	125	-	ns
			10 V	50	100	ns
			15 V	35	-	ns
tPZH	OFF-state to HIGH propagation delay	Sn to nYn, nZ; VI = 1.0 V; see Figure 9	5 V	125	-	ns
			10 V	50	100	ns
			15 V	35	-	ns

11.1 Waveforms and test circuit

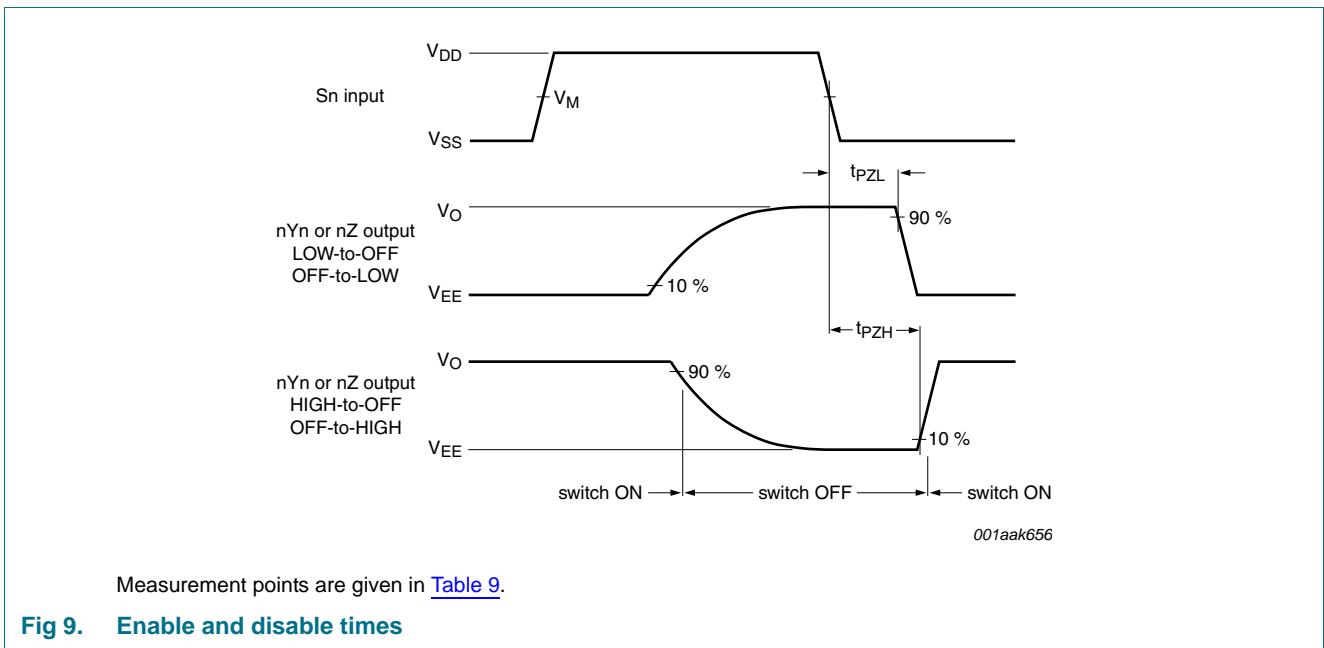
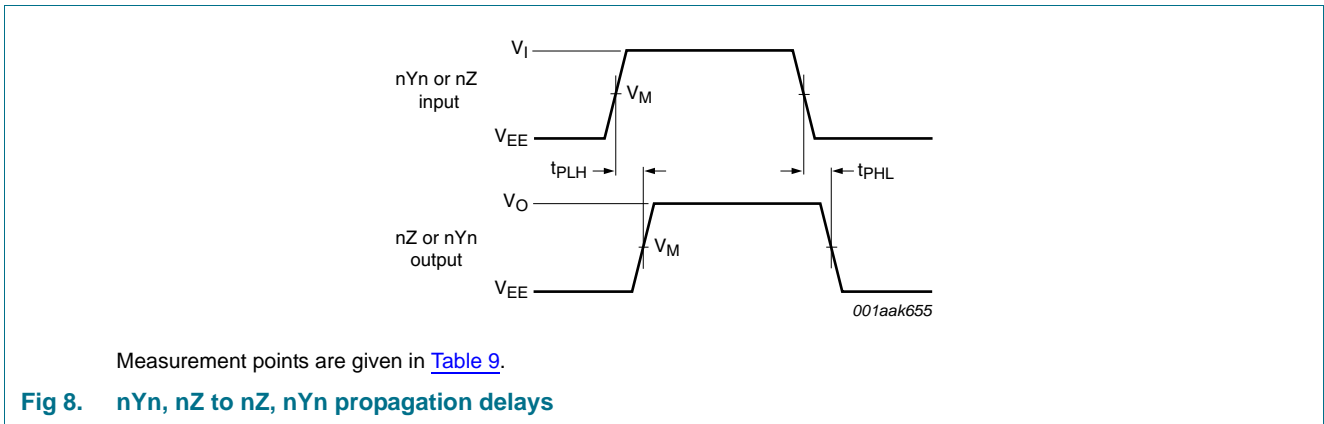
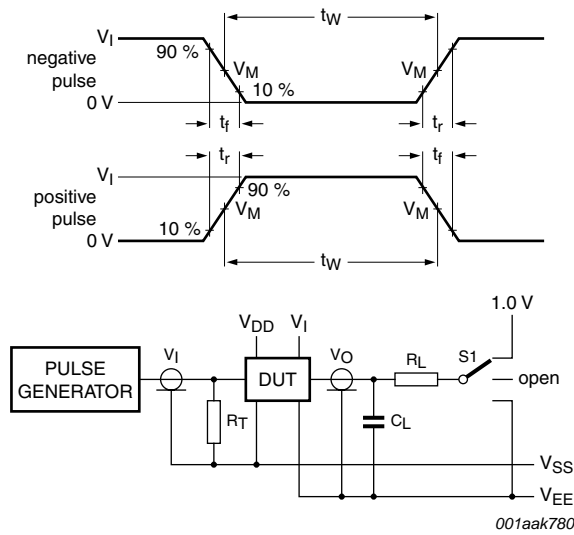


Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).

Definitions:

DUT = Device Under Test.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including test jig and probe.

R_L = Load resistance.

Fig 10. Test circuit for measuring switching times

Table 10. Test data

Input				Load		S1 position			
nYn, nZ	Sn	t _r , t _f	V _M	C _L	R _L	t _{PHL} , t _{PLH}	t _{PZH}	t _{PZL}	Other
V _I or V _{EE}	V _{DD} or V _{SS}	≤ 20 ns	0.5V _{DD}	50 pF	10 kΩ	V _{EE}	V _{EE}	1.0 V	V _{EE}

Table 11. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown; $V_{EE} = V_{SS} = 0 V$; $t_r = t_f \leq 20 ns$; $T_{amb} = 25 ^\circ C$.

Symbol	Parameter	V _{DD}	Typical formula for P _D (μW)	Where:
P _D	dynamic power dissipation	5 V	$P_D = 1300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz;
		10 V	$P_D = 6100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz;
		15 V	$P_D = 15600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF;
				V_{DD} = supply voltage in V;
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

11.2 Transfer characteristics

Table 12. Control input characteristics

$V_{SS} = V_{EE} = 0$ V unless otherwise specified.

Symbol	Parameter	Conditions	T _{amb} = 25 °C		T _{amb} = -40 °C to +85 °C		Unit
			Min	Max	Min	Max	
V _{T+}	positive-going threshold voltage	V _{DD} = 5 V	-	2.90	-	3.00	V
		V _{DD} = 10 V	-	4.37	-	4.50	V
V _{T-}	negative-going threshold voltage	V _{DD} = 5 V	1.03	-	1.00	-	V
		V _{DD} = 10 V	2.10	-	2.00	-	V
V _H	hysteresis voltage	V _{DD} = 5 V	0.16	-	0.10	-	V
		V _{DD} = 10 V	0.11	-	0.10	-	V

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

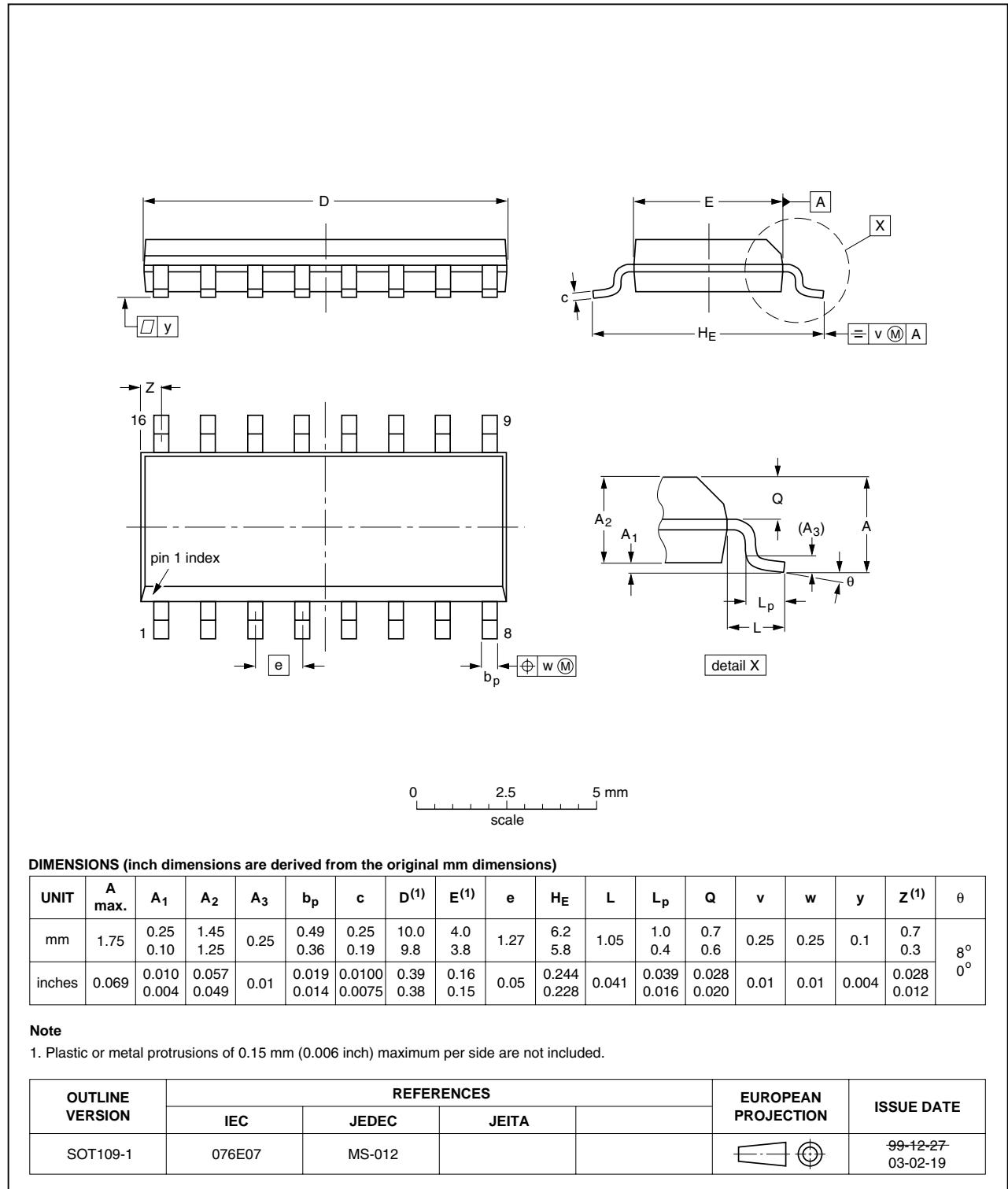


Fig 11. Package outline SOT109-1 (SO16)

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4952B_3	20091216	Product data sheet	-	HEF4952B_2
Modifications:		<ul style="list-style-type: none">Title changed from 8-channel analog multiplexer/demultiplexer.Section 1 "General description" modified.Section 8 "Limiting values" I_{IK} conditions updated.Abbreviations section removed.		
HEF4952B_2	20091002	Product data sheet	-	HEF4952B_1
HEF4952B_1	20060320	Product data sheet	-	-

14. Legal information

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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