

# HEF4517B

## Dual 64-bit static shift register

Rev. 06 — 10 December 2009

Product data sheet

### 1. General description

The HEF4517B consists of two identical, independent 64-bit static shift registers. Each register has separate clock (nCP), data input (nD), parallel input-enable/output-enable (nPE/ $\overline{\text{OE}}$ ) and four 3-state outputs of the 16th, 32nd, 48th, and 64th bit positions (nQ16 to nQ64). Data at the nD input is entered into the first bit on the LOW-to-HIGH transition of the clock, regardless of the state of nPE/ $\overline{\text{OE}}$ .

When nPE/ $\overline{\text{OE}}$  is LOW, the outputs are enabled and it is in the 64-bit serial mode.

When nPE/ $\overline{\text{OE}}$  is HIGH, the outputs are disabled (high-impedance OFF-state), the 64-bit shift register is divided into four 16-bit shift registers with nD, nQ16, nQ32 and nQ48 as data inputs of the 1st, 17th, 33rd, and 49th bit respectively. Schmitt-trigger action in the clock input makes the circuit highly tolerant of slower clock rise and fall times.

It operates over a recommended  $V_{\text{DD}}$  power supply range of 3 V to 15 V referenced to  $V_{\text{SS}}$  (usually ground). Unused inputs must be connected to  $V_{\text{DD}}$ ,  $V_{\text{SS}}$ , or another input. It is also suitable for use over the full industrial ( $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ) temperature range.

### 2. Features

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Applications

- Industrial

### 4. Ordering information

Table 1. Ordering information

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
HEF4517BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4517BT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1



5. Functional diagram

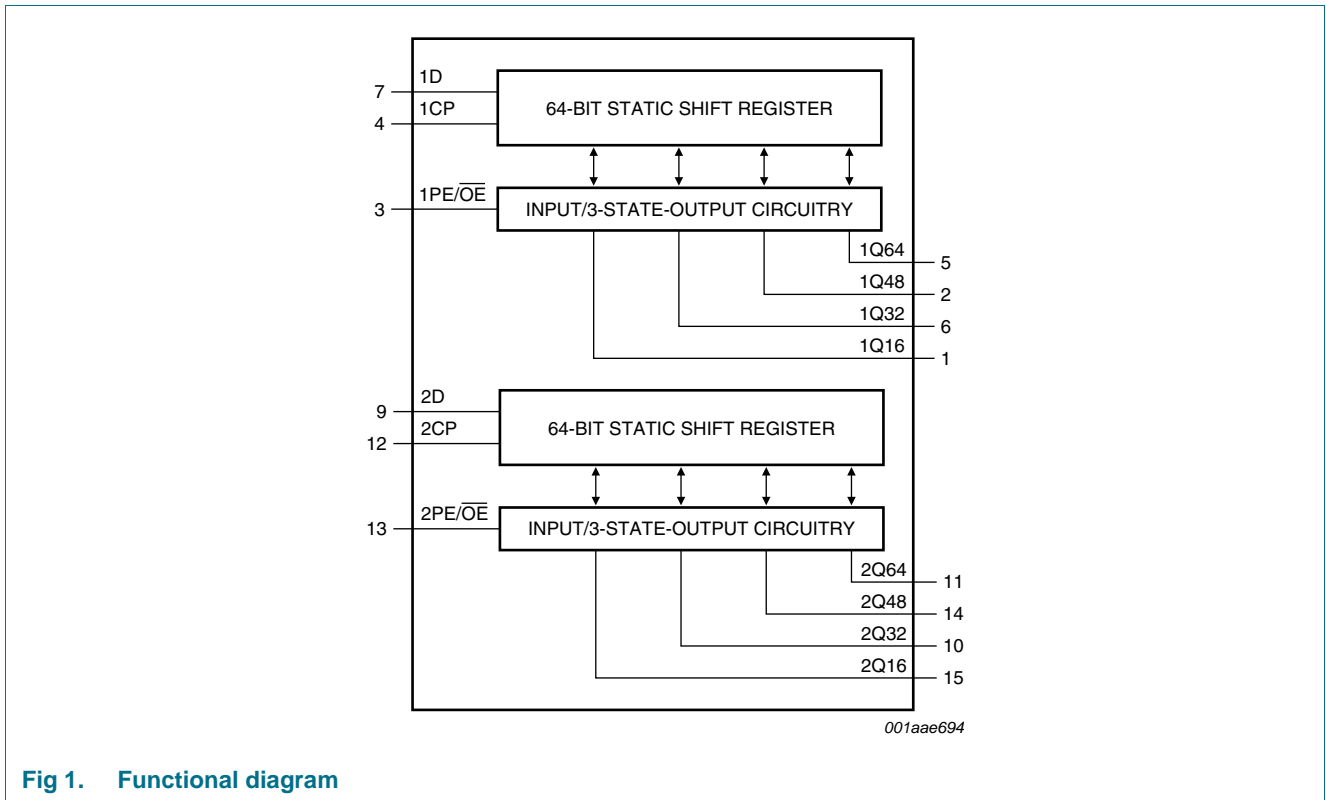


Fig 1. Functional diagram

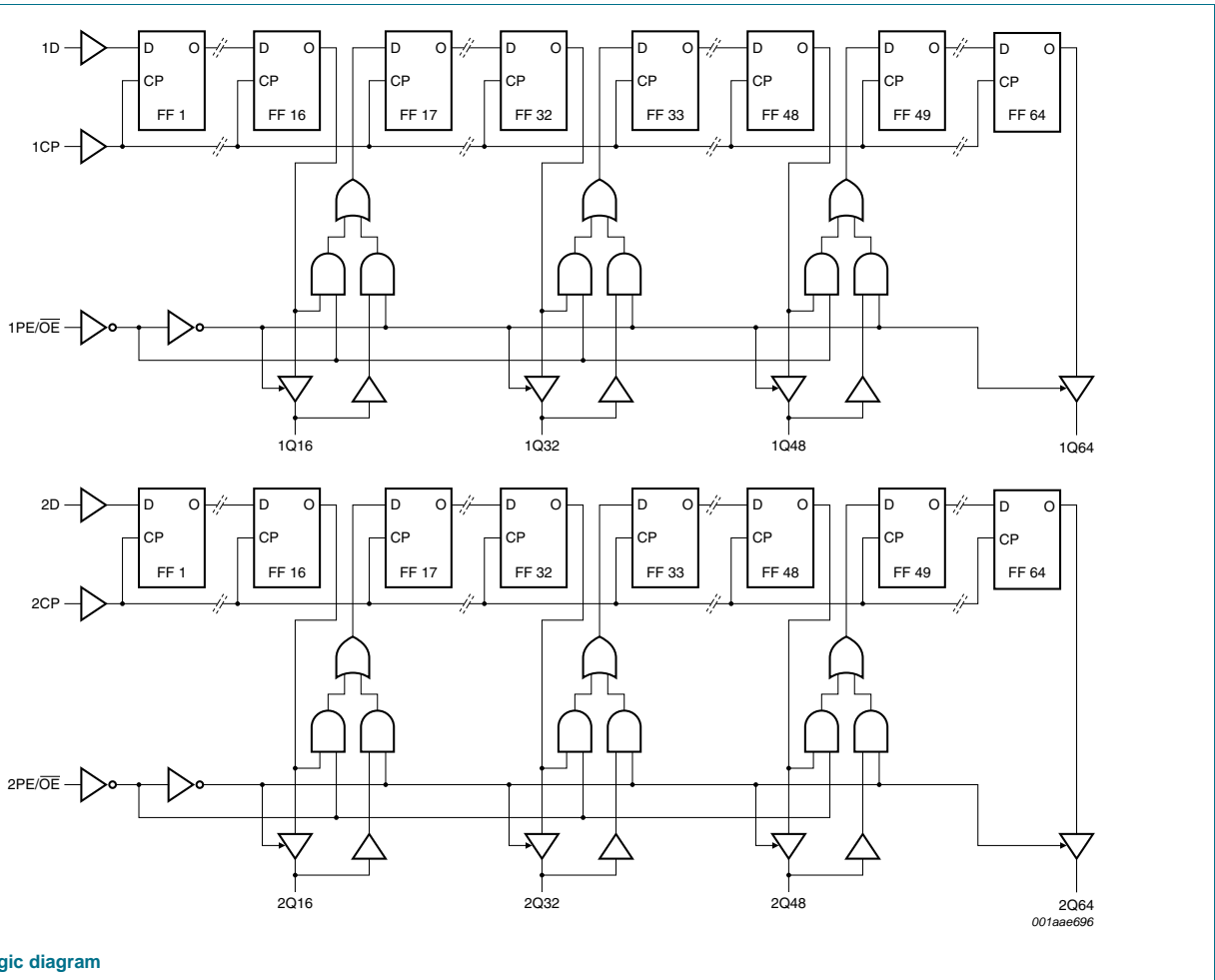
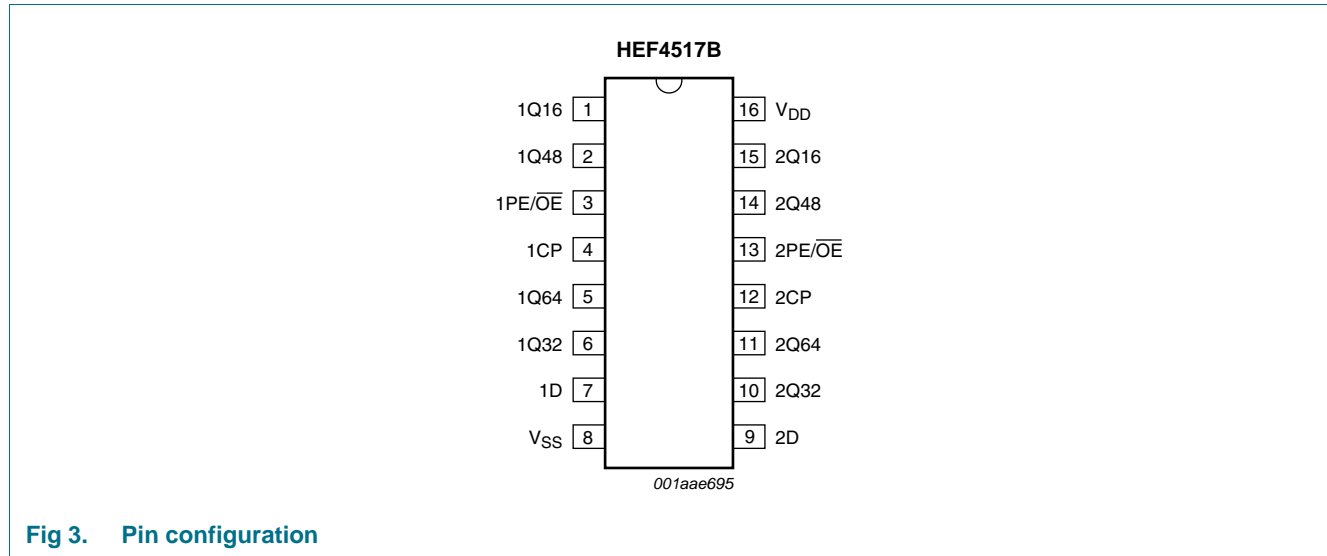


Fig 2. Logic diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
1Q16, 2Q16	1, 15	3-state input/output
1Q48, 2Q48	2, 14	3-state input/output
1PE/ $\overline{OE}$ , 2PE/ $\overline{OE}$	3, 13	parallel input-enable/output-enable input
1CP, 2CP	4, 12	clock input
1Q64, 2Q64	5, 11	3-state input/output
1Q32, 2Q32	6, 10	3-state input/output
1D, 2D	7, 9	data input
V <sub>SS</sub>	8	ground supply voltage
V <sub>DD</sub>	16	supply voltage

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Inputs			Inputs/outputs				Mode
nCP	nD	nPE/OE	nQ16	nQ32	nQ48	nQ64	
↑	data entered into 1st bit	L	content of 16th bit displayed	content of 32nd bit displayed	content of 48th bit displayed	content of 64th bit displayed	One 64-bit shift register. The content of the shift register is shifted over one stage
↑	data entered into 1st bit	H	data at nQ16 entered into 17th bit	data at nQ32 entered into 33rd bit	data at nQ48 entered into 49th bit	remains in 'Z' state	Four 16-bit shift register. The content of the shift registers is shifted over one stage
↓	X	L	no change	no change	no change	no change	no change
↓	X	H	Z	Z	Z	Z	no change

- [1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance state;  
 ↑ = positive-going transition; ↓ = negative-going transition.

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	±10	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	±10	mA
$I_{IO}$	input/output current		-	±10	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	DIP16 package	<sup>[1]</sup> -	750	mW
		SO16 package	<sup>[2]</sup> -	500	mW
P	power dissipation	per output	-	100	mW

- [1] For DIP16 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

- [2] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-1.7	-	-1.4	-	-1.1	-	mA
		$V_O = 4.6\text{ V}$	5 V	-0.52	-	-0.44	-	-0.36	-	mA
		$V_O = 9.5\text{ V}$	10 V	-1.3	-	-1.1	-	-0.9	-	mA
		$V_O = 13.5\text{ V}$	15 V	-3.6	-	-3.0	-	-2.4	-	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	50	-	50	-	375	$\mu\text{A}$
			10 V	-	100	-	100	-	750	$\mu\text{A}$
			15 V	-	200	-	200	-	1500	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	-	7.5	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; for test circuit see [Figure 8](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	nCP to nQn; see <a href="#">Figure 4</a>	5 V	[1] $193\text{ ns} + (0.55\text{ ns/pF})C_L$	-	220	440	ns
			10 V	$74\text{ ns} + (0.23\text{ ns/pF})C_L$	-	85	170	ns
			15 V	$52\text{ ns} + (0.16\text{ ns/pF})C_L$	-	60	120	ns
$t_{PLH}$	LOW to HIGH propagation delay	nCP to nQn; see <a href="#">Figure 4</a>	5 V	[1] $163\text{ ns} + (0.55\text{ ns/pF})C_L$	-	190	380	ns
			10 V	$64\text{ ns} + (0.23\text{ ns/pF})C_L$	-	75	150	ns
			15 V	$42\text{ ns} + (0.16\text{ ns/pF})C_L$	-	50	100	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	nPE/ $\overline{\text{OE}}$ to nQn; see <a href="#">Figure 5</a>	5 V		-	40	80	ns
			10 V		-	30	60	ns
			15 V		-	25	50	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	nPE/ $\overline{\text{OE}}$ to nQn; see <a href="#">Figure 5</a>	5 V		-	45	90	ns
			10 V		-	25	50	ns
			15 V		-	20	40	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	nPE/ $\overline{\text{OE}}$ to nQn; see <a href="#">Figure 5</a>	5 V		-	50	100	ns
			10 V		-	30	60	ns
			15 V		-	25	50	ns
$t_{PZL}$	OFF-state to LOW propagation delay	nPE/ $\overline{\text{OE}}$ to nQn; see <a href="#">Figure 5</a>	5 V		-	60	120	ns
			10 V		-	30	60	ns
			15 V		-	25	50	ns
$t_t$	transition time	nQn; see <a href="#">Figure 6</a>	5 V	[1] $10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
$t_{su}$	set-up time	nQn, nD to nCP; see <a href="#">Figure 7</a>	5 V		30	10	-	ns
			10 V		25	5	-	ns
			15 V		20	5	-	ns
$t_h$	hold time	nQn, nD to nCP; see <a href="#">Figure 7</a>	5 V		45	15	-	ns
			10 V		30	10	-	ns
			15 V		25	10	-	ns
$t_W$	pulse width	nQn, nD to nCP; see <a href="#">Figure 7</a>	5 V		-	95	190	ns
			10 V		-	40	80	ns
			15 V		-	30	60	ns
$f_{max}$	maximum frequency	see <a href="#">Figure 7</a>	5 V		2	5	-	MHz
			10 V		6	12	-	MHz
			15 V		8	16	-	MHz

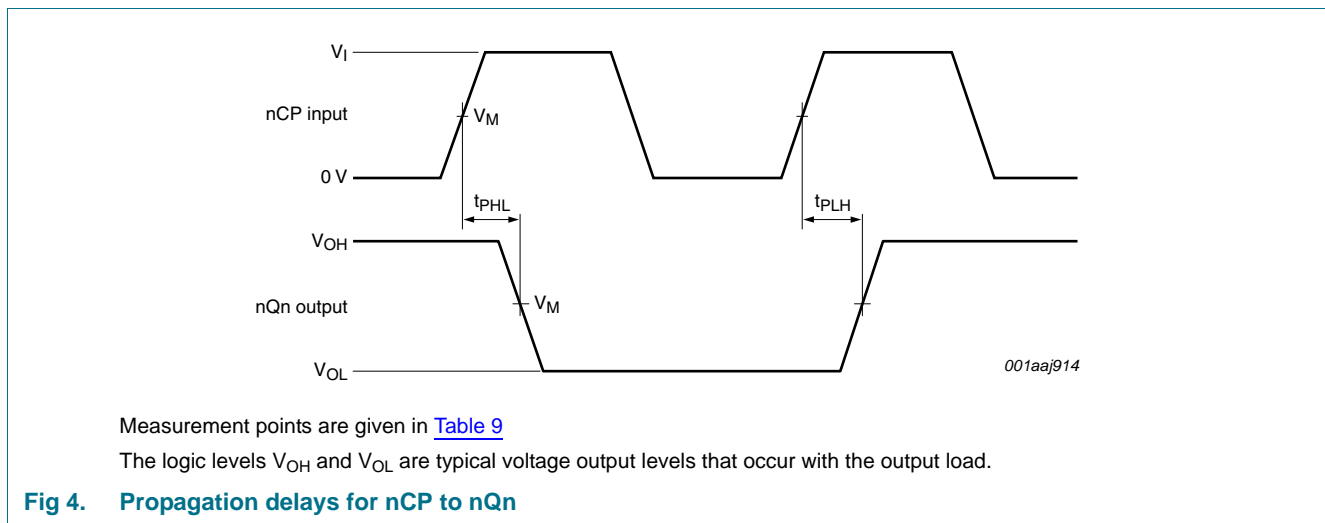
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

**Table 8. Dynamic power dissipation  $P_D$**

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 7000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz,
		10 V	$P_D = 28000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_o$ = output frequency in MHz,
		15 V	$P_D = 70000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.

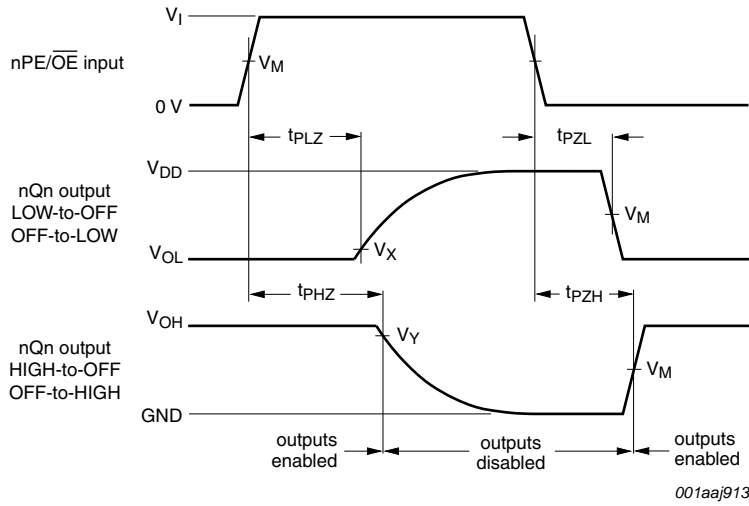
## 12. Waveforms



**Table 9. Measurement points**

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
$0.5V_I$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$

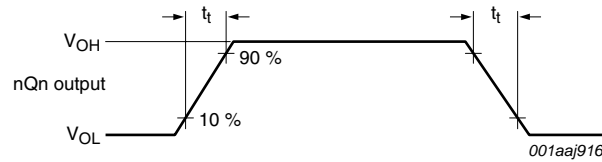




Measurement points are given in [Table 9](#)

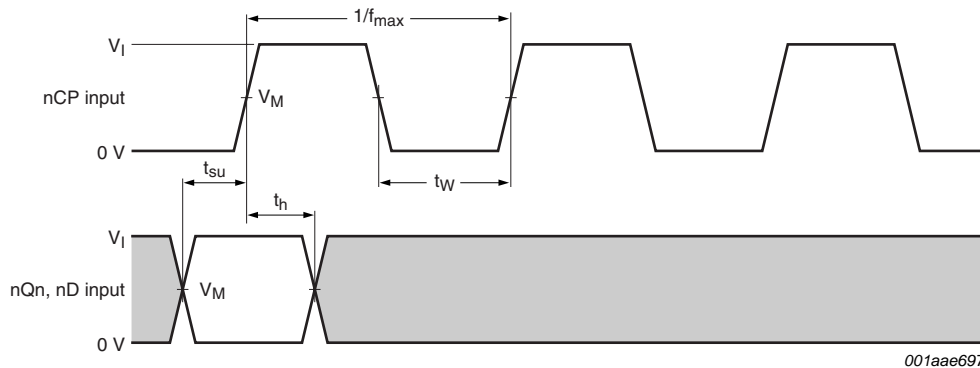
The logic levels  $V_{OH}$  and  $V_{OL}$  are typical voltage output levels that occur with the output load.

**Fig 5. Enable and disable times and 3-state propagation delays**



The logic levels  $V_{OH}$  and  $V_{OL}$  are typical voltage output levels that occur with the output load.

**Fig 6. Transition times for nQn**

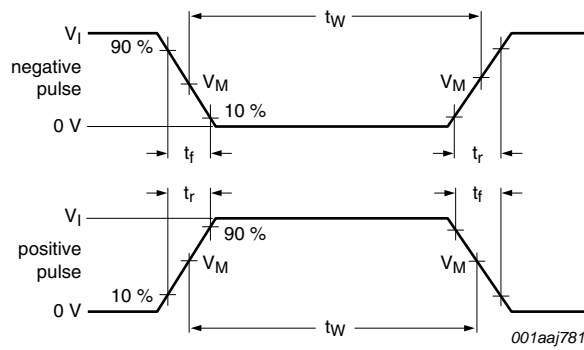


The shading indicates where the data (nQn and nD) is permitted to change for predictable output changes.

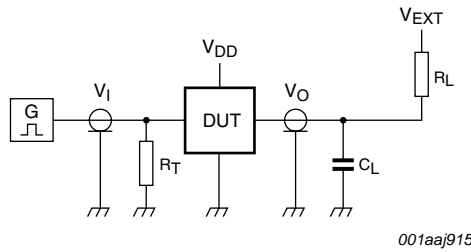
Measurement points are given in [Table 9](#)

The logic levels  $V_{OH}$  and  $V_{OL}$  are typical voltage output levels that occur with the output load.

**Fig 7. Waveforms showing minimum clock pulse width and maximum frequency and set-up and hold times for nQn (as data input) or nD to nCP**



a. Input waveforms



b. Test circuit

Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 8. Test circuit for switching times

Table 10. Test data

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
5 V to 15 V	$V_{DD}$	$\leq 20$ ns	50 pF	1 k $\Omega$	open	$2V_{DD}$	GND

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

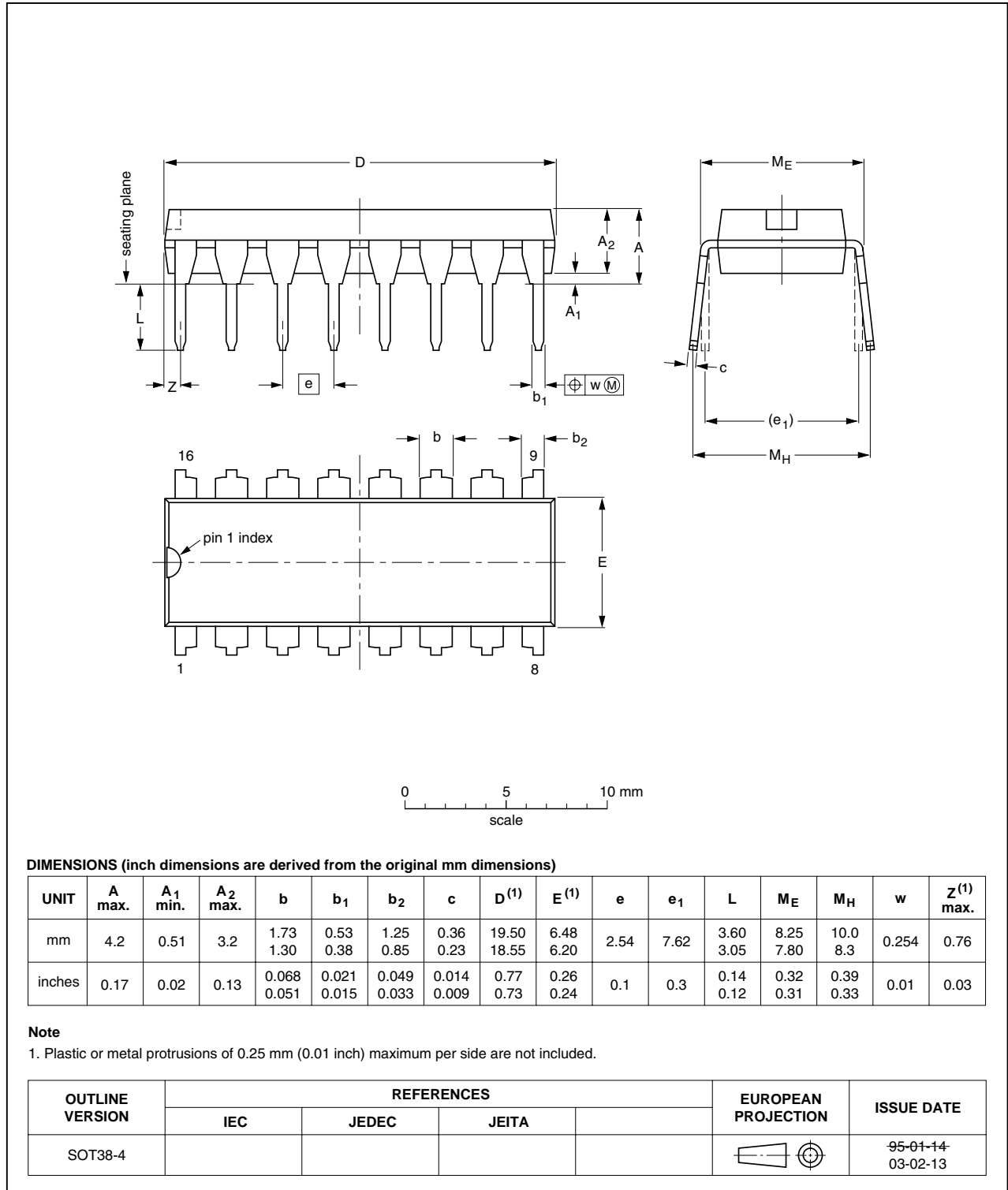


Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1

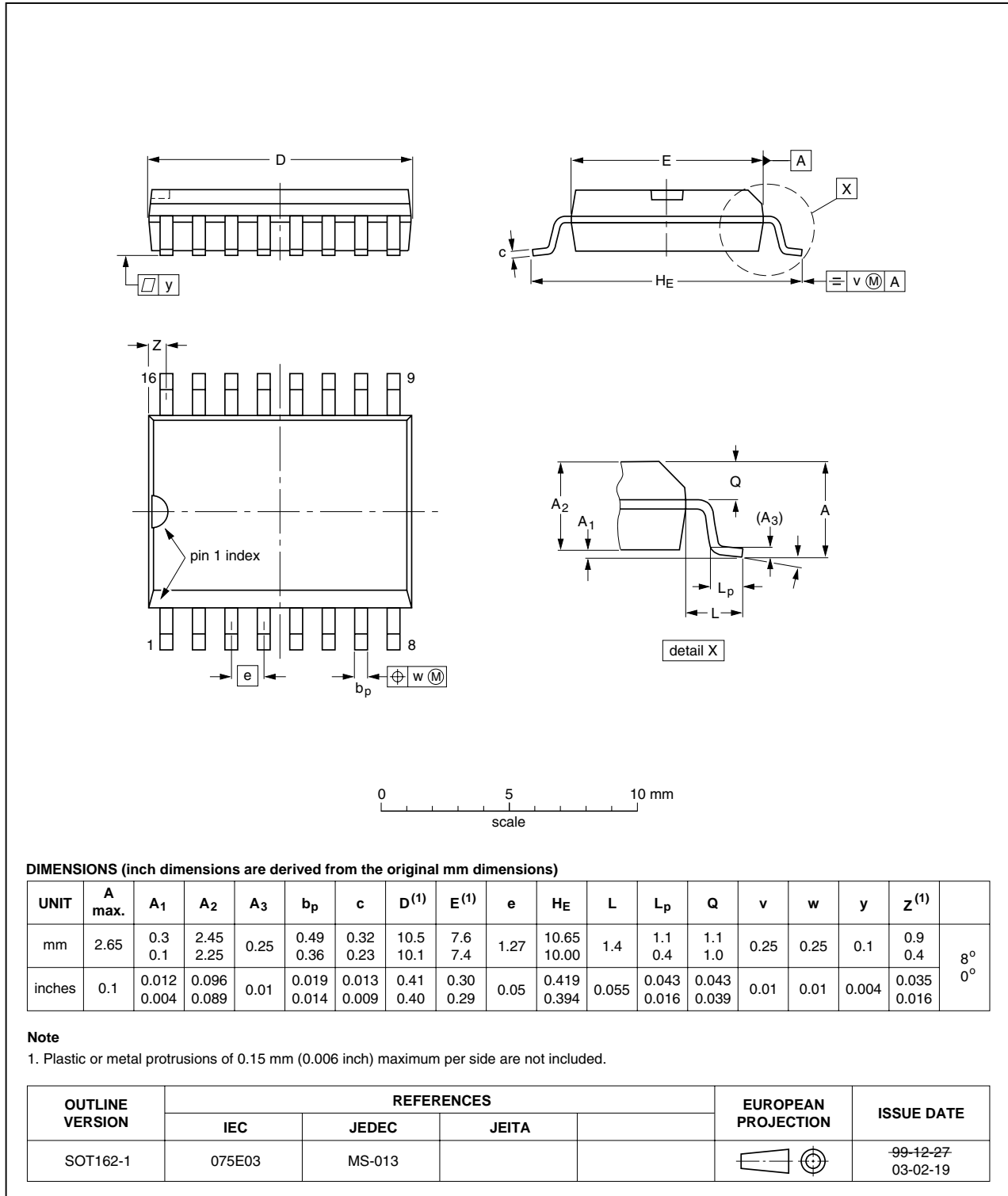


Fig 10. Package outline SOT162-1 (SO16)

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4517B_6	20091210	Product data sheet	-	HEF4517B_5
Modifications:	• <a href="#">Section 9 "Recommended operating conditions"</a> $\Delta t/\Delta V$ values updated.			
HEF4517B_5	20090728	Product data sheet	-	HEF4517B_4
HEF4517B_4	20090406	Product data sheet	-	HEF4517B_CNV_3
HEF4517B_CNV_3	19950101	Product specification	-	HEF4517B_CNV_2
HEF4517B_CNV_2	19950101	Product specification	-	-

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### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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