DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4505B
LSI
64-bit, 1-bit per word random access read/write memory

Product specification
File under Integrated Circuits, IC04

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Philips Semiconductors

PHILIPS

64-bit, 1-bit per word random access read/write memory

HEF4505B LSI

DESCRIPTION

The HEF4505B is a 64-bit, 1-bit per word, fully decoded and completely static, random access memory. The memory is strobed for reading or writing only when the strobe input (ST), chip enable inputs (CE_1 and CE_2) are HIGH simultaneously. The output data is available at the data output (D_{OUT}) only when the memory is strobed, the read/write input ($R/\overline{W}$) is HIGH and after the read access time has passed. Note that the three-state output is initially disabled and always goes to the LOW state before data is valid. The output is disabled in the high-impedance OFF-state, when the memory is not strobed or $R/\overline{W}$ is LOW. $R/\overline{W}$ may remain HIGH during a read cycle or LOW during a write cycle. The output data has the same polarity as the input data.

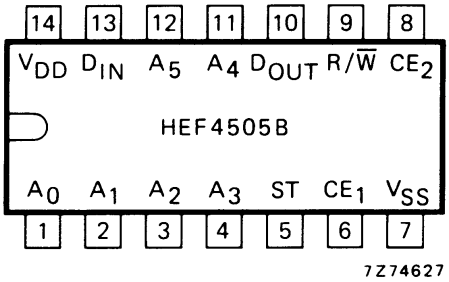


Fig.1 Pinning diagram.

HEF4505BP(N): 14-lead DIL; plastic (SOT27-1)

HEF4505BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

( ): Package Designator North America

PINNING

A_0 to A_5	address inputs
CE_1, CE_2	chip enable inputs
$R/\overline{W}$	read/write input
ST	strobe input
D_{IN}	data input
D_{OUT}	data output

FUNCTION TABLE

ST, CE_1, CE_2	$R/\overline{W}$	D_{OUT}	MODE
L	L	Z	disabled
H	L	Z	write
L	H	Z	disabled
H	H	equal to memory data	read

Note

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   Z = high-impedance OFF-state

SUPPLY VOLTAGE

RATING	OPERATING
–0,5 to +15	4,5 to 15 V

Note

1. Minimum standby voltage for data retention is 3 V.

FAMILY DATA, I_{DD} LIMITS category LSI

See Family Specifications

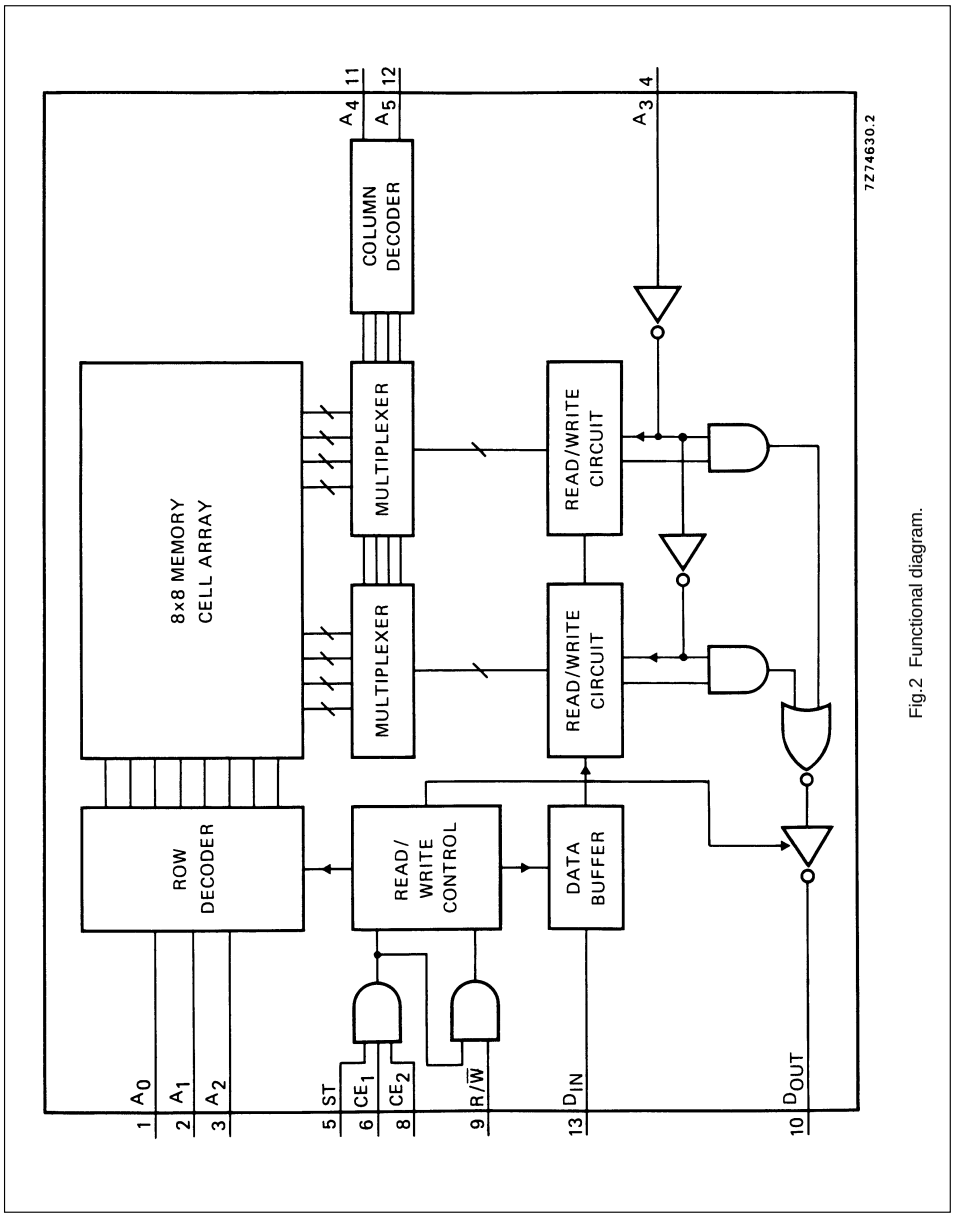


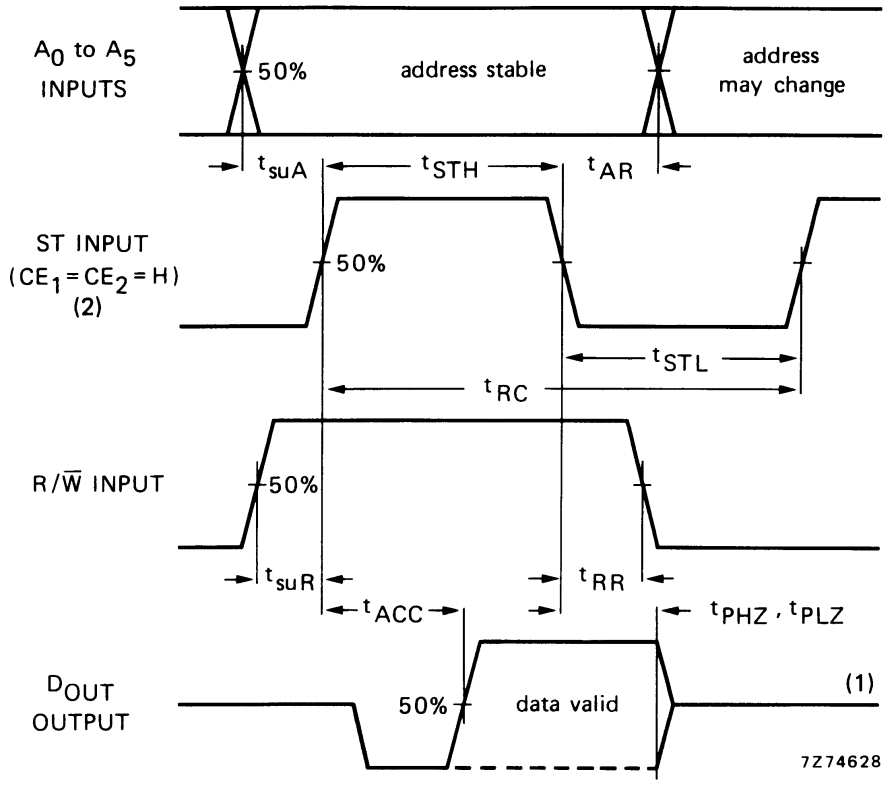
Fig.2 Functional diagram.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Minimum strobe pulse width; LOW	5	t_{STL}	75	35		ns	
	10		45	22		ns	
	15		30	15		ns	
Read cycle time	5	t_{RC}		350	700	ns	
	10			250	500	ns	
	15			210	420	ns	
Write cycle time	5	t_{WC}		220	440	ns	
	10			125	250	ns	
	15			75	150	ns	
Read access time	5	t_{ACC}		330	660	ns	303 ns + (0,55 ns/pF) C_L
	10			135	270	ns	124 ns + (0,23 ns/pF) C_L
	15			100	200	ns	92 ns + (0,16 ns/pF) C_L
Address recovery time	5	t_{AR}	80	40		ns	
	10		40	20		ns	
	15		25	10		ns	
Read recovery time	5	t_{RR}	180	90		ns	
	10		120	60		ns	
	15		90	45		ns	
Write recovery time	5	t_{WR}	75	35		ns	
	10		45	25		ns	
	15		40	20		ns	
3-state propagation delays							
Output disable times	5	t_{PHZ}, t_{PLZ}		105	210	ns	
	10			60	125	ns	
	15			55	115	ns	
Set-up times	5		–20	–40		ns	
$A_n \rightarrow ST$	10	t_{suA}	–10	–20		ns	
	15		–5	–10		ns	
	5		–30	–60		ns	
$R/\overline{W} \rightarrow ST$	10	t_{suR}	–15	–30		ns	
	15		–5	–10		ns	
	5		160	80		ns	
$D_{IN} \rightarrow ST$	10	t_{suD}	75	35		ns	
	15		45	20		ns	
	5		240	120		ns	
$R/\overline{W} \rightarrow ST$	10	t_{suW}	100	50		ns	
	15		75	35		ns	

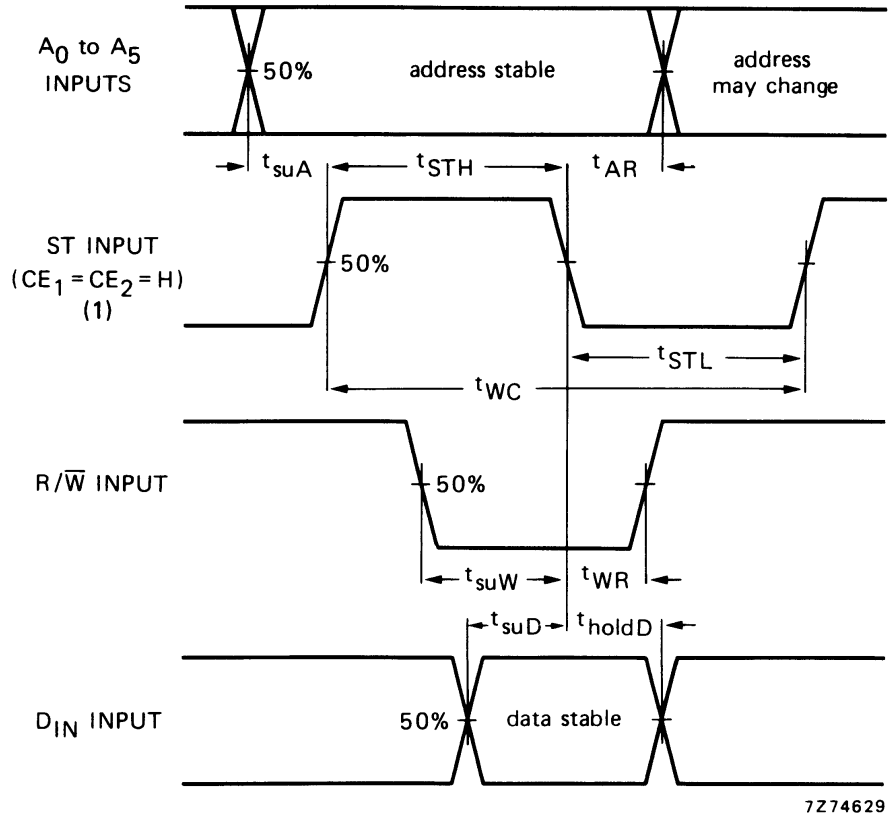
	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Hold time	5		–20	–40		ns	
$D_{IN} \rightarrow$ ST	10	t_{holdD}	5	–10		ns	
	15		10	0		ns	



(1) Output in high impedance OFF-state.

(2) $t_{STHmin} = t_{RCmax} - t_{STLmin}$.

Fig.3 Read cycle timing diagram.



(1) $t_{STHmin} = t_{WCmax} - t_{STLmin}$.

Fig.4 Write cycle timing diagram.

APPLICATION INFORMATION

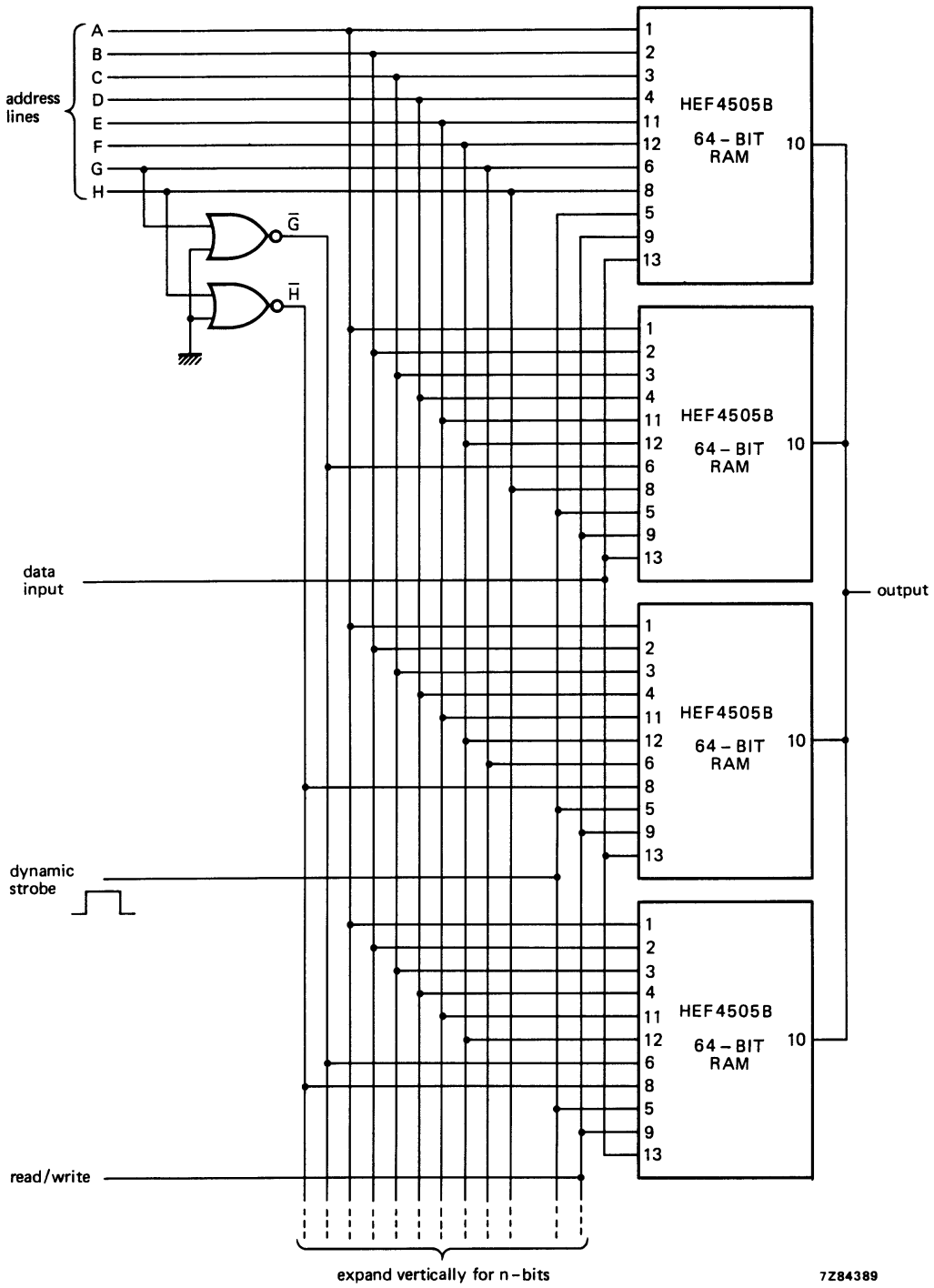


Fig.5 256-word by n-bit static read/write memory using HEF4505B ICs.

Figure 5 shows a 256-word by n-bit static RAM system. The outputs of the four HEF4505B circuits are tied together to form 256 words by 1-bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and AND-ing them with the strobe input.

Fan-in and fan-out of the memory are limited only by speed requirements. The extremely low input and output leakage currents keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

The memory system shown in Fig.5 can be interfaced directly with other ICs of the LOCMOS HE family. No external components are required.

Non-volatile information storage is allowed due to very low power dissipation when the memory is powered by a small standby battery. Figure 6 shows an optional standby power supply circuit for making a LOCMOS memory 'non-volatile'. When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor (R) which sets the charging rate. In Fig.6 the sustaining voltage is V_B, and + V is the ordinary voltage from a power supply. V_{DD} is connected to the power supply pin of the memory. Low-leakage diodes are recommended to conserve battery power.

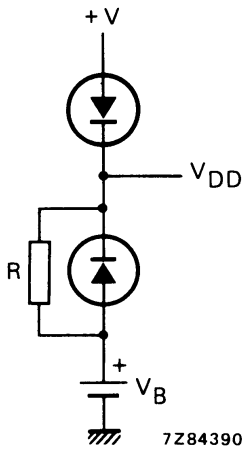


Fig.6 Standby battery circuit.